DSP56309

Advance Information
24-BIT GENERAL PURPOSE DIGITAL SIGNAL PROCESSOR

The DSP56309 is a member of the DSP56300 core family of programmable CMOS digital signal processors (DSPs). This family uses a high performance, single-clock-cycle-per-instruction engine providing a two-fold performance increase over Motorola's popular DSP56000 core, while retaining code compatibility. Significant architectural enhancements in the DSP56300 family include a barrel shifter, 24-bit addressing, an instruction cache, and direct memory access (DMA). The DSP56309 offers 80 / 100 MIPS at 3.0–3.6 V using an internal 80 / 100 MHz clock. The large on-chip memory is ideal for wireless infrastructure and wireless local-loop applications. The DSP56300 core family offers a new level of performance in speed and power provided by its rich instruction set and low-power dissipation, thus enabling a new generation of wireless, multimedia, and telecommunications products.

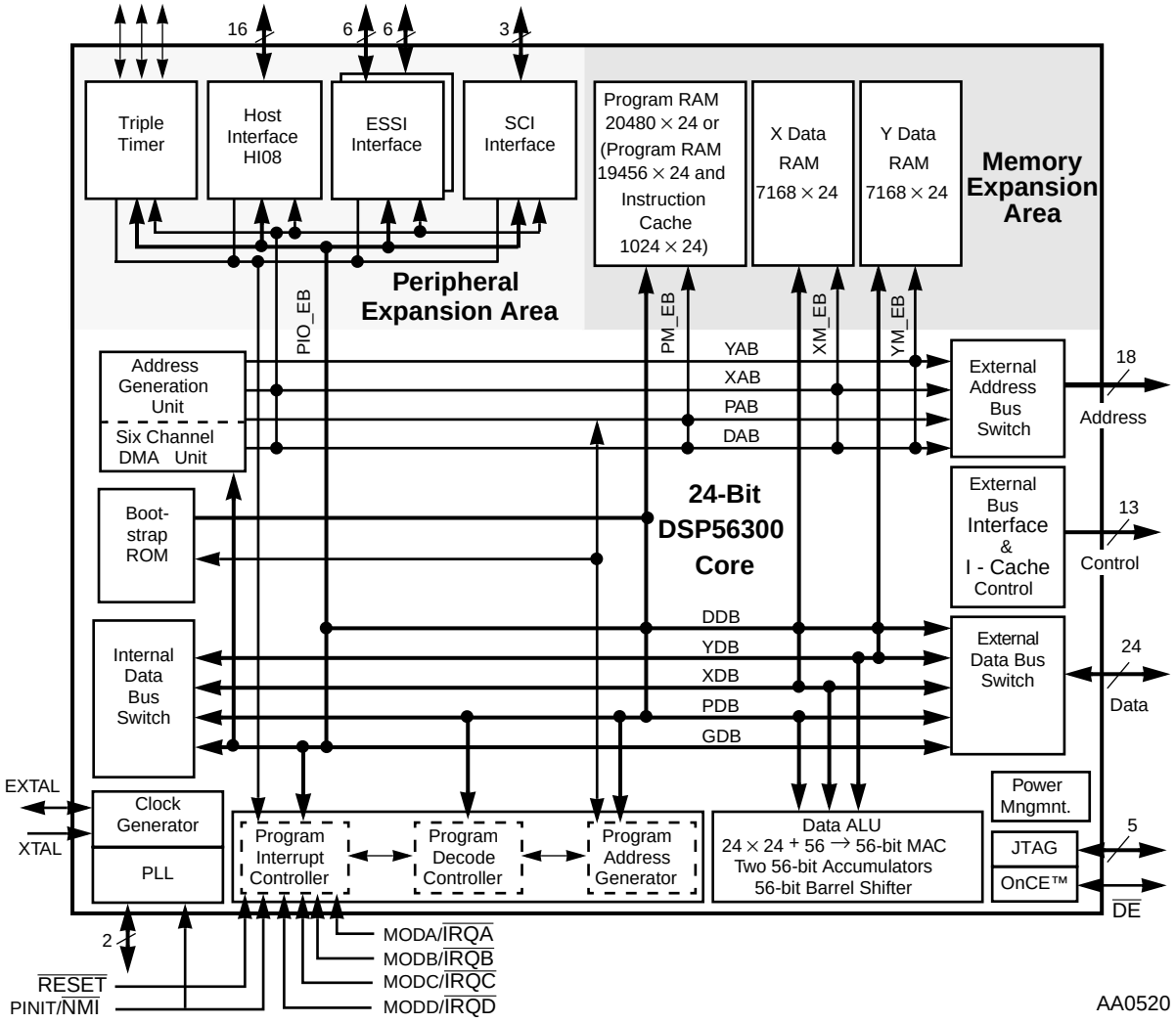

Figure 1 DSP56309 Block Diagram

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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FOR TECHNICAL ASSISTANCE:

Telephone: 1-800-521-6274

Email: dsphelp@dsp.sps.mot.com

Internet: http://www.motorola-dsp.com

Data Sheet Conventions

$\overline{\text{OVERBAR}}$	Used to indicate a signal that is active when pulled low (For example, the $\overline{\text{RESET}}$ pin is active when low.)
"asserted"	Means that a high true (active high) signal is high or that a low true (active low) signal is low
"deasserted"	Means that a high true (active high) signal is low or that a low true (active low) signal is high

Examples:

Signal/Symbol	Logic State	Signal State	Voltage[1]
$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
PIN	True	Asserted	V_{IH}/V_{OH}
PIN	False	Deasserted	V_{IL}/V_{OL}

Note: Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.

FEATURES

High Performance DSP56300 Core

- 80- and 100-million instructions per second (MIPS) with an 80- and 100-MHz clock at 3.0–3.6 V
- Object-code compatible with the DSP56000 core
- Highly parallel instruction set
- Data arithmetic logic unit (ALU)
  - Fully pipelined 24 x 24-bit parallel multiplier-accumulator (MAC)
  - 56-bit parallel barrel shifter (fast shift and normalization; bit stream generation and parsing)
  - Conditional ALU instructions
  - 24-bit or 16-bit arithmetic support under software control
- Program control unit (PCU)
  - Position independent code (PIC) support
  - Addressing modes optimized for DSP applications (including immediate offsets)
  - On-chip instruction cache controller
  - On-chip memory-expandable hardware stack
  - Nested hardware DO loops
  - Fast auto-return interrupts
- Direct memory access (DMA)
  - Six DMA channels supporting internal and external accesses
  - One-, two-, and three-dimensional transfers (including circular buffering)
  - End-of-block-transfer interrupts
  - Triggering from interrupt lines, all peripherals, and DMA channels
- Phase-locked loop (PLL)
  - Allows change of low-power divide factor (DF) without loss of lock
  - Output clock with skew elimination
- Hardware debugging support
  - On-Chip Emulation (OnCE™) module
  - Joint Test Action Group (JTAG) test access port (TAP)
  - Address trace mode reflects internal program RAM accesses at the external port

On-Chip Memory

- Program RAM, Instruction Cache, X data RAM, and Y data RAM size are programmable.

Instruction Cache	Switch Mode	Program RAM Size	Instruction Cache Size	X Data RAM Size	Y Data RAM Size
disabled	disabled	20480 × 24-bit	0	7168 × 24-bit	7168 × 24-bit
enabled	disabled	19456 × 24-bit	1024 × 24-bit	7168 × 24-bit	7168 × 24-bit
disabled	enabled	24576 × 24-bit	0	5120 × 24-bit	5120 × 24-bit
enabled	enabled	23552 × 24-bit	1024 × 24-bit	5120 × 24-bit	5120 × 24-bit

- 192 x 24-bit bootstrap ROM

Off-Chip Memory Expansion

- External memory expansion port
- Data memory expansion to two 256K × 24-bit word memory spaces (or up to two 4 M × 24-bit word memory spaces by using the address attribute AA0–AA3 signals)
- Program memory expansion to one 256K × 24-bit words memory space (or up to one 4 M × 24-bit word memory space by using the address attribute AA0–AA3 signals)
- Simultaneous glueless interface to four blocks of either SRAM or DRAM through chip select logic
- Supports interleaved, non-interfering access to both types of memory without losing in-page DRAM access, including DMA-driven access

On-Chip Peripherals

- Enhanced DSP56000-like 8-bit parallel host interface (HI08) supports a variety of buses (e.g., industry standard architecture) and provides glueless connection to a number of industry standard microcomputers, microprocessors, and DSPs
- Two enhanced synchronous serial interfaces (ESSI0 and ESSI1), each with one receiver and three transmitters (allows six-channel home theater)
- Serial communications interface (SCI) with baud rate generator
- Triple timer module
- Up to 34 programmable general purpose input / output (GPIO) pins, depending on which peripherals are enabled

Reduced Power Dissipation

- Very low-power CMOS design
- Fully-static logic, operation frequency down to 0 Hz (dc)
- Wait and stop low-power standby modes
- Optimized, cycle-by-cycle power management circuitry (instruction-dependent, peripheral-dependent, and mode-dependent)

TARGET APPLICATIONS

The DSP56309 is intended for applications benefiting from a large amount of on-chip memory, such as wireless infrastructure applications.

PRODUCT DOCUMENTATION

The three documents listed in the following table are required for a complete description of the DSP56309 and are necessary to design properly with the part. Chip errata—if any exist—are available at the Motorola website. Documentation is available from the following locations:

- A local Motorola distributor
- A Motorola semiconductor sales office
- A Motorola Literature Distribution Center
- The World Wide Web (WWW)

See the back cover for specific addresses and phone numbers.

See your Motorola distributor for detailed information about the multiple support options available to you.

Table 1 DSP56309 Documentation

Name	Description	Order Number
DSP56300 Family Manual	Detailed description of the DSP56300 family processor core and instruction set	DSP56300FM/AD
DSP56309 User's Manual	Detailed functional description of the DSP56309 memory configuration, operation, and register programming	DSP56309UM/D
DSP56309 Technical Data	DSP56309 features list and physical, electrical, timing, and package specifications	DSP56309/D

SECTION 1

PINOUT DIAGRAM

SIGNAL GROUPINGS

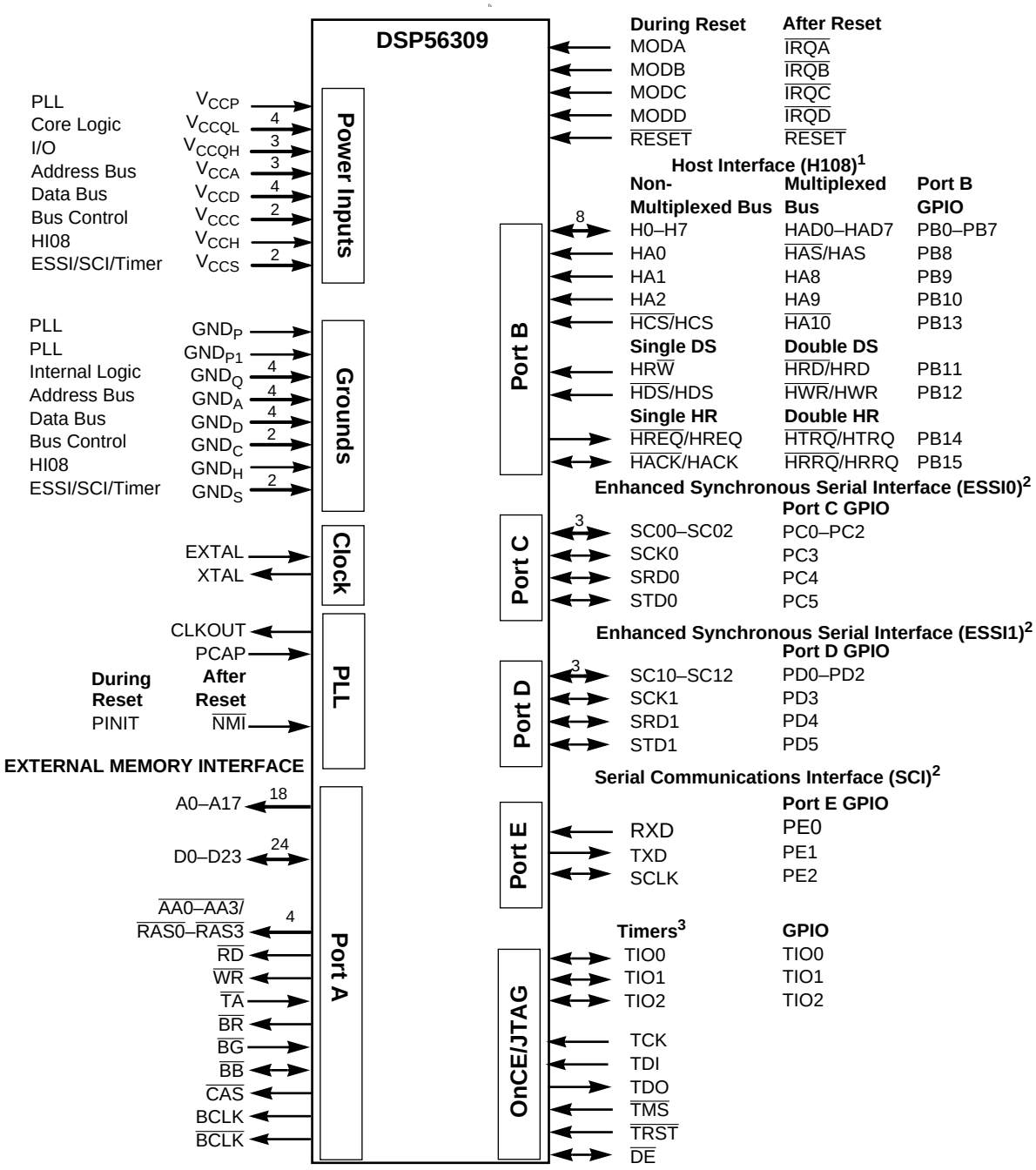
The input and output signals of the DSP56309 are organized into functional groups, as shown in **Table 1-1** and as illustrated in **Figure 1-1**. For a complete description of these signals, see the *DSP56309 User's Manual,* especially *Section 2, Signal/Connection Descriptions*.

Table 1-1 Functional Signal Groupings in the DSP56309

Functional Group		Number of Signals
Power (V_{CC})		20
Ground (GND)		19
Clock		2
PLL		3
Address bus	Port A[1]	18
Data bus		24
Bus control		13
Interrupt and mode control		5
Host interface (HI08)	Port B[2]	16
Enhanced synchronous serial interface (ESSI)	Ports C and D[3]	12
Serial communication interface (SCI)	Port E[4]	3
Timer		3
OnCE/JTAG port		6

Note:
1. Port A signals define the external memory interface port, including the external address bus, data bus, and control signals.
2. Port B signals are the HI08 port signals multiplexed with the GPIO signals.
3. Port C and D signals are the two ESSI port signals multiplexed with the GPIO signals.
4. Port E signals are the SCI port signals multiplexed with the GPIO signals.

Figure 1-1 is a diagram of DSP56309 signals by functional group.



Notes:
1. The HI08 port supports a non-multiplexed or a multiplexed bus, single or double data strobe (DS), and single or double host request (HR) configurations. Because each of these modes is configured independently, any combination of these modes is possible. These HI08 signals can also be configured alternately as GPIO signals (PB0–PB15). Signals with dual designations (e.g., HAS/HAS) have configurable polarity.
2. The ESSI0, ESSI1, and SCI signals are multiplexed with the port C GPIO signals (PC0–PC5), port D GPIO signals (PD0–PD5), and port E GPIO signals (PE0–PE2), respectively.
3. TIO0–TIO2 can be configured as GPIO signals.

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Figure 1-1 Signals Identified by Functional Group

In the DSP56309, certain pins have a weak keeper. Accordingly, a tri-stateable signal on such a pin is not electrically disconnected during a reset; rather, such a signal is driven by the weak keeper, as documented in the *DSP56309 User's Manual, Section 2, Signal/Connection Descriptions*. Consequently, the value of pull-up or pull-down resistors on such pins should be taken into account for those signals. The value of such resistors appears in the *DSP56309 User's Manual, Section 2, Signal/Connection Descriptions* in the description of those signals. **Table 1-2** lists the pins that have a weak keeper.

Table 1-2 Pins with Weak Keepers on the DSP56309

Block	Pins
Host	HP[0:4]
	HP[5:15]
Data	HD[0:6]
	HD[7:23]
Enhanced synchronous serial interface (ESSI)	SC12
	SC11
	SRD1
	STD1
	SC10
	SCK1
	SRD0
	STD0
	SC00
	SCK0
	SC02
	SC01
Timer	TIO[0:2]
Synchronous communication interface (SCI)	RXD
	TXD
	SCLK

SECTION 2

SPECIFICATIONS

INTRODUCTION

The DSP56309 is fabricated in high density CMOS with transistor-transistor logic (TTL) compatible inputs and outputs. The DSP56309 specifications are preliminary, based on design simulations, and may not be fully tested or guaranteed at this early stage of the product life cycle. In particular, certain speeds may not yet be available at certain power ranges. Finalized specifications will be published after full characterization and device qualifications are complete.

MAXIMUM RATINGS

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CCX}).

Note: In the calculation of timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a "maximum" value for a specification will never occur in the same device that has a "minimum" value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 2-1 Maximum Ratings

Rating[1]	Symbol	Value[1, 2]	Unit
Supply Voltage • PLL (V_{CCP}) and core (V_{CCQL}) • Other (I/O)	V_{CCx}	 −0.3 to +3.3 −0.3 to +4.0	V
All input voltages	V_{IN}	GND − 0.3 to V_{CC} + 0.3	V
Current drain per pin excluding V_{CC} and GND	I	10	mA
Operating temperature range[3]	T_J	−40 to +100	°C
Storage temperature	T_{STG}	−55 to +150	°C

Note: 1. GND = 0 V, V_{CCx} = 3.3 V ± 0.3 V, T_J = –40°C to +100°C, CL = 50 pF
2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the maximum rating may affect device reliability or cause permanent damage to the device.
3. See **Thermal Design Considerations** on page 4-1 for an equation relating ambient and junction temperature.

THERMAL CHARACTERISTICS

Table 2-2 Thermal Characteristics

Characteristic	Symbol	TQFP Value	PBGA[1] Value	PBGA[2] Value	Unit
Junction-to-ambient thermal resistance[3]	$R_{\theta JA}$ or θ_{JA}	49.3	49.4	28.5	°C/W
Junction-to-case thermal resistance[4]	$R_{\theta JC}$ or θ_{JC}	8.2	12.0	—	°C/W
Thermal characterization parameter	Ψ_{JT}	5.5	2.0	—	°C/W

Note: 1. These are simulated values; testing is not complete. See **Note 3** for test board conditions.
2. These are simulated values; testing is not complete. The test board has two, 2-ounce signal layers and two 1-ounce solid ground planes internal to the test board.
3. Junction-to-ambient thermal resistance is based on measurements on a horizontal single-sided printed circuit board per SEMI G38-87 in natural convection. (SEMI is Semiconductor Equipment and Materials International, 805 East Middlefield Rd., Mountain View, CA 94043, (415) 964-5111.) Measurements were done with parts mounted on thermal test boards conforming to specification EIA/JESD51-3.
4. Junction-to-case thermal resistance is based on measurements using a cold plate per SEMI G30-88, with the exception that the cold plate temperature is used for the case temperature.

DC ELECTRICAL CHARACTERISTICS

Table 2-3 DC Electrical Characteristics[1]

Characteristics	Symbol	Min	Typ	Max	Unit
Supply voltage (V_{CCQL}, V_{CCP}, V_{CCQH}, V_{CCA}, V_{CCD}, V_{CCC}, V_{CCH}, V_{CCS})	V_{CCx}	3.0	3.3	3.6	V
Input high voltage • D0–D23, $\overline{BG}$, $\overline{BB}$, $\overline{TA}$ • MOD[2] / $\overline{IRQ}$[2], $\overline{RESET}$, PINIT / $\overline{NMI}$ and all JTAG / ESSI / SCI / Timer / HI08 pins • EXTAL[3]	 V_{IH} V_{IHP} V_{IHX}	 2.0 2.0 $0.8 \times V_{CCQH}$	 — — —	 V_{CCQH} V_{CCQH} + 0.3 V_{CCQH}	 V V V
Input low voltage • D0–D23, $\overline{BG}$, $\overline{BB}$, $\overline{TA}$, MOD[2] / $\overline{IRQ}$[2], $\overline{RESET}$, PINIT • All JTAG / ESSI / SCI / Timer / HI08 pins • EXTAL[3]	V_{IL} V_{ILP} V_{ILX}	–0.3 –0.3 –0.3	— — —	0.8 0.8 $0.2 \times V_{CCQH}$	V V V
Input leakage current	I_{IN}	–10	—	10	µA
High impedance (off-state) input current (@ 2.4 V / 0.4 V)	I_{TSI}	–10	—	10	µA
Output high voltage • TTL (I_{OH} = –0.4 mA)[4,5] • CMOS (I_{OH} = –10 µA)[4]	V_{OH} 	 V_{CC} – 0.4 V_{CCQH} – 0.01	 — —	 — —	 V V
Output low voltage • TTL (port A I_{OL} = 1.6 mA, non-port A I_{OL} = 3.2 mA, open-drain pins I_{OL} = 6.7 mA)[4,5] • CMOS (I_{OL} = 10 µA)[4]	V_{OL} 	 — —	 — —	 0.4 0.01	 V V
Internal supply current[6]: • In normal mode • In wait mode[7] • In stop mode[8]	 I_{CCI} I_{CCW} I_{CCS}	 — — —	 **80 MHz**: 128 **100 MHz**: 160 5 100	 — — — —	 mA mA mA µA
PLL supply current in stop mode[4]		—	1	2.5	mA
Input capacitance[4]	C_{IN}	—	—	10	pF

Table 2-3 DC Electrical Characteristics[1](Continued)

Characteristics	Symbol	Min	Typ	Max	Unit

Note:
1. V_{CCx} = 3.3 V ± 0.3 V; T_J = –40˚C to +100 ˚C, C_L = 50 pF
2. Refers to MODA / $\overline{\text{IRQA}}$, MODB / $\overline{\text{IRQB}}$, MODC / $\overline{\text{IRQC}}$, and MODD / $\overline{\text{IRQD}}$ pins
3. Driving EXTAL to the low V_{IHX} or the high V_{ILX} value may cause additional power consumption (dc current). To minimize power consumption, the minimum V_{IHX} should be no lower than $0.9 \times V_{CCx}$ and the maximum V_{ILX} should be no higher than $0.1 \times V_{CCx}$.
4. Periodically sampled and not 100% tested
5. This characteristic does not apply to XTAL and PCAP.
6. **Power Consumption Considerations** on page 4-4 provides a formula to compute the estimated current requirements in normal mode. In order to obtain these results, all inputs must be terminated (i.e., not allowed to float). Measurements are based on synthetic intensive DSP benchmarks such as those in the *DSP56309 User's Manual*. The power consumption numbers in this specification are 90% of the measured results of this benchmark. This reflects typical DSP applications. Typical internal supply current is measured with V_{CCx} = 3.3 V at T_J = 100˚C. Maximum internal supply current may vary widely and is application dependent.
7. In order to obtain these results, all inputs must be terminated (i.e., not allowed to float). PLL and XTAL signals are disabled during stop state.
8. In order to obtain these results, all inputs, which are not disconnected at stop mode, must be terminated (i.e., not allowed to float).

AC ELECTRICAL CHARACTERISTICS

The timing waveforms shown in the ac electrical characteristics section are tested with a V_{IL} maximum of 0.3 V and a V_{IH} minimum of 2.4 V for all pins except EXTAL, which is tested using the input levels shown in Note 6 of the previous table. AC timing specifications, which are referenced to a device input signal, are measured in production with respect to the 50% point of the respective input signal's transition. DSP56309 output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at 0.8 V and 2.0 V, respectively.

INTERNAL CLOCKS

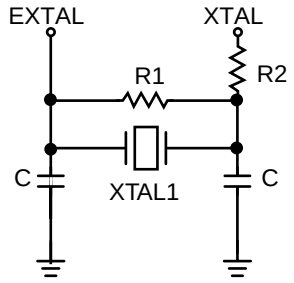
Table 2-4 Internal Clocks, CLKOUT

Characteristics	Symbol	Expression[1, 2]		
		Min	**Typ**	**Max**
Internal operation frequency and CLKOUT with PLL enabled	f	—	(Ef × MF) / (PDF × DF)	—
Internal operation frequency and CLKOUT with PLL disabled	f	—	Ef / 2	—
Internal clock and CLKOUT high period • With PLL disabled • With PLL enabled and MF ≤ 4 • With PLL enabled and MF > 4	T_H	— 0.49 × ET_C × PDF × DF / MF 0.47 × ET_C × PDF × DF / MF	ET_C — —	— 0.51 × ET_C × PDF × DF / MF 0.53 × ET_C × PDF × DF / MF
Internal clock and CLKOUT low period • With PLL disabled • With PLL enabled and MF ≤ 4 • With PLL enabled and MF > 4	T_L	— 0.49 × ET_C × PDF × DF / MF 0.47 × ET_C × PDF × DF / MF	ET_C — —	— 0.51 × ET_C × PDF × DF / MF 0.53 × ET_C × PDF × DF / MF
Internal clock and CLKOUT cycle time with PLL enabled	T_C	—	ET_C × PDF × DF / MF	—
Internal clock and CLKOUT cycle time with PLL disabled	T_C	—	2 × ET_C	—
Instruction cycle time	I_{CYC}	—	T_C	—

Note: 1. DF = Division factor
Ef = External frequency
ET_C = External clock cycle
MF = Multiplication factor
PDF = Predivision factor
T_C = Internal clock cycle
2. See *PLL and Clock Generation* in the *DSP56300 Family Manual* for a detailed discussion of the PLL.

EXTERNAL CLOCK OPERATION

The DSP56309 system clock may be derived from the on–chip crystal oscillator, as shown in **Figure 1** on the cover page, or it may be externally supplied. An externally supplied square wave voltage source should be connected to EXTAL, as in **Figure 2-2**, leaving XTAL physically disconnected from the board or socket.

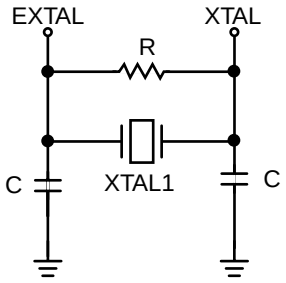


Fundamental Frequency
Fork Crystal Oscillator

Suggested Component Values:

f_{OSC} = 32.768 kHz
R1= 3.9 MΩ ± 10%
C = 22 pF ± 20%
R2 = 200 kΩ ± 10%

Calculations were done for a 32.768 kHz crystal with the following parameters:
a load capacitance (C_L) of 12.5 pF,
a shunt capacitance (C_0) of 1.8 pF,
a series resistance of 40 kΩ, and
a drive level of 1 μW.



Fundamental Frequency
Crystal Oscillator

Suggested Component Values:

f_{OSC} = 4 MHz
R = 680 kΩ ± 10%
C = 56 pF ± 20%

f_{OSC} = 20 MHz
R = 680 kΩ ± 10%
C = 22 pF ± 20%

Calculations were done for a 4/20 MHz crystal with the following parameters:
a C_L of 30/20 pF,
a C_0 of 7/6 pF,
a series resistance of 100/20 Ω, and
a drive level of 2 mW.

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Figure 2-1 Crystal Oscillator Circuits

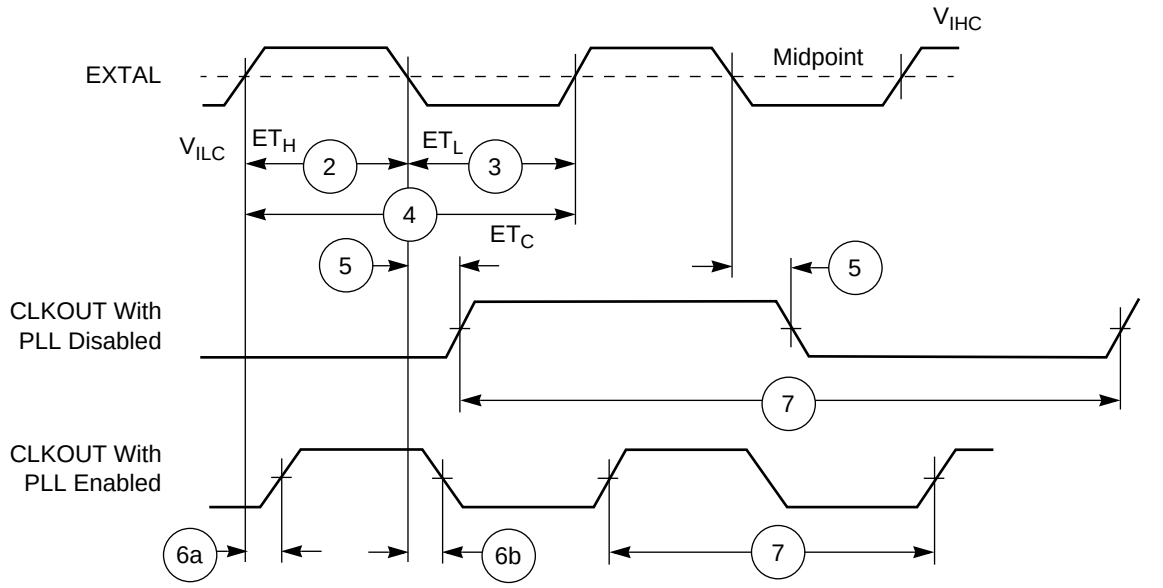


Figure 2-2 External Clock Timing

Table 2-5 Clock Operation

No.	Characteristics	Symbol	80 MHz		100 MHz	
			Min	Max	Min	Max
1	Frequency of EXTAL (EXTAL Pin Frequency) The rise and fall time of this external clock should be 3 ns maximum.	Ef	0	80.0	0	100.0
2	EXTAL input high[1, 2] • With PLL disabled (46.7%–53.3% duty cycle[3]) • With PLL enabled (42.5%–57.5% duty cycle[3])	ET_H	5.84 ns 5.31 ns	∞ 157.0 µs	4.67 ns 4.25 ns	∞ 157.0 µs
3	EXTAL input low[1, 2] • With PLL disabled (46.7%–53.3% duty cycle[3]) • With PLL enabled (42.5%–57.5% duty cycle[3])	ET_L	5.84 ns 5.31 ns	∞ 157.0 µs	4.67 ns 4.25 ns	∞ 157.0 µs
4	EXTAL cycle time[2] • With PLL disabled • With PLL enabled	ET_C	12.50 ns 12.50 ns	∞ 273.1 µs	10.00 ns 10.00 ns	∞ 273.1 µs

Table 2-5 Clock Operation(Continued)

No.	Characteristics	Symbol	80 MHz		100 MHz	
			Min	Max	Min	Max
5	CLKOUT change from EXTAL fall with PLL disabled	—	4.3 ns	11.0 ns	4.3 ns	11.0 ns
6	CLKOUT rising edge from EXTAL rising edge with PLL enabled (MF = 1, PDF = 1, Ef > 15 MHz)[4, 5]	—	0.0 ns	1.8 ns	0.0 ns	1.8 ns
	CLKOUT falling edge from EXTAL rising edge with PLL enabled (MF = 2 or 4, PDF = 1, Ef > 15 MHz)[4, 5]	—	0.0 ns	1.8 ns	0.0 ns	1.8 ns
	CLKOUT falling edge from EXTAL falling edge with PLL enabled (MF ≤ 4, PDF ≠ 1, Ef / PDF > 15 MHz)[4, 5]	—	0.0 ns	1.8 ns	0.0 ns	1.8 ns
7	Instruction cycle time = I_{CYC} = T_C[6] as in **Table 2-4** (46.7%–53.3% duty cycle) • With PLL disabled • With PLL enabled	I_{CYC}	 25.0 ns 12.50 ns	 ∞ 8.53 µs	 20.0 ns 10.00 ns	 ∞ 8.53 µs

Note:
1. Measured at 50% of the input transition
2. The maximum value for PLL enabled is given for minimum V_{CO} and maximum MF.
3. The indicated duty cycle is for the specified maximum frequency for which a part is rated. The minimum clock high or low time required for correction operation, however, remains the same at lower operating frequencies; therefore, when a lower clock frequency is used, the signal symmetry may vary from the specified duty cycle as long as the minimum high time and low time requirements are met.
4. Periodically sampled and not 100% tested.
5. The skew is not guaranteed for any other MF value.
6. The maximum value for PLL enabled is given for minimum V_{CO} and maximum DF.

PHASE-LOCKED LOOP (PLL) CHARACTERISTICS

Table 2-6 PLL Characteristics

Characteristics	80 MHz		100 MHz		Unit
	Min	Max	Min	Max	
V_{CO} frequency when PLL enabled ($MF \times E_f \times 2 / PDF$)	30	160	30	200	MHz
PLL external capacitor (PCAP pin to V_{CCP}) (C_{PCAP}[1)] •@ MF ≤ 4 •@ MF > 4	 (MF × 580) – 100 MF × 830	 (MF ×780) – 140 MF × 1470	 (MF × 580) – 100 MF × 830	 (MF × 780) – 140 MF × 1470	 pF pF

Note: C_{PCAP} is the value of the PLL capacitor (connected between the PCAP pin and V_{CCP}). The recommended value in pF for C_{PCAP} can be computed from one of the following equations:
$(680 \times MF) - 120$, for $MF < 4$, or
$1100 \times MF$, for $MF \geq 4$.

RESET, STOP, MODE SELECT, AND INTERRUPT TIMING

Table 2-7 Reset, Stop, Mode Select, and Interrupt Timing[1]

No.	Characteristics	Expression	80 MHz		100 MHz		Unit
			Min	Max	Min	Max	
8	Delay from $\overline{\text{RESET}}$ assertion to all pins at reset value[2]	—	—	26.0	—	26.0	ns
9	Required $\overline{\text{RESET}}$ duration[3]						
	•Power on, external clock generator, PLL disabled	$50 \times ET_C$	625.0	—	500.0	—	ns
	•Power on, external clock generator, PLL enabled	$1000 \times ET_C$	12.5	—	10.0	—	µs
	•Power on, internal oscillator	$75000 \times ET_C$	1.0	—	0.75	—	ms
	•During STOP, XTAL disabled (PCTL Bit 16 = 0)	$75000 \times ET_C$	1.0	—	0.75	—	ms
	•During STOP, XTAL enabled (PCTL Bit 16 = 1)	$2.5 \times T_C$	31.3	—	25.0	—	ns
	•During normal operation	$2.5 \times T_C$	31.3	—	25.0	—	ns

Table 2-7 Reset, Stop, Mode Select, and Interrupt Timing[1](Continued)

No.	Characteristics	Expression	80 MHz		100 MHz		Unit
			Min	Max	Min	Max	
10	Delay from asynchronous $\overline{\text{RESET}}$ deassertion to first external address output (internal reset deassertion)[4]						
	• Minimum	**80 MHz**: $3.25 \times T_C + 2.0$	42.6	—	—	—	ns
		100 MHz: $3.25 \times T_C + 2.0$	—	—	34.5	—	ns
	• Maximum	**80 MHz**: $20.25\ T_C + 9.95$	—	263.1	—	—	ns
		100 MHz: $20.25\ T_C + 7.50$	—	—	—	211.5	ns
11	Synchronous reset setup time from $\overline{\text{RESET}}$ deassertion to CLKOUT transition 1	T_C					
	• Minimum		7.4	—	5.9	—	ns
	• Maximum		—	12.5	—	10.0	ns
12	Synchronous reset deasserted, delay time from the CLKOUT transition 1 to the first external address output						
	• Minimum	$3.25 \times T_C + 1.0$	41.6	—	33.5	—	ns
	• Maximum	$20.25\ T_C + 5.0$	—	258.1	—	207.5	ns
13	Mode select setup time	—	30.0	—	30.0	—	ns
14	Mode select hold time	—	0.0	—	0.0	—	ns
15	Minimum edge-triggered interrupt request assertion width	—	8.25	—	6.6	—	ns
16	Minimum edge-triggered interrupt request deassertion width	—	8.25	—	6.6	—	ns
17	Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{NMI}}$ assertion to external memory access address out valid						
	• Caused by first interrupt instruction fetch	$4.25 \times T_C + 2.0$	55.1	—	44.5	—	ns
	• Caused by first interrupt instruction execution	$7.25 \times T_C + 2.0$	92.6	—	74.5	—	ns

Table 2-7 Reset, Stop, Mode Select, and Interrupt Timing[1](Continued)

No.	Characteristics	Expression	80 MHz		100 MHz		Unit
			Min	Max	Min	Max	
18	Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{NMI}}$ assertion to general-purpose transfer output valid caused by first interrupt instruction execution	$10 \times T_C + 5.0$	130.0	—	105.0	—	ns
19	Delay from address output valid caused by first interrupt instruction execute to interrupt request deassertion for level sensitive fast interrupts[6, 7]	**80 MHz**[5]: $3.75 \times T_C + WS \times T_C - 12.4$	—	Note 5		Note 5	ns
		100 MHz[5]: $3.75 \times T_C + WS \times T_C - 10.94$			—		ns
20	Delay from $\overline{\text{RD}}$ assertion to interrupt request deassertion for level sensitive fast interrupts[6, 7]	**80 MHz**[5]: $3.25 \times T_C + WS \times T_C - 12.4$	—	Note 5		Note 5	ns
		100 MHz[5]: $3.25 \times T_C + WS \times T_C - 10.94$			—		ns
21	Delay from $\overline{\text{WR}}$ assertion to interrupt request deassertion for level sensitive fast interrupts[6, 7]			Note 5		Note 5	
	• DRAM for all WS	**80 MHz**[5]: $(WS + 3.5) \times T_C - 12.4$	—				ns
		100 MHz[5]: $(WS + 3.5) \times T_C - 10.94$			—		ns
	• SRAM WS = 1	**80 MHz**[5]: $(WS + 3.5) \times T_C - 12.4$	—				ns
		100 MHz[5]: $(WS + 3.5) \times T_C - 10.94$			—		ns
	• SRAM WS = 2, 3	**80 MHz**[5]: $(WS + 3) \times T_C - 12.4$	—				ns
		100 MHz[5]: $(WS + 3) \times T_C - 10.94$			—		ns
	• SRAM WS ≥ 4	**80 MHz**[5]: $(WS + 2.5) \times T_C - 12.4$	—				ns
		100 MHz[5]: $(WS + 2.5) \times T_C - 10.94$			—		ns
22	Synchronous interrupt setup time from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{NMI}}$ assertion to the CLKOUT transition 2	—	7.4	T_C	5.9	T_C	ns

Table 2-7 Reset, Stop, Mode Select, and Interrupt Timing[1](Continued)

No.	Characteristics	Expression	80 MHz		100 MHz		Unit
			Min	Max	Min	Max	
23	Synchronous interrupt delay time from the CLKOUT transition 2 to the first external address output valid caused by the first instruction fetch after coming out of wait processing state						
	• Minimum	$9.25 \times T_C + 1.0$	116.6	—	93.5	—	ns
	• Maximum	$24.75 \times T_C + 5.0$	—	314.4	—	252.5	ns
24	Duration for $\overline{IRQA}$ assertion to recover from Stop state	—	7.4	—	5.9	—	ns
25	Delay from $\overline{IRQA}$ assertion to fetch of first instruction (when exiting stop)[2, 8]						
	• PLL is not active during stop (PCTL bit 17 = 0) and stop delay is enabled (OMR bit 6 = 0)	$PLC \times ET_C \times PDF + (128K - PLC/2) \times T_C$	1.6	17.0	1.3	13.6	ms
	• PLL is not active during stop (PCTL bit 17 = 0) and stop delay is not enabled (OMR bit 6 = 1)	$PLC \times ET_C \times PDF + (23.75 \pm 0.5) \times T_C$	290.6 ns	15.4 ms	232.5 ns	12.3 ms	
	• PLL is active during stop (PCTL bit 17 = 1) (implies no Stop delay)	$(8.25 \pm 0.5) \times T_C$	96.9	109.4	77.5	87.5	ns
26	Duration of level sensitive $\overline{IRQA}$ assertion to ensure interrupt service (when exiting stop)[2, 8]						
	• PLL is not active during stop (PCTL bit 17 = 0) and stop delay is enabled (OMR bit 6 = 0)	$PLC \times ET_C \times PDF + (128K - PLC/2) \times T_C$	17.0	—	13.6	—	ms
	• PLL is not active during stop (PCTL bit 17 = 0) and stop delay is not enabled (OMR bit 6 = 1)	$PLC \times ET_C \times PDF + (20.5 \pm 0.5) \times T_C$	15.4	—	12.3	—	ms
	• PLL is active during stop (PCTL bit 17 = 1) (implies no stop delay)	$5.5 \times T_C$	68.8	—	55.0	—	ns

Table 2-7 Reset, Stop, Mode Select, and Interrupt Timing[1](Continued)

No.	Characteristics	Expression	80 MHz		100 MHz		Unit
			Min	Max	Min	Max	
27	Interrupt requests rate						
	• HI08, ESSI, SCI, Timer	$12T_C$	—	150.0	—	120.0	ns
	• DMA	$8T_C$	—	100.0	—	80.0	ns
	• $\overline{IRQ}$, $\overline{NMI}$ (edge trigger)	$8T_C$	—	100.0	—	80.0	ns
	• $\overline{IRQ}$, $\overline{NMI}$ (level trigger)	$12T_C$	—	150.0	—	120.0	ns
28	DMA requests rate						
	• Data read from HI08, ESSI, SCI	$6T_C$	—	75.0	—	60.0	ns
	• Data write to HI08, ESSI, SCI	$7T_C$	—	87.5	—	70.0	ns
	• Timer	$2T_C$	—	25.0	—	20.0	ns
	• $\overline{IRQ}$, $\overline{NMI}$ (edge trigger)	$3T_C$	—	37.5	—	30.0	ns
29	Delay from $\overline{IRQA}$, $\overline{IRQB}$, $\overline{IRQC}$, $\overline{IRQD}$, $\overline{NMI}$ assertion to external memory (DMA source) access address out valid	$4.25 \times T_C + 2.0$	55.1	—	44.0	—	ns

Note:
1. V_{CCQL} = 3.3 V ± 0.3 V; T_J = –40°C to +100°C, C_L = 50 pF
2. Periodically sampled and not 100% tested.
3. For an external clock generator, $\overline{RESET}$ duration is measured during the time in which $\overline{RESET}$ is asserted, V_{CCx} is valid, and the EXTAL input is active and valid.

   For internal oscillator, $\overline{RESET}$ duration is measured during the time in which $\overline{RESET}$ is asserted and V_{CCx} is valid. The specified timing reflects the crystal oscillator stabilization time after power-up. This number is affected both by the specifications of the crystal and other components connected to the oscillator and reflects worst case conditions.

   When the V_{CCx} is valid, but the other "required $\overline{RESET}$ duration" conditions (as specified above) have not been yet met, the device circuitry will be in an uninitialized state that can result in significant power consumption and heat-up. Designs should minimize this state to the shortest possible duration.
4. If PLL does not lose lock, then these values are valid.
5. Use expression to compute maximum value.
6. When using fast interrupts and $\overline{IRQA}$, $\overline{IRQB}$, $\overline{IRQC}$, and $\overline{IRQD}$ are defined as level-sensitive, timings 19 through 21 apply to prevent multiple interrupt service. To avoid these timing restrictions, the deasserted edge-triggered mode is recommended when using fast interrupts. Long interrupts are recommended when using level-sensitive mode.
7. WS = number of wait states (measured in clock cycles, number of T_C)
8. When there is an expression with both a minimum and maximum value, use the expression to compute worst case.

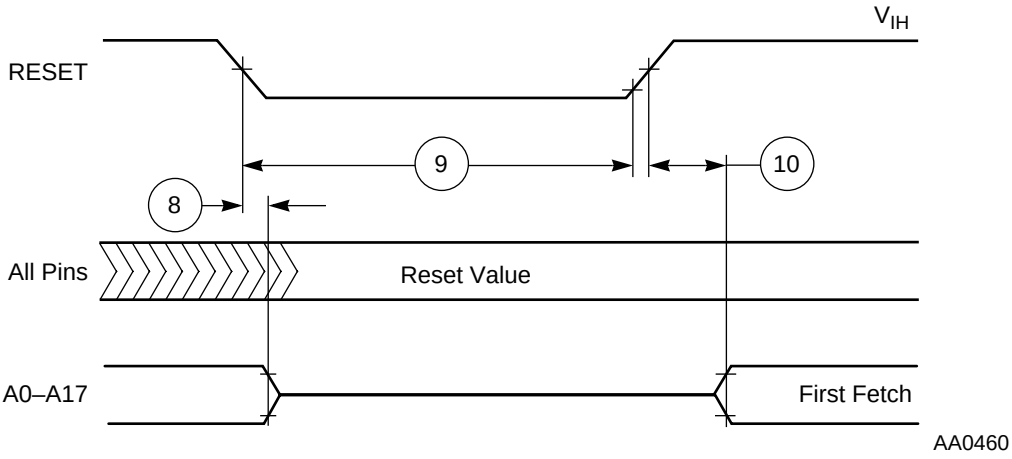


Figure 2-3 Reset Timing

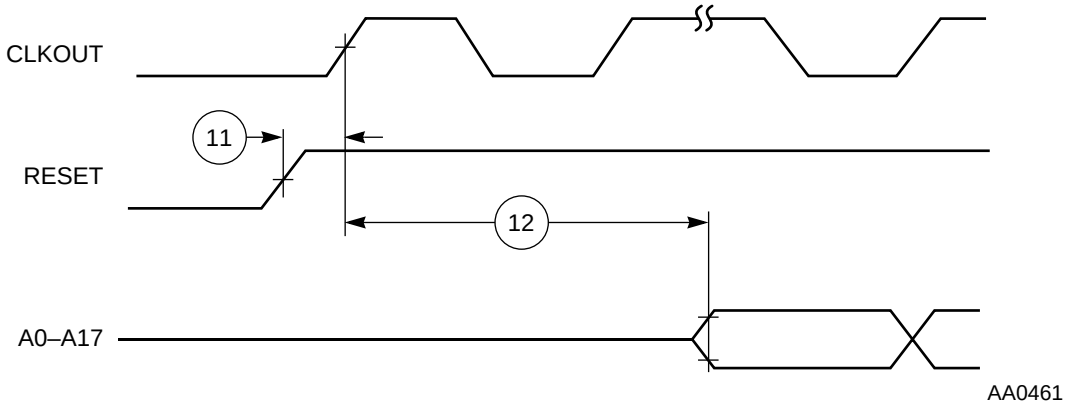
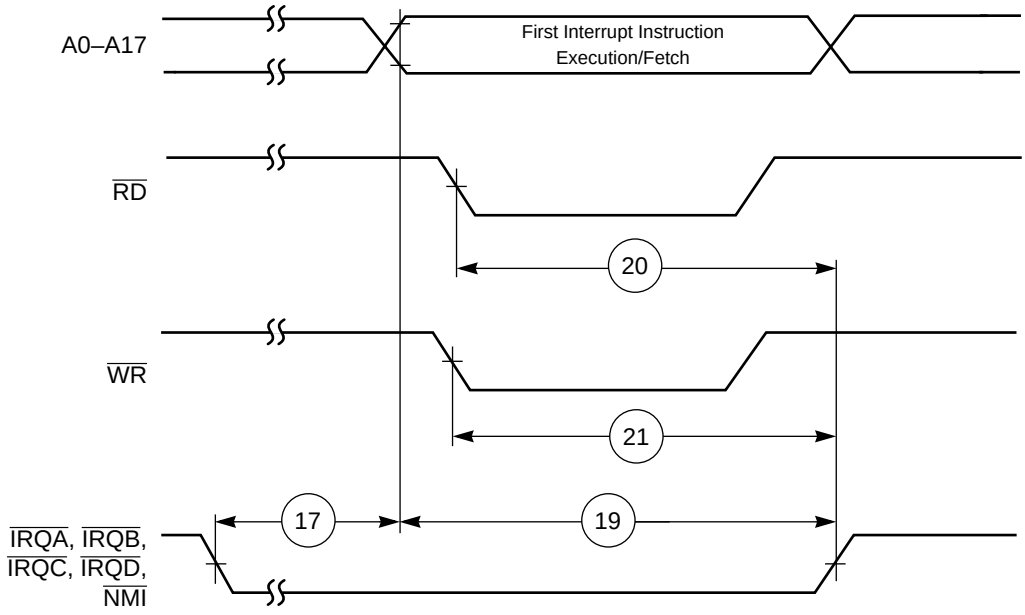
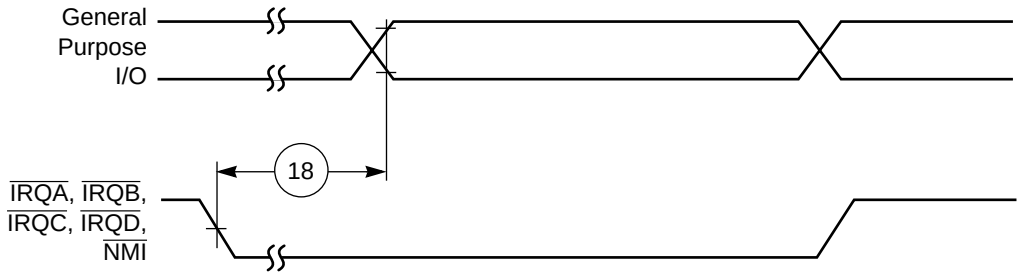


Figure 2-4 Synchronous Reset Timing



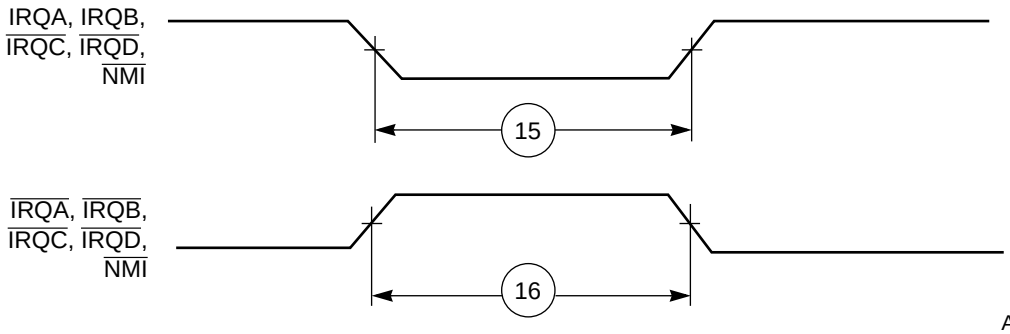
a) First Interrupt Instruction Execution



b) General Purpose I/O

AA0462

Figure 2-5 External Fast Interrupt Timing



AA0463

Figure 2-6 External Interrupt Timing (Negative Edge-Triggered)

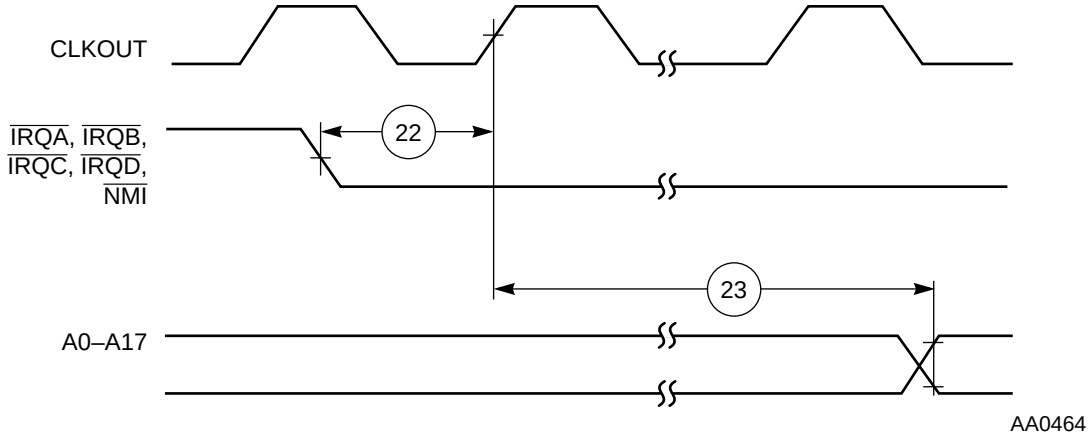


Figure 2-7 Synchronous Interrupt from Wait State Timing

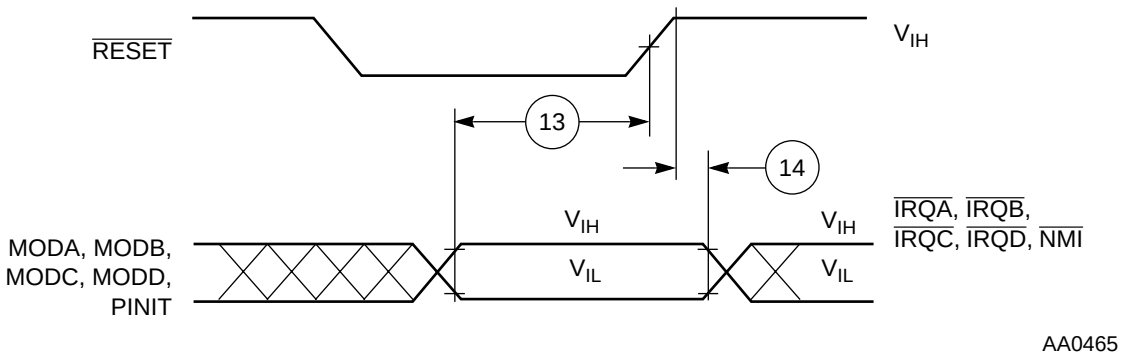


Figure 2-8 Operating Mode Select Timing

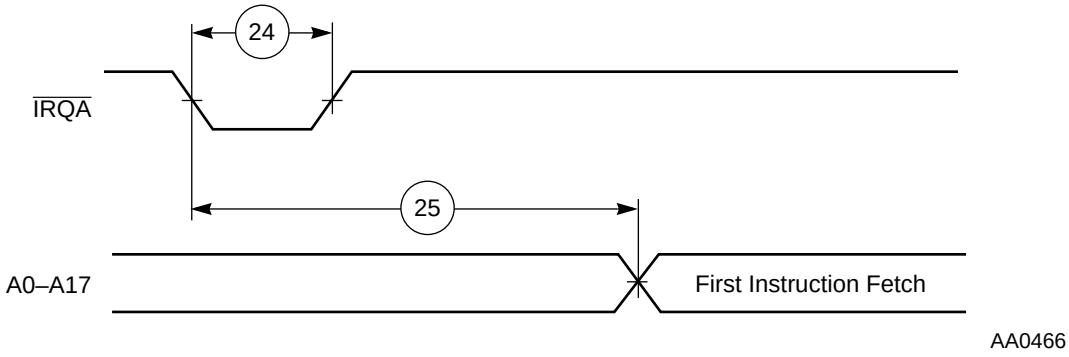


Figure 2-9 Recovery from Stop State Using IRQA

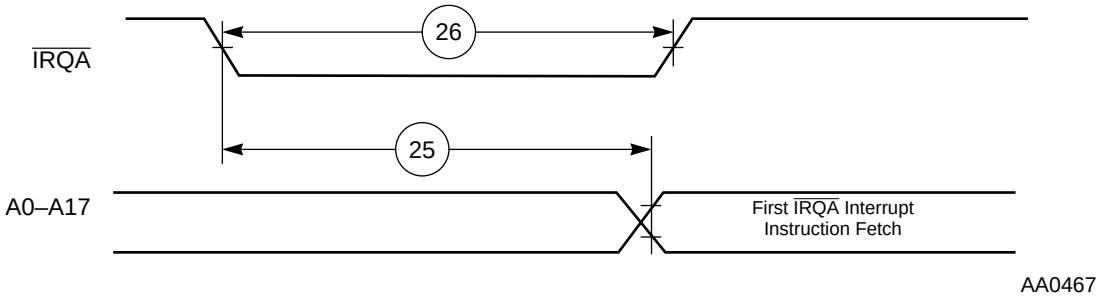


Figure 2-10 Recovery from Stop State Using IRQA Interrupt Service

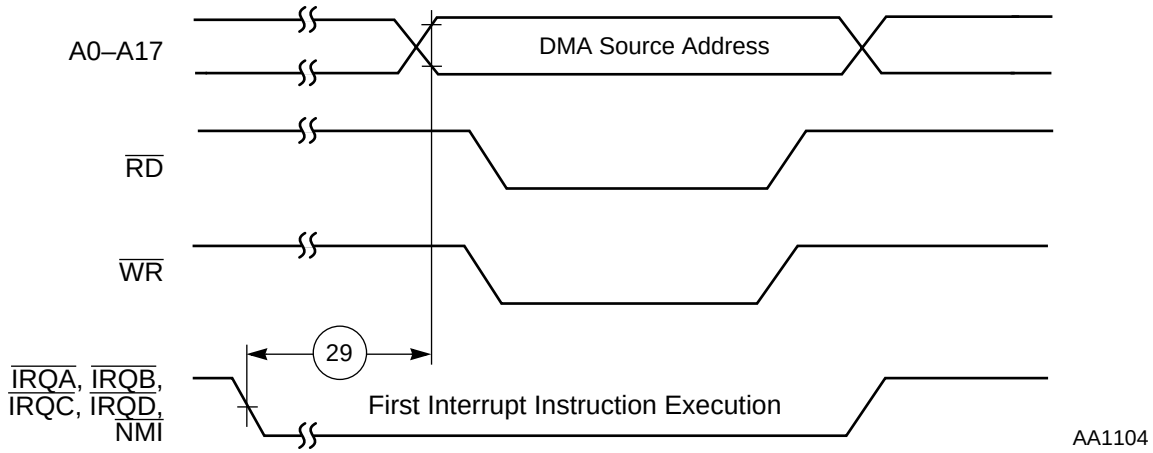


Figure 2-11 External Memory Access (DMA Source) Timing

EXTERNAL MEMORY INTERFACE (PORT A)

SRAM Timing

Table 2-8 SRAM Read and Write Accesses[1]

No.	Characteristics	Symbol	Expression[2]	80 MHz		100 MHz		Unit
				Min	Max	Min	Max	
100	Address valid and AA assertion pulse width	t_{RC}, t_{WC}	$(WS + 1) \times T_C - 4.0$ [1 ≤ WS ≤ 3]	21.0	—	16.0	—	ns
			$(WS + 2) \times T_C - 4.0$ [4 ≤ WS ≤ 7]	71.0	—	56.0	—	ns
			$(WS + 3) \times T_C - 4.0$ [WS ≥ 8]	133.5	—	106.0	—	ns
101	Address and AA valid to $\overline{WR}$ assertion	t_{AS}	**80 MHz:** $0.25 \times T_C - 3.0$ [WS = 1]	0.1	—	—	—	ns
			100 MHz: $0.25 \times T_C - 2.4$ [WS = 1]	—	—	0.1	—	ns
			All frequencies: $0.75 \times T_C - 4.0$ [2 ≤ WS ≤ 3]	5.4	—	3.5	—	ns
			$1.25 \times T_C - 4.0$ [WS ≥ 4]	11.6	—	8.5	—	ns
102	$\overline{WR}$ assertion pulse width	t_{WP}	$1.5 \times T_C - 4.5$ [WS = 1]	14.3	—	10.5	—	ns
			$WS \times T_C - 4.0$ [2 ≤ WS ≤ 3]	21.0	—	16.0	—	ns
			$(WS - 0.5) \times T_C - 4.0$ [WS ≥ 4]	39.8	—	31.0	—	ns
103	$\overline{WR}$ deassertion to address not valid	t_{WR}	**80 MHz:** $0.25 \times T_C - 3.0$ [1 ≤ WS ≤ 3]	0.1	—	—	—	ns
			100 MHz: $0.25 \times T_C - 2.4$ [1 ≤ WS ≤ 3]	—	—	0.1	—	ns
			All frequencies: $1.25 \times T_C - 4.0$ [4 ≤ WS ≤ 7]	11.6	—	8.5	—	ns
			$2.25 \times T_C - 4.0$ [WS ≥ 8]	24.1	—	18.5	—	ns

Table 2-8 SRAM Read and Write Accesses[1](Continued)

No.	Characteristics	Symbol	Expression[2]	80 MHz		100 MHz		Unit
				Min	Max	Min	Max	
104	Address and AA valid to input data valid	t_{AA}, t_{AC}	**80 MHz:** $(WS + 0.75) \times T_C - 9.5$ $[WS \geq 1]$ **100 MHz:** $(WS + 0.75) \times T_C - 8.0$ $[WS \geq 1]$	— —	12.4 —	— —	— 9.5	ns ns
105	$\overline{RD}$ assertion to input data valid	t_{OE}	**80 MHz:** $(WS + 0.25) \times T_C - 9.5$ $[WS \geq 1]$ **100 MHz:** $(WS + 0.25) \times T_C - 8.0$ $[WS \geq 1]$	— —	6.1 —	— —	— 4.5	ns ns
106	$\overline{RD}$ deassertion to data not valid (data hold time)	t_{OHZ}	—	0.0	—	0.0	—	ns
107	Address valid to $\overline{WR}$ deassertion	t_{AW}	$(WS + 0.75) \times T_C - 4.0$ $[WS \geq 1]$	17.9	—	13.5	—	ns
108	Data valid to $\overline{WR}$ deassertion (data setup time)	t_{DS} (t_{DW})	**80 MHz:** $(WS - 0.25) \times T_C - 3.3$ $[WS \geq 1]$ **100 MHz:** $(WS - 0.25) \times T_C - 2.75$ $[WS \geq 1]$	6.1 —	— —	— 4.8	— —	ns ns
109	Data hold time from $\overline{WR}$ deassertion	t_{DH}	**80 MHz:** $0.25 \times T_C - 3.0$ $[1 \leq WS \leq 3]$ **100 MHz:** $0.25 \times T_C - 2.4$ $[1 \leq WS \leq 3]$ All frequencies: $1.25 \times T_C - 3.8$ $[4 \leq WS \leq 7]$ $2.25 \times T_C - 3.8$ $[WS \geq 8]$	0.1 — 11.8 24.3	— — — —	— 0.1 8.7 18.7	— — — —	ns ns ns ns
110	$\overline{WR}$ assertion to data active	—	$0.75 \times T_C - 3.7$ $[WS = 1]$ $0.25 \times T_C - 3.7$ $[2 \leq WS \leq 3]$ $-0.25 \times T_C - 3.7$ $[WS \geq 4]$	5.7 –0.6 –6.8	— — —	3.8 –1.2 –6.2	— — —	ns ns ns

Table 2-8 SRAM Read and Write Accesses[1](Continued)

No.	Characteristics	Symbol	Expression[2]	80 MHz		100 MHz		Unit
				Min	Max	Min	Max	
111	$\overline{WR}$ deassertion to data high impedance	—	$0.25 \times T_C + 0.2$ [1 ≤ WS ≤ 3]	—	3.3	—	2.7	ns
			$1.25 \times T_C + 0.2$ [4 ≤ WS ≤ 7]	—	15.8	—	12.7	ns
			$2.25 \times T_C + 0.2$ [WS ≥ 8]	—	28.3	—	22.7	ns
112	Previous $\overline{RD}$ deassertion to data active (write)	—	$1.25 \times T_C - 4.0$ [1 ≤ WS ≤ 3]	11.6	—	8.5	—	ns
			$2.25 \times T_C - 4.0$ [4 ≤ WS ≤ 7]	24.1	—	18.5	—	ns
			$3.25 \times T_C - 4.0$ [WS ≥ 8]	36.6	—	28.5	—	ns
113	$\overline{RD}$ deassertion time	—	$0.75 \times T_C - 4.0$ [1 ≤ WS ≤ 3]	5.4	—	3.5	—	ns
			$1.75 \times T_C - 4.0$ [4 ≤ WS ≤ 7]	17.9	—	13.5	—	ns
			$2.75 \times T_C - 4.0$ [WS ≥ 8]	30.4	—	23.5	—	ns
114	$\overline{WR}$ deassertion time	—	$0.5 \times T_C - 3.5$ [WS = 1]	2.8	—	1.5	—	ns
			$T_C - 3.5$ [2 ≤ WS ≤ 3]	9.0	—	6.5	—	ns
			$2.5 \times T_C - 3.5$ [4 ≤ WS ≤ 7]	27.8	—	21.5	—	ns
			$3.5 \times T_C - 3.5$ [WS ≥ 8]	40.3	—	31.5	—	ns
115	Address valid to $\overline{RD}$ assertion	—	$0.5 \times T_C - 4$	2.3	—	1.0	—	ns
116	$\overline{RD}$ assertion pulse width	—	$(WS + 0.25) \times T_C - 3.8$	11.8	—	8.7	—	ns
117	$\overline{RD}$ deassertion to address not valid	—	$0.25 \times T_C - 3.0$ [1 ≤ WS ≤ 3]	0.1	—	0.0	—	ns
			$1.25 \times T_C - 3.0$ [4 ≤ WS ≤ 7]	12.6	—	9.5	—	ns
			$2.25 \times T_C - 3.0$ [WS ≥ 8]	25.1	—	19.5	—	ns

Note: 1. V_{CCQL} = 3.3 V ± 0.3 V; T_J = –40˚C to +100 ˚C, C_L = 50 pF
2. WS is the number of wait states specified in the bus control register (BCR).

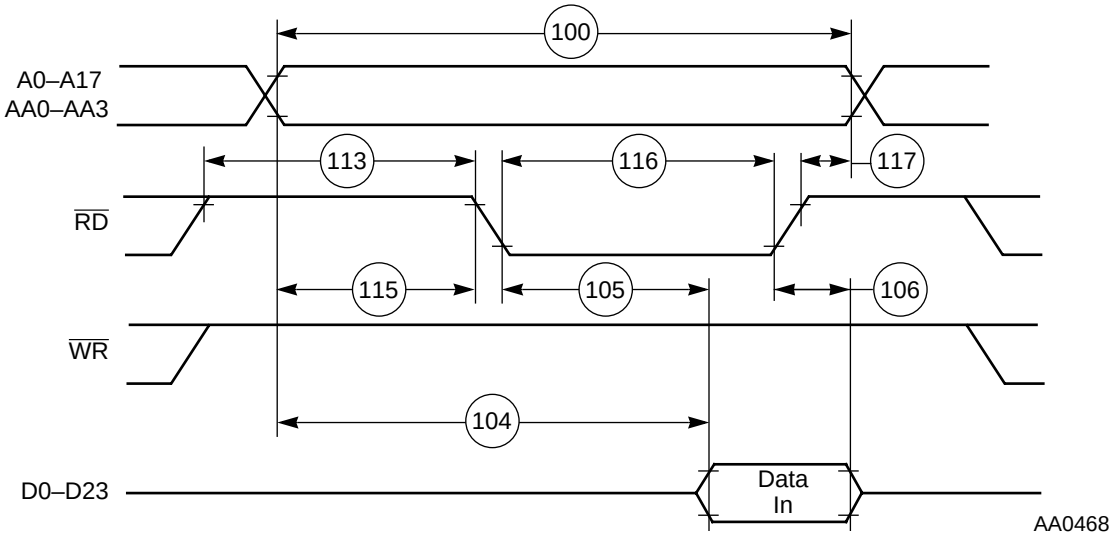


Figure 2-12 SRAM Read Access

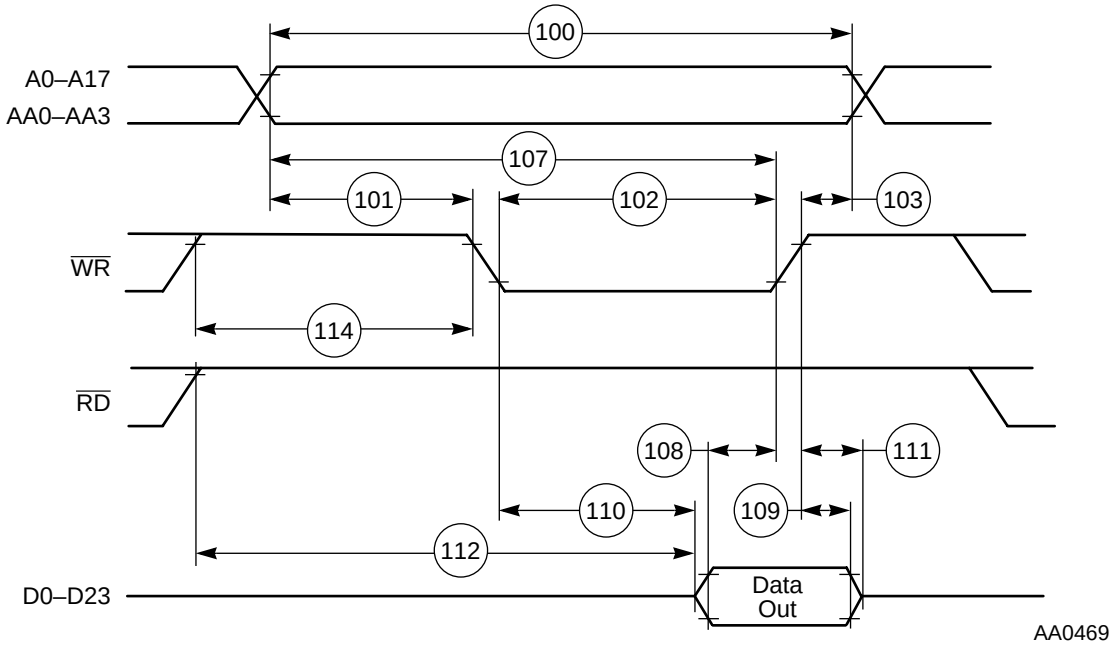


Figure 2-13 SRAM Write Access

DRAM Timing

The selection guides provided in **Figure 2-14** and **Figure 2-17** on page 2-33 should be used for primary selection only. Final selection should be based on the timing provided in the following tables. As an example, the selection guide suggests that four wait states must be used for 100 MHz operation when using page mode DRAM. However, by using the information in the appropriate table, a designer may choose to evaluate whether fewer wait states might be used by determining which timing prevents operation at 100 MHz, running the chip at a slightly lower frequency (e.g., 95 MHz), using faster DRAM (if it becomes available), and control factors such as capacitive and resistive load to improve overall system performance.

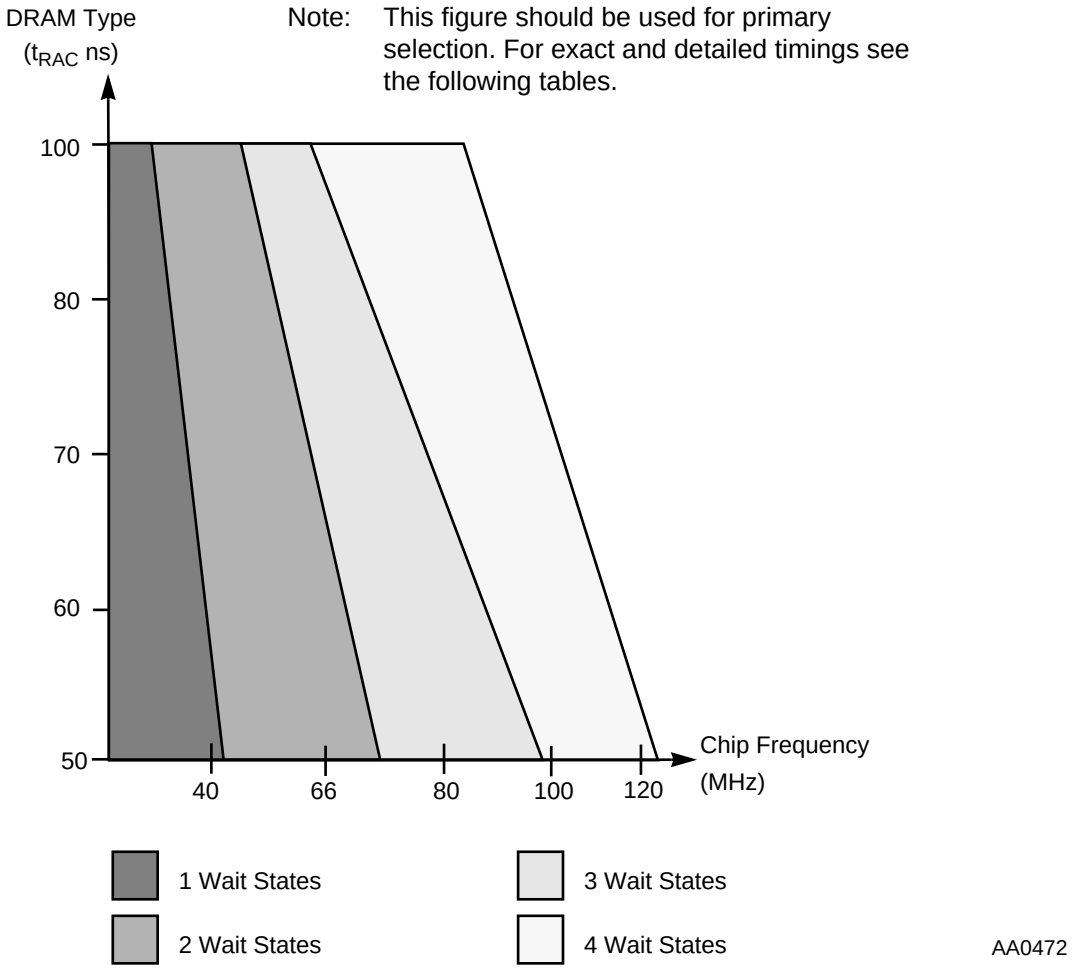


Figure 2-14 DRAM Page Mode Wait States Selection Guide

Table 2-9 DRAM Page Mode Timings, One Wait State (Low-Power Applications)[1, 2, 3] (Cont.)

No.	Characteristics	Symbol	Expression	20 MHz[4]		30 MHz[4]		Unit
				Min	Max	Min	Max	
131	Page mode cycle time	t_{PC}	$1.25 \times T_C$	62.5	—	41.7	—	ns
132	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	$T_C - 7.5$	—	42.5	—	25.8	ns
133	Column address valid to data valid (read)	t_{AA}	$1.5 \times T_C - 7.5$	—	67.5	—	42.5	ns
134	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}	—	0.0	—	0.0	—	ns
135	Last $\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$0.75 \times T_C - 4.0$	33.5	—	21.0	—	ns
136	Previous $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion	t_{RHCP}	$2 \times T_C - 4.0$	96.0	—	62.7	—	ns
137	$\overline{CAS}$ assertion pulse width	t_{CAS}	$0.75 \times T_C - 4.0$	33.5	—	21.0	—	ns
138	Last $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion[5]	t_{CRP}						
	• BRW[1:0] = 00		$1.75 \times T_C - 6.0$	81.5	—	52.3	—	ns
	• BRW[1:0] = 01		$3.25 \times T_C - 6.0$	156.5	—	102.2	—	ns
	• BRW[1:0] = 10		$4.25 \times T_C - 6.0$	206.5	—	135.5	—	ns
	• BRW[1:0] = 11		$6.25 \times T_C - 6.0$	306.5	—	202.1	—	ns
139	$\overline{CAS}$ deassertion pulse width	t_{CP}	$0.5 \times T_C - 4.0$	21.0	—	12.7	—	ns
140	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$0.5 \times T_C - 4.0$	21.0	—	12.7	—	ns
141	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$0.75 \times T_C - 4.0$	33.5	—	21.0	—	ns
142	Last column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$2 \times T_C - 4.0$	96.0	—	62.7	—	ns
143	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$0.75 \times T_C - 3.8$	33.7	—	21.2	—	ns
144	$\overline{CAS}$ deassertion to $\overline{WR}$ assertion	t_{RCH}	$0.25 \times T_C - 3.7$	8.8	—	4.6	—	ns
145	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$0.5 \times T_C - 4.2$	20.8	—	12.5	—	ns
146	$\overline{WR}$ assertion pulse width	t_{WP}	$1.5 \times T_C - 4.5$	70.5	—	45.5	—	ns
147	Last $\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$1.75 \times T_C - 4.3$	83.2	—	54.0	—	ns

Table 2-9 DRAM Page Mode Timings, One Wait State (Low-Power Applications)[1, 2, 3] (Cont.)

No.	Characteristics	Symbol	Expression	20 MHz[4]		30 MHz[4]		Unit
				Min	Max	Min	Max	
148	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$1.75 \times T_C - 4.3$	83.2	—	54.0	—	ns
149	Data valid to $\overline{CAS}$ assertion (Write)	t_{DS}	$0.25 \times T_C - 4.0$	8.5	—	4.3	—	ns
150	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$0.75 \times T_C - 4.0$	33.5	—	21.0	—	ns
151	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$T_C - 4.3$	45.7	—	29.0	—	ns
152	Last $\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$1.5 \times T_C - 4.0$	71.0	—	46.0	—	ns
153	$\overline{RD}$ assertion to data valid	t_{GA}	$T_C - 7.5$	—	42.5	—	25.8	ns
154	$\overline{RD}$ deassertion to data not valid [6]	t_{GZ}	—	0.0	—	0.0	—	ns
155	$\overline{WR}$ assertion to data active	—	$0.75 \times T_C - 0.3$	37.2	—	24.7	—	ns
156	$\overline{WR}$ deassertion to data high impedance	—	$0.25 \times T_C$	—	12.5	—	8.3	ns

Note:
1. The number of wait states for page mode access is specified in the data control register.
2. The refresh period is specified in the data control register.
3. All the timings are calculated for the worst case. Some of the timings are better for specific cases (e.g., t_{PC} equals $2 \times T_C$ for read-after-read or write-after-write sequences).
4. Reduced DSP clock speed allows use of page mode DRAM with one wait state as in **Figure 2-14**.
5. BRW[1:0] (DRAM control register bits) defines the number of wait states that should be inserted in each DRAM out-of-page access.
6. $\overline{RD}$ deassertion will always occur after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.

Table 2-10 DRAM Page Mode Timings, Two Wait States[1, 2, 3, 4]

No.	Characteristics	Symbol	Expression	80 MHz		Unit
				Min	Max	
131	Page mode cycle time	t_{PC}	$2.75 \times T_C$	34.4	—	ns
132	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	$1.5 \times T_C - 6.5$	—	12.3	ns
133	Column address valid to data valid (read)	t_{AA}	$2.5 \times T_C - 6.5$	—	24.8	ns
134	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}	—	0.0	—	ns

Table 2-10 DRAM Page Mode Timings, Two Wait States[1, 2, 3, 4](Continued)

No.	Characteristics	Symbol	Expression	80 MHz		Unit
				Min	Max	
135	Last $\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$1.75 \times T_C - 4.0$	17.9	—	ns
136	Previous $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion	t_{RHCP}	$3.25 \times T_C - 4.0$	36.6	—	ns
137	$\overline{CAS}$ assertion pulse width	t_{CAS}	$1.5 \times T_C - 4.0$	14.8	—	ns
138	Last $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion[5]	t_{CRP}				
	• BRW[1:0] = 00		$2.0 \times T_C - 6.0$	19.0	—	ns
	• BRW[1:0] = 01		$3.5 \times T_C - 6.0$	37.8	—	ns
	• BRW[1:0] = 10		$4.5 \times T_C - 6.0$	50.3	—	ns
	• BRW[1:0] = 11		$6.5 \times T_C - 6.0$	75.3	—	ns
139	$\overline{CAS}$ deassertion pulse width	t_{CP}	$1.25 \times T_C - 4.0$	11.6	—	ns
140	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$T_C - 4.0$	8.5	—	ns
141	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$1.75 \times T_C - 4.0$	17.9	—	ns
142	Last column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$3 \times T_C - 4.0$	33.5	—	ns
143	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$1.25 \times T_C - 3.8$	11.8	—	ns
144	$\overline{CAS}$ deassertion to $\overline{WR}$ assertion	t_{RCH}	$0.5 \times T_C - 3.7$	2.6	—	ns
145	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$1.5 \times T_C - 4.2$	14.6	—	ns
146	$\overline{WR}$ assertion pulse width	t_{WP}	$2.5 \times T_C - 4.5$	26.8	—	ns
147	Last $\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$2.75 \times T_C - 4.3$	30.1	—	ns
148	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$2.5 \times T_C - 4.3$	27.0	—	ns
149	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	$0.25 \times T_C - 3.0$	0.1	—	ns
150	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$1.75 \times T_C - 4.0$	17.9	—	ns
151	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$T_C - 4.3$	8.2	—	ns

Table 2-10 DRAM Page Mode Timings, Two Wait States[1, 2, 3, 4] (Continued)

No.	Characteristics	Symbol	Expression	80 MHz		Unit
				Min	Max	
152	Last $\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$2.5 \times T_C - 4.0$	27.3	—	ns
153	$\overline{RD}$ assertion to data valid	t_{GA}	$1.75 \times T_C - 6.5$	—	15.4	ns
154	$\overline{RD}$ deassertion to data not valid[6]	t_{GZ}	—	0.0	—	ns
155	$\overline{WR}$ assertion to data active	—	$0.75 \times T_C - 0.3$	9.1	—	ns
156	$\overline{WR}$ deassertion to data high impedance	—	$0.25 \times T_C$	—	3.1	ns

Note:
1. The number of wait states for page mode access is specified in the data control register. The refresh period is also specified in the data control register.
2. The asynchronous delays specified in the expressions are valid for DSP56309.
3. There are no DRAMs fast enough to meet the specifications for two wait state page mode @ 100MHz, as indicated in **Figure 2-14** on page 2-22.
4. All the timings are calculated for the worst case. Some of the timings are better for specific cases (e.g., t_{PC} equals $3 \times T_C$ for read-after-read or write-after-write sequences).
5. BRW[1:0] (DRAM control register bits) defines the number of wait states that should be inserted in each DRAM out-of-page access.
6. $\overline{RD}$ deassertion will always occur after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.

Table 2-11 DRAM Page Mode Timings, Three Wait States[1, 2, 3]

No.	Characteristics	Symbol	Expression	80 MHz		100 MHz		Unit
				Min	Max	Min	Max	
131	Page mode cycle time	t_{PC} [4]	$3.5 \times T_C$	43.8	—	35.0	—	ns
132	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	**80 MHz**: $2 \times T_C - 6.5$ **100 MHz**: $2 \times T_C - 5.7$	 — —	 18.5 —	 — —	 — 14.3	 ns ns
133	Column address valid to data valid (read)	t_{AA}	**80 MHz**: $3 \times T_C - 6.5$ **100 MHz**: $3 \times T_C - 5.7$	 — —	 31.0 —	 — —	 — 24.3	 ns ns
134	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}	—	0.0	—	0.0	—	ns
135	Last $\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$2.5 \times T_C - 4.0$	27.3	—	21.0	—	ns

Table 2-11 DRAM Page Mode Timings, Three Wait States[1, 2, 3](Continued)

No.	Characteristics	Symbol	Expression	80 MHz		100 MHz		Unit
				Min	Max	Min	Max	
136	Previous $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion	t_{RHCP}	$4.5 \times T_C - 4.0$	52.3	—	41.0	—	ns
137	$\overline{CAS}$ assertion pulse width	t_{CAS}	$2 \times T_C - 4.0$	21.0	—	16.0	—	ns
138	Last $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion[5]	t_{CRP}						
	•BRW[1:0] = 00		$2.25 \times T_C - 6.0$	22.2	—	16.5	—	ns
	•BRW[1:0] = 01		$3.75 \times T_C - 6.0$	40.9	—	31.5	—	ns
	•BRW[1:0] = 10		$4.75 \times T_C - 6.0$	53.4	—	41.5	—	ns
	•BRW[1:0] = 11		$6.75 \times T_C - 6.0$	78.4	—	61.5	—	ns
139	$\overline{CAS}$ deassertion pulse width	t_{CP}	$1.5 \times T_C - 4.0$	14.8	—	11.0	—	ns
140	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$T_C - 4.0$	8.5	—	6.0	—	ns
141	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$2.5 \times T_C - 4.0$	27.3	—	21.0	—	ns
142	Last column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$4 \times T_C - 4.0$	46.0	—	36.0	—	ns
143	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$1.25 \times T_C - 3.8$	11.8	—	8.7	—	ns
144	$\overline{CAS}$ deassertion to $\overline{WR}$ assertion	t_{RCH}	$0.75 \times T_C - 3.7$	5.7	—	3.8	—	ns
145	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$2.25 \times T_C - 4.2$	23.9	—	18.3	—	ns
146	$\overline{WR}$ assertion pulse width	t_{WP}	$3.5 \times T_C - 4.5$	39.3	—	30.5	—	ns
147	Last $\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$3.75 \times T_C - 4.3$	42.6	—	33.2	—	ns
148	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$3.25 \times T_C - 4.3$	36.3	—	28.2	—	ns
149	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	$0.5 \times T_C - 4.0$	2.3	—	1.0	—	ns
150	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$2.5 \times T_C - 4.0$	27.3	—	21.0	—	ns
151	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$1.25 \times T_C - 4.3$	11.3	—	8.2	—	ns
152	Last $\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$3.5 \times T_C - 4.0$	39.8	—	31.0	—	ns

Table 2-11 DRAM Page Mode Timings, Three Wait States[1, 2, 3](Continued)

No.	Characteristics	Symbol	Expression	80 MHz		100 MHz		Unit
				Min	Max	Min	Max	
153	$\overline{RD}$ assertion to data valid	t_{GA}	**80 MHz**: $2.5 \times T_C - 6.5$ **100 MHz**: $2.5 \times T_C - 5.7$	— —	24.8 —	— —	— 19.3	ns ns
154	$\overline{RD}$ deassertion to data not valid[6]	t_{GZ}	—	0.0	—	0.0	—	ns
155	$\overline{WR}$ assertion to data active	—	$0.75 \times T_C - 0.3$	9.1	—	7.2	—	ns
156	$\overline{WR}$ deassertion to data high impedance	—	$0.25 \times T_C$	—	3.1	—	2.5	ns

Note:
1. The number of wait states for Page mode access is specified in the data control register.
2. The refresh period is specified in the data control register.
3. The asynchronous delays specified in the expressions are valid for DSP56309.
4. All the timings are calculated for the worst case. Some of the timings are better for specific cases (e.g., t_{PC} equals $4 \times T_C$ for read-after-read or write-after-write sequences).
5. BRW[1:0] (DRAM control register bits) defines the number of wait states that should be inserted in each DRAM out-of page-access.
6. $\overline{RD}$ deassertion will always occur after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.

Table 2-12 DRAM Page Mode Timings, Four Wait States[1, 2, 3]

No.	Characteristics	Symbol	Expression	80 MHz		100 MHz		Unit
				Min	Max	Min	Max	
131	Page mode cycle time	t_{PC}[4]	$4.5 \times T_C$	56.3	—	45.0	—	ns
132	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	**80 MHz**: $2.75 \times T_C - 6.5$ **100 MHz**: $2.75 \times T_C - 5.7$	— —	27.9 —	— —	— 21.8	ns ns
133	Column address valid to data valid (read)	t_{AA}	**80 MHz**: $3.75 \times T_C - 6.5$ **100 MHz**: $3.75 \times T_C - 5.7$	— —	40.4 —	— —	— 31.8	ns ns
134	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}	—	0.0	—	0.0	—	ns
135	Last $\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$3.5 \times T_C - 4.0$	39.8	—	31.0	—	ns
136	Previous $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion	t_{RHCP}	$6 \times T_C - 4.0$	71.0	—	56.0	—	ns
137	$\overline{CAS}$ assertion pulse width	t_{CAS}	$2.5 \times T_C - 4.0$	27.3	—	21.0	—	ns

Table 2-12 DRAM Page Mode Timings, Four Wait States[1, 2, 3](Continued)

No.	Characteristics	Symbol	Expression	80 MHz		100 MHz		Unit
				Min	Max	Min	Max	
138	Last $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion[5]	t_{CRP}						
	• BRW[1:0] = 00		$2.75 \times T_C - 6.0$	28.4	—	21.5	—	ns
	• BRW[1:0] = 01		$4.25 \times T_C - 6.0$	47.2	—	36.5	—	ns
	• BRW[1:0] = 10		$5.25 \times T_C - 6.0$	59.7	—	46.5	—	ns
	• BRW[1:0] = 11		$6.25 \times T_C - 6.0$	72.2	—	56.5	—	ns
139	$\overline{CAS}$ deassertion pulse width	t_{CP}	$2 \times T_C - 4.0$	21.0	—	16.0	—	ns
140	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$T_C - 4.0$	8.5	—	6.0	—	ns
141	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$3.5 \times T_C - 4.0$	39.8	—	31.0	—	ns
142	Last column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$5 \times T_C - 4.0$	58.5	—	46.0	—	ns
143	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$1.25 \times T_C - 3.8$	11.8	—	8.7	—	ns
144	$\overline{CAS}$ deassertion to $\overline{WR}$ assertion	t_{RCH}	$1.25 \times T_C - 3.7$	11.9	—	8.8	—	ns
145	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$3.25 \times T_C - 4.2$	36.4	—	28.3	—	ns
146	$\overline{WR}$ assertion pulse width	t_{WP}	$4.5 \times T_C - 4.5$	51.8	—	40.5	—	ns
147	Last $\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$4.75 \times T_C - 4.3$	55.1	—	43.2	—	ns
148	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$3.75 \times T_C - 4.3$	42.6	—	33.2	—	ns
149	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	$0.5 \times T_C - 4.0$	2.3	—	1.0	—	ns
150	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$3.5 \times T_C - 4.0$	39.8	—	31.0	—	ns
151	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$1.25 \times T_C - 4.3$	11.3	—	8.2	—	ns
152	Last $\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$4.5 \times T_C - 4.0$	52.3	—	41.0	—	ns

Table 2-12 DRAM Page Mode Timings, Four Wait States[1, 2, 3](Continued)

No.	Characteristics	Symbol	Expression	80 MHz		100 MHz		Unit
				Min	Max	Min	Max	
153	$\overline{RD}$ assertion to data valid	t_{GA}	**80 MHz**: $3.25 \times T_C - 6.5$ **100 MHz**: $3.25 \times T_C - 5.7$	— —	34.1 —	— —	— 26.8	ns ns
154	$\overline{RD}$ deassertion to data not valid[6]	t_{GZ}	—	0.0	—	0.0	—	ns
155	$\overline{WR}$ assertion to data active	—	$0.75 \times T_C - 0.3$	9.1	—	7.2	—	ns
156	$\overline{WR}$ deassertion to data high impedance	—	$0.25 \times T_C$	—	3.1	—	2.5	ns

Note:
1. The number of wait states for Page mode access is specified in the data control register.
2. The refresh period is specified in the data control register.
3. The asynchronous delays specified in the expressions are valid for DSP56309.
4. All the timings are calculated for the worst case. Some of the timings are better for specific cases (e.g., t_{PC} equals $3 \times T_C$ for read-after-read or write-after-write sequences).
5. BRW[1:0] (DRAM control register bits) defines the number of wait states that should be inserted in each DRAM out-of-page access.
6. $\overline{RD}$ deassertion will always occur after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.

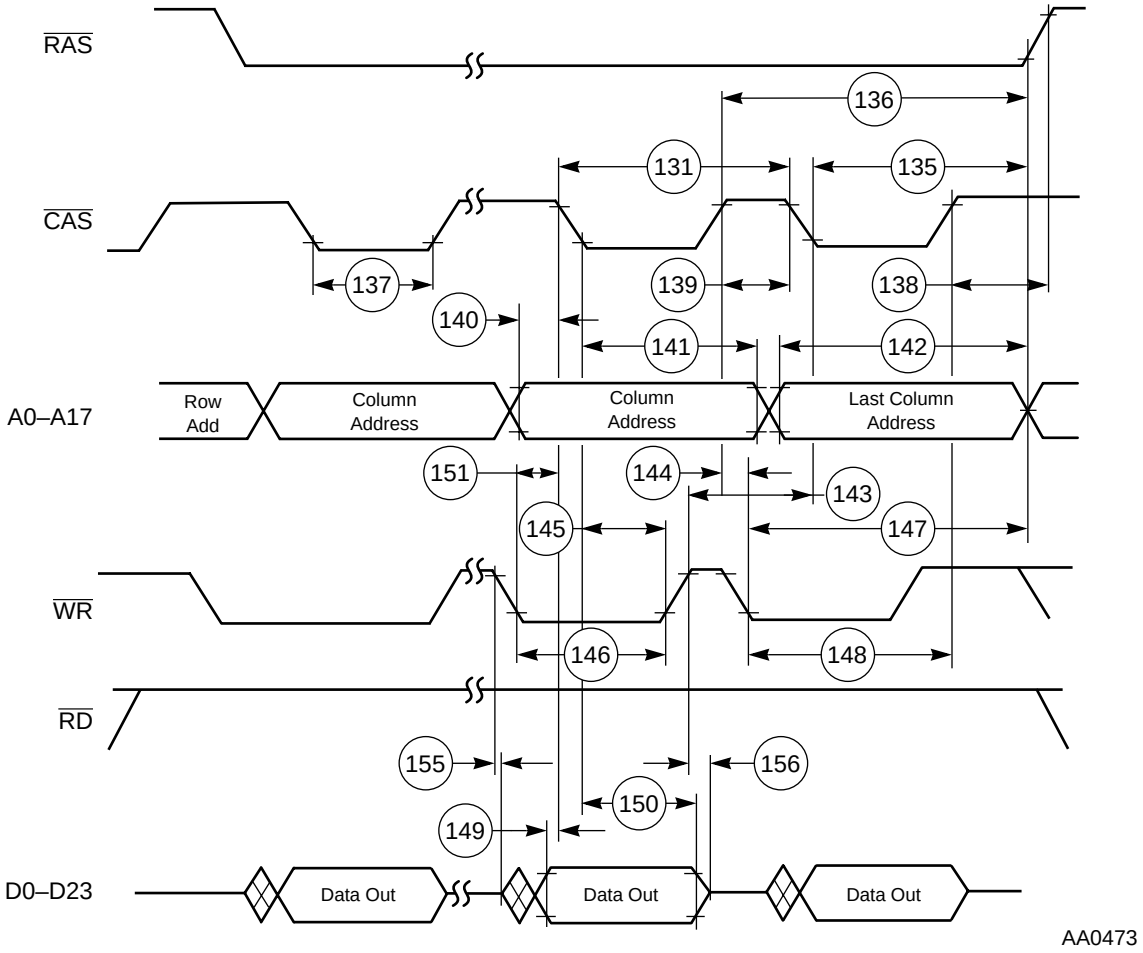


Figure 2-15 DRAM Page Mode Write Accesses

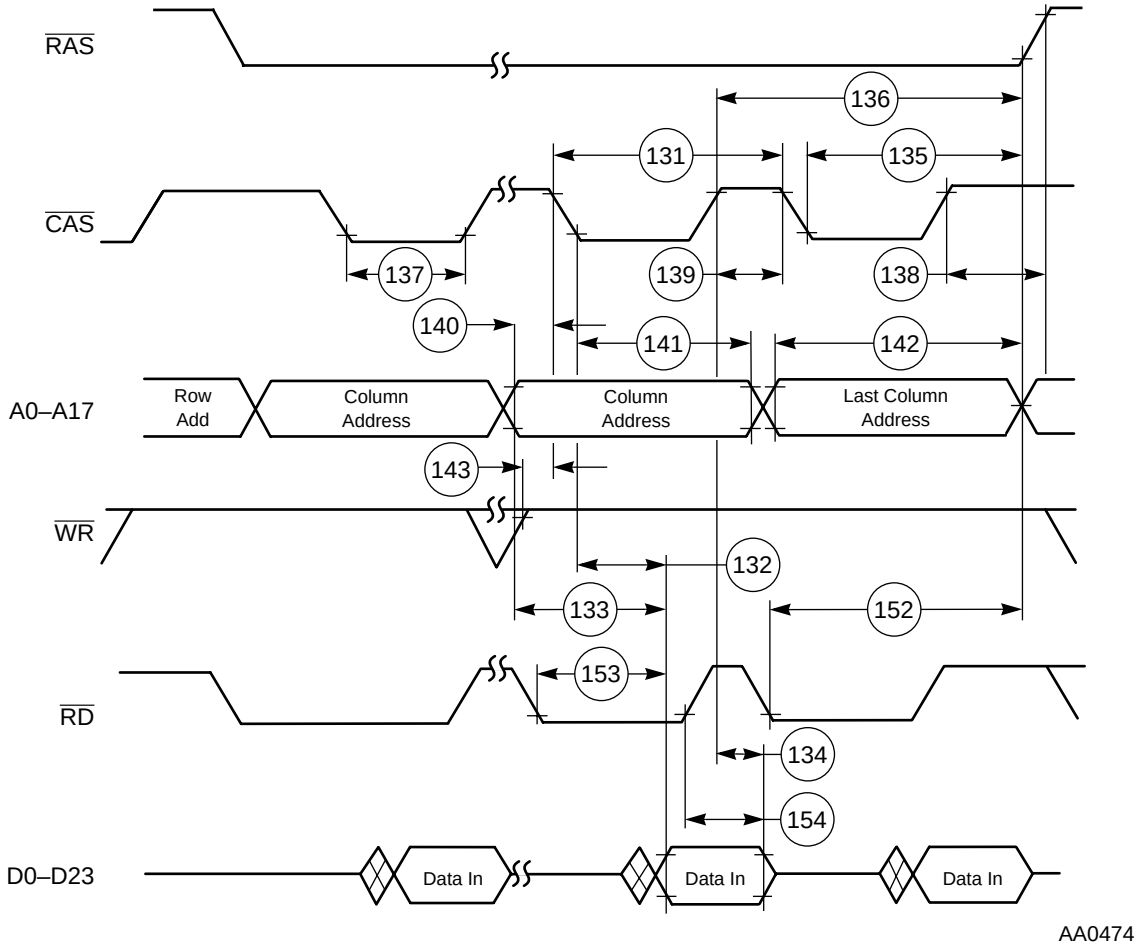


Figure 2-16 DRAM Page Mode Read Accesses

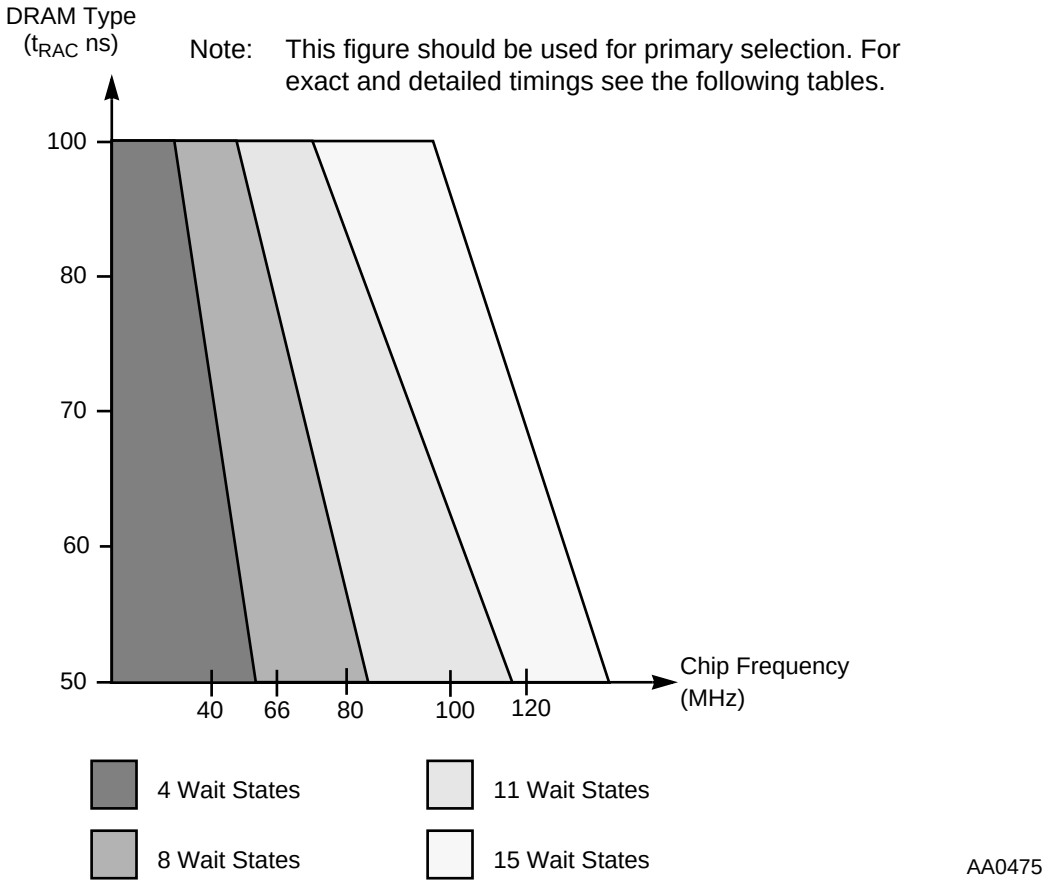


Figure 2-17 DRAM Out-of-Page Wait States Selection Guide

Table 2-13 DRAM Out-of-Page and Refresh Timings, Four Wait States[1, 2]

No.	Characteristics	Symbol	Expression	20 MHz[3]		30 MHz[3]		Unit
				Min	Max	Min	Max	
157	Random read or write cycle time	t_{RC}	$5 \times T_C$	250.0	—	166.7	—	ns
158	$\overline{RAS}$ assertion to data valid (read)	t_{RAC}	$2.75 \times T_C - 7.5$	—	130.0	—	84.2	ns
159	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	$1.25 \times T_C - 7.5$	—	55.0	—	34.2	ns
160	Column address valid to data valid (read)	t_{AA}	$1.5 \times T_C - 7.5$	—	67.5	—	42.5	ns
161	$\overline{CAS}$ deassertion to data not valid (read hold time)[4]	t_{OFF}	—	0.0	—	0.0	—	ns

Table 2-13 DRAM Out-of-Page and Refresh Timings, Four Wait States[1, 2](Continued)

No.	Characteristics	Symbol	Expression	20 MHz[3]		30 MHz[3]		Unit
				Min	Max	Min	Max	
162	$\overline{RAS}$ deassertion to $\overline{RAS}$ assertion	t_{RP}	$1.75 \times T_C - 4.0$	83.5	—	54.3	—	ns
163	$\overline{RAS}$ assertion pulse width	t_{RAS}	$3.25 \times T_C - 4.0$	158.5	—	104.3	—	ns
164	$\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$1.75 \times T_C - 4.0$	83.5	—	54.3	—	ns
165	$\overline{RAS}$ assertion to $\overline{CAS}$ deassertion	t_{CSH}	$2.75 \times T_C - 4.0$	133.5	—	87.7	—	ns
166	$\overline{CAS}$ assertion pulse width	t_{CAS}	$1.25 \times T_C - 4.0$	58.5	—	37.7	—	ns
167	$\overline{RAS}$ assertion to $\overline{CAS}$ assertion	t_{RCD}	$1.5 \times T_C \pm 2$	73.0	77.0	48.0	52.0	ns
168	$\overline{RAS}$ assertion to column address valid	t_{RAD}	$1.25 \times T_C \pm 2$	60.5	64.5	39.7	43.7	ns
169	$\overline{CAS}$ deassertion to $\overline{RAS}$ assertion	t_{CRP}	$2.25 \times T_C - 4.0$	108.5	—	71.0	—	ns
170	$\overline{CAS}$ deassertion pulse width	t_{CP}	$1.75 \times T_C - 4.0$	83.5	—	54.3	—	ns
171	Row address valid to $\overline{RAS}$ assertion	t_{ASR}	$1.75 \times T_C - 4.0$	83.5	—	54.3	—	ns
172	$\overline{RAS}$ assertion to row address not valid	t_{RAH}	$1.25 \times T_C - 4.0$	58.5	—	37.7	—	ns
173	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$0.25 \times T_C - 4.0$	8.5	—	4.3	—	ns
174	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$1.75 \times T_C - 4.0$	83.5	—	54.3	—	ns
175	$\overline{RAS}$ assertion to column address not valid	t_{AR}	$3.25 \times T_C - 4.0$	158.5	—	104.3	—	ns
176	Column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$2 \times T_C - 4.0$	96.0	—	62.7	—	ns
177	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$1.5 \times T_C - 3.8$	71.2	—	46.2	—	ns
178	$\overline{CAS}$ deassertion to $\overline{WR}$ assertion	t_{RCH}	$0.75 \times T_C - 3.7$	33.8	—	21.3	—	ns
179	$\overline{RAS}$ deassertion to $\overline{WR}$ assertion	t_{RRH}	$0.25 \times T_C - 3.7$	8.8	—	4.6	—	ns

Table 2-13 DRAM Out-of-Page and Refresh Timings, Four Wait States[1, 2](Continued)

No.	Characteristics	Symbol	Expression	20 MHz[3]		30 MHz[3]		Unit
				Min	Max	Min	Max	
180	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$1.5 \times T_C - 4.2$	70.8	—	45.8	—	ns
181	$\overline{RAS}$ assertion to $\overline{WR}$ deassertion	t_{WCR}	$3 \times T_C - 4.2$	145.8	—	95.8	—	ns
182	$\overline{WR}$ assertion pulse width	t_{WP}	$4.5 \times T_C - 4.5$	220.5	—	145.5	—	ns
183	$\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$4.75 \times T_C - 4.3$	233.2	—	154.0	—	ns
184	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$4.25 \times T_C - 4.3$	208.2	—	137.4	—	ns
185	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	$2.25 \times T_C - 4.0$	108.5	—	71.0	—	ns
186	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$1.75 \times T_C - 4.0$	83.5	—	54.3	—	ns
187	$\overline{RAS}$ assertion to data not valid (write)	t_{DHR}	$3.25 \times T_C - 4.0$	158.5	—	104.3	—	ns
188	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$3 \times T_C - 4.3$	145.7	—	95.7	—	ns
189	$\overline{CAS}$ assertion to $\overline{RAS}$ assertion (refresh)	t_{CSR}	$0.5 \times T_C - 4.0$	21.0	—	12.7	—	ns
190	$\overline{RAS}$ deassertion to $\overline{CAS}$ assertion (refresh)	t_{RPC}	$1.25 \times T_C - 4.0$	58.5	—	37.7	—	ns
191	$\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$4.5 \times T_C - 4.0$	221.0	—	146.0	—	ns
192	$\overline{RD}$ assertion to data valid	t_{GA}	$4 \times T_C - 7.5$	—	192.5	—	125.8	ns
193	$\overline{RD}$ deassertion to data not valid[4]	t_{GZ}	—	0.0	—	0.0	—	ns
194	$\overline{WR}$ assertion to data active	—	$0.75 \times T_C - 0.3$	37.2	—	24.7	—	ns
195	$\overline{WR}$ deassertion to data high impedance	—	$0.25 \times T_C$	—	12.5	—	8.3	ns

Note:
1. The number of wait states for out-of-page access is specified in the data control register.
2. The refresh period is specified in the data control register.
3. Reduced DSP clock speed allows use of DRAM out-of-page access with four wait states, as in **Figure 2-17** on page 2-33.
4. $\overline{RD}$ deassertion will always occur after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.

Table 2-14 DRAM Out-of-Page and Refresh Timings, Eight Wait States[1, 2]

No.	Characteristics	Symbol	Expression[3]	80 MHz		100 MHz		Unit
				Min	Max	Min	Max	
157	Random read or write cycle time	t_{RC}	$9 \times T_C$	112.5	—	90.0	—	ns
158	$\overline{RAS}$ assertion to data valid (read)	t_{RAC}	**80 MHz**: $4.75 \times T_C - 6.5$ **100 MHz**: $4.75 \times T_C - 5.7$	 — —	 52.9 —	 — —	 — 41.8	 ns ns
159	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	**80 MHz**: $2.25 \times T_C - 6.5$ **100 MHz**: $2.25 \times T_C - 5.7$	 — —	 21.6 —	 — —	 — 16.8	 ns ns
160	Column address valid to data valid (read)	t_{AA}	**80 MHz**: $3 \times T_C - 6.5$ **100 MHz**: $3 \times T_C - 5.7$	 — —	 31.0 —	 — —	 — 24.3	 ns ns
161	$\overline{CAS}$ deassertion to data not valid (read hold time)[4]	t_{OFF}	—	0.0	—	0.0	—	ns
162	$\overline{RAS}$ deassertion to $\overline{RAS}$ assertion	t_{RP}	$3.25 \times T_C - 4.0$	36.6	—	28.5	—	ns
163	$\overline{RAS}$ assertion pulse width	t_{RAS}	$5.75 \times T_C - 4.0$	67.9	—	53.5	—	ns
164	$\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$3.25 \times T_C - 4.0$	36.6	—	28.5	—	ns
165	$\overline{RAS}$ assertion to $\overline{CAS}$ deassertion	t_{CSH}	$4.75 \times T_C - 4.0$	55.4	—	43.5	—	ns
166	$\overline{CAS}$ assertion pulse width	t_{CAS}	$2.25 \times T_C - 4.0$	24.1	—	18.5	—	ns
167	$\overline{RAS}$ assertion to $\overline{CAS}$ assertion	t_{RCD}	$2.5 \times T_C \pm 2$	29.3	33.3	23.0	27.0	ns
168	$\overline{RAS}$ assertion to column address valid	t_{RAD}	$1.75 \times T_C \pm 2$	19.9	23.9	15.5	19.5	ns
169	$\overline{CAS}$ deassertion to $\overline{RAS}$ assertion	t_{CRP}	$4.25 \times T_C - 4.0$	49.1	—	38.5	—	ns
170	$\overline{CAS}$ deassertion pulse width	t_{CP}	$2.75 \times T_C - 4.0$	30.4	—	23.5	—	ns
171	Row address valid to $\overline{RAS}$ assertion	t_{ASR}	$3.25 \times T_C - 4.0$	36.6	—	28.5	—	ns
172	$\overline{RAS}$ assertion to row address not valid	t_{RAH}	$1.75 \times T_C - 4.0$	17.9	—	13.5	—	ns

Table 2-14 DRAM Out-of-Page and Refresh Timings, Eight Wait States[1, 2](Continued)

No.	Characteristics	Symbol	Expression[3]	80 MHz		100 MHz		Unit
				Min	Max	Min	Max	
173	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$0.75 \times T_C - 4.0$	5.4	—	3.5	—	ns
174	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$3.25 \times T_C - 4.0$	36.6	—	28.5	—	ns
175	$\overline{RAS}$ assertion to column address not valid	t_{AR}	$5.75 \times T_C - 4.0$	67.9	—	53.5	—	ns
176	Column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$4 \times T_C - 4.0$	46.0	—	36.0	—	ns
177	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$2 \times T_C - 3.8$	21.2	—	16.2	—	ns
178	$\overline{CAS}$ deassertion to $\overline{WR}$[5] assertion	t_{RCH}	$1.25 \times T_C - 3.7$	11.9	—	8.8	—	ns
179	$\overline{RAS}$ deassertion to $\overline{WR}$[5] assertion	t_{RRH}	**80 MHz**: $0.25 \times T_C - 3.0$ **100 MHz**: $0.25 \times T_C - 2.4$	 0.1 —	 — —	 — 0.1	 — —	 ns ns
180	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$3 \times T_C - 4.2$	33.3	—	25.8	—	ns
181	$\overline{RAS}$ assertion to $\overline{WR}$ deassertion	t_{WCR}	$5.5 \times T_C - 4.2$	64.6	—	50.8	—	ns
182	$\overline{WR}$ assertion pulse width	t_{WP}	$8.5 \times T_C - 4.5$	101.8	—	80.5	—	ns
183	$\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$8.75 \times T_C - 4.3$	105.1	—	83.2	—	ns
184	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$7.75 \times T_C - 4.3$	92.6	—	73.2	—	ns
185	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	$4.75 \times T_C - 4.0$	55.4	—	43.5	—	ns
186	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$3.25 \times T_C - 4.0$	36.6	—	28.5	—	ns
187	$\overline{RAS}$ assertion to data not valid (write)	t_{DHR}	$5.75 \times T_C - 4.0$	67.9	—	53.5	—	ns
188	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$5.5 \times T_C - 4.3$	64.5	—	50.7	—	ns
189	$\overline{CAS}$ assertion to $\overline{RAS}$ assertion (refresh)	t_{CSR}	$1.5 \times T_C - 4.0$	14.8	—	11.0	—	ns

Table 2-14 DRAM Out-of-Page and Refresh Timings, Eight Wait States[1, 2](Continued)

No.	Characteristics	Symbol	Expression[3]	80 MHz		100 MHz		Unit
				Min	Max	Min	Max	
190	$\overline{RAS}$ deassertion to $\overline{CAS}$ assertion (refresh)	t_{RPC}	$1.75 \times T_C - 4.0$	17.9	—	13.5	—	ns
191	$\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$8.5 \times T_C - 4.0$	102.3	—	81.0	—	ns
192	$\overline{RD}$ assertion to data valid	t_{GA}	**80 MHz**: $7.5 \times T_C - 6.5$ **100 MHz**: $7.5 \times T_C - 5.7$	 — —	 87.3 —	 — —	 — 69.3	 ns ns
193	$\overline{RD}$ deassertion to data not valid[4]	t_{GZ}	0.0	0.0	—	0.0	—	ns
194	$\overline{WR}$ assertion to data active	—	$0.75 \times T_C - 0.3$	9.1	—	7.2	—	ns
195	$\overline{WR}$ deassertion to data high impedance	—	$0.25 \times T_C$	—	3.1	—	2.5	ns

Note:
1. The number of wait states for out-of-page access is specified in the data control register.
2. The refresh period is specified in the data control register.
3. The asynchronous delays specified in the expressions are valid for DSP56309.
4. $\overline{RD}$ deassertion will always occur after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.
5. Either t_{RCH} or t_{RRH} must be satisfied for read cycles.

Table 2-15 DRAM Out-of-Page and Refresh Timings, Eleven Wait States[1, 2]

No.	Characteristics	Symbol	Expression[3]	80 MHz		100 MHz		Unit
				Min	Max	Min	Max	
157	Random read or write cycle time	t_{RC}	$12 \times T_C$	150.0	—	120.0	—	ns
158	$\overline{RAS}$ assertion to data valid (read)	t_{RAC}	**80 MHz**: $6.25 \times T_C - 6.5$ **100 MHz**: $6.25 \times T_C - 5.7$	 — —	 71.6 —	 — —	 — 56.8	 ns ns
159	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	**80 MHz**: $3.75 \times T_C - 6.5$ **100 MHz**: $3.75 \times T_C - 5.7$	 — —	 40.4 —	 — —	 — 31.8	 ns ns

Table 2-15 DRAM Out-of-Page and Refresh Timings, Eleven Wait States[1, 2](Continued)

No.	Characteristics	Symbol	Expression[3]	80 MHz		100 MHz		Unit
				Min	Max	Min	Max	
160	Column address valid to data valid (read)	t_{AA}	**80 MHz**: $4.5 \times T_C - 6.5$ **100 MHz**: $4.5 \times T_C - 5.7$	— —	49.8 —	— —	— 39.3	ns ns
161	$\overline{CAS}$ deassertion to data not valid (read hold time)[4]	t_{OFF}	—	0.0	—	0.0	—	ns
162	$\overline{RAS}$ deassertion to $\overline{RAS}$ assertion	t_{RP}	$4.25 \times T_C - 4.0$	49.1	—	38.5	—	ns
163	$\overline{RAS}$ assertion pulse width	t_{RAS}	$7.75 \times T_C - 4.0$	92.9	—	73.5	—	ns
164	$\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$5.25 \times T_C - 4.0$	61.6	—	48.5	—	ns
165	$\overline{RAS}$ assertion to $\overline{CAS}$ deassertion	t_{CSH}	$6.25 \times T_C - 4.0$	74.1	—	58.5	—	ns
166	$\overline{CAS}$ assertion pulse width	t_{CAS}	$3.75 \times T_C - 4.0$	42.9	—	33.5	—	ns
167	$\overline{RAS}$ assertion to $\overline{CAS}$ assertion	t_{RCD}	$2.5 \times T_C \pm 2$	29.3	33.3	23.0	27.0	ns
168	$\overline{RAS}$ assertion to column address valid	t_{RAD}	$1.75 \times T_C \pm 2$	19.9	23.9	15.5	19.5	ns
169	$\overline{CAS}$ deassertion to $\overline{RAS}$ assertion	t_{CRP}	$5.75 \times T_C - 4.0$	67.9	—	53.5	—	ns
170	$\overline{CAS}$ deassertion pulse width	t_{CP}	$4.25 \times T_C - 4.0$	49.1	—	38.5	—	ns
171	Row address valid to $\overline{RAS}$ assertion	t_{ASR}	$4.25 \times T_C - 4.0$	49.1	—	38.5	—	ns
172	$\overline{RAS}$ assertion to row address not valid	t_{RAH}	$1.75 \times T_C - 4.0$	17.9	—	13.5	—	ns
173	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$0.75 \times T_C - 4.0$	5.4	—	3.5	—	ns
174	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$5.25 \times T_C - 4.0$	61.6	—	48.5	—	ns
175	$\overline{RAS}$ assertion to column address not valid	t_{AR}	$7.75 \times T_C - 4.0$	92.9	—	73.5	—	ns
176	Column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$6 \times T_C - 4.0$	71.0	—	56.0	—	ns
177	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$3.0 \times T_C - 3.8$	33.7	—	26.2	—	ns

Table 2-15 DRAM Out-of-Page and Refresh Timings, Eleven Wait States[1, 2](Continued)

No.	Characteristics	Symbol	Expression[3]	80 MHz		100 MHz		Unit
				Min	Max	Min	Max	
178	$\overline{CAS}$ deassertion to $\overline{WR}$[5] assertion	t_{RCH}	$1.75 \times T_C - 3.7$	18.2	—	13.8	—	ns
179	$\overline{RAS}$ deassertion to $\overline{WR}$[5] assertion	t_{RRH}	**80 MHz**: $0.25 \times T_C - 3.0$ **100 MHz**: $0.25 \times T_C - 2.4$	 0.1 —	 — —	 — 0.1	 — —	 ns ns
180	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$5 \times T_C - 4.2$	58.3	—	45.8	—	ns
181	$\overline{RAS}$ assertion to $\overline{WR}$ deassertion	t_{WCR}	$7.5 \times T_C - 4.2$	89.6	—	70.8	—	ns
182	$\overline{WR}$ assertion pulse width	t_{WP}	$11.5 \times T_C - 4.5$	139.3	—	110.5	—	ns
183	$\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$11.75 \times T_C - 4.3$	142.7	—	113.2	—	ns
184	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$10.25 \times T_C - 4.3$	130.1	—	103.2	—	ns
185	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	$5.75 \times T_C - 4.0$	67.9	—	53.5	—	ns
186	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$5.25 \times T_C - 4.0$	61.6	—	48.5	—	ns
187	$\overline{RAS}$ assertion to data not valid (write)	t_{DHR}	$7.75 \times T_C - 4.0$	92.9	—	73.5	—	ns
188	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$6.5 \times T_C - 4.3$	77.0	—	60.7	—	ns
189	$\overline{CAS}$ assertion to $\overline{RAS}$ assertion (refresh)	t_{CSR}	$1.5 \times T_C - 4.0$	14.8	—	11.0	—	ns
190	$\overline{RAS}$ deassertion to $\overline{CAS}$ assertion (refresh)	t_{RPC}	$2.75 \times T_C - 4.0$	30.4	—	23.5	—	ns
191	$\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$11.5 \times T_C - 4.0$	139.8	—	111.0	—	ns
192	$\overline{RD}$ assertion to data valid	t_{GA}	**80 MHz**: $10 \times T_C - 6.5$ **100 MHz**: $10 \times T_C - 5.7$	 — —	 118.5 —	 — —	 — 94.3	 ns ns
193	$\overline{RD}$ deassertion to data not valid[4]	t_{GZ}	—	0.0	—	0.0	—	ns
194	$\overline{WR}$ assertion to data active	—	$0.75 \times T_C - 0.3$	9.1	—	7.2	—	ns

Table 2-15 DRAM Out-of-Page and Refresh Timings, Eleven Wait States[1, 2](Continued)

No.	Characteristics	Symbol	Expression[3]	80 MHz		100 MHz		Unit
				Min	Max	Min	Max	
195	$\overline{WR}$ deassertion to data high impedance	—	$0.25 \times T_C$	—	3.1	—	2.5	ns

Note:
1. The number of wait states for out-of-page access is specified in the data control register.
2. The refresh period is specified in the data control register.
3. The asynchronous delays specified in the expressions are valid for DSP56309.
4. $\overline{RD}$ deassertion will always occur after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.
5. Either t_{RCH} or t_{RRH} must be satisfied for read cycles.

Table 2-16 DRAM Out-of-Page and Refresh Timings, Fifteen Wait States[1, 2]

No.	Characteristics	Symbol	Expression	80 MHz		100 MHz		Unit
				Min	Max	Min	Max	
157	Random read or write cycle time	t_{RC}	$16 \times T_C$	200.0	—	160.0	—	ns
158	$\overline{RAS}$ assertion to data valid (read)	t_{RAC}	**80 MHz**: $8.25 \times T_C - 6.5$ **100 MHz**: $8.25 \times T_C - 5.7$	— —	96.6 —	— —	— 76.8	ns ns
159	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	**80 MHz**: $4.75 \times T_C - 6.5$ **100 MHz**: $4.75 \times T_C - 5.7$	— —	52.9 —	— —	— 41.8	ns ns
160	Column address valid to data valid (read)	t_{AA}	**80 MHz**: $5.5 \times T_C - 6.5$ **100 MHz**: $5.5 \times T_C - 5.7$	— —	62.3 —	— —	— 49.3	ns ns
161	$\overline{CAS}$ deassertion to data not valid (read hold time)[3]	t_{OFF}	0.0	0.0	—	0.0	—	ns
162	$\overline{RAS}$ deassertion to $\overline{RAS}$ assertion	t_{RP}	$6.25 \times T_C - 4.0$	74.1	—	58.5	—	ns
163	$\overline{RAS}$ assertion pulse width	t_{RAS}	$9.75 \times T_C - 4.0$	117.9	—	93.5	—	ns
164	$\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$6.25 \times T_C - 4.0$	74.1	—	58.5	—	ns
165	$\overline{RAS}$ assertion to $\overline{CAS}$ deassertion	t_{CSH}	$8.25 \times T_C - 4.0$	99.1	—	78.5	—	ns
166	$\overline{CAS}$ assertion pulse width	t_{CAS}	$4.75 \times T_C - 4.0$	55.4	—	43.5	—	ns

Table 2-16 DRAM Out-of-Page and Refresh Timings, Fifteen Wait States[1, 2](Continued)

No.	Characteristics	Symbol	Expression	80 MHz		100 MHz		Unit
				Min	Max	Min	Max	
167	$\overline{RAS}$ assertion to $\overline{CAS}$ assertion	t_{RCD}	$3.5 \times T_C \pm 2$	41.8	45.8	33.0	37.0	ns
168	$\overline{RAS}$ assertion to column address valid	t_{RAD}	$2.75 \times T_C \pm 2$	32.4	36.4	25.5	29.5	ns
169	$\overline{CAS}$ deassertion to $\overline{RAS}$ assertion	t_{CRP}	$7.75 \times T_C - 4.0$	92.9	—	73.5	—	ns
170	$\overline{CAS}$ deassertion pulse width	t_{CP}	$6.25 \times T_C - 4.0$	74.1	—	58.5	—	ns
171	Row address valid to $\overline{RAS}$ assertion	t_{ASR}	$6.25 \times T_C - 4.0$	74.1	—	58.5	—	ns
172	$\overline{RAS}$ assertion to row address not valid	t_{RAH}	$2.75 \times T_C - 4.0$	30.4	—	23.5	—	ns
173	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$0.75 \times T_C - 4.0$	5.4	—	3.5	—	ns
174	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$6.25 \times T_C - 4.0$	74.1	—	58.5	—	ns
175	$\overline{RAS}$ assertion to column address not valid	t_{AR}	$9.75 \times T_C - 4.0$	117.9	—	93.5	—	ns
176	Column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$7 \times T_C - 4.0$	83.5	—	66.0	—	ns
177	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$5 \times T_C - 3.8$	58.7	—	46.2	—	ns
178	$\overline{CAS}$ deassertion to $\overline{WR}$[4] assertion	t_{RCH}	$1.75 \times T_C - 3.7$	18.2	—	13.8	—	ns
179	$\overline{RAS}$ deassertion to $\overline{WR}$[4] assertion	t_{RRH}	**80 MHz**: $0.25 \times T_C - 3.0$ **100 MHz**: $0.25 \times T_C - 2.4$	 0.1 —	 — —	 — 0.1	 — —	 ns ns
180	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$6 \times T_C - 4.2$	70.8	—	55.8	—	ns
181	$\overline{RAS}$ assertion to $\overline{WR}$ deassertion	t_{WCR}	$9.5 \times T_C - 4.2$	114.6	—	90.8	—	ns
182	$\overline{WR}$ assertion pulse width	t_{WP}	$15.5 \times T_C - 4.5$	189.3	—	150.5	—	ns
183	$\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$15.75 \times T_C - 4.3$	192.6	—	153.2	—	ns

Table 2-16 DRAM Out-of-Page and Refresh Timings, Fifteen Wait States[1, 2](Continued)

No.	Characteristics	Symbol	Expression	80 MHz		100 MHz		Unit
				Min	Max	Min	Max	
184	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	**80 MHz:** $14.25 \times T_C - 4.3$ **100 MHz:** $14.75 \times T_C - 4.3$	180.1 —	—	— 143.2	—	ns ns
185	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	$8.75 \times T_C - 4.0$	105.4	—	83.5	—	ns
186	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$6.25 \times T_C - 4.0$	74.1	—	58.5	—	ns
187	$\overline{RAS}$ assertion to data not valid (write)	t_{DHR}	$9.75 \times T_C - 4.0$	117.9	—	93.5	—	ns
188	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$9.5 \times T_C - 4.3$	114.5	—	90.7	—	ns
189	$\overline{CAS}$ assertion to $\overline{RAS}$ assertion (refresh)	t_{CSR}	$1.5 \times T_C - 4.0$	14.8	—	11.0	—	ns
190	$\overline{RAS}$ deassertion to $\overline{CAS}$ assertion (refresh)	t_{RPC}	$4.75 \times T_C - 4.0$	55.4	—	43.5	—	ns
191	$\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$15.5 \times T_C - 4.0$	189.8	—	151.0	—	ns
192	$\overline{RD}$ assertion to data valid	t_{GA}	**80 MHz**: $14 \times T_C - 6.5$ **100 MHz**: $14 \times T_C - 5.7$	— —	168.5 —	— —	— 134.3	ns ns
193	$\overline{RD}$ deassertion to data not valid[3]	t_{GZ}	—	0.0	—	0.0	—	ns
194	$\overline{WR}$ assertion to data active	—	$0.75 \times T_C - 0.3$	9.1	—	7.2	—	ns
195	$\overline{WR}$ deassertion to data high impedance	—	$0.25 \times T_C$	—	3.1	—	2.5	ns

Note:
1. The number of wait states for out-of-page access is specified in the data control register.
2. The refresh period is specified in the data control register.
3. $\overline{RD}$ deassertion will always occur after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.
4. Either t_{RCH} or t_{RRH} must be satisfied for read cycles.

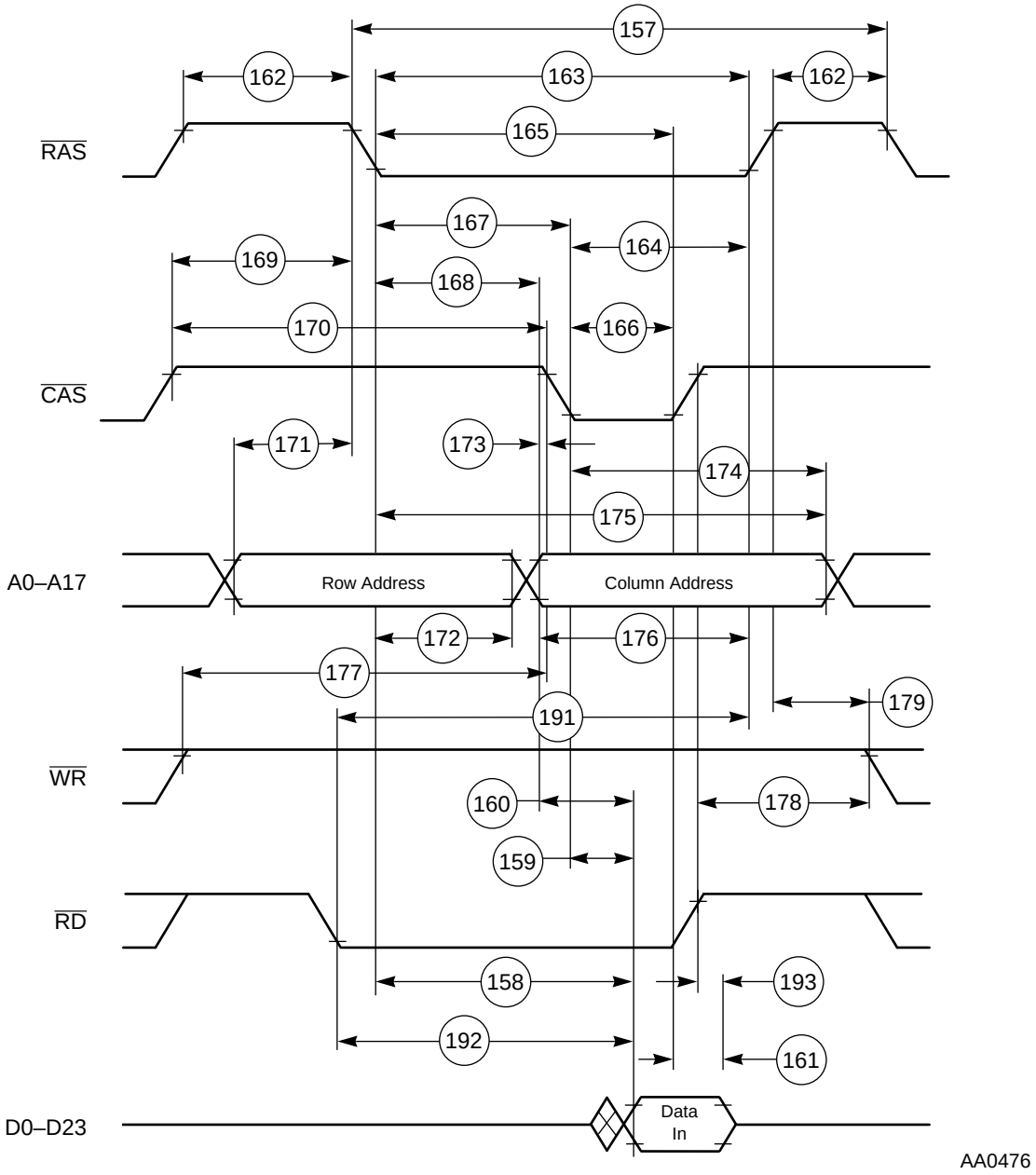


Figure 2-18 DRAM Out-of-Page Read Access

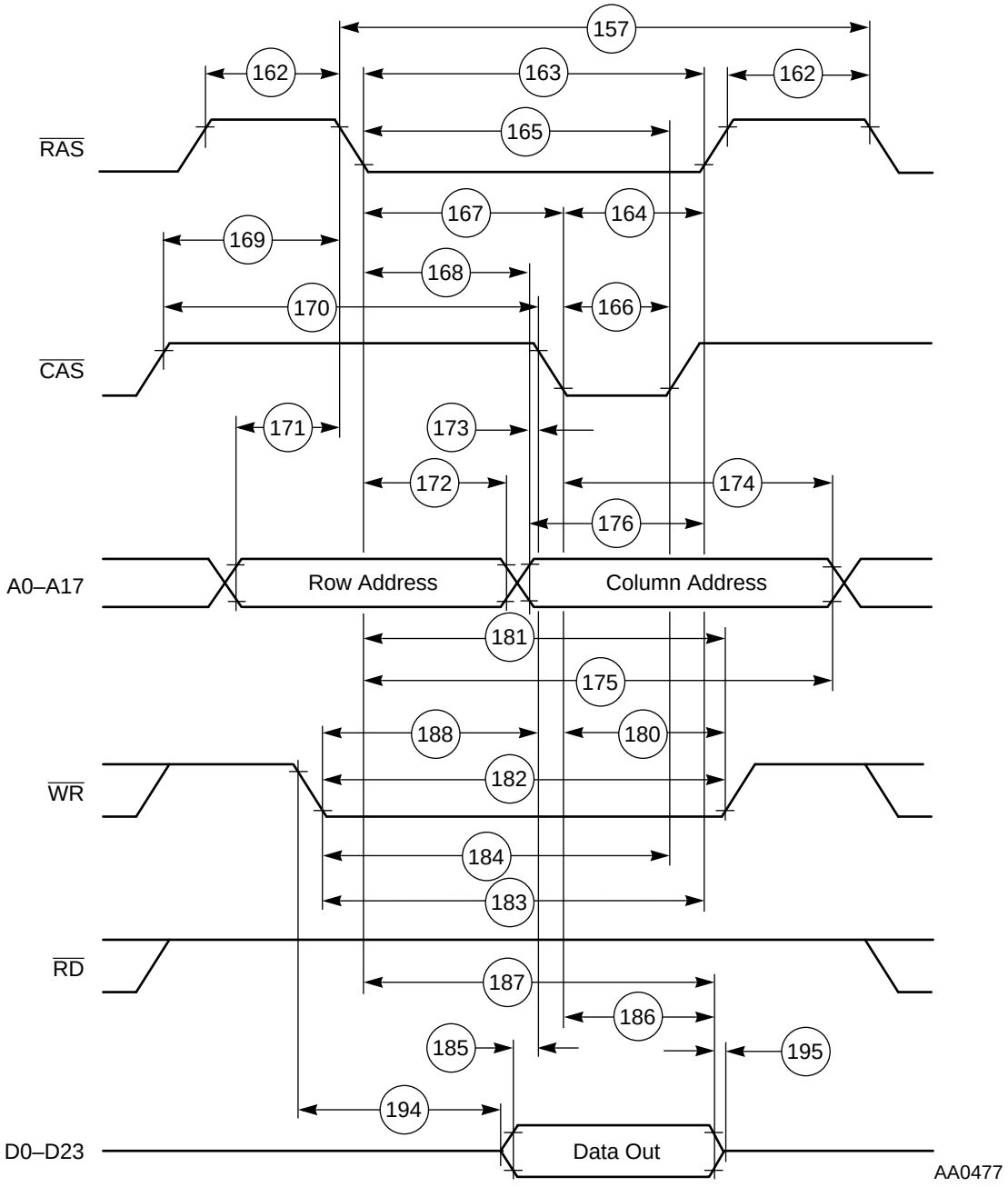


Figure 2-19 DRAM Out-of-Page Write Access

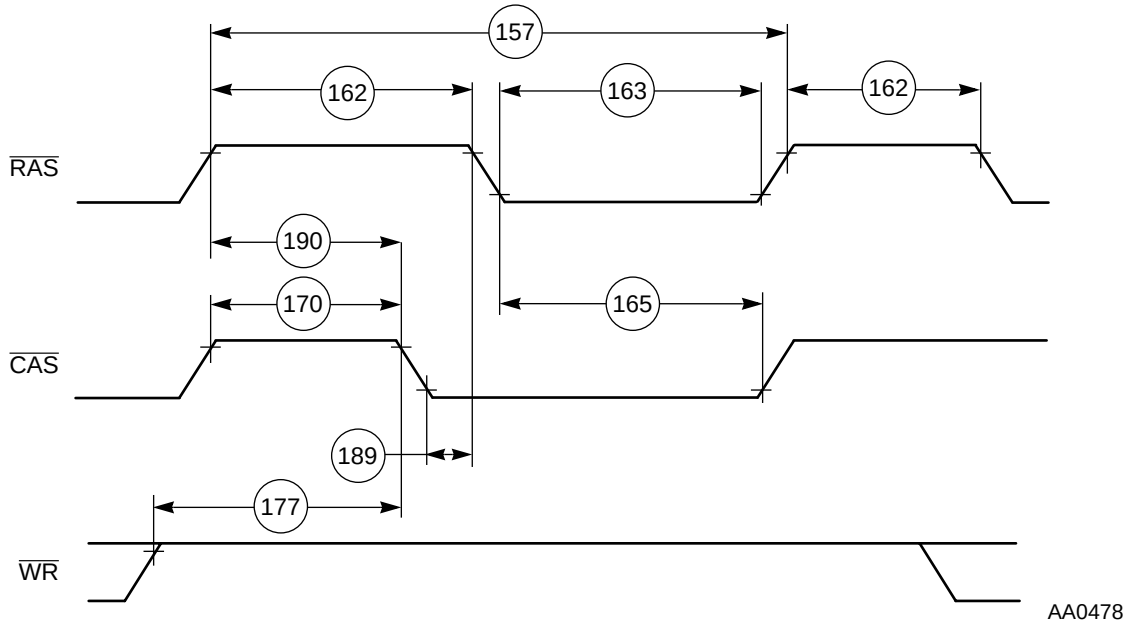


Figure 2-20 DRAM Refresh Access

Synchronous Timings (SRAM)

Table 2-17 External Bus Synchronous Timings (SRAM Access)[1]

No.	Characteristics	Expression[2, 3]	80 MHz		100 MHz		Unit
			Min	Max	Min	Max	
198	CLKOUT high to address, and AA valid[4]	**80 MHz**: $0.25 \times T_C + 4.5$ **100 MHz**: $0.25 \times T_C + 4.0$	— —	7.6 —	— —	— 6.5	ns ns
199	CLKOUT high to address, and AA invalid[4]	$0.25 \times T_C$	3.1	—	2.5	—	ns
200	$\overline{TA}$ valid to CLKOUT high (setup time)	—	5.0	—	4.0	—	ns
201	CLKOUT high to $\overline{TA}$ invalid (hold time)	—	0.0	—	0.0	—	ns
202	CLKOUT high to data out active	$0.25 \times T_C$	3.1	—	2.5	—	ns
203	CLKOUT high to data out valid	**80 MHz**[5]: $0.25 \times T_C + 4.5$ **100 MHz**[5]: $0.25 \times T_C + 4.0$	4.1 —	7.6 —	— 3.3	— 6.5	ns ns
204	CLKOUT high to data out invalid	$0.25 \times T_C$	3.1	—	2.5	—	ns
205	CLKOUT high to data out high impedance	**80 MHz**: $0.25 \times T_C + 0.5$ **100 MHz**: $0.25 \times T_C$	— —	3.6 —	— —	— 2.5	ns ns
206	Data in valid to CLKOUT high (setup)	—	5.0	—	4.0	—	ns
207	CLKOUT high to data in invalid (hold)	—	0.0	—	0.0	—	ns
208	CLKOUT high to $\overline{RD}$ assertion	**80 MHz**[5]: $0.75 \times T_C + 4.5$ **100 MHz**[5]: $0.75 \times T_C + 4.0$	10.4 —	13.9 —	— 8.2	— 11.5	ns ns
209	CLKOUT high to $\overline{RD}$ deassertion	—	0.0	4.5	0.0	4.0	ns

Table 2-17 External Bus Synchronous Timings (SRAM Access)[1](Continued)

No.	Characteristics	Expression[2, 3]	80 MHz		100 MHz		Unit
			Min	Max	Min	Max	
210	CLKOUT high to $\overline{WR}$ assertion[6]	**80 MHz[5]**: $0.5 \times T_C + 4.8$ [WS = 1 or WS ≥ 4]	7.6	11.1	—	—	ns
		100 MHz[5]: $0.5 \times T_C + 4.3$ [WS = 1 or WS ≥ 4]	—	—	6.3	9.3	ns
		All frequencies: [2 ≤ WS ≤ 3]	1.3	4.8	1.3	4.3	ns
211	CLKOUT high to $\overline{WR}$ deassertion	—	0.0	4.3	0.0	3.8	ns

Note:
1. External bus synchronous timings should be used only for reference to the clock and *not* for relative timings.
2. WS is the number of wait states specified in the bus control register (BCR).
3. The asynchronous delays specified in the expressions are valid for DSP56309.
4. T198 and T199 are valid for address trace mode if the ATE bit in the OMR is set. Use the status of $\overline{BR}$ (See T212) to determine whether the access referenced by A0–A23 is internal or external, when this mode is enabled.
5. When both a minimum and maximum value are shown, use the expression to calculate the worst case.
6. If WS > 1, $\overline{WR}$ assertion refers to the next rising edge of CLKOUT.

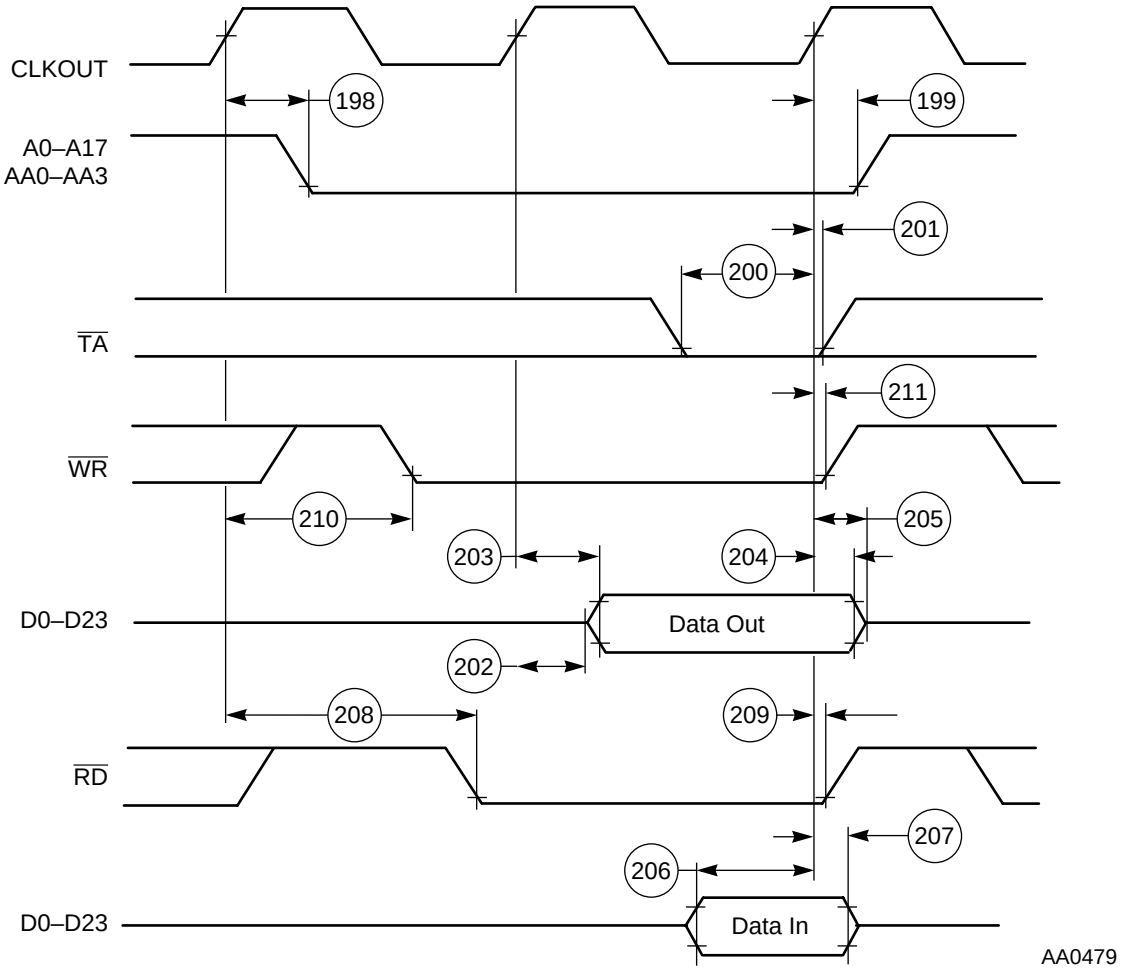


Figure 2-21 Synchronous Bus Timings SRAM 1 WS (BCR Controlled)

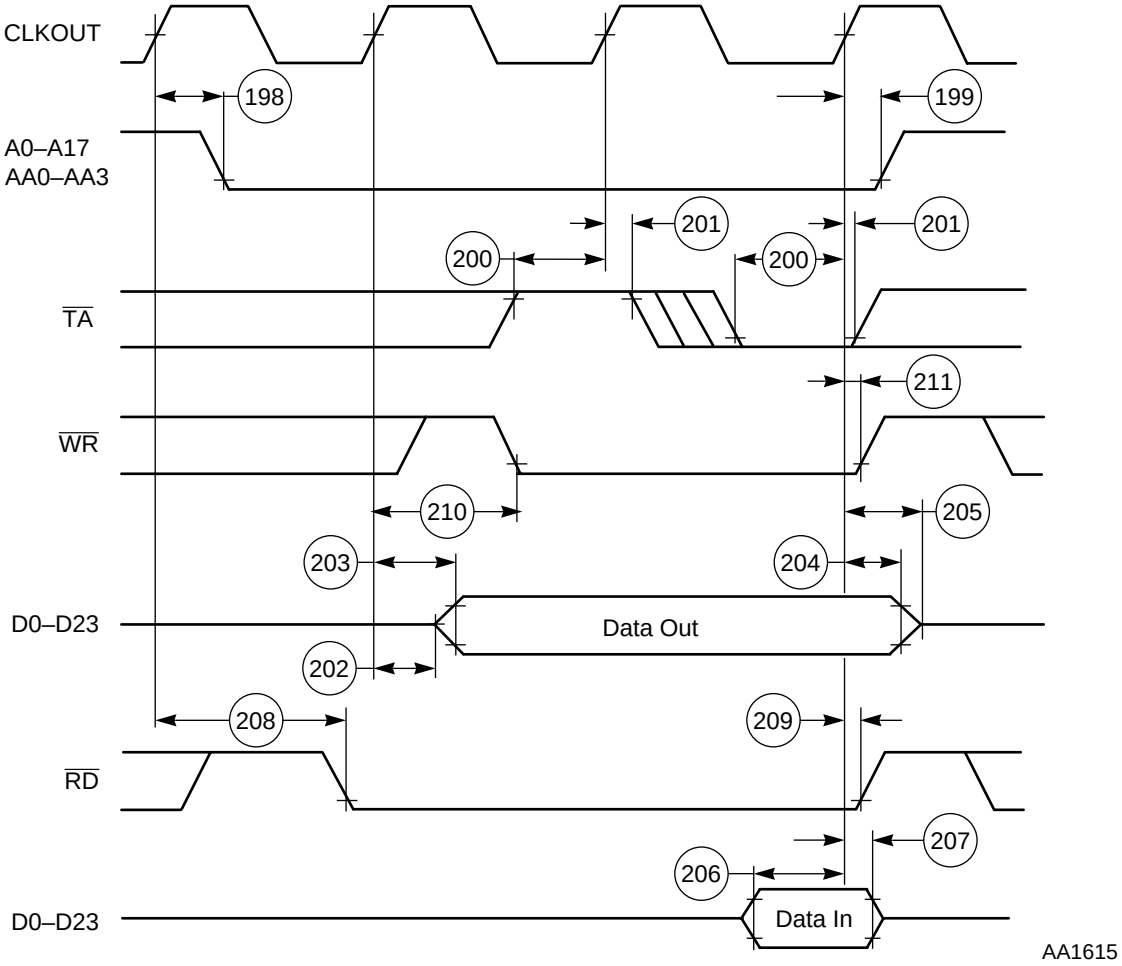


Figure 2-22 Synchronous Bus Timings SRAM, 2 or More WS, $\overline{\text{TA}}$ Controlled

Arbitration Timings

Table 2-18 Arbitration Bus Timings[1]

No.	Characteristics	Expression	80 MHz		100 MHz		Unit
			Min	Max	Min	Max	
212	CLKOUT high to $\overline{BR}$ assertion / deassertion[2]	—	1.0	4.5	1.0	4.0	ns
213	$\overline{BG}$ asserted / deasserted to CLKOUT high (setup)	—	5.0	—	4.0	—	ns
214	CLKOUT high to $\overline{BG}$ deasserted / asserted (hold)	—	0.0	—	0.0	—	ns
215	$\overline{BB}$ deassertion to CLKOUT high (input setup)	—	5.0	—	4.0	—	ns
216	CLKOUT high to $\overline{BB}$ assertion (input hold)	—	0.0	—	0.0	—	ns
217	CLKOUT high to $\overline{BB}$ assertion (output)	—	1.0	4.5	1.0	4.0	ns
218	CLKOUT high to $\overline{BB}$ deassertion (output)	—	1.0	4.5	1.0	4.0	ns
219	$\overline{BB}$ high to $\overline{BB}$ high impedance (output)	—	—	5.6	—	4.5	ns
220	CLKOUT high to address and controls active	$0.25 \times T_C$	3.1	—	2.5	—	ns
221	CLKOUT high to address and controls high impedance	**80 MHz**: $0.25 \times T_C + 0.5$ **100 MHz**: $0.25 \times T_C$	— —	3.6 —	— —	— 2.5	ns ns
222	CLKOUT high to AA active	$0.25 \times T_C$	3.1	—	2.5	—	ns
223	CLKOUT high to AA deassertion	**80 MHz**[3]: $0.25 \times T_C + 4.5$ **100 MHz**[3]: $0.25 \times T_C + 4.0$	4.1 —	7.6 —	— 3.2	— 6.5	ns ns
224	CLKOUT high to AA high impedance	**80 MHz**: $0.75 \times T_C + 0.5$ **100 MHz**: $0.75 \times T_C$	— —	9.9 —	— —	— 7.5	ns ns

Note:
1. The asynchronous delays specified in the expressions are valid for DSP56309.
2. T212 is valid for address trace mode when the ATE bit in the OMR is set. $\overline{BR}$ is deasserted for internal accesses and asserted for external accesses.
3. When both a minimum and maximum value are shown, use the expression to calculate the worst case.

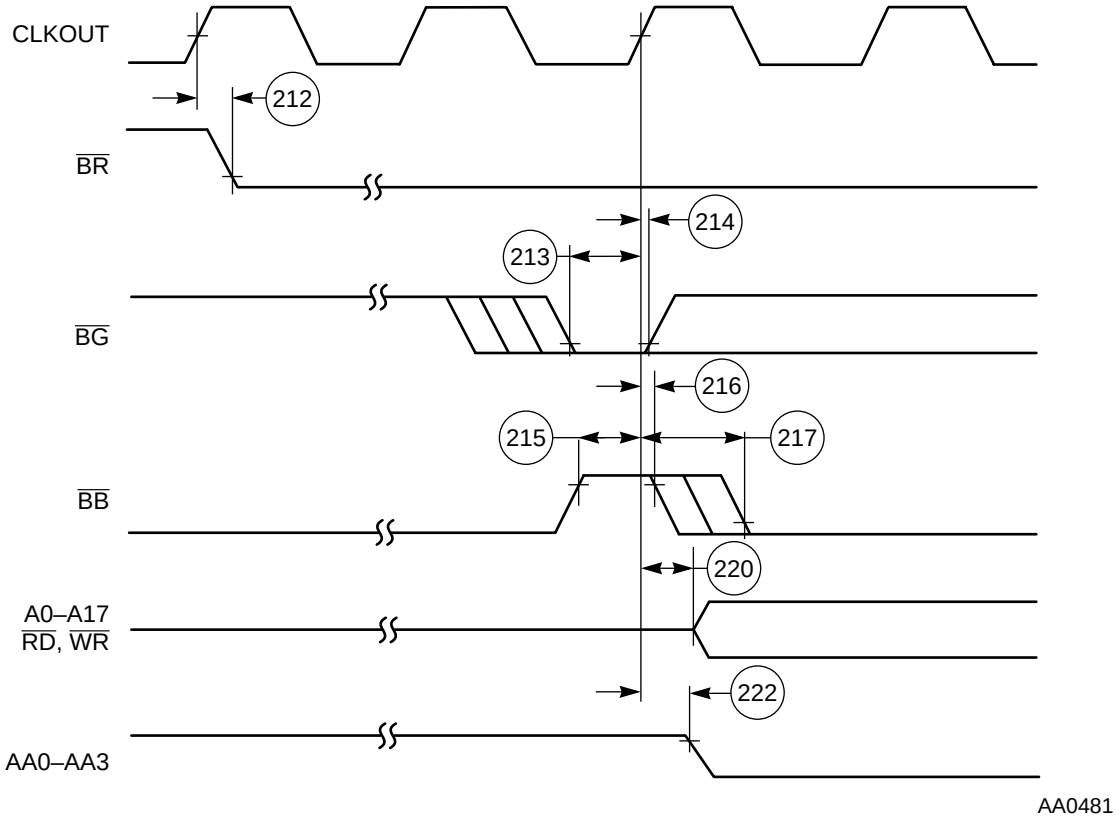


Figure 2-23 Bus Acquisition Timings

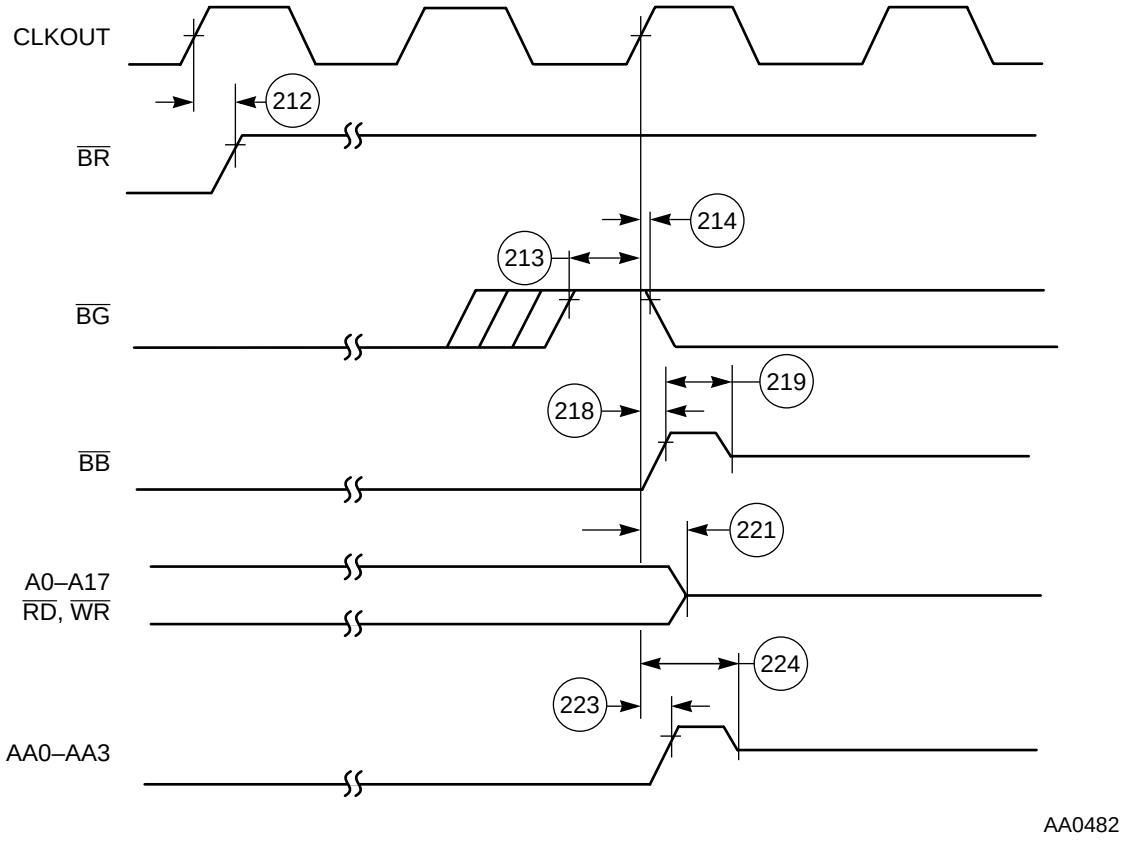


Figure 2-24 Bus Release Timings Case 1 (BRT Bit in OMR Cleared)

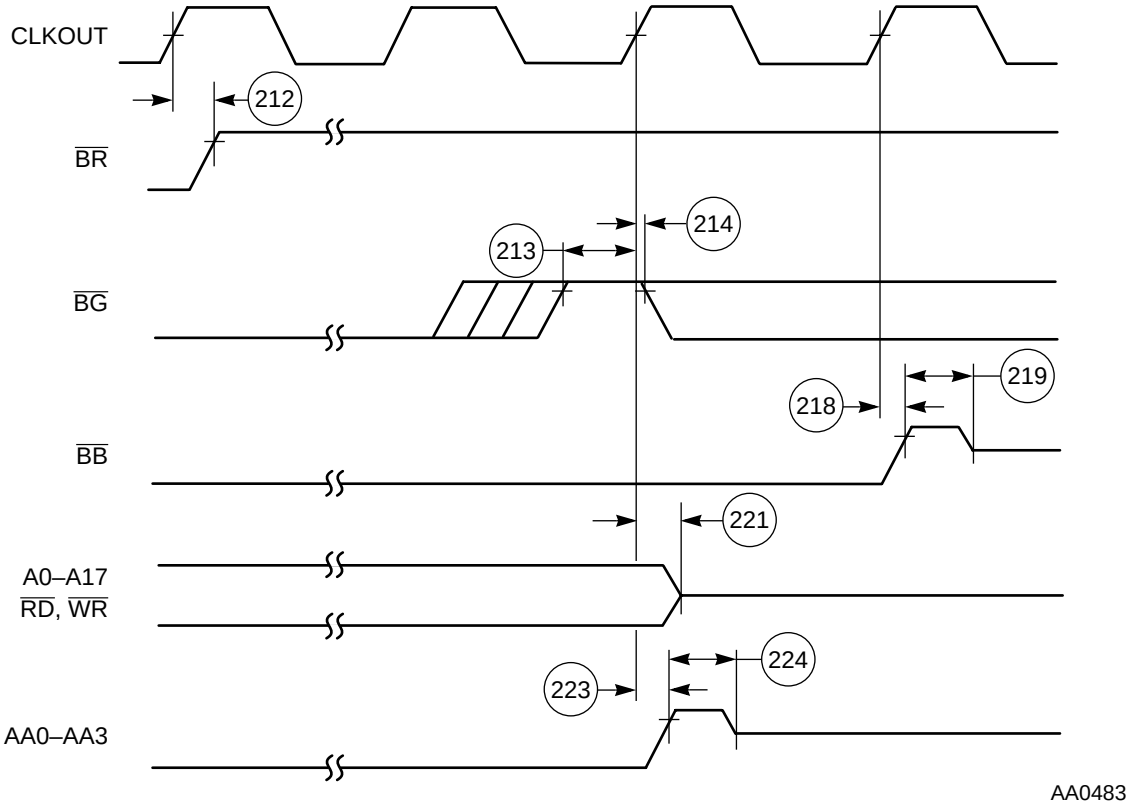


Figure 2-25 Bus Release Timings Case 2 (BRT Bit in OMR Set)

HOST INTERFACE TIMING

Table 2-19 Host Interface Timing[1, 2, 3]

No.	Characteristic	Expression	80 MHz		100 MHz		Unit
			Min	Max	Min	Max	
317	Read data strobe assertion width[4] $\overline{HACK}$ assertion width	**80 MHz**: $T_C + 12.4$ **100 MHz**: $T_C + 9.0$	24.9 —	— —	— 19.9	— —	ns ns
318	Read data strobe deassertion width[4] $\overline{HACK}$ deassertion width	—	12.4	—	9.9	—	ns
319	Read data strobe deassertion width[4] after "last data register" reads,[5, 6] or between two consecutive CVR, ICR, or ISR reads[7] $\overline{HACK}$ deassertion width after "last data register" reads[5, 6]	**80 MHz**: $2.5 \times T_C + 8.3$ **100 MHz**: $2.5 \times T_C + 6.6$	39.5 —	— —	— 33.6	— —	ns ns
320	Write data strobe assertion width[8]	—	16.5	—	13.2	—	ns
321	Write data strobe deassertion width[8]	**80 MHz**: $2.5 \times T_C + 8.3$ **100 MHz**: $2.5 \times T_C + 6.6$	39.5 —	— —	— 33.6	— —	ns ns
322	$\overline{HAS}$ assertion width	—	12.4	—	9.9	—	ns
323	$\overline{HAS}$ deassertion to data strobe assertion[9]	—	0.0	—	0.0	—	ns
324	Host data input setup time before write data strobe deassertion[8]	—	12.4	—	9.9	—	ns
325	Host data input hold time after write data strobe deassertion[8]	—	4.1	—	3.3	—	ns
326	Read data strobe assertion to output data active from high impedance[4] $\overline{HACK}$ assertion to output data active from high impedance	—	4.1	—	3.3	—	ns
327	Read data strobe assertion to output data valid[4] $\overline{HACK}$ assertion to output data valid	—	—	26.68	—	23.54	ns
328	Read data strobe deassertion to output data high impedance[4] $\overline{HACK}$ deassertion to output data high impedance	—	—	12.4	—	9.9	ns
329	Output data hold time after read data strobe deassertion[4] Output data hold time after $\overline{HACK}$ deassertion	—	4.1	—	4.1	—	ns

Table 2-19 Host Interface Timing[1, 2, 3] (Continued)

No.	Characteristic	Expression	80 MHz		100 MHz		Unit
			Min	Max	Min	Max	
330	$\overline{HCS}$ assertion to read data strobe deassertion[4]	**80 MHz**: $T_C + 12.4$ **100 MHz**: $T_C + 9.9$	24.9 —	— —	— 19.9	— —	ns ns
331	$\overline{HCS}$ assertion to write data strobe deassertion[8]	—	12.4	—	9.9	—	ns
332	$\overline{HCS}$ assertion to output data valid	—	—	20.6	—	16.5	ns
333	$\overline{HCS}$ hold time after data strobe deassertion[9]	—	0.0	—	0.0	—	ns
334	Address (AD7–AD0) setup time before $\overline{HAS}$ deassertion (HMUX=1)	—	5.8	—	4.7	—	ns
335	Address (AD7–AD0) hold time after $\overline{HAS}$ deassertion (HMUX=1)	—	4.1	—	3.3	—	ns
336	A10–A8 (HMUX=1), A2–A0 (HMUX=0), HR / $\overline{W}$ setup time before data strobe assertion[9] • Read • Write	—	 0 5.8	 — —	 0 4.7	 — —	 ns ns
337	A10–A8 (HMUX=1), A2–A0 (HMUX=0), HR / $\overline{W}$ hold time after data strobe deassertion[9]	—	4.1	—	3.3	—	ns
338	Delay from read data strobe deassertion to host request assertion for “last data register” read[4, 5, 10]	**80 MHz**: $2 \times T_C + 20.6$ **100 MHz**: $2 \times T_C + 20.6$	45.6 —	— —	— 36.5	— —	ns ns
339	Delay from write data strobe deassertion to host request assertion for “last data register” write[5, 8, 10]	**80 MHz**: $1.5 \times T_C + 20.6$ **100 MHz**: $1.5 \times T_C + 16.5$	39.4 —	— —	— 31.5	— —	ns ns
340	Delay from data strobe assertion to host request deassertion for “last data register” read or write (HROD=0)[5, 9, 10]	—	—	22.55	—	20.24	ns
341	Delay from data strobe assertion to host request deassertion for “last data register” read or write (HROD=1, open drain host request)[5, 9, 10, 11]	—	—	300.0	—	300.0	ns

Table 2-19 Host Interface Timing[1, 2, 3] (Continued)

No.	Characteristic	Expression	80 MHz		100 MHz		Unit
			Min	Max	Min	Max	

Note:
1. See *Host Port Usage* in the *DSP56309 User's Manual, Section 2, Signal/Connection Descriptions.*
2. In the timing diagrams below, the controls pins are drawn as active low. The pin polarity is programmable.
3. V_{CCQL} = 3.3 V ± 0.3 V; T_J = –40˚C to +100 ˚C, C_L = 50 pF
4. The read data strobe is HRD in the dual data strobe mode and HDS in the single data strobe mode.
5. The "last data register" is the register at address $7, which is the last location to be read or written in data transfers. This is RXL / TXL in the little endian mode (HBE = 0), or RXH / TXH in the big endian mode (HBE = 1).
6. This timing is applicable only if a read from the "last data register" is followed by a read from the RXL, RXM, or RXH registers without first polling RXDF or HREQ bits, or waiting for the assertion of the HREQ signal.
7. This timing is applicable only if two consecutive reads from one of these registers are executed.
8. The write data strobe is HWR in the dual data strobe mode and HDS in the single data strobe mode.
9. The data strobe is host read (HRD) or host write (HWR) in the dual data strobe mode and host data strobe (HDS) in the single data strobe mode.
10. The host request is HREQ in the single host request mode and HRRQ and HTRQ in the double host request mode.
11. In this calculation, the host request signal is pulled up by a 4.7 kΩ resistor in the open-drain mode.

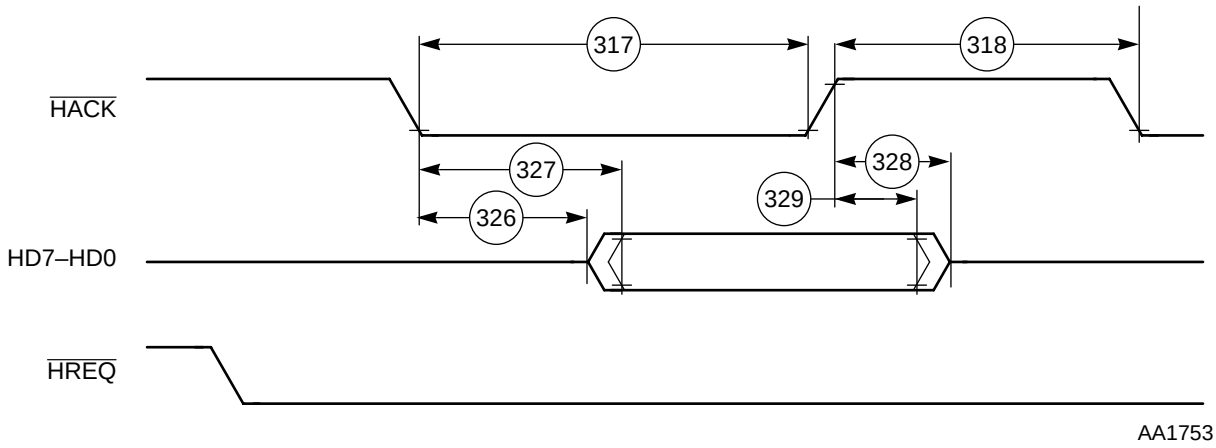


Figure 2-26 Host Interrupt Vector Register (IVR) Read Timing Diagram

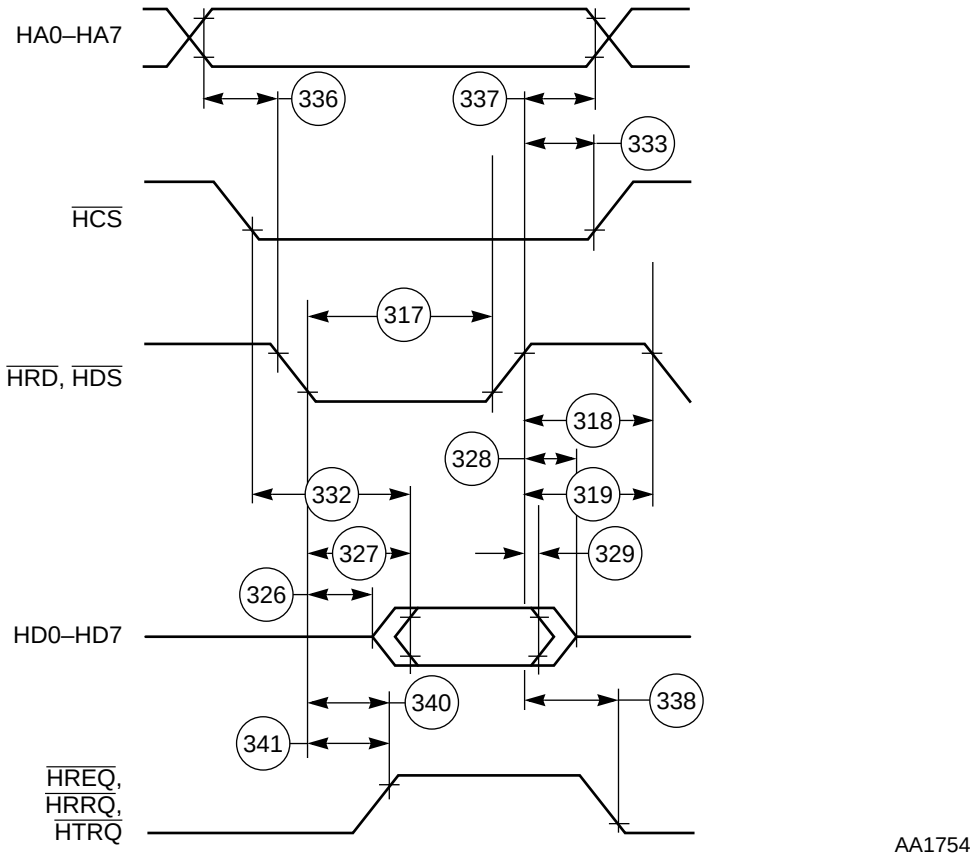


Figure 2-27 Read Timing Diagram, Non-Multiplexed Bus

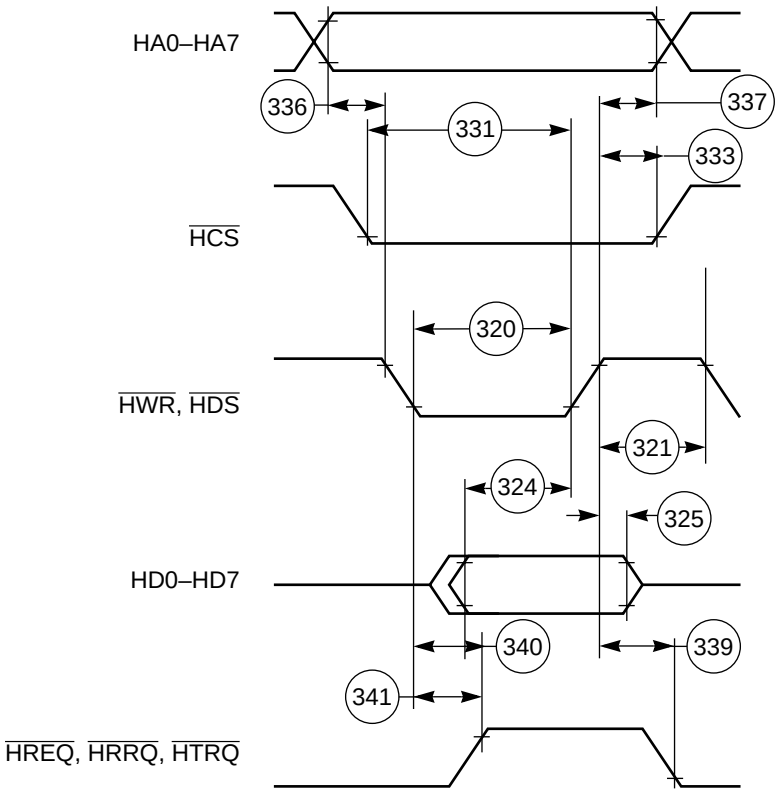


Figure 2-28 Write Timing Diagram, Non-Multiplexed Bus

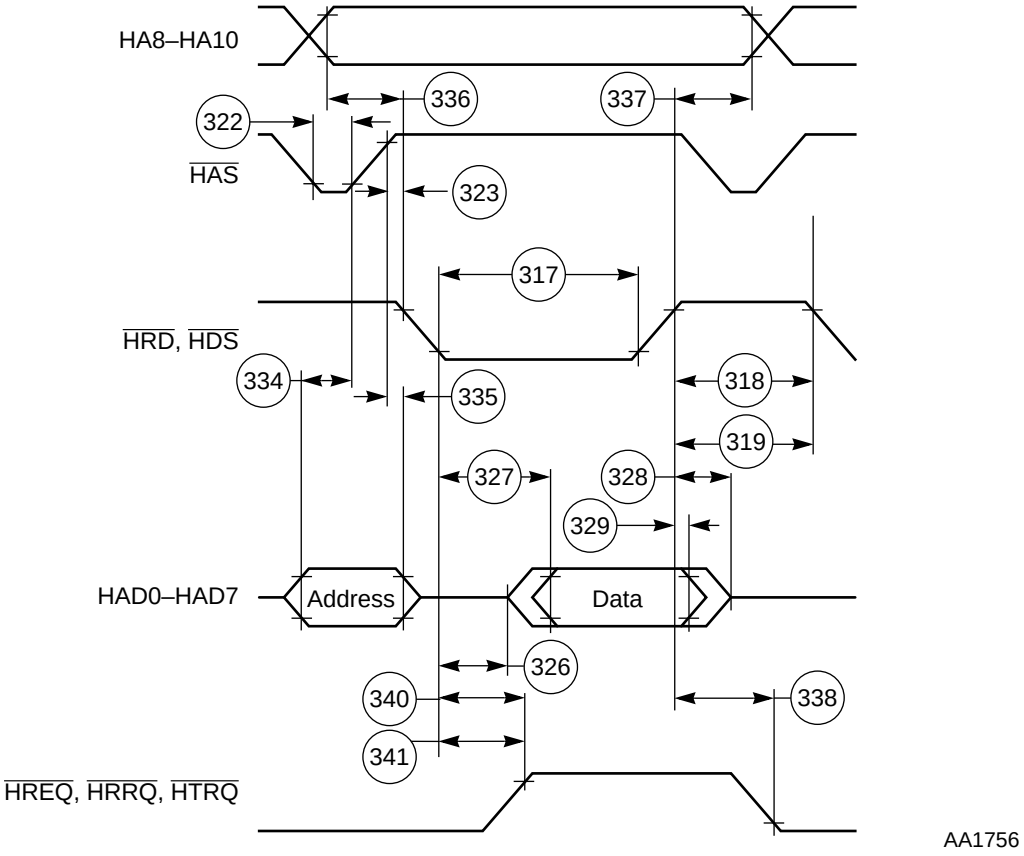


Figure 2-29 Read Timing Diagram, Multiplexed Bus

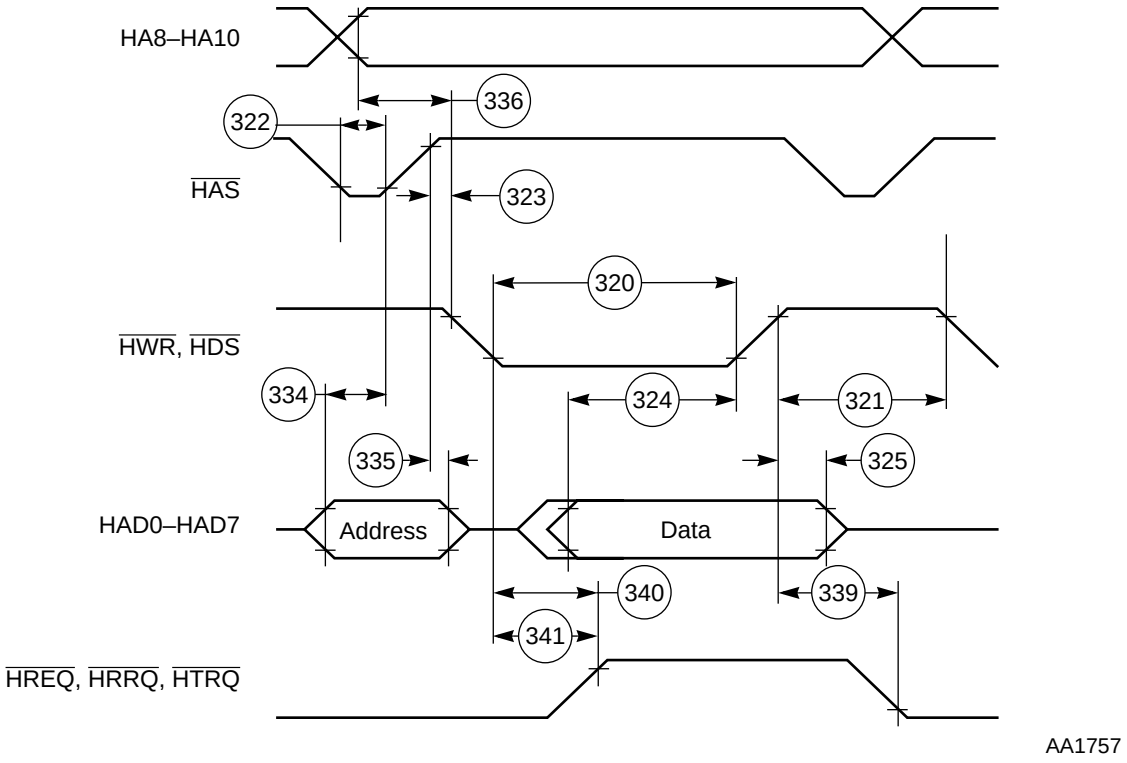


Figure 2-30 Write Timing Diagram, Multiplexed Bus

SCI TIMING

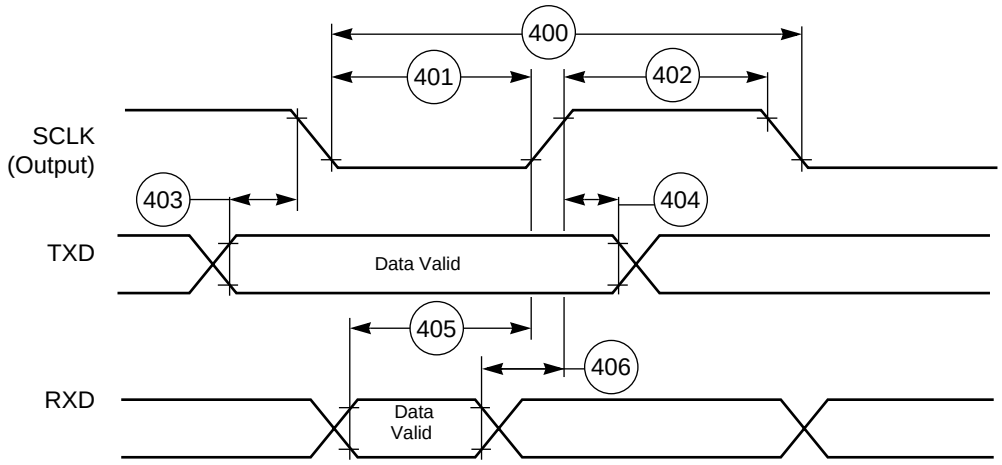
Table 2-20 SCI Timing[1]

No.	Characteristics	Symbol	Expression	80 MHz		100 MHz		Unit
				Min	Max	Min	Max	
400	Synchronous clock cycle	t_{SCC}[2]	$8 \times T_C$	100.0	—	80.0	—	ns
401	Clock low period	—	$t_{SCC} / 2 - 10.0$	40.0	—	30.0	—	ns
402	Clock high period	—	$t_{SCC} / 2 - 10.0$	40.0	—	30.0	—	ns
403	Output data setup to clock falling edge (internal clock)	—	$t_{SCC} / 4 + 0.5 \times T_C - 17.0$	14.3	—	8.0	—	ns
404	Output data hold after clock rising edge (internal clock)	—	$t_{SCC} / 4 - 0.5 \times T_C$	18.8	—	15.0	—	ns
405	Input data setup time before clock rising edge (internal clock)	—	$t_{SCC} / 4 + 0.5 \times T_C + 25.0$	56.3	—	50.0	—	ns
406	Input data not valid before clock rising edge (internal clock)	—	$t_{SCC} / 4 + 0.5 \times T_C - 5.5$	—	25.8	—	19.5	ns
407	Clock falling edge to output data valid (external clock)	—	—	—	32.0	—	32.0	ns
408	Output data hold after clock rising edge (external clock)	—	$T_C + 8.0$	20.5	—	18.0	—	ns
409	Input data setup time before clock rising edge (external clock)	—	—	0.0	—	0.0	—	ns
410	Input data hold time after clock rising edge (external clock)	—	—	9.0	—	9.0	—	ns
411	Asynchronous clock cycle	t_{ACC}[3]	$64 \times T_C$	800.0	—	640.0	—	ns
412	Clock low period	—	$t_{ACC} / 2 - 10.0$	390.0	—	310.0	—	ns
413	Clock high period	—	$t_{ACC} / 2 - 10.0$	390.0	—	310.0	—	ns

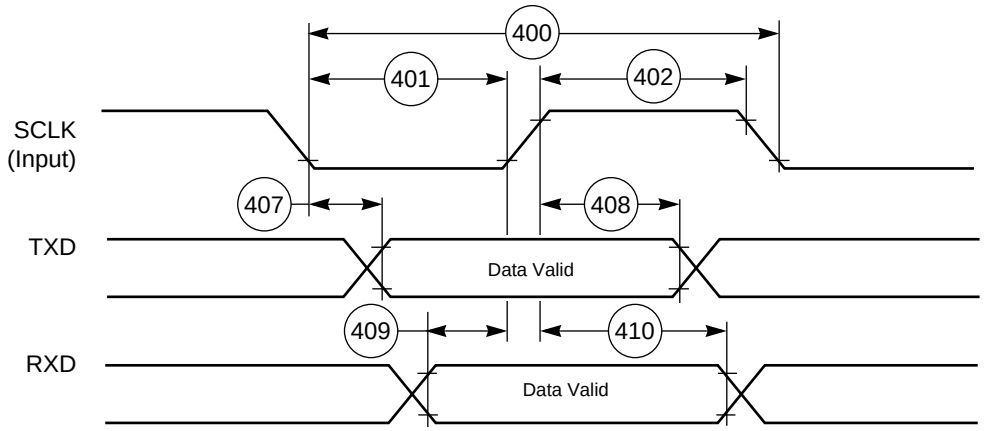
Table 2-20 SCI Timing[1]

No.	Characteristics	Symbol	Expression	80 MHz		100 MHz		Unit
				Min	Max	Min	Max	
414	Output data setup to clock rising edge (internal clock)	—	$t_{ACC}/2 - 30.0$	370.0	—	290.0	—	ns
415	Output data hold after clock rising edge (internal clock)	—	$t_{ACC}/2 - 30.0$	370.0	—	290.0	—	ns

Note:
1. V_{CCQL} = 3.3 V ± 0.3 V; T_J = –40˚C to +100 ˚C, C_L = 50 pF
2. t_{SCC} = synchronous clock cycle time (For internal clock, t_{SCC} is determined by the SCI clock control register and T_C.)
3. t_{ACC} = asynchronous clock cycle time; value given for 1X clock mode (For internal clock, t_{ACC} is determined by the SCI clock control register and T_C.)



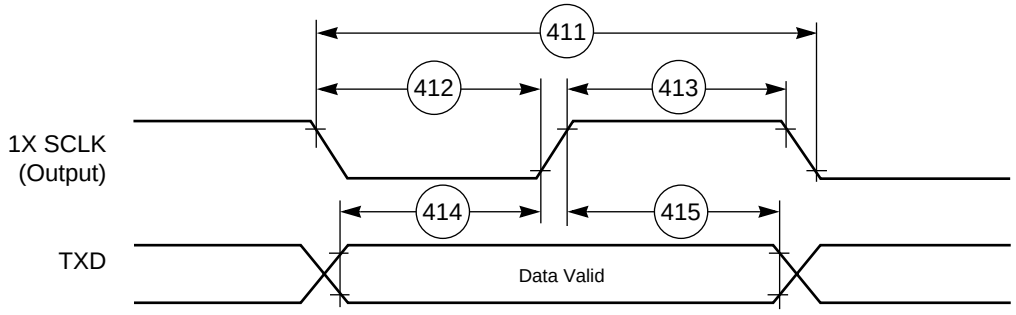
a) Internal Clock



b) External Clock

AA0488

Figure 2-31 SCI Synchronous Mode Timing



AA0489

Figure 2-32 SCI Asynchronous Mode Timing

ESSI0/ESSI1 TIMING

Table 2-21 ESSI Timings[1]

No.	Characteristics[2, 3]	Symbol	Expression	80 MHz		100 MHz		Condition[4]	Unit
				Min	Max	Min	Max		
430	Clock cycle[5]	t_{SSICC}	$3 \times T_C$ $4 \times T_C$	37.5 50.0	— —	30.0 40.0	— —	x ck i ck	ns
431	Clock high period •For internal clock •For external clock	—	 $2 \times T_C - 10.0$ $1.5 \times T_C$	 15.0 18.8	 — —	 10.0 15.0	 — —	—	 ns ns
432	Clock low period •For internal clock •For external clock	—	 $2 \times T_C - 10.0$ $1.5 \times T_C$	 15.0 18.8	 — —	 10.0 15.0	 — —	—	 ns ns
433	RXC rising edge to FSR out (bl) high	—	—	— —	37.0 22.0	— —	37.0 22.0	x ck i ck a	ns
434	RXC rising edge to FSR out (bl) low	—	—	— —	37.0 22.0	— —	37.0 22.0	x ck i ck a	ns
435	RXC rising edge to FSR out (wr) high[6]	—	—	— —	39.0 24.0	— —	39.0 24.0	x ck i ck a	ns
436	RXC rising edge to FSR out (wr) low[6]	—	—	— —	39.0 24.0	— —	39.0 24.0	x ck i ck a	ns
437	RXC rising edge to FSR out (wl) high	—	—	— —	36.0 21.0	— —	36.0 21.0	x ck i ck a	ns
438	RXC rising edge to FSR out (wl) low	—	—	— —	37.0 22.0	— —	37.0 22.0	x ck i ck a	ns
439	Data in setup time before RXC (SCK in synchronous mode) falling edge	—	—	0.0 19.0	— —	0.0 19.0	— —	x ck i ck	ns
440	Data in hold time after RXC falling edge	—	—	5.0 3.0	— —	5.0 3.0	— —	x ck i ck	ns
441	FSR input (bl, wr) high before RXC falling edge[6]	—	—	23.0 1.0	— —	23.0 1.0	— —	x ck i ck a	ns
442	FSR input (wl) high before RXC falling edge	—	—	23.0 1.0	— —	23.0 1.0	— —	x ck i ck a	ns
443	FSR input hold time after RXC falling edge	—	—	3.0 0.0	— —	3.0 0.0	— —	x ck i ck a	ns
444	Flags input setup before RXC falling edge	—	—	0.0 19.0	— —	0.0 19.0	— —	x ck i ck s	ns

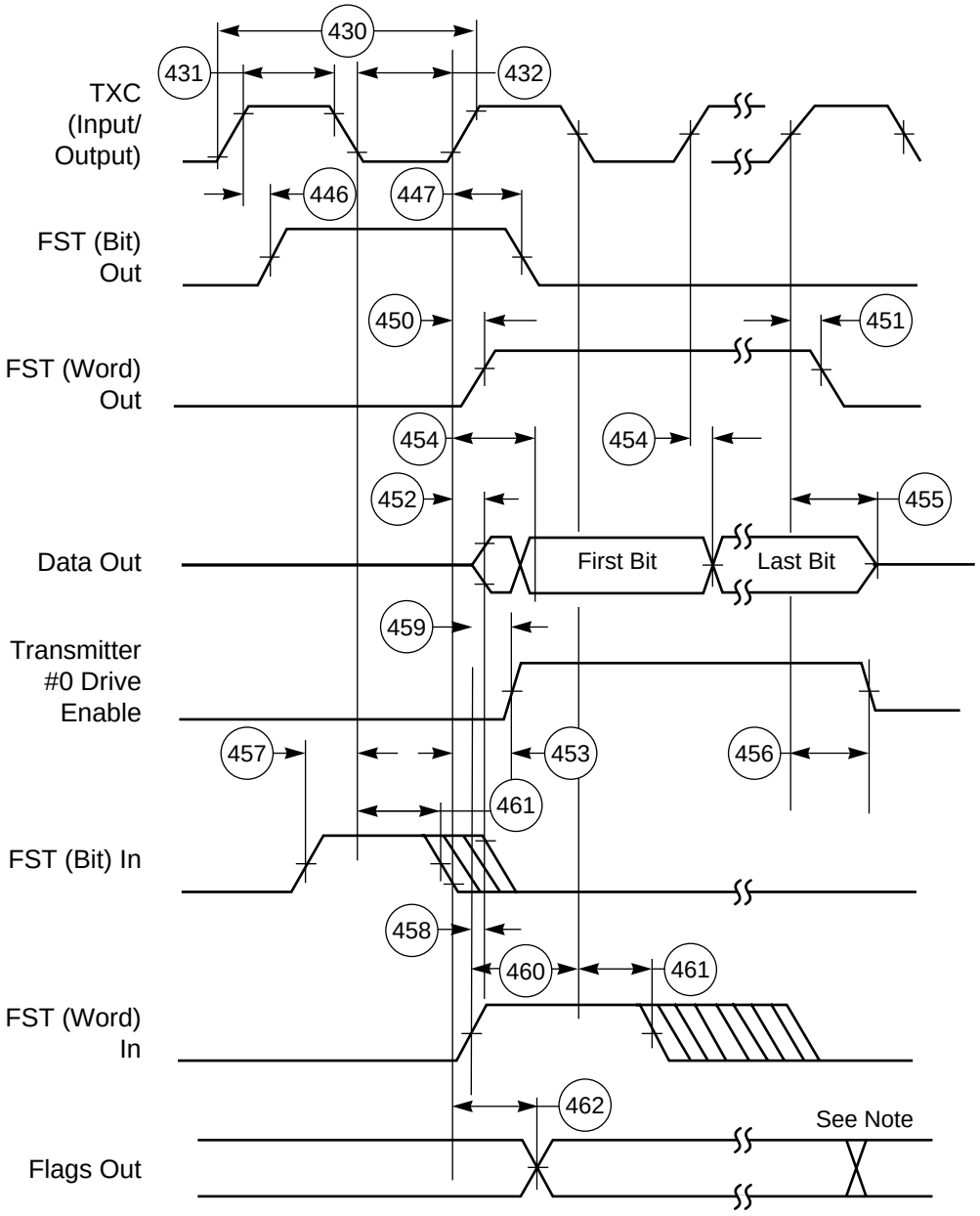
Table 2-21 ESSI Timings[1]

No.	Characteristics[2, 3]	Symbol	Expression	80 MHz		100 MHz		Condition[4]	Unit
				Min	Max	Min	Max		
445	Flags input hold time after RXC falling edge	—	—	6.0 0.0	— —	6.0 0.0	— —	x ck i ck s	ns
446	TXC rising edge to FST out (bl) high	—	—	— —	29.0 15.0	— —	29.0 15.0	x ck i ck	ns
447	TXC rising edge to FST out (bl) low	—	—	— —	31.0 17.0	— —	31.0 17.0	x ck i ck	ns
448	TXC rising edge to FST out (wr) high[6]	—	—	— —	31.0 17.0	— —	31.0 17.0	x ck i ck	ns
449	TXC rising edge to FST out (wr) low[6]	—	—	— —	33.0 19.0	— —	33.0 19.0	x ck i ck	ns
450	TXC rising edge to FST out (wl) high	—	—	— —	30.0 16.0	— —	30.0 16.0	x ck i ck	ns
451	TXC rising edge to FST out (wl) low	—	—	— —	31.0 17.0	— —	31.0 17.0	x ck i ck	ns
452	TXC rising edge to data out enable from high impedance	—	—	— —	31.0 17.0	— —	31.0 17.0	x ck i ck	ns
453	TXC rising edge to transmitter #0 drive enable assertion	—	—	— —	34.0 20.0	— —	34.0 20.0	x ck i ck	ns
454	TXC rising edge to data out valid	—	$35 + 0.5 \times T_C$ 21.0	— —	41.3 21.0	— —	40.0 21.0	x ck i ck	ns
455	TXC rising edge to data out high impedance[7]	—	—	— —	31.0 16.0	— —	31.0 16.0	x ck i ck	ns
456	TXC rising edge to transmitter #0 drive enable deassertion[7]	—	—	— —	34.0 20.0	— —	34.0 20.0	x ck i ck	ns
457	FST input (bl, wr) setup time before TXC falling edge[6]	—	—	2.0 21.0	— —	2.0 21.0	— —	x ck i ck	ns
458	FST input (wl) to data out enable from high impedance	—	—	—	27.0	—	27.0	—	ns
459	FST input (wl) to transmitter #0 drive enable assertion	—	—	—	31.0	—	31.0	—	ns

Table 2-21 ESSI Timings[1]

No.	Characteristics[2, 3]	Symbol	Expression	80 MHz		100 MHz		Condition[4]	Unit
				Min	Max	Min	Max		
460	FST input (wl) setup time before TXC falling edge	—	—	2.0 21.0	— —	2.0 21.0	— —	x ck i ck	ns
461	FST input hold time after TXC falling edge	—	—	4.0 0.0	— —	4.0 0.0	— —	x ck i ck	ns
462	Flag output valid after TXC rising edge	—	—	— —	32.0 18.0	— —	32.0 18.0	x ck i ck	ns

Note:
1. V_{CCQL} = 3.3 V ± 0.3 V; T_J = –40˚C to +100 ˚C, C_L = 50 pF
2. bl = bit length
   wl = word length
   wr = word length relative
3. TXC (SCK pin) = transmit clock
   RXC (SC0 or SCK pin) = receive clock
   FST (SC2 Pin) = transmit frame sync
   FSR (SC1 or SC2 pin) receive frame sync
4. i ck = internal clock
   x ck = external clock
   i ck a = internal clock, asynchronous mode
   (Asynchronous implies that TXC and RXC are two different clocks)
   i ck s = internal clock, synchronous mode
   (Synchronous implies that TXC and RXC are the same clock)
5. For the internal clock, the external clock cycle is defined by Icyc and the ESSI control register.
6. The word-relative frame sync signal waveform relative to the clock operates in the same manner as the bit-length frame sync signal waveform, but spreads from one serial clock before first bit clock (same as bit length frame sync signal), until the one before last bit clock of the first word in frame.
7. Periodically sampled and not 100% tested



Note: In network mode, output flag transitions can occur at the start of each time slot within the frame. In normal mode, the output flag state is asserted for the entire frame period.

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Figure 2-33 ESSI Transmitter Timing

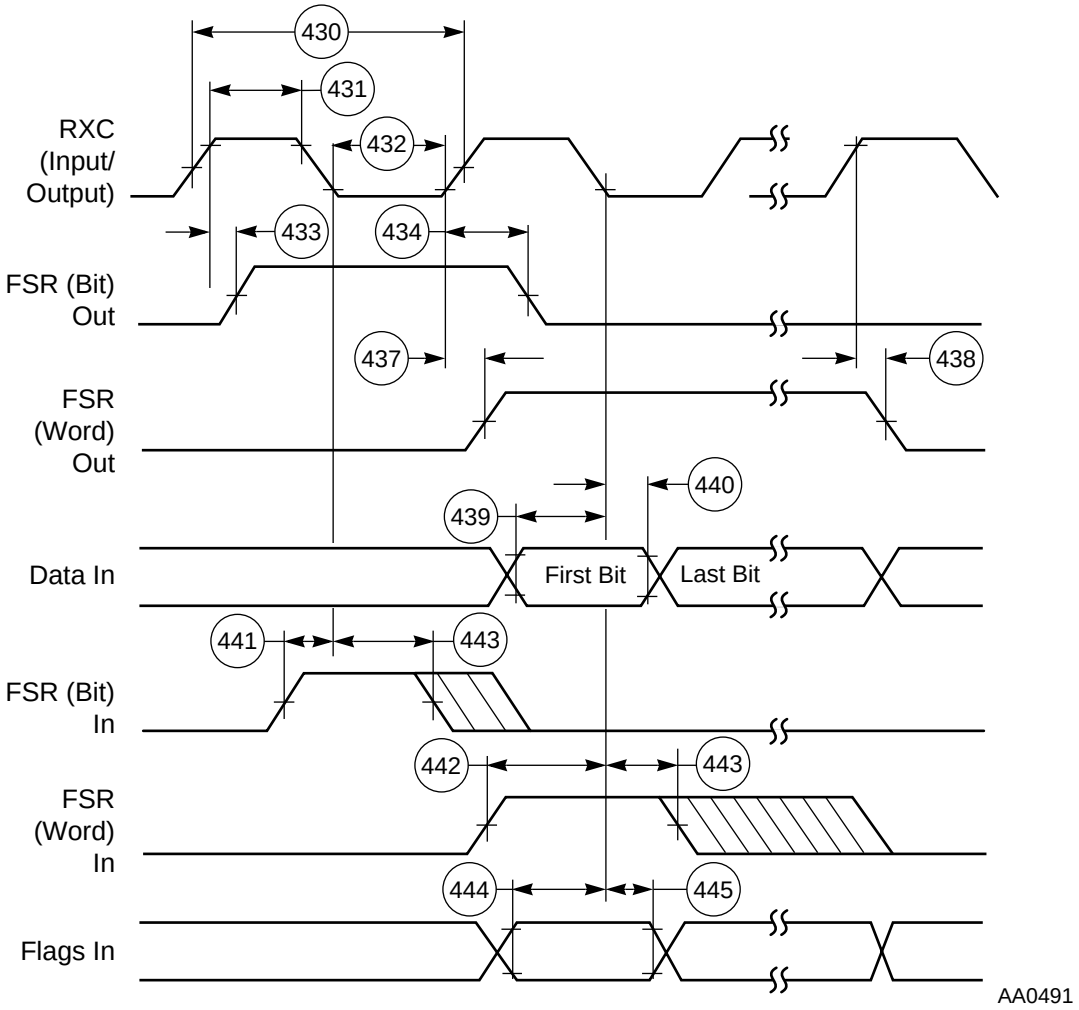


Figure 2-34 ESSI Receiver Timing

TIMER TIMING

Table 2-22 Timer Timing

No.	Characteristics	Expression	80 MHz		100 MHz		Unit
			Min	Max	Min	Max	
480	TIO Low	$2 \times T_C + 2.0$	27.0	—	22.0	—	ns
481	TIO High	$2 \times T_C + 2.0$	27.0	—	22.0	—	ns
482	Timer setup time from TIO (Input) assertion to CLKOUT rising edge	—	9.0	12.5	9.0	10.0	ns
483	Synchronous timer delay time from CLKOUT rising edge to the external memory access address out valid caused by first interrupt instruction execution	$10.25 \times T_C + 1.0$	129.1	—	103.5	—	ns
484	CLKOUT rising edge to TIO (Output) assertion • Minimum • Maximum	 $0.5 \times T_C + 3.5$ $0.5 \times T_C + 19.8$	 9.8 —	 — 26.1	 8.5 —	 — 24.8	 ns ns
485	CLKOUT rising edge to TIO (Output) deassertion • Minimum • Maximum	 $0.5 \times T_C + 3.5$ **80 MHz:** $0.5 \times T_C + 19.8$ **100 MHz**: $0.5 \times T_C + 19.0$	 9.8 — —	 — 26.1 —	 8.5 — —	 — — 24.8	 ns ns ns
Note: $V_{CCQL} = 3.3\ V \pm 0.3\ V$; $T_J = -40^{\circ}C$ to $+100^{\circ}C$, $C_L = 50\ pF$							

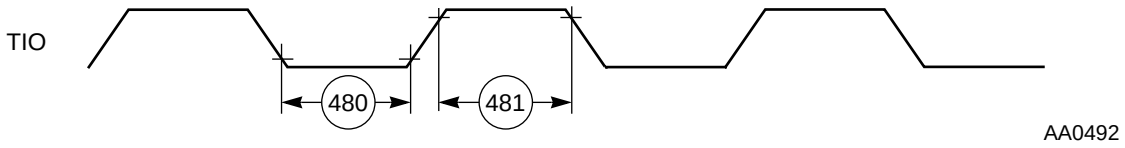


Figure 2-35 TIO Timer Event Input Restrictions

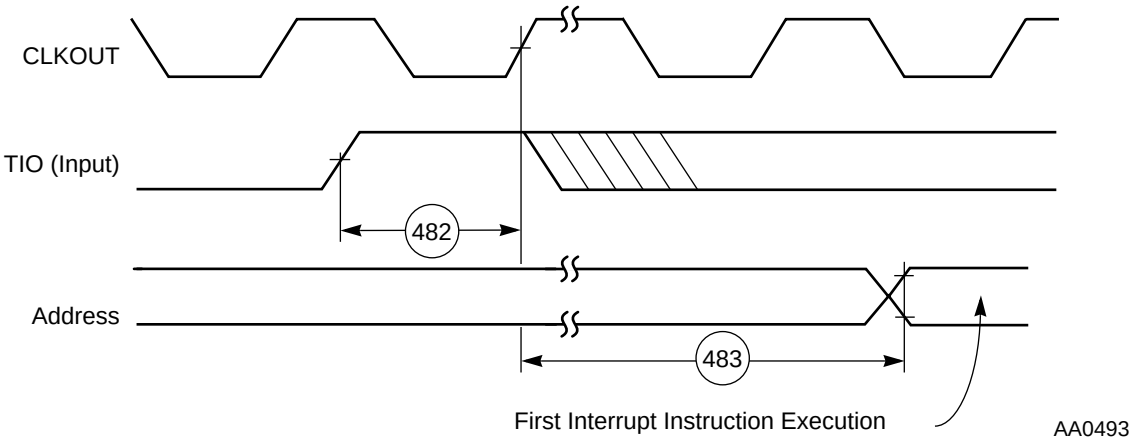


Figure 2-36 Timer Interrupt Generation

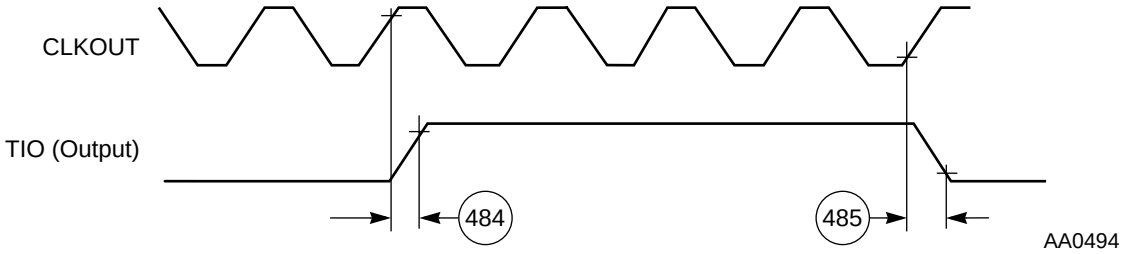
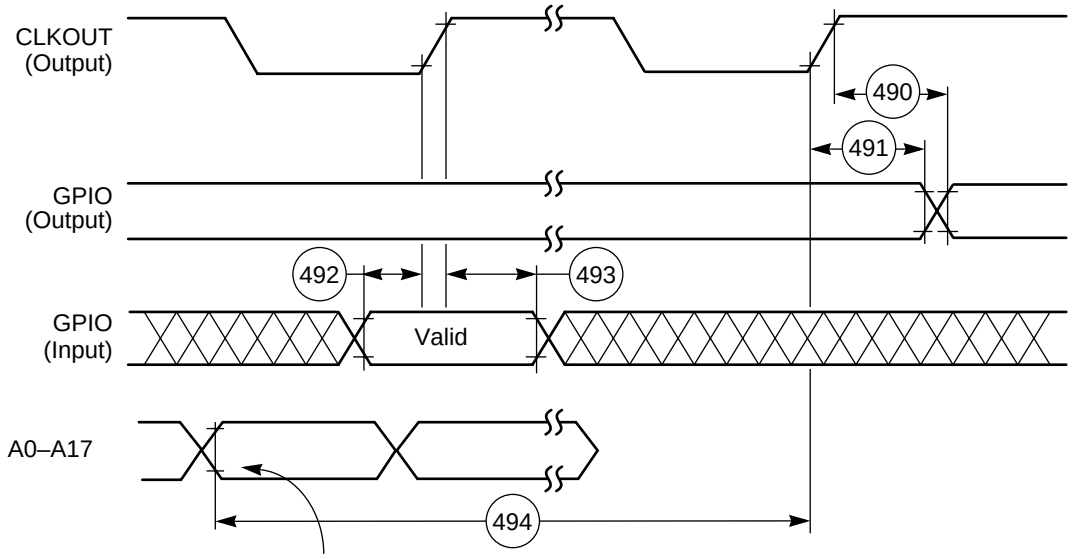


Figure 2-37 External Pulse Generation

GPIO TIMING

Table 2-23 GPIO Timing

No.	Characteristics	Expression	80 MHz		100 MHz		Unit
			Min	Max	Min	Max	
490	CLKOUT edge to GPIO out valid (GPIO out delay time)	—	—	31.0	—	31.0	ns
491	CLKOUT edge to GPIO out not valid (GPIO out hold time)	—	3.0	—	3.0	—	ns
492	GPIO In valid to CLKOUT edge (GPIO in set-up time)	—	12.0	—	12.0	—	ns
493	CLKOUT edge to GPIO in not valid (GPIO in hold time)	—	0.0	—	0.0	—	ns
494	Fetch to CLKOUT edge before GPIO change	$6.75 \times T_C$	84.4	—	67.5	—	ns
Note: V_{CCQL} = 3.3 V ± 0.3 V; T_J = –40˚C to +100 ˚C, C_L = 50 pF							



Fetch the instruction MOVE X0,X:(R0); X0 contains the new value of GPIO and R0 contains the address of GPIO data register.

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Figure 2-38 GPIO Timing

JTAG TIMING

Table 2-24 JTAG Timing[1, 2]

No.	Characteristics	All frequencies		Unit
		Min	Max	
500	TCK frequency of operation ($1/(T_C \times 3)$; maximum 22 MHz)	0.0	22.0	MHz
501	TCK cycle time in Crystal mode	45.0	—	ns
502	TCK clock pulse width measured at 1.5 V	20.0	—	ns
503	TCK rise and fall times	0.0	3.0	ns
504	Boundary scan input data setup time	5.0	—	ns
505	Boundary scan input data hold time	24.0	—	ns
506	TCK low to output data valid	0.0	40.0	ns
507	TCK low to output high impedance	0.0	40.0	ns
508	TMS, TDI data setup time	5.0	—	ns
509	TMS, TDI data hold time	25.0	—	ns
510	TCK low to TDO data valid	0.0	44.0	ns
511	TCK low to TDO high impedance	0.0	44.0	ns
512	$\overline{\text{TRST}}$ assert time	100.0	—	ns
513	$\overline{\text{TRST}}$ setup time to TCK low	40.0	—	ns

Note: 1. V_{CCQL} = 3.3 V ± 0.3 V; T_J = –40°C to +100 °C, C_L = 50 pF
2. All timings apply to OnCE module data transfers because it uses the JTAG port as an interface.

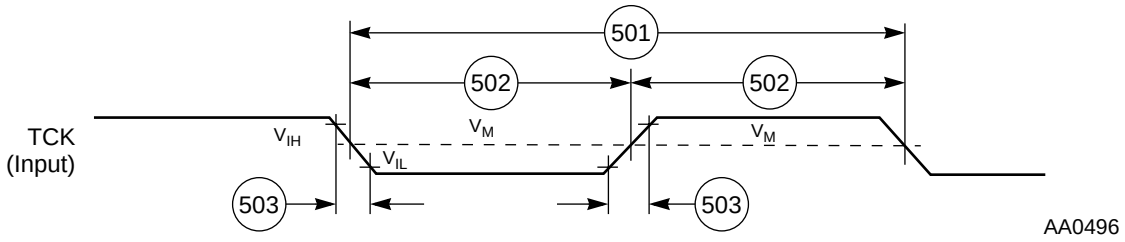


Figure 2-39 Test Clock Input Timing Diagram

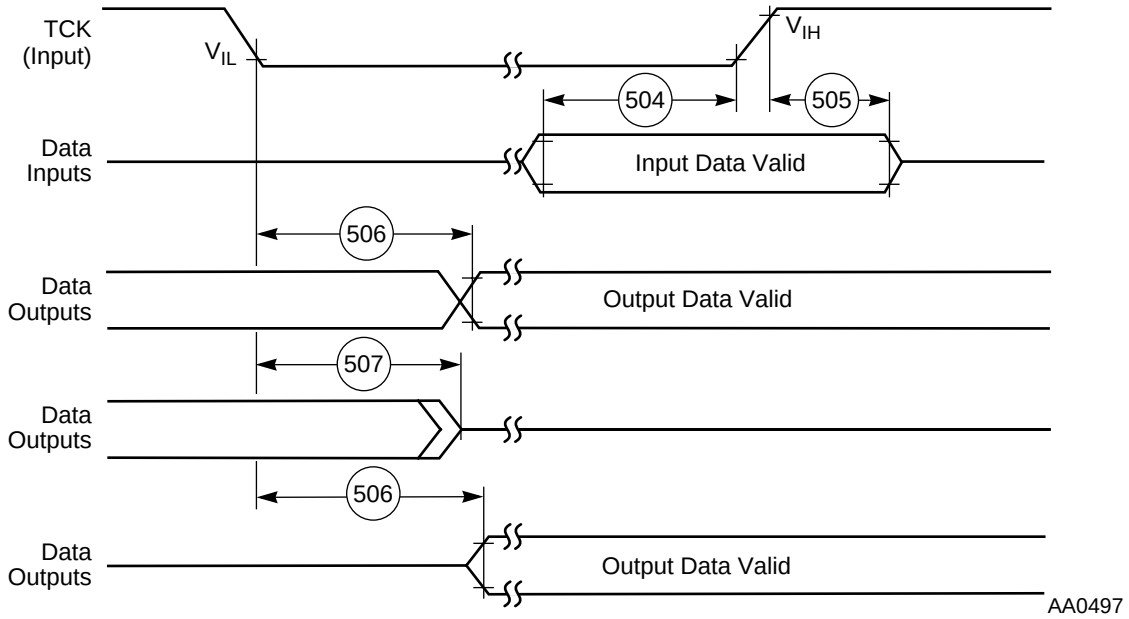


Figure 2-40 Boundary Scan (JTAG) Timing Diagram

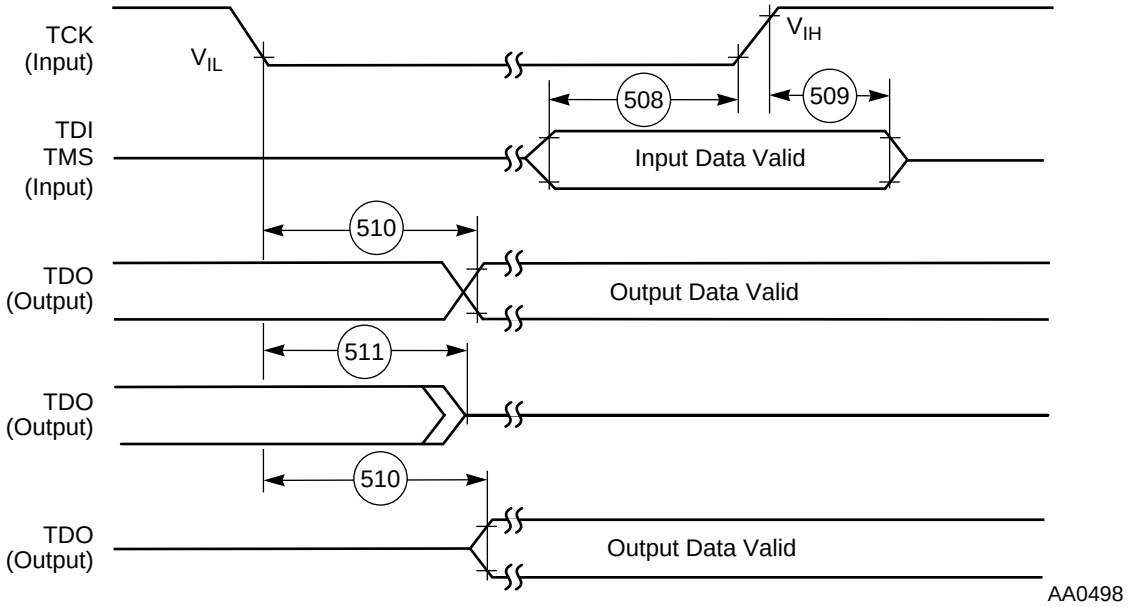


Figure 2-41 Test Access Port Timing Diagram

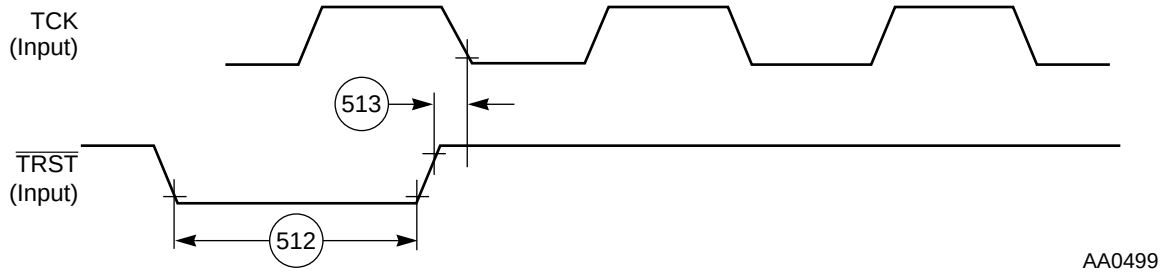


Figure 2-42 TRST Timing Diagram

OnCE MODULE TIMING

Table 2-25 OnCE Module Timing

No.	Characteristics	Expression	80 MHz		100 MHz		Unit
			Min	Max	Min	Max	
500	TCK frequency of operation	$1/(T_C \times 3)$, max 22.0 MHz	0.0	22.0	0.0	22.0	MHz
514	DE assertion time in order to enter debug mode	$1.5 \times T_C + 10.0$	28.8	—	25.0	—	ns
515	Response time when DSP56309 is executing NOP instructions from internal memory	$5.5 \times T_C + 30.0$	—	98.8	—	85.0	ns
516	Debug acknowledge assertion time	$3 \times T_C + 10.0$	47.5	—	40.0	—	ns
Note: V_{CCQL} = 3.3 V ± 0.3 V; T_J = –40°C to +100 °C, C_L = 50 pF							

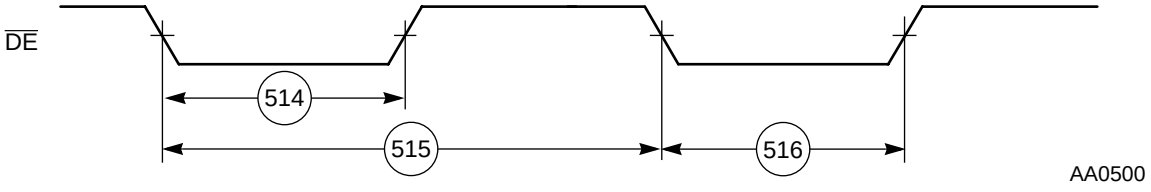


Figure 2-43 OnCE—Debug Request

SECTION 3

PACKAGING

PIN-OUT AND PACKAGE INFORMATION

This sections provides information about the available packages for this product, including diagrams of the package pinouts and tables describing how the signals described in *DSP56309 User's Manual, Section 2, Signal/Connection Descriptions* are allocated for each package.

The DSP56309 is available in two package types:

- 144-pin thin quad flat pack (TQFP)
- 196-pin plastic ball grid array (PBGA)

TQFP Package Description

Top and bottom views of the TQFP package are shown in **Figure 3-1** and **Figure 3-2** with their pin-outs.

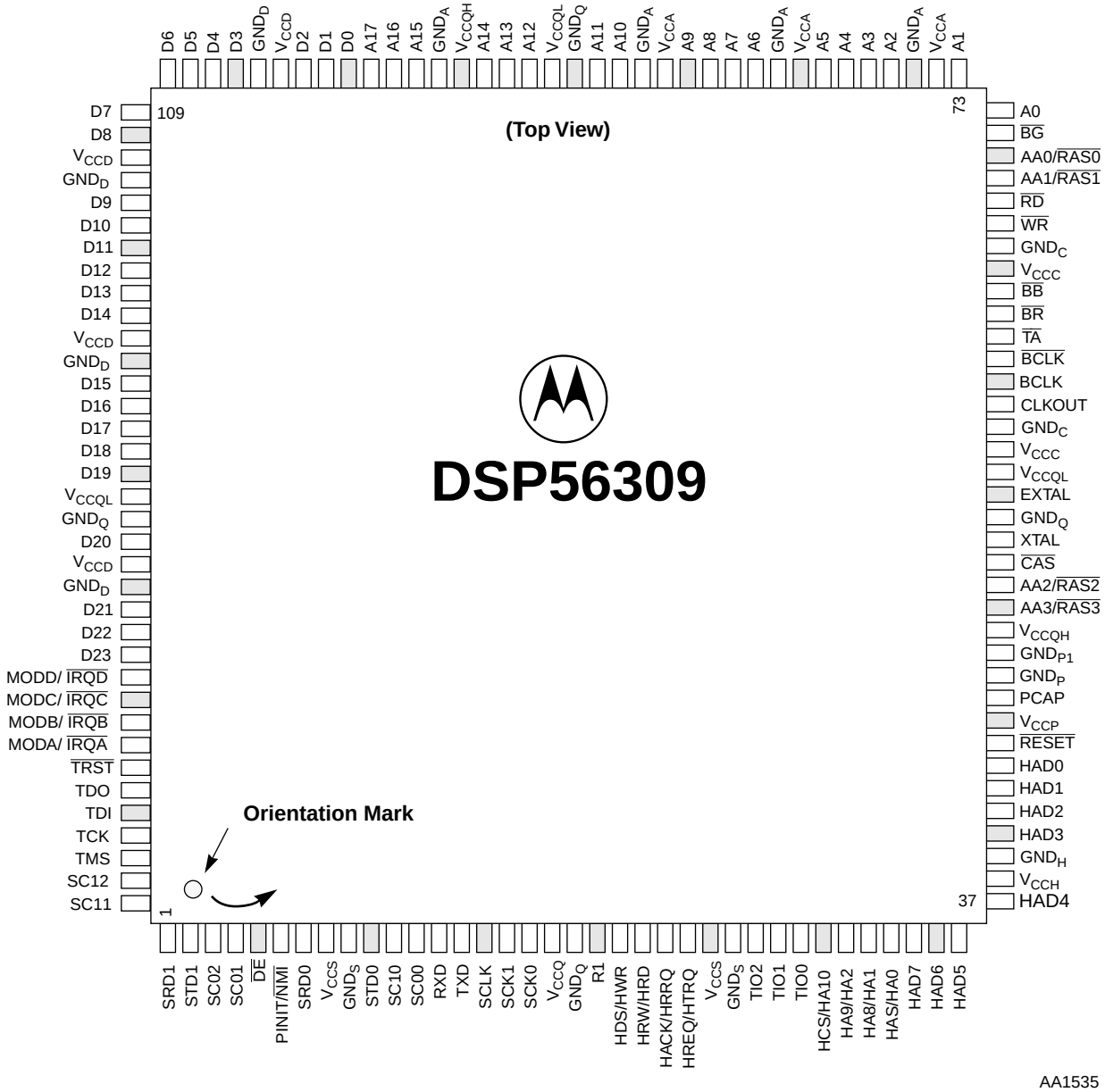


Figure 3-1 DSP56309 Thin Quad Flat Pack (TQFP), Top View

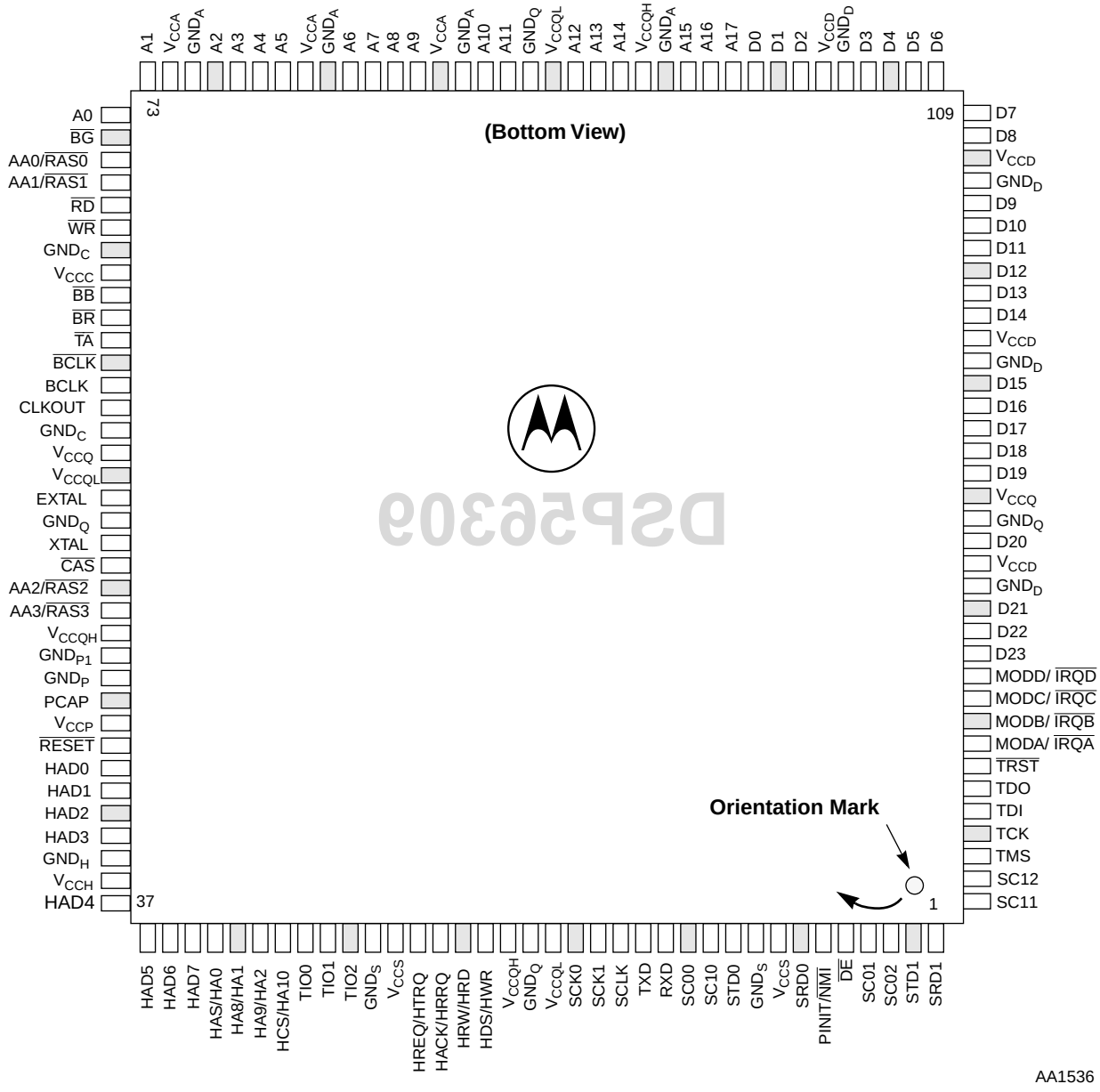


Figure 3-2 DSP56309 Thin Quad Flat Pack (TQFP), Bottom View

Table 3-1 DSP56309 TQFP Signal Identification by Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	SRD1 or PD4	26	GND_S	51	AA2/$\overline{RAS2}$
2	STD1 or PD5	27	TIO2	52	$\overline{CAS}$
3	SC02 or PC2	28	TIO1	53	XTAL
4	SC01 or PC1	29	TIO0	54	GND_Q
5	$\overline{DE}$	30	$\overline{HCS}$/HCS, HA10, or PB13	55	EXTAL
6	PINIT/$\overline{NMI}$	31	HA2, HA9, or PB10	56	V_{CCQL}
7	SRD0 or PC4	32	HA1, HA8, or PB9	57	V_{CCC}
8	V_{CCS}	33	HA0, $\overline{HAS}$/HAS, or PB8	58	GND_C
9	GND_S	34	H7, HAD7, or PB7	59	CLKOUT
10	STD0 or PC5	35	H6, HAD6, or PB6	60	BCLK
11	SC10 or PD0	36	H5, HAD5, or PB5	61	$\overline{BCLK}$
12	SC00 or PC0	37	H4, HAD4, or PB4	62	$\overline{TA}$
13	RXD or PE0	38	V_{CCH}	63	$\overline{BR}$
14	TXD or PE1	39	GND_H	64	$\overline{BB}$
15	SCLK or PE2	40	H3, HAD3, or PB3	65	V_{CCC}
16	SCK1 or PD3	41	H2, HAD2, or PB2	66	GND_C
17	SCK0 or PC3	42	H1, HAD1, or PB1	67	$\overline{WR}$
18	V_{CCQL}	43	H0, HAD0, or PB0	68	$\overline{RD}$
19	GND_Q	44	$\overline{RESET}$	69	AA1/$\overline{RAS1}$
20	V_{CCQH}	45	V_{CCP}	70	AA0/$\overline{RAS0}$
21	$\overline{HDS}$/HDS, $\overline{HWR}$/HWR, or PB12	46	PCAP	71	$\overline{BG}$
22	HRW, $\overline{HRD}$/HRD, or PB11	47	GND_P	72	A0
23	$\overline{HACK}$/HACK, $\overline{HRRQ}$/HRRQ, or PB15	48	GND_{P1}	73	A1
24	$\overline{HREQ}$/HREQ, $\overline{HTRQ}$/HTRQ, or PB14	49	V_{CCQH}	74	V_{CCA}
25	V_{CCS}	50	AA3/$\overline{RAS3}$	75	GND_A

Table 3-1 DSP56309 TQFP Signal Identification by Pin Number (Continued)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
76	A2	99	A17	122	D16
77	A3	100	D0	123	D17
78	A4	101	D1	124	D18
79	A5	102	D2	125	D19
80	V_{CCA}	103	V_{CCD}	126	V_{CCQL}
81	GND_A	104	GND_D	127	GND_Q
82	A6	105	D3	128	D20
83	A7	106	D4	129	V_{CCD}
84	A8	107	D5	130	GND_D
85	A9	108	D6	131	D21
86	V_{CCA}	109	D7	132	D22
87	GND_A	110	D8	133	D23
88	A10	111	V_{CCD}	134	MODD / $\overline{IRQD}$
89	A11	112	GND_D	135	MODC / $\overline{IRQC}$
90	GND_Q	113	D9	136	MODB / $\overline{IRQB}$
91	V_{CCQL}	114	D10	137	MODA / $\overline{IRQA}$
92	A12	115	D11	138	$\overline{TRST}$
93	A13	116	D12	139	TDO
94	A14	117	D13	140	TDI
95	V_{CCQH}	118	D14	141	TCK
96	GND_A	119	V_{CCD}	142	TMS
97	A15	120	GND_D	143	SC12 or PD2
98	A16	121	D15	144	SC11 or PD1

Note: Signal names are based on configured functionality. Most pins supply a single signal. Some pins provide a signal with dual functionality, such as the MODx/$\overline{IRQx}$ pins that select an operating mode after $\overline{RESET}$ is deasserted, but act as interrupt lines during operation. Some signals have configurable polarity; these names are shown with and without overbars, such as $\overline{HAS}$/HAS. Some pins have two or more configurable functions; names assigned to these pins indicate the function for a specific configuration. For example, pin 34 is data line H7 in non-multiplexed bus mode, data/address line HAD7 in multiplexed bus mode, or GPIO line PB7 when the GPIO function is enabled for this pin.

Table 3-2 DSP56309 TQFP Signal Identification by Name

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
A0	72	$\overline{BG}$	71	D7	109
A1	73	$\overline{BR}$	63	D8	110
A10	88	$\overline{CAS}$	52	D9	113
A11	89	CLKOUT	59	$\overline{DE}$	5
A12	92	D0	100	EXTAL	55
A13	93	D1	101	GND_A	75
A14	94	D10	114	GND_A	81
A15	97	D11	115	GND_A	87
A16	98	D12	116	GND_A	96
A17	99	D13	117	GND_C	58
A2	76	D14	118	GND_C	66
A3	77	D15	121	GND_D	104
A4	78	D16	122	GND_D	112
A5	79	D17	123	GND_D	120
A6	82	D18	124	GND_D	130
A7	83	D19	125	GND_H	39
A8	84	D2	102	GND_P	47
A9	85	D20	128	GND_{P1}	48
AA0	70	D21	131	GND_Q	19
AA1	69	D22	132	GND_Q	54
AA2	51	D23	133	GND_Q	90
AA3	50	D3	105	GND_Q	127
$\overline{BB}$	64	D4	106	GND_S	9
BCLK	60	D5	107	GND_S	26
$\overline{BCLK}$	61	D6	108	H0	43

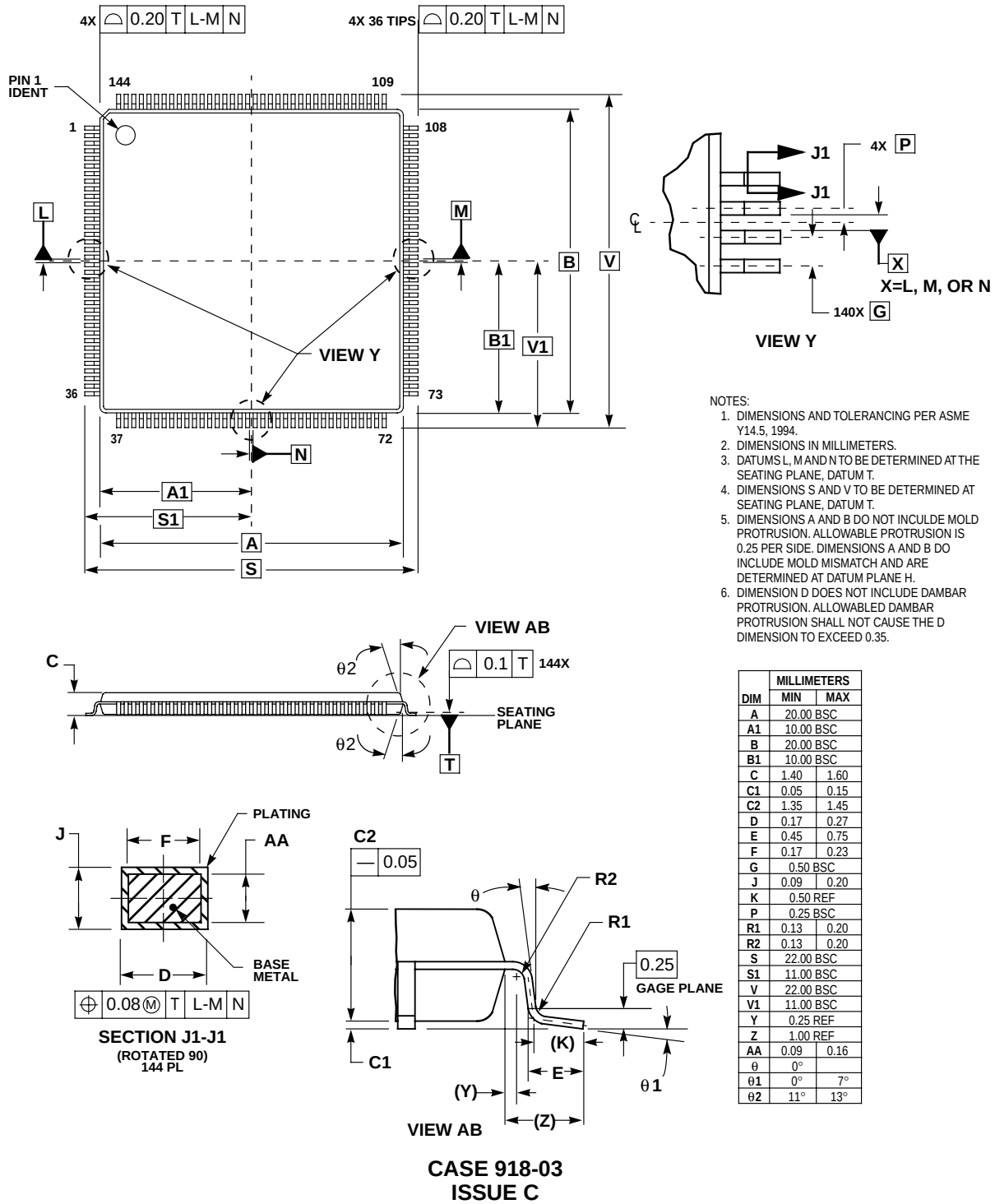
Table 3-2 DSP56309 TQFP Signal Identification by Name (Continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
H1	42	$\overline{\text{HRD}}$ / HRD	22	PB4	37
H2	41	$\overline{\text{HREQ}}$ / HREQ	24	PB5	36
H3	40	$\overline{\text{HRRQ}}$ / HRRQ	23	PB6	35
H4	37	HRW	22	PB7	34
H5	36	$\overline{\text{HTRQ}}$ / HTRQ	24	PB8	33
H6	35	$\overline{\text{HWR}}$ / HWR	21	PB9	32
H7	34	$\overline{\text{IRQA}}$	137	PC0	12
HA0	33	$\overline{\text{IRQB}}$	136	PC1	4
HA1	32	$\overline{\text{IRQC}}$	135	PC2	3
HA10	30	$\overline{\text{IRQD}}$	134	PC3	17
HA2	31	MODA	137	PC4	7
HA8	32	MODB	136	PC5	10
HA9	31	MODC	135	PCAP	46
$\overline{\text{HACK}}$ / HACK	23	MODD	134	PD0	11
HAD0	43	$\overline{\text{NMI}}$	6	PD1	144
HAD1	42	PB0	43	PD2	143
HAD2	41	PB1	42	PD3	16
HAD3	40	PB10	31	PD4	1
HAD4	37	PB11	22	PD5	2
HAD5	36	PB12	21	PE0	13
HAD6	35	PB13	30	PE1	14
HAD7	34	PB14	24	PE2	15
HAS	33	PB15	23	PINIT	6
$\overline{\text{HCS}}$ / HCS	30	PB2	41	$\overline{\text{RAS0}}$	70
$\overline{\text{HDS}}$ / HDS	21	PB3	40	$\overline{\text{RAS1}}$	69

Table 3-2 DSP56309 TQFP Signal Identification by Name (Continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
$\overline{RAS2}$	51	STD1	2	V_{CCD}	111
$\overline{RAS3}$	50	$\overline{TA}$	62	V_{CCD}	119
$\overline{RD}$	68	TCK	141	V_{CCD}	129
$\overline{RESET}$	44	TDI	140	V_{CCH}	38
RXD	13	TDO	139	V_{CCP}	45
SC00	12	TIO0	29	V_{CCQH}	20
SC01	4	TIO1	28	V_{CCQH}	49
SC02	3	TIO2	27	V_{CCQH}	95
SC10	11	TMS	142	V_{CCQL}	18
SC11	144	$\overline{TRST}$	138	V_{CCQL}	56
SC12	143	TXD	14	V_{CCQL}	91
SCK0	17	V_{CCA}	74	V_{CCQL}	126
SCK1	16	V_{CCA}	80	V_{CCS}	8
SCLK	15	V_{CCA}	86	V_{CCS}	25
SRD0	7	V_{CCC}	57	$\overline{WR}$	67
SRD1	1	V_{CCC}	65	XTAL	53
STD0	10	V_{CCD}	103		

TQFP Package Mechanical Drawing



DIM	MILLIMETERS MIN	MAX
A	20.00 BSC	
A1	10.00 BSC	
B	20.00 BSC	
B1	10.00 BSC	
C	1.40	1.60
C1	0.05	0.15
C2	1.35	1.45
D	0.17	0.27
E	0.45	0.75
F	0.17	0.23
G	0.50 BSC	
J	0.09	0.20
K	0.50 REF	
P	0.25 BSC	
R1	0.13	0.20
R2	0.13	0.20
S	22.00 BSC	
S1	11.00 BSC	
V	22.00 BSC	
V1	11.00 BSC	
Y	0.25 REF	
Z	1.00 REF	
AA	0.09	0.16
θ	0°	
θ1	0°	7°
θ2	11°	13°

Figure 3-3 DSP56309 Mechanical Information, 144-pin TQFP Package

PBGA Package Description

Top and bottom views of the PBGA package are shown in **Figure 3-4** and **Figure 3-5** with their pin-outs.

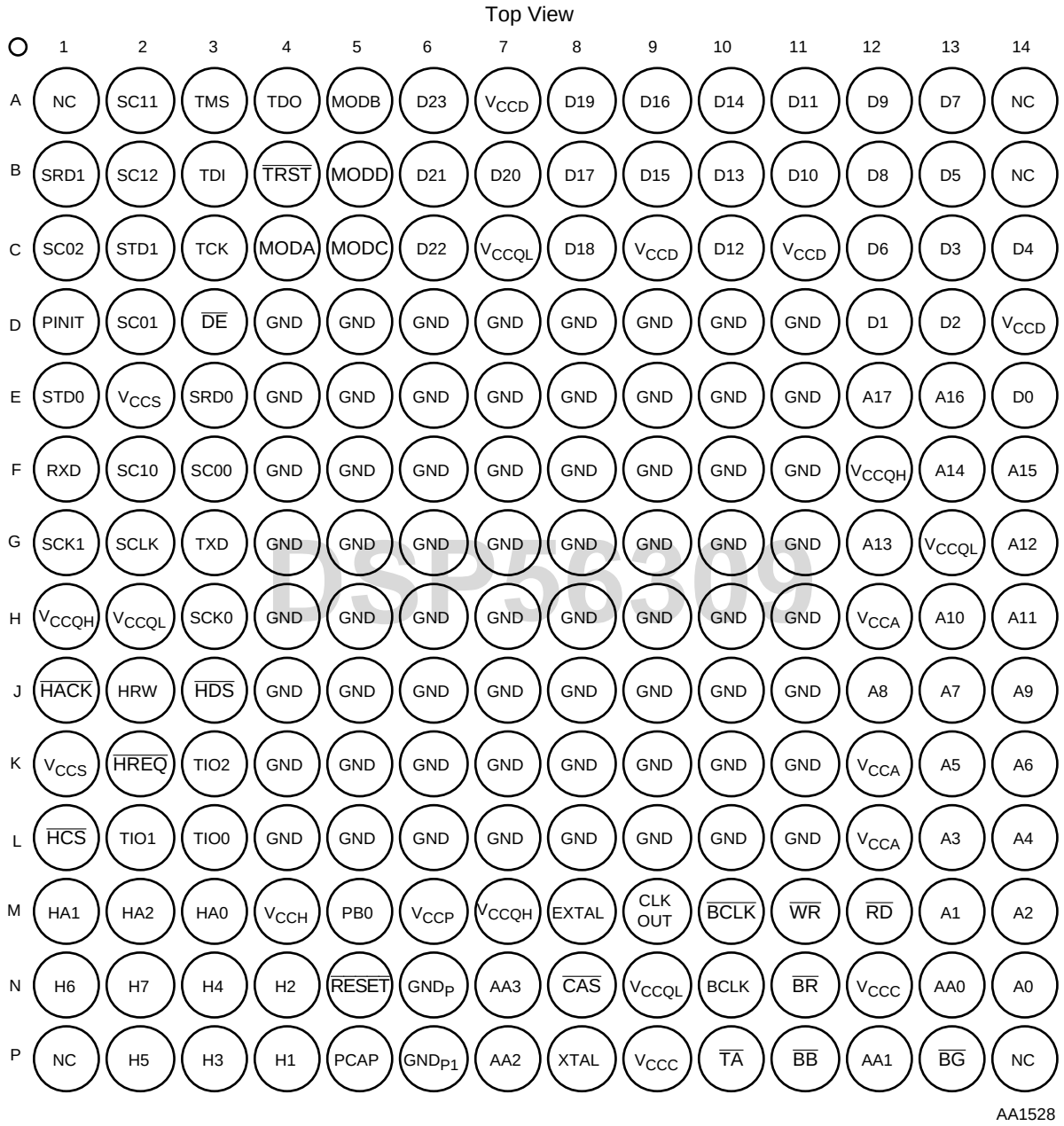


Figure 3-4 DSP56309 Plastic Ball Grid Array (PBGA), Top View

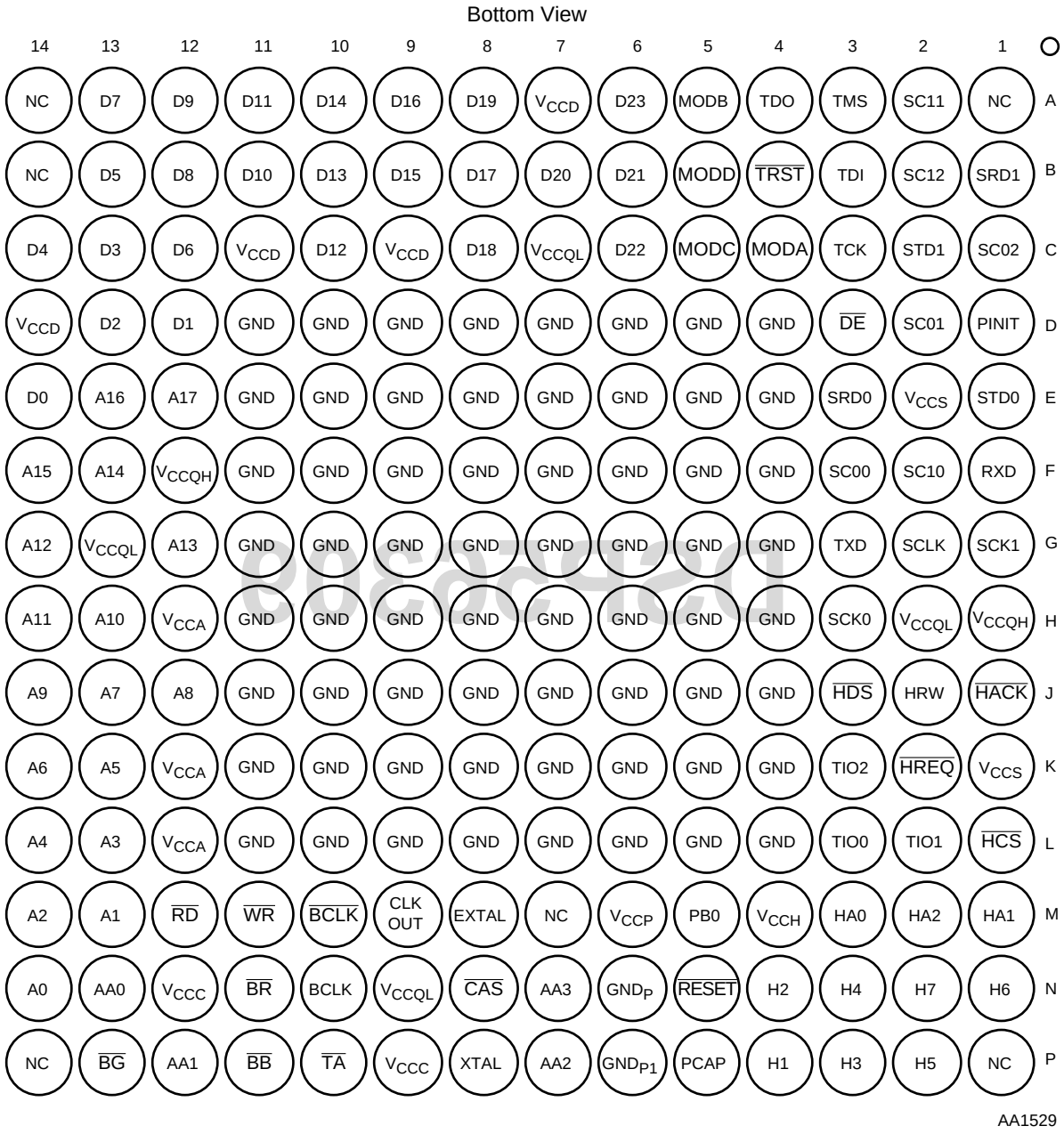


Figure 3-5 DSP56309 Plastic Ball Grid Array (PBGA), Bottom View

Table 3-3 DSP56309 PBGA Signal Identification by Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
A1	Not Connected (NC), reserved	B12	D8	D9	GND
A2	SC11 or PD1	B13	D5	D10	GND
A3	TMS	B14	NC	D11	GND
A4	TDO	C1	SC02 or PC2	D12	D1
A5	MODB / $\overline{\text{IRQB}}$	C2	STD1 or PD5	D13	D2
A6	D23	C3	TCK	D14	V_{CCD}
A7	V_{CCD}	C4	MODA / $\overline{\text{IRQA}}$	E1	STD0 or PC5
A8	D19	C5	MODC / $\overline{\text{IRQC}}$	E2	V_{CCS}
A9	D16	C6	D22	E3	SRD0 or PC4
A10	D14	C7	V_{CCQL}	E4	GND
A11	D11	C8	D18	E5	GND
A12	D9	C9	V_{CCD}	E6	GND
A13	D7	C10	D12	E7	GND
A14	NC	C11	V_{CCD}	E8	GND
B1	SRD1 or PD4	C12	D6	E9	GND
B2	SC12 or PD2	C13	D3	E10	GND
B3	TDI	C14	D4	E11	$\overline{\text{GND}}$
B4	$\overline{\text{TRST}}$	D1	PINIT / $\overline{\text{NMI}}$	E12	A17
B5	MODD / $\overline{\text{IRQD}}$	D2	SC01 or PC1	E13	A16
B6	D21	D3	$\overline{\text{DE}}$	E14	D0
B7	D20	D4	GND	F1	RXD or PE0
B8	D17	D5	GND	F2	SC10 or PD0
B9	D15	D6	GND	F3	SC00 or PC0
B10	D13	D7	GND	F4	GND
B11	D10	D8	GND	F5	GND

Table 3-3 DSP56309 PBGA Signal Identification by Pin Number (Continued)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
F6	GND	H3	SCK0 or PC3	J14	A9
F7	GND	H4	GND	K1	V_{CCS}
F8	GND	H5	GND	K2	$\overline{\text{HREQ}}$ / HREQ, $\overline{\text{HTRQ}}$ / HTRQ, or PB14
F9	GND	H6	GND	K3	TIO2
F10	GND	H7	GND	K4	GND
F11	GND	H8	GND	K5	GND
F12	V_{CCQH}	H9	GND	K6	GND
F13	A14	H10	GND	K7	GND
F14	A15	H11	GND	K8	GND
G1	SCK1 or PD3	H12	V_{CCA}	K9	GND
G2	SCLK or PE2	H13	A10	K10	GND
G3	TXD or PE1	H14	A11	K11	GND
G4	GND	J1	$\overline{\text{HACK}}$ / HACK, $\overline{\text{HRRQ}}$ / HRRQ, or PB15	K12	V_{CCA}
G5	GND	J2	HRW, $\overline{\text{HRD}}$ / HRD, or PB11	K13	A5
G6	GND	J3	$\overline{\text{HDS}}$ / HDS, $\overline{\text{HWR}}$ / HWR, or PB12	K14	A6
G7	GND	J4	GND	L1	$\overline{\text{HCS}}$ / HCS, HA10, or PB13
G8	GND	J5	GND	L2	TIO1
G9	GND	J6	GND	L3	TIO0
G10	GND	J7	GND	L4	GND
G11	GND	J8	GND	L5	GND
G12	A13	J9	GND	L6	GND
G13	V_{CCQL}	J10	GND	L7	GND
G14	A12	J11	GND	L8	GND
H1	V_{CCQH}	J12	A8	L9	GND
H2	V_{CCQL}	J13	A7	L10	GND

Table 3-3 DSP56309 PBGA Signal Identification by Pin Number (Continued)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
L11	GND	M13	A1	P1	NC
L12	V_{CCA}	M14	A2	P2	H5, HAD5, or PB5
L13	A3	N1	H6, HAD6, or PB6	P3	H3, HAD3, or PB3
L14	A4	N2	H7, HAD7, or PB7	P4	H1, HAD1, or PB1
M1	HA1, HA8, or PB9	N3	H4, HAD4, or PB4	P5	PCAP
M2	HA2, HA9, or PB10	N4	H2, HAD2, or PB2	P6	GND_{P1}
M3	HA0, $\overline{HAS}$/HAS, or PB8	N5	$\overline{RESET}$	P7	AA2/$\overline{RAS2}$
M4	V_{CCH}	N6	GND_P	P8	XTAL
M5	H0, HAD0, or PB0	N7	AA3/$\overline{RAS3}$	P9	V_{CCC}
M6	V_{CCP}	N8	$\overline{CAS}$	P10	$\overline{TA}$
M7	V_{CCQH}	N9	V_{CCQL}	P11	$\overline{BB}$
M8	EXTAL	N10	BCLK	P12	AA1/$\overline{RAS1}$
M9	CLKOUT	N11	$\overline{BR}$	P13	$\overline{BG}$
M10	$\overline{BCLK}$	N12	V_{CCC}	P14	NC
M11	$\overline{WR}$	N13	AA0/$\overline{RAS0}$		
M12	$\overline{RD}$	N14	A0		

Note: Signal names are based on configured functionality. Most connections supply a single signal. Some connections provide a signal with dual functionality, such as the MODx/$\overline{IRQx}$ pins that select an operating mode after $\overline{RESET}$ is deasserted, but act as interrupt lines during operation. Some signals have configurable polarity; these names are shown with and without overbars, such as $\overline{HAS}$/HAS. Some connections have two or more configurable functions; names assigned to these connections indicate the function for a specific configuration. For example, connection N2 is data line H7 in non-multiplexed bus mode, data/address line HAD7 in multiplexed bus mode, or GPIO line PB7 when the GPIO function is enabled for this pin. Unlike the TQFP package, most of the GND pins are connected internally in the center of the connection array and act as heat sink for the chip. Therefore, except for GND_P and GND_{P1} that support the PLL, other GND signals do not support individual subsystems in the chip.

Table 3-4 DSP56309 PBGA Signal Identification by Name

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
A0	N14	$\overline{BG}$	P13	D7	A13
A1	M13	$\overline{BR}$	N11	D8	B12
A10	H13	$\overline{CAS}$	N8	D9	A12
A11	H14	CLKOUT	M9	$\overline{DE}$	D3
A12	G14	D0	E14	EXTAL	M8
A13	G12	D1	D12	GND	D4
A14	F13	D10	B11	GND	D5
A15	F14	D11	A11	GND	D6
A16	E13	D12	C10	GND	D7
A17	E12	D13	B10	GND	D8
A2	M14	D14	A10	GND	D9
A3	L13	D15	B9	GND	D10
A4	L14	D16	A9	GND	D11
A5	K13	D17	B8	GND	E4
A6	K14	D18	C8	GND	E5
A7	J13	D19	A8	GND	E6
A8	J12	D2	D13	GND	E7
A9	J14	D20	B7	GND	E8
AA0	N13	D21	B6	GND	E9
AA1	P12	D22	C6	GND	E10
AA2	P7	D23	A6	GND	E11
AA3	N7	D3	C13	GND	F4
$\overline{BB}$	P11	D4	C14	GND	F5
$\overline{BCLK}$	M10	D5	B13	GND	F6
BCLK	N10	D6	C12	GND	F7

Table 3-4 DSP56309 PBGA Signal Identification by Name (Continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
GND	F8	GND	J9	H4	N3
GND	F9	GND	J10	H5	P2
GND	F10	GND	J11	H6	N1
GND	F11	GND	K4	H7	N2
GND	G4	GND	K5	HA0	M3
GND	G5	GND	K6	HA1	M1
GND	G6	GND	K7	HA10	L1
GND	G7	GND	K8	HA2	M2
GND	G8	GND	K9	HA8	M1
GND	G9	GND	K10	HA9	M2
GND	G10	GND	K11	$\overline{\text{HACK}}$/HACK	J1
GND	G11	GND	L4	HAD0	M5
GND	H4	GND	L5	HAD1	P4
GND	H5	GND	L6	HAD2	N4
GND	H6	GND	L7	HAD3	P3
GND	H7	GND	L8	HAD4	N3
GND	H8	GND	L9	HAD5	P2
GND	H9	GND	L10	HAD6	N1
GND	H10	GND	L11	HAD7	N2
GND	H11	GND_P	N6	$\overline{\text{HAS}}$/HAS	M3
GND	J4	GND_{P1}	P6	$\overline{\text{HCS}}$/HCS	L1
GND	J5	H0	M5	$\overline{\text{HDS}}$/HDS	J3
GND	J6	H1	P4	$\overline{\text{HRD}}$/HRD	J2
GND	J7	H2	N4	$\overline{\text{HREQ}}$/HREQ	K2
GND	J8	H3	P3	$\overline{\text{HRRQ}}$/HRRQ	J1

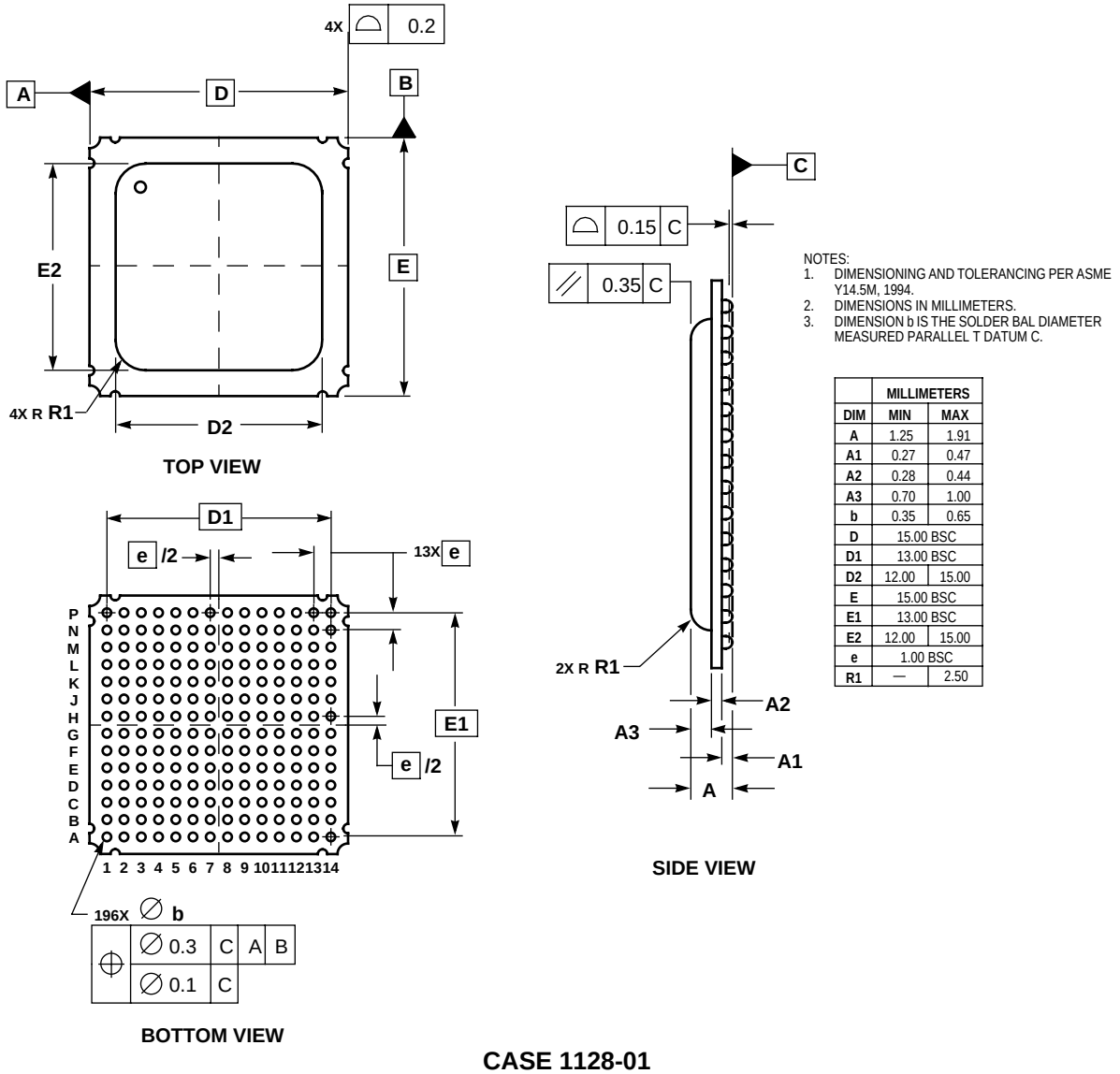
Table 3-4 DSP56309 PBGA Signal Identification by Name (Continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
HRW	J2	PB2	N4	$\overline{\text{RAS0}}$	N13
$\overline{\text{HTRQ}}$/HTRQ	K2	PB3	P3	$\overline{\text{RAS1}}$	P12
$\overline{\text{HWR}}$/HWR	J3	PB4	N3	$\overline{\text{RAS2}}$	P7
$\overline{\text{IRQA}}$	C4	PB5	P2	$\overline{\text{RAS3}}$	N7
$\overline{\text{IRQB}}$	A5	PB6	N1	$\overline{\text{RD}}$	M12
$\overline{\text{IRQC}}$	C5	PB7	N2	$\overline{\text{RESET}}$	N5
$\overline{\text{IRQD}}$	B5	PB8	M3	RXD	F1
MODA	C4	PB9	M1	SC00	F3
MODB	A5	PC0	F3	SC01	D2
MODC	C5	PC1	D2	SC02	C1
MODD	B5	PC2	C1	SC10	F2
NC	A1	PC3	H3	SC11	A2
NC	A14	PC4	E3	SC12	B2
NC	B14	PC5	E1	SCK0	H3
NC	P1	PCAP	P5	SCK1	G1
NC	P14	PD0	F2	SCLK	G2
$\overline{\text{NMI}}$	D1	PD1	A2	SRD0	E3
PB0	M5	PD2	B2	SRD1	B1
PB1	P4	PD3	G1	STD0	E1
PB10	M2	PD4	B1	STD1	C2
PB11	J2	PD5	C2	$\overline{\text{TA}}$	P10
PB12	J3	PE0	F1	TCK	C3
PB13	L1	PE1	G3	TDI	B3
PB14	K2	PE2	G2	TDO	A4
PB15	J1	PINIT	D1	TIO0	L3

Table 3-4 DSP56309 PBGA Signal Identification by Name (Continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
TIO1	L2	V_{CCC}	P9	V_{CCQH}	M7
TIO2	K3	V_{CCD}	A7	V_{CCQL}	C7
TMS	A3	V_{CCD}	C9	V_{CCQL}	G13
$\overline{TRST}$	B4	V_{CCD}	C11	V_{CCQL}	H2
TXD	G3	V_{CCD}	D14	V_{CCQL}	N9
V_{CCA}	H12	V_{CCH}	M4	V_{CCS}	E2
V_{CCA}	K12	V_{CCP}	M6	V_{CCS}	K1
V_{CCA}	L12	V_{CCQH}	F12	$\overline{WR}$	M11
V_{CCC}	N12	V_{CCQH}	H1	XTAL	P8

PBGA Package Mechanical Drawing



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION b IS THE SOLDER BAL DIAMETER MEASURED PARALLEL T DATUM C.

	MILLIMETERS	
DIM	MIN	MAX
A	1.25	1.91
A1	0.27	0.47
A2	0.28	0.44
A3	0.70	1.00
b	0.35	0.65
D	15.00 BSC	
D1	13.00 BSC	
D2	12.00	15.00
E	15.00 BSC	
E1	13.00 BSC	
E2	12.00	15.00
e	1.00 BSC	
R1	—	2.50

CASE 1128-01
ISSUE B **DATE 11/22/96**

Figure 3-6 DSP56309 Mechanical Information, 196-pin PBGA Package

ORDERING DRAWINGS

Complete mechanical information regarding DSP56309 packaging is available by facsimile through Motorola's Mfax system. Call the following number to obtain information by facsimile:

(602) 244-6609

The Mfax automated system requests the following information:

- The receiving facsimile telephone number including area code or country code
- The caller's Personal Identification Number (PIN)

  Note: For first time callers, the system provides instructions for setting up a PIN, which requires entry of a name and telephone number.

- The type of information requested:
  - Instructions for using the system
  - A literature order form
  - Specific part technical information or data sheets
  - Other information described by the system messages

A total of three documents may be ordered per call.

The DSP56309 144-pin TQFP package mechanical drawing is referenced as 918-03. The reference number for the 196-pin PBGA package is 1128-01.

SECTION 4

DESIGN CONSIDERATIONS

THERMAL DESIGN CONSIDERATIONS

An estimation of the chip junction temperature, T_J, in °C can be obtained from this equation:

Equation 1: $T_J = T_A + (P_D \times R_{\theta JA})$

Where:

T_A	=	ambient temperature ˚C
$R_{\theta JA}$	=	package junction-to-ambient thermal resistance ˚C/W
P_D	=	power dissipation in package

Historically, thermal resistance has been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

Equation 2: $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

Where:

$R_{\theta JA}$	=	package junction-to-ambient thermal resistance ˚C/W
$R_{\theta JC}$	=	package junction-to-case thermal resistance ˚C/W
$R_{\theta CA}$	=	package case-to-ambient thermal resistance ˚C/W

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board (PCB), or otherwise change the thermal dissipation capability of the area surrounding the device on a PCB. This model is most useful for ceramic packages with heat sinks; some 90% of the heat flow is dissipated through the case to the heat sink and out to the ambient environment. For ceramic packages, in situations where the heat flow is split between a path to the case and an alternate path through the PCB, analysis of the device thermal performance may need the additional modeling capability of a system level thermal simulation tool.

The thermal performance of plastic packages is more dependent on the temperature of the PCB to which the package is mounted. Again, if the estimations obtained from $R_{\theta JA}$ do not satisfactorily answer whether the thermal performance is adequate, a system level model may be appropriate.

Thermal Design Considerations

A complicating factor is the existence of three common ways for determining the junction-to-case thermal resistance in plastic packages:

- To minimize temperature variation across the surface, the thermal resistance is measured from the junction to the outside surface of the package (case) closest to the chip mounting area when that surface has a proper heat sink.
- To define a value approximately equal to a junction-to-board thermal resistance, the thermal resistance is measured from the junction to where the leads are attached to the case.
- If the temperature of the package case (T_T) is determined by a thermocouple, the thermal resistance is computed using the value obtained by the equation $(T_J - T_T) / P_D$.

As noted above, the junction-to-case thermal resistances quoted in this data sheet are determined using the first definition. From a practical standpoint, that value is also suitable for determining the junction temperature from a case thermocouple reading in forced convection environments. In natural convection, using the junction-to-case thermal resistance to estimate junction temperature from a thermocouple reading on the case of the package will estimate a junction temperature slightly hotter than actual temperature. Hence, the new thermal metric, thermal characterization parameter or Ψ_{JT}, has been defined to be $(T_J - T_T) / P_D$. This value gives a better estimate of the junction temperature in natural convection when using the surface temperature of the package. Remember that surface temperature readings of packages are subject to significant errors caused by inadequate attachment of the sensor to the surface and to errors caused by heat loss to the sensor. The recommended technique is to attach a 40-gauge thermocouple wire and bead to the top center of the package with thermally conductive epoxy.

ELECTRICAL DESIGN CONSIDERATIONS

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

Use the following list of recommendations to assure correct DSP operation:

- Provide a low-impedance path from the board power supply to each V_{CC} pin on the DSP and from the board ground to each GND pin.
- Use at least six 0.01–0.1 µF bypass capacitors positioned as close as possible to the four sides of the package to connect the V_{CC} power source to GND.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{CC} and GND pins are less than 0.5 in per capacitor lead.
- Use at least a four-layer PCB with two inner layers for V_{CC} and GND.
- Because the DSP output signals have fast rise and fall times, PCB trace lengths should be minimal. This recommendation particularly applies to the address and data buses as well as the $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{TA}}$, and $\overline{\text{BG}}$ pins. Maximum PCB trace lengths on the order of 6 inches are recommended.
- Consider all device loads and parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{CC} and GND circuits.
- All inputs must be terminated (i.e., not allowed to float) using CMOS levels, except for the three pins with internal pull-up resistors ($\overline{\text{TRST}}$, TMS, $\overline{\text{DE}}$).
- Take special care to minimize noise levels on V_{CCP}, GND_P, and GND_{P1} pins.
- The following pins must be asserted after power-up: $\overline{\text{RESET}}$ and $\overline{\text{TRST}}$.
- If multiple DSP56309 devices are on the same board, check for cross-talk or excessive spikes on the supplies due to synchronous operation of the devices.
- RESET must be asserted when the chip is powered up. A stable EXTAL signal should be supplied before deassertion of RESET.

POWER CONSUMPTION CONSIDERATIONS

Power dissipation is a key issue in portable DSP applications. Some of the factors which affect current consumption are described in this section. Most of the current consumed by CMOS devices is alternating current (ac), which is charging and discharging the capacitances of the pins and internal nodes.

Current consumption is described by this equation:

Equation 3: $I = C \times V \times f$

Where: C = node/pin capacitance
V = voltage swing
f = frequency of node/pin toggle

Example 1 Current Consumption

For a port A address pin loaded with 50 pF capacitance, operating at 3.3 V, and with a 66 MHz clock, toggling at its maximum possible rate (33 MHz), the current consumption is given by this equation:

Equation 4: $I = 50 \times 10^{-12} \times 3.3 \times 33 \times 10^{6} = 5.48 \text{ mA}$

The maximum internal current (I_{CCI}max) value reflects the typical possible switching of the internal buses on best-case operation conditions, which is not necessarily a real application case. The typical internal current (I_{CCItyp}) value reflects the average switching of the internal buses on typical operating conditions.

For applications that require very low current consumption, do the following:

- Set the EBD bit when not accessing external memory.
- Minimize external memory accesses, and use internal memory accesses.
- Minimize the number of pins that are switching.
- Minimize the capacitive load on the pins.
- Connect the unused inputs to pull-up or pull-down resistors.
- Disable unused peripherals.
- Disable unused pin activity (e.g., CLKOUT, XTAL).

One way to evaluate power consumption is to use a current per MIPS measurement methodology to minimize specific board effects (i.e., to compensate for measured board current not caused by the DSP). A benchmark power consumption test algorithm is listed in **Appendix A** of the **DSP56309 User's Manual**. Use the test algorithm, specific test current measurements, and the following equation to derive the current per MIPS value:

Equation 5: $I/MIPS = I/MHz = (I_{typF2} - I_{typF1})/(F2 - F1)$

where:
I_{typF2} = current at F2
I_{typF1} = current at F1
F2 = high frequency (any specified operating frequency)
F1 = low frequency (any specified operating frequency less than F2)

Note: F1 should be significantly less than F2. For example, F2 could be 66 MHz and F1 could be 33 MHz. The degree of difference between F1 and F2 determines the amount of precision with which the current rating can be determined for an application.

PLL PERFORMANCE ISSUES

The following explanations should be considered as general observations on expected PLL behavior. There is no testing that verifies these exact numbers. These observations were measured on a limited number of parts and were not verified over the entire temperature and voltage ranges.

Phase Skew Performance

The phase skew of the PLL is defined as the time difference between the falling edges of EXTAL and CLKOUT for a given capacitive load on CLKOUT, over the entire process, temperature, and voltage ranges. As defined in **Figure 2-2** on page 2-7, for input frequencies greater than 15 MHz and the MF ≤ 4, this skew is greater than or equal to 0.0 ns and less than 1.8 ns; otherwise, this skew is not guaranteed. However, for MF < 10 and input frequencies greater than 10 MHz, this skew is between –1.4 ns and +3.2 ns.

Phase Jitter Performance

The phase jitter of the PLL is defined as the variations in the skew between the falling edges of EXTAL and CLKOUT for a given device in specific temperature, voltage, input frequency, MF, and capacitive load on CLKOUT. These variations are a result of the PLL locking mechanism. For input frequencies greater than 15 MHz and MF ≤ 4, this jitter is less than ±0.6 ns; otherwise, this jitter is not guaranteed. However, for MF < 10 and input frequencies greater than 10 MHz, this jitter is less than ±2 ns.

Frequency Jitter Performance

The frequency jitter of the PLL is defined as the variation of the frequency of CLKOUT. For small MF (MF < 10) this jitter is smaller than 0.5%. For mid-range MF (10 < MF < 500) this jitter is between 0.5% and approximately 2%. For large MF (MF > 500), the frequency jitter is 2–3%.

Input (EXTAL) Jitter Requirements

The allowed jitter on the frequency of EXTAL is 0.5%. If the rate of change of the frequency of EXTAL is slow (i.e., it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (i.e., it does not stay at an extreme value for a long time), then the allowed jitter can be 2%. The phase and frequency jitter performance results are only valid if the input jitter is less than the prescribed values.

SECTION 5

ORDERING INFORMATION

Consult a Motorola Semiconductor sales office or authorized distributor to determine product availability and to place an order.

Table 5-1 Ordering Information

Part	Supply Voltage	Package Type	Pin Count	Frequency (MHz)	Order Number
DSP56309	3.3 V	Thin quad flat pack (TQFP)	144	80	XC56309PV80
				100	XC56309PV100
		Plastic ball grid array (PBGA)	196	80	XC56309GC80
				100	XC56309GC100

INDEX

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Denver, Colorado 80217
1 (800) 441-2447
1 (303) 675-2140

Asia/Pacific:
Motorola Semiconductors H.K. Ltd.
8B Tai Ping Industrial Park
51 Ting Kok Road
Tai Po, N.T., Hong Kong
852-26629298

Japan:
Nippon Motorola Ltd.
SPD, Strategic Planning Office, 141
4-32-1, Nishi- Gotanda
Shinagawa-ku, Tokyo, Japan
81-3-5487-8488

Mfax™:
RMFAX0@email.sps.mot.com
TOUCHTONE (602) 244-6609
USA and Canada ONLY:
1 (800) 774-1848

Technical Resource Center:
1 (800) 521-6274

DSP Helpline
dsphelp@dsp.sps.mot.com

Internet:
http://www.motorola-dsp.com