

64K	X25648/49	8K x 8 Bit
32K	X25328/29	4K x 8 Bit
16K	X25168/69	2K x 8 Bit

V_{CC} Supervisory Circuit w/Serial E²PROM

FEATURES

- Low V_{CC} Detection and Reset Assertion
 - Reset Signal Valid to V_{CC}=1V
- Save Critical Data With Block Lock™ Protection
 - Block Lock™ Protect 0, 1/4, 1/2 or all of Serial E²PROM Memory Array
- In Circuit Programmable ROM Mode
- Long Battery Life With Low Power Consumption
 - <1μA Max Standby Current
 - <5mA Max Active Current during Write
 - <400μA Max Active Current during Read
- 1.8V to 3.6V, 2.7V to 5.5V and 4.5V to 5.5V Power Supply Operation
- 2MHz Clock Rate
- Minimize Programming Time
 - 32 Byte Page Write Mode
 - Self-Timed Write Cycle
 - 5ms Write Cycle Time (Typical)
- SPI Modes (0,0 & 1,1)
- Built-in Inadvertent Write Protection
 - Power-Up/Power-Down Protection Circuitry
 - Write Enable Latch
 - Write Protect Pin
- High Reliability
- Available Packages
 - 14-Lead SOIC (X2564X)
 - 14-Lead TSSOP (X2532X, X2516X)
 - 8-Lead SOIC (X2532X, X2516X)

DESCRIPTION

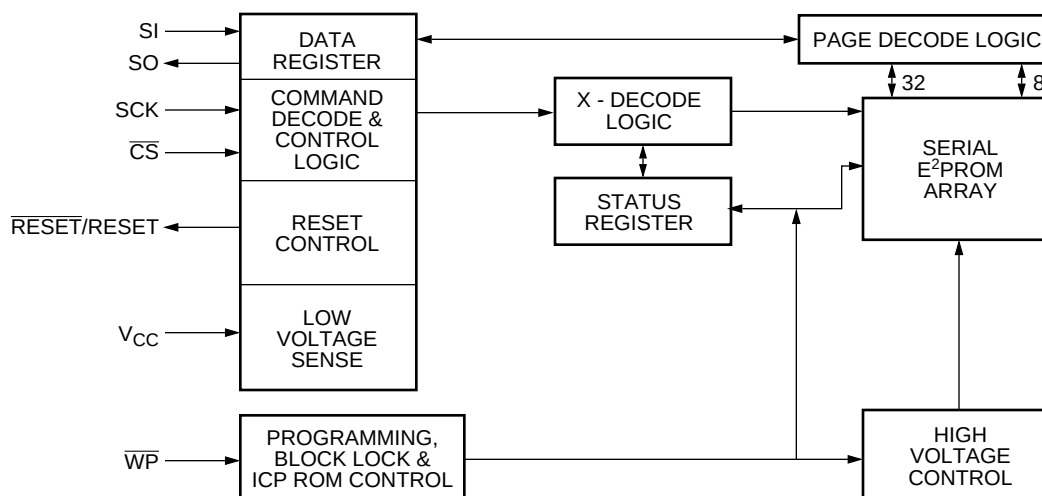
These devices combines two popular functions, Supply Voltage Supervision and Serial E²PROM Memory in one package. This combination lowers system cost, reduces board space requirements, and increases reliability.

The user's system is protected from low voltage conditions by the devices low V_{CC} detection circuitry. When V_{CC} falls below the minimum V_{CC} trip point, the system is reset. $\overline{\text{RESET}}$ /RESET is asserted until V_{CC} returns to proper operating levels and stabilizes.

The memory portion of the device is a CMOS Serial E²PROM array with Xicor's Block Lock™ Protection. The array is internally organized as x 8. The device features a Serial Peripheral Interface (SPI) and software protocol allowing operation on a simple four-wire bus.

The device utilizes Xicor's proprietary Direct Write™ cell, providing a minimum endurance of 100,000 cycles per page and a minimum data retention of 100 years.

BLOCK DIAGRAM



7036 FRM 01

X25648/49

X25328/29

X25168/69

PIN DESCRIPTIONS

Serial Output (SO)

SO is a push/pull serial data output pin. During a read cycle, data is shifted out on this pin. Data is clocked out by the falling edge of the serial clock.

Serial Input (SI)

SI is a serial data input pin. All opcodes, byte addresses, and data to be written to the memory are input on this pin. Data is latched by the rising edge of the serial clock.

Serial Clock (SCK)

The Serial Clock controls the serial bus timing for data input and output. Opcodes, addresses, or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin change after the falling edge of the clock input.

Chip Select ($\overline{CS}$)

When $\overline{CS}$ is HIGH, the device is deselected and the SO output pin is at high impedance and unless a nonvolatile write cycle is underway, the device will be in the standby power mode. $\overline{CS}$ LOW enables the device, placing it in the active power mode. It should be noted that after power-up, a HIGH to LOW transition on $\overline{CS}$ is required prior to the start of any operation.

Write Protect ($\overline{WP}$)

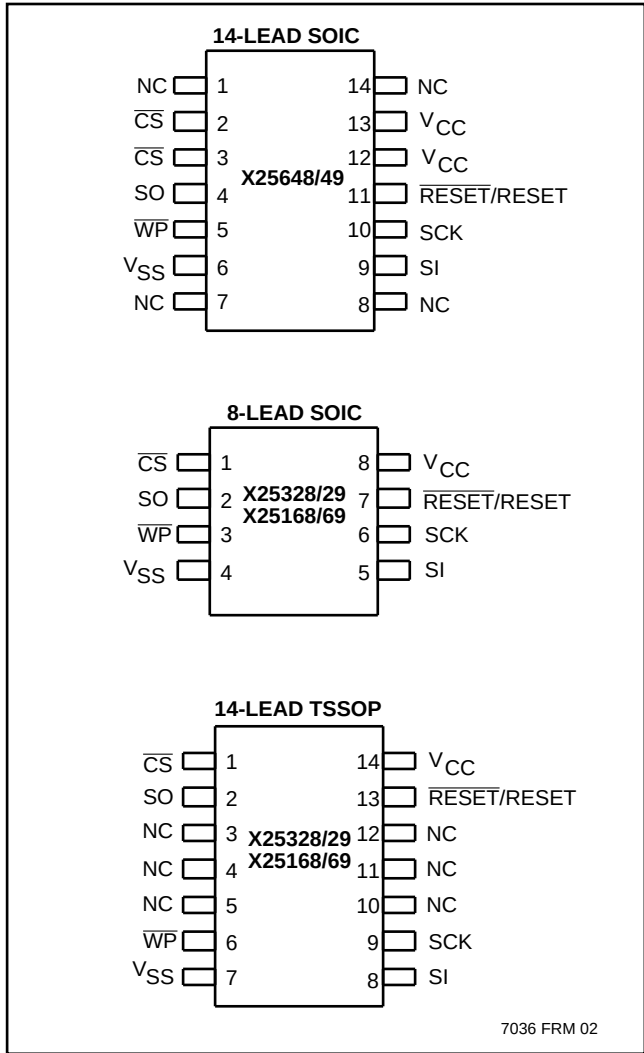
When $\overline{WP}$ is low and the nonvolatile bit WPEN is “1”, nonvolatile writes to the device Status Register are disabled, but the part otherwise functions normally. When $\overline{WP}$ is held high, all functions, including nonvolatile writes to the Status Register operate normally. If an internal Status Register Write Cycle has already been initiated, $\overline{WP}$ going low while WPEN is a “1” will have no effect on this write. Subsequent write attempts to the Status Register under these conditions will be disabled.

The $\overline{WP}$ pin function is blocked when the WPEN bit in the Status Register is “0”. This allows the user to install the device in a system with $\overline{WP}$ pin grounded and still be able to program the Status Register. The $\overline{WP}$ pin functions will be enabled when the WPEN bit is set to a “1”.

Reset ($\overline{RESET}$ /RESET)

$\overline{RESET}$ /RESET is an active LOW/HIGH, open drain output which goes active whenever Vcc falls below the minimum Vcc sense level. It will remain active until Vcc rises above the minimum Vcc sense level for 200ms.

PIN CONFIGURATION



PIN NAMES

Symbol	Description
$\overline{CS}$	Chip Select Input
SO	Serial Output
SI	Serial Input
SCK	Serial Clock Input
$\overline{WP}$	Program Protect Input
VSS	Ground
VCC	Supply Voltage
$\overline{RESET}$ /RESET	Reset Output

7036 FRM T01

PRINCIPLES OF OPERATION

The device is designed to interface directly with the synchronous Serial Peripheral Interface (SPI) of many popular microcontroller families.

The device monitors V_{CC} and asserts $\overline{RESET}/RESET$ output if the supply voltage falls below a preset minimum V_{trip} . The device contains an 8-bit instruction register. It is accessed via the SI input, with data being clocked in on the rising edge of SCK. $\overline{CS}$ must be LOW during the entire operation.

All instructions (Table 1), addresses and data are transferred MSB first. Data input on the SI line is latched on the first rising edge of SCK after $\overline{CS}$ goes LOW. Data is output on the SO line by the falling edge of SCK. SCK is static, allowing the user to stop the clock and then start it again to resume operations where left off.

Write Enable Latch

The device contains a Write Enable Latch. This latch must be SET before a Write Operation is initiated. The WREN instruction will set the latch and the WRDI instruction will reset the latch (Figure 3). This latch is automatically reset upon a power-up condition and after the completion of a valid Write Cycle.

Status Register

The RDSR instruction provides access to the Status Register. The Status Register may be read at any time, even during a Write Cycle. The Status Register is formatted as follows:

7	6	5	4	3	2	1	0
WPEN	FLB	1	1	BL1	BL0	WEL	WIP

7036 FRM T02

The Write-In-Progress (WIP) bit is a volatile, read only bit and indicates whether the device is busy with an internal nonvolatile write operation. The WIP bit is read using the RDSR instruction. When set to a "1", a nonvolatile write operation is in progress. When set to a "0", no write is in progress.

The Write Enable Latch (WEL) bit indicates the Status of the Write Enable Latch. When WEL=1, the latch is set HIGH and when WEL=0 the latch is reset LOW. The WEL bit is a volatile, read only bit. It can be set by the WREN instruction and can be reset by the WRDS instruction.

The Block Lock bits, BL0 and BL1, set the level of Block Lock™ Protection. These nonvolatile bits are programmed using the WRSR instruction and allow the user to protect one quarter, one half, all or none of the E²PROM array. Any portion of the array that is Block Lock Protected can be read but not written. It will remain protected until the BL bits are altered to disable Block Lock Protection of that portion of memory.

Status Register Bits		Array Addresses Protected		
BL1	BL0	X2564X	X2532X	X2516X
0	0	None	None	None
0	1	\$1800–\$1FFF	\$0C00–\$0FFF	\$0600–\$07FF
1	0	\$1000–\$1FFF	\$0800–\$0FFF	\$0400–\$07FF
1	1	\$0000–\$1FFF	\$0000–\$0FFF	\$0000–\$07FF

7036 FRM T03

Bits 4 and 5 of the Status Register will be read as "1's" and must be written as "1's" on all Status Register writes.

Table 1. Instruction Set

Instruction Name	Instruction Format*	Operation
WREN	0000 0110	Set the Write Enable Latch (Enable Write Operations)
SFLB	0000 0000	Set Flag Bit
WRDI/RFLB	0000 0100	Reset the Write Enable Latch/Reset Flag Bit
RSDR	0000 0101	Read Status Register
WRSR	0000 0001	Write Status Register (BlockLock, WPEN & Flag Bits)
READ	0000 0011	Read Data from Memory Array Beginning at Selected Address
WRITE	0000 0010	Write Data to Memory Array Beginning at Selected Address

*Instructions are shown MSB in leftmost position. Instructions are transferred MSB first.

7036 FRM T04

The read only FLAG bit shows the status of a volatile latch that can be set and reset by the system using the SFLB and RFLB instructions. The Flag bit is automatically reset upon power up.

The nonvolatile WPEN bit is programmed using the WRSR instruction. This bit works in conjunction with the WP pin to provide Programmable Hardware Write Protection (Table 2). When WP is LOW and the WPEN bit is programmed HIGH, all Status Register Write Operations are disabled.

In Circuit Programmable ROM Mode

This mechanism protects the Block Lock and Watchdog bits from inadvertent corruption. It may be used to perform an In Circuit Programmable ROM function by hard-wiring the WP pin to ground, writing and Block Locking the desired portion of the array to be ROM, and then programming the WPEN bit HIGH.

Read Sequence

When reading from the E²PROM memory array, CS is first pulled low to select the device. The 8-bit READ instruction is transmitted to the device, followed by the 16-bit address. After the READ opcode and address are sent, the data stored in the memory at the selected address is shifted out on the SO line. The data stored in memory at the next address can be read sequentially by continuing to provide clock pulses. The address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached, the address counter rolls over to address \$0000 allowing the read cycle to be continued indefinitely. The read operation is terminated by taking CS high. Refer to the Read E²PROM Array Sequence (Figure 1).

To read the Status Register, the CS line is first pulled low to select the device followed by the 8-bit RDSR instruction. After the RDSR opcode is sent, the contents of the Status Register are shifted out on the SO line. Refer to the Read Status Register Sequence (Figure 2).

Write Sequence

Prior to any attempt to write data into the device, the "Write Enable" Latch (WEL) must first be set by issuing the WREN instruction (Figure 3). CS is first taken LOW, then the WREN instruction is clocked into the device. After all eight bits of the instruction are transmitted, CS must then be taken HIGH. If the user continues the Write Operation without taking CS HIGH after issuing the WREN instruction, the Write Operation will be ignored.

To write data to the E²PROM memory array, the user then issues the WRITE instruction followed by the 16 bit address and then the data to be written. Any unused bits are specified to be "0's". The WRITE operation minimally takes 32 clocks. CS must go low and remain low for the duration of the operation. If the address counter reaches the end of a page and the clock continues, the counter will roll back to the first address of the page and overwrite any data that may have been previously written.

For the Page Write Operation (byte or page write) to be completed, CS can only be brought HIGH after bit 0 of the last data byte to be written is clocked in. If it is brought HIGH at any other time, the write operation will not be completed (Figure 4).

To write to the Status Register, the WRSR instruction is followed by the data to be written (Figure 5). Data bits 0 and 1 must be "0". Data bits 4 and 5 must be "1".

Table 2.

STATUS REGISTER	STATUS REGISTER	DEVICE PIN	BLOCK	BLOCK	STATUS REGISTER
WEL	WPEN	WP#	PROTECTED BLOCK	UNPROTECTED BLOCK	WPEN, BL0, BL1 BITS
0	X	X	Protected	Protected	Protected
1	1	0	Protected	Writable	Protected
1	0	X	Protected	Writable	Writable
1	X	1	Protected	Writable	Writable

7036 FRM T06

While the write is in progress following a Status Register or E²PROM Sequence, the Status Register may be read to check the WIP bit. During this time the WIP bit will be high.

$\overline{\text{RESET}}$ /RESET Operation

The $\overline{\text{RESET}}$ (X25XX8) output is designed to go LOW whenever V_{CC} has dropped below the minimum trip point, V_{trip} .

The RESET (X25XX9) output is designed to go HIGH whenever V_{CC} has dropped below the minimum trip point, V_{trip} .

The $\overline{\text{RESET}}$ /RESET output is an open drain output and requires a pull up resistor.

Operational Notes

The device powers-up in the following state:

- The device is in the low power standby state.
- A HIGH to LOW transition on $\overline{\text{CS}}$ is required to enter an active state and receive an instruction.
- SO pin is high impedance.
- The Write Enable Latch is reset.
- The Flag Bit is reset.
- Reset Signal is active for t_{PURST} .

Data Protection

The following circuitry has been included to prevent inadvertent writes:

- A WREN instruction must be issued to set the Write Enable Latch.
- $\overline{\text{CS}}$ must come HIGH at the proper clock count in order to start a nonvolatile write cycle.

Figure 1. Read E²PROM Array Sequence

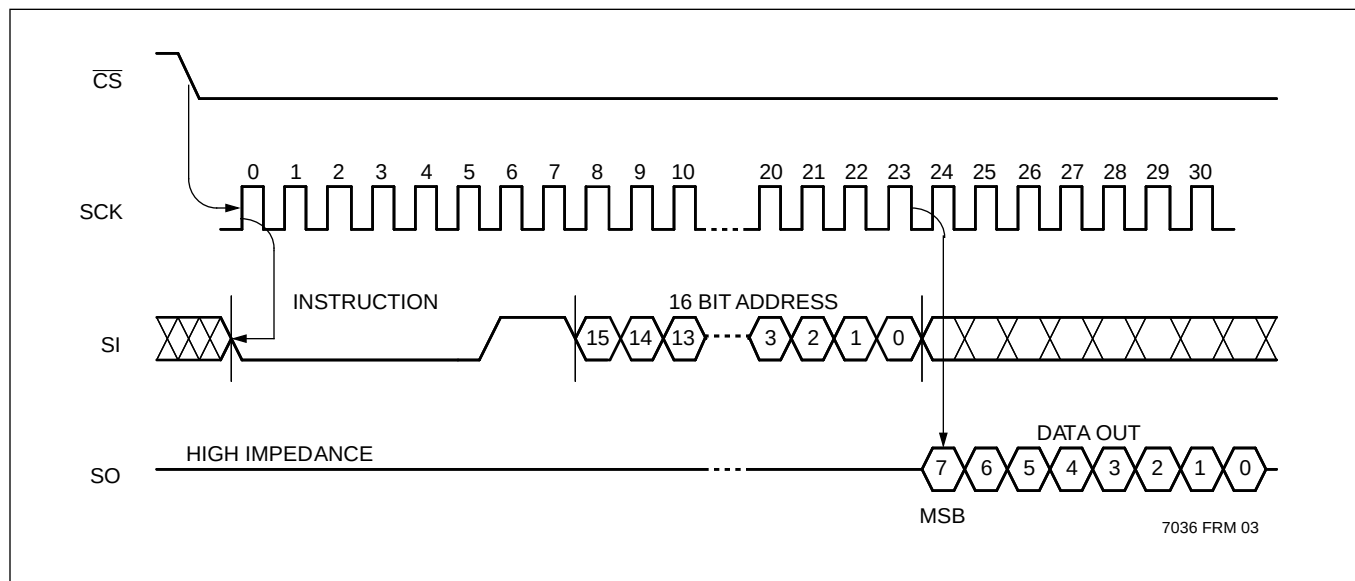


Figure 2. Read Status Register Sequence

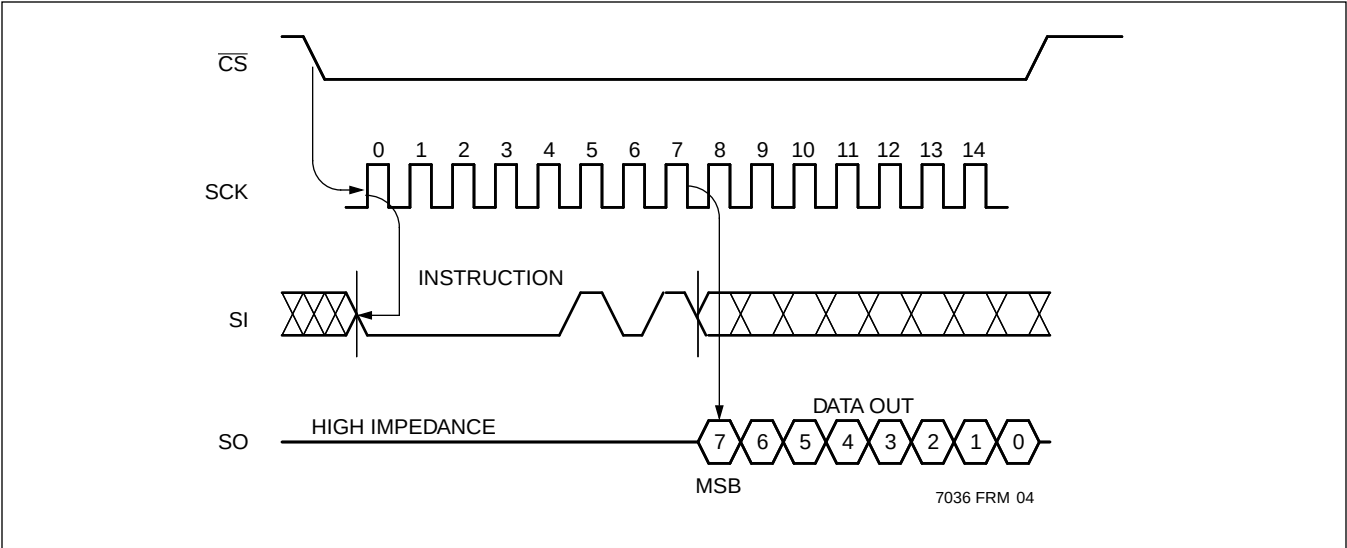


Figure 3. Write Enable Latch Sequence

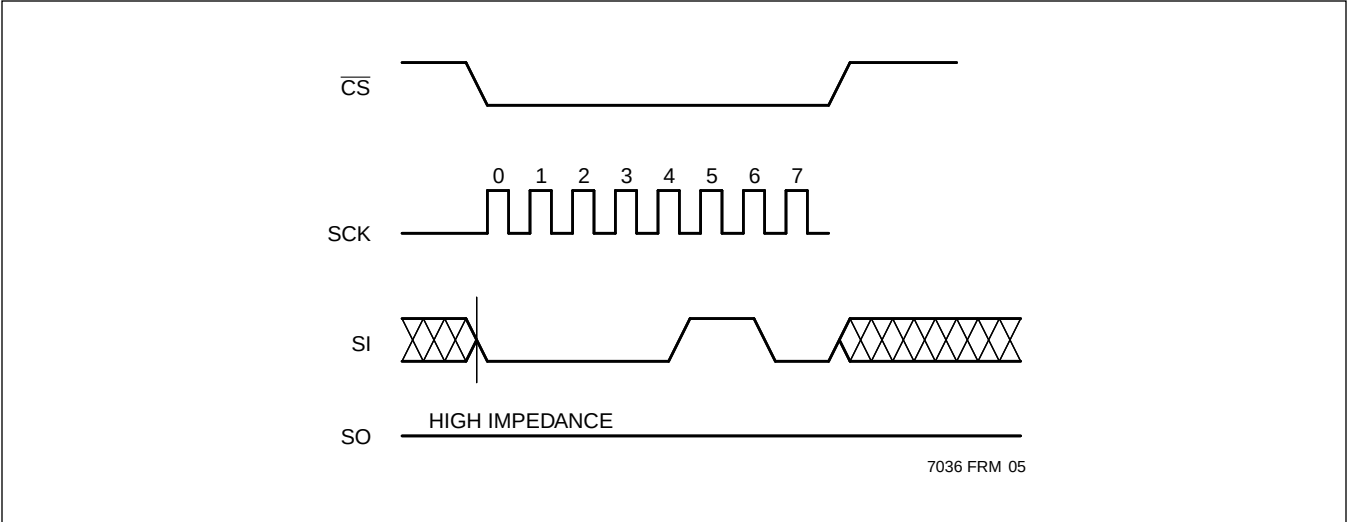


Figure 4. Write Sequence

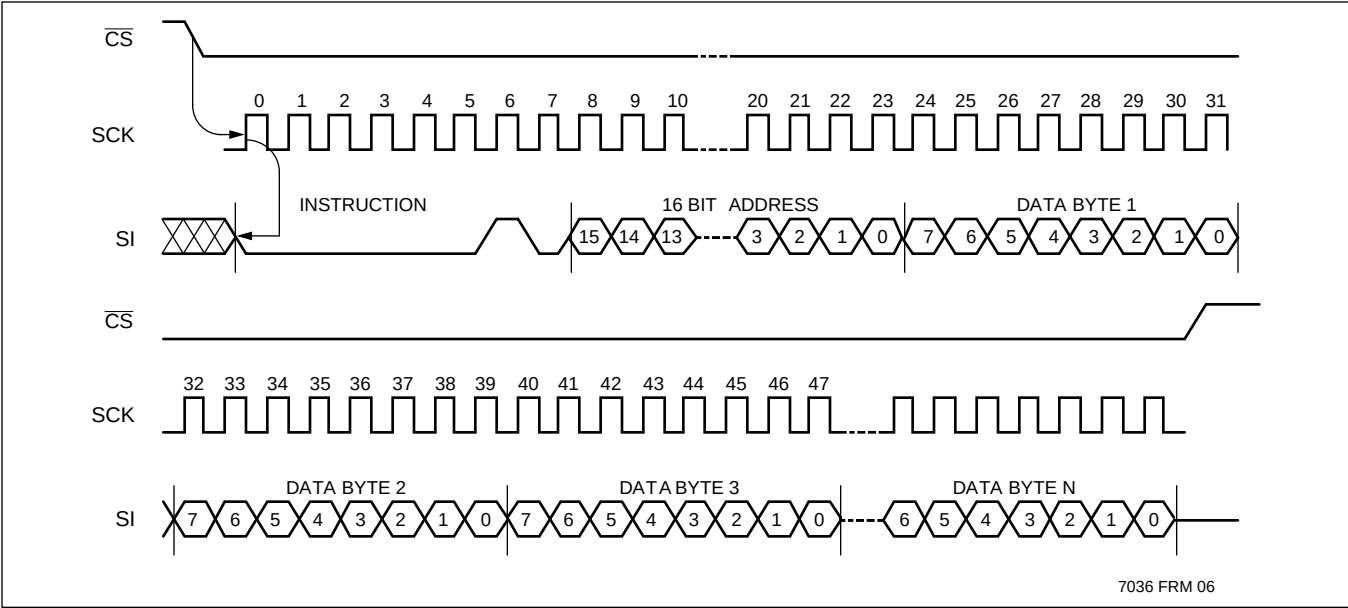
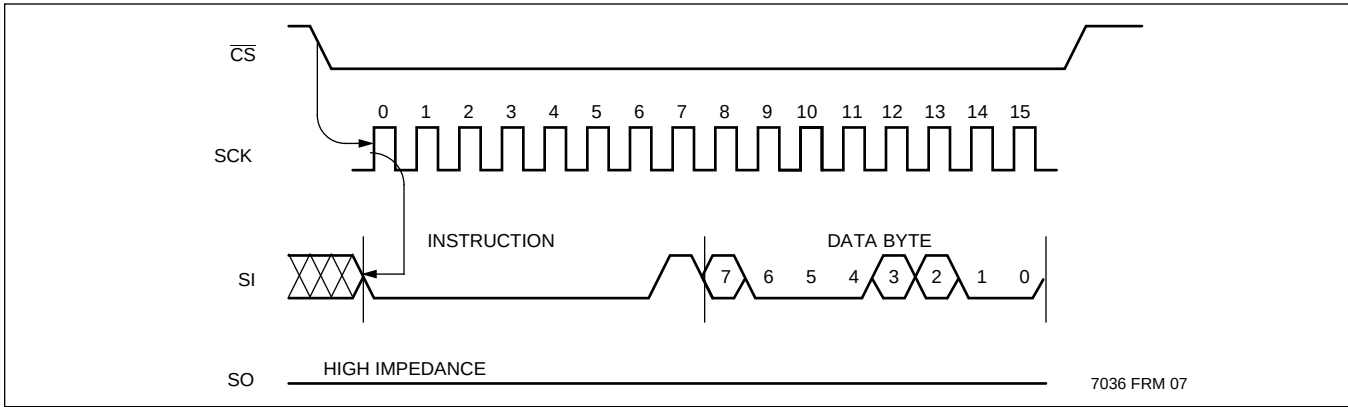


Figure 5. Status Register Write Sequence



Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

X25648/49**X25328/29****X25168/69****ABSOLUTE MAXIMUM RATINGS***

Temperature under Bias–65°C to +135°C
 Storage Temperature–65°C to +150°C
 Voltage on any Pin with Respect to V_{SS} –1.0V to +7V
 D.C. Output Current5mA
 Lead Temperature (Soldering, 10 seconds)..... 300°C

RECOMMENDED OPERATING CONDITIONS

Temp	Min.	Max.
Commercial	0°C	70°C
Industrial	–40°C	+85°C

7036 FRM T07

***COMMENT**

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Supply Voltage	Limits
X25XXX–1.8	1.8V–3.6V
X25XXX–2.7	2.7V to 5.5V
X25XXX	4.5V–5.5V

7036 FRM T08

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC1}	V_{CC} Write Current (Active)			5	mA	$SCK = V_{CC} \times 0.1/V_{CC} \times 0.9$ @ 2MHz, SO = Open
I_{CC2}	V_{CC} Read Current (Active)			0.4	mA	$SCK = V_{CC} \times 0.1/V_{CC} \times 0.9$ @ 2MHz, SO = Open
I_{SB1}	V_{CC} Standby Current WDT=OFF			1	μA	$\overline{CS} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC} , $V_{CC} = 5.5V$
I_{SB2}	V_{CC} Standby Current WDT=ON			50	μA	$\overline{CS} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC} , $V_{CC} = 5.5V$
I_{SB3}	V_{CC} Standby Current WDT=ON			20	μA	$\overline{CS} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC} , $V_{CC} = 3.6V$
I_{LI}	Input Leakage Current		0.1	10	μA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output Leakage Current		0.1	10	μA	$V_{OUT} = V_{SS}$ to V_{CC}
$V_{IL}^{(1)}$	Input LOW Voltage	–0.5		$V_{CC} \times 0.3$	V	
$V_{IH}^{(1)}$	Input HIGH Voltage	$V_{CC} \times 0.7$		$V_{CC} + 0.5$	V	
V_{OL1}	Output LOW Voltage			0.4	V	$V_{CC} > 3.3V$, $I_{OL} = 2.1mA$
V_{OL2}	Output LOW Voltage			0.4	V	$2V < V_{CC} \leq 3.3V$, $I_{OL} = 1mA$
V_{OL3}	Output LOW Voltage			0.4	V	$V_{CC} \leq 2V$, $I_{OL} = 0.5mA$
V_{OH1}	Output HIGH Voltage	$V_{CC} - 0.8$			V	$V_{CC} > 3.3V$, $I_{OH} = -1.0mA$
V_{OH2}	Output HIGH Voltage	$V_{CC} - 0.4$			V	$2V < V_{CC} \leq 3.3V$, $I_{OH} = -0.4mA$
V_{OH3}	Output HIGH Voltage	$V_{CC} - 0.2$			V	$V_{CC} \leq 2V$, $I_{OH} = -0.25mA$
V_{OLRS}	Reset Output LOW Voltage			0.4	V	$I_{OL} = 1mA$

7036 FRM T09

POWER-UP TIMING

Symbol	Parameter	Min.	Max.	Units
$t_{PUR}^{(2)}$	Power-up to Read Operation		1	ms
$t_{PUW}^{(2)}$	Power-up to Write Operation		5	ms

7036 FRM T10

CAPACITANCE $T_A = +25^\circ C$, $f = 1MHz$, $V_{CC} = 5V$.

Symbol	Test	Max.	Units	Conditions
$C_{OUT}^{(2)}$	Output Capacitance (SO, $\overline{RESET}$, RESET)	8	pF	$V_{OUT} = 0V$
$C_{IN}^{(2)}$	Input Capacitance (SCK, SI, $\overline{CS}$, WP)	6	pF	$V_{IN} = 0V$

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

7036 FRM T11

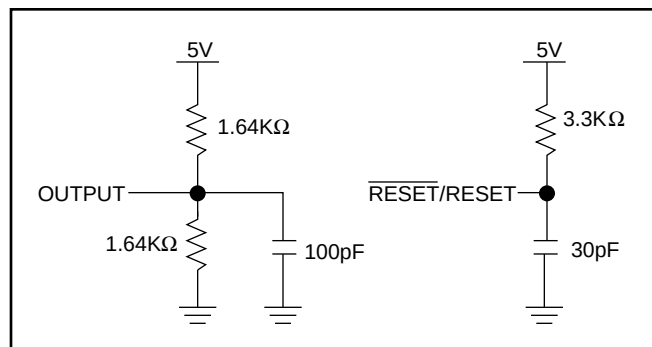
(2) This parameter is periodically sampled and not 100% tested.

X25648/49

X25328/29

X25168/69

EQUIVALENT A.C. LOAD CIRCUIT AT 5V V_{CC}



A.C. TEST CONDITIONS

Input Pulse Levels	$V_{CC} \times 0.1$ to $V_{CC} \times 0.9$
Input Rise and Fall Times	10ns
Input and Output Timing Level	$V_{CC} \times 0.5$

7036 FRM T12

A.C. CHARACTERISTICS (Over recommended operating conditions, unless otherwise specified)

Data Input Timing

Symbol	Parameter	Voltage Range	Min.	Max.	Units
f_{SCK}	Clock Frequency	2.7V–5.5V 1.8V–3.6V	0	2 1	MHz
t_{CYC}	Cycle Time	2.7V–5.5V 1.8V–3.6V	500 1000		ns
t_{LEAD}	$\overline{CS}$ Lead Time	2.7V–5.5V 1.8V–3.6V	250 500		ns
t_{LAG}	$\overline{CS}$ Lag Time	2.7V–5.5V 1.8V–3.6V	250 500		ns
t_{WH}	Clock HIGH Time	2.7V–5.5V 1.8V–3.6V	200 400		ns
t_{WL}	Clock LOW Time	2.7V–5.5V 1.8V–3.6V	200 400		ns
t_{SU}	Data Setup Time	2.7V–5.5V 1.8V–3.6V	50		ns
t_H	Data Hold Time	2.7V–5.5V 1.8V–3.6V	50		ns
$t_{RI}^{(3)}$	Input Rise Time	2.7V–5.5V 1.8V–3.6V		100	ns
$t_{FI}^{(3)}$	Input Fall Time	2.7V–5.5V 1.8V–3.6V		100	ns
t_{CS}	$\overline{CS}$ Deselect Time	2.7V–5.5V 1.8V–3.6V	500		ns
$t_{WC}^{(4)}$	Write Cycle Time	2.7V–5.5V 1.8V–3.6V		10	ms

7036 FRM T13

Data Output Timing

Symbol	Parameter	Part Number	Min.	Max.	Units
f_{SCK}	Clock Frequency	2.7V–5.5V 1.8V–3.6V	0	2 1	MHz
t_{DIS}	Output Disable Time	2.7V–5.5V 1.8V–3.6V		250	ns
t_{V}	Output Valid from Clock Low	2.7V–5.5V 1.8V–3.6V		250 400	ns
t_{HO}	Output Hold Time	2.7V–5.5V 1.8V–3.6V	0		ns
$t_{\text{RO}}^{(3)}$	Output Rise Time	2.7V–5.5V 1.8V–3.6V		100	ns
$t_{\text{FO}}^{(3)}$	Output Fall Time	2.7V–5.5V 1.8V–3.6V		100	ns

7036 FRM T14

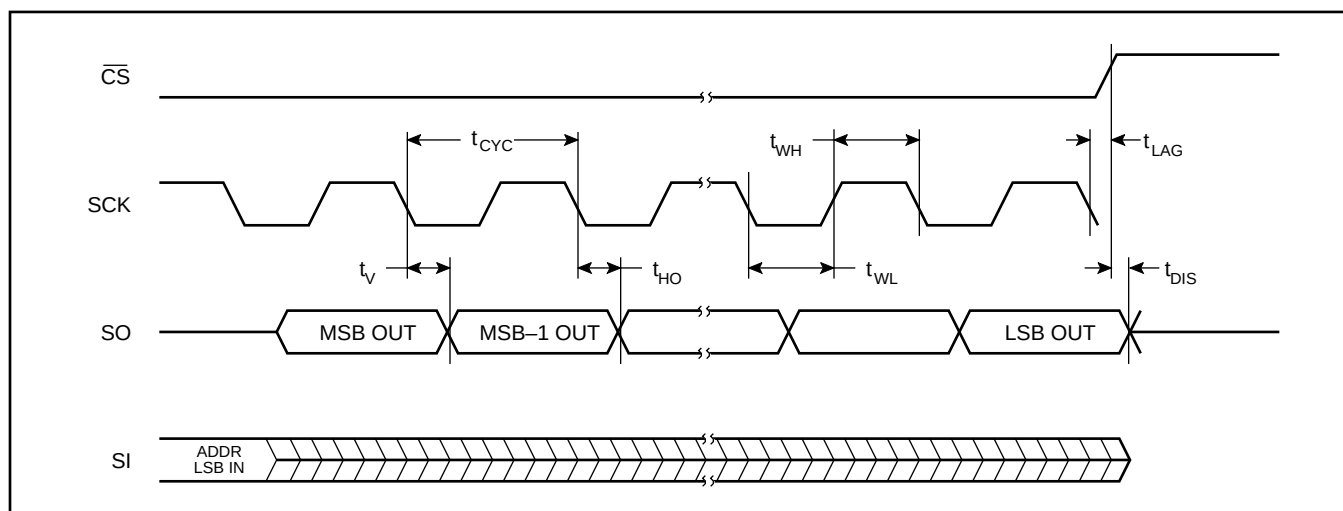
Notes: (3) This parameter is periodically sampled and not 100% tested.
 (4) t_{WC} is the time from the rising edge of CS after a valid write sequence has been sent to the end of the self-timed internal nonvolatile write cycle.

X25648/49

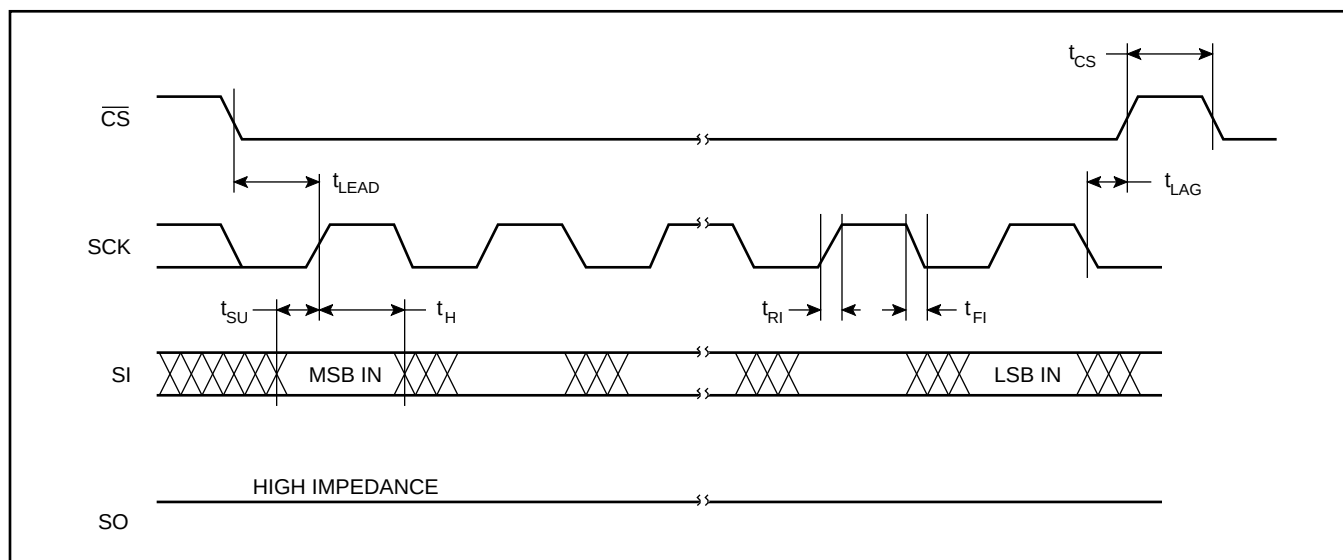
X25328/29

X25168/69

Serial Output Timing



Serial Input Timing

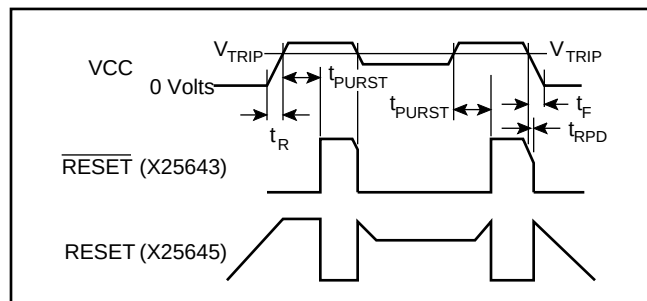


X25648/49

X25328/29

X25168/69

Power-Up and Power-Down Timing



RESET Output Timing

Symbol	Parameter	Min.	Typ.	Max.	Units
V _{TRIP}	Reset Trip Point Voltage, 5V Device	4.25		4.5	V
	Reset Trip Point Voltage, 2.7V Device	2.55		2.7	V
	Reset Trip Point Voltage, 1.8V Device	1.7		1.8	V
t _{PURST}	Power-up Reset Timeout	100	200	280	ms
t _{RPD} ⁽⁵⁾	V _{CC} Detect to Reset/Output			500	ns
t _F ⁽⁵⁾	V _{CC} Fall Time	0.1			ns
t _R ⁽⁵⁾	V _{CC} Rise Time	0.1			ns
V _{RVALID}	Reset Valid V _{CC}	1			V

7036 FRM T15

Notes: (5) This parameter is periodically sampled and not 100% tested.

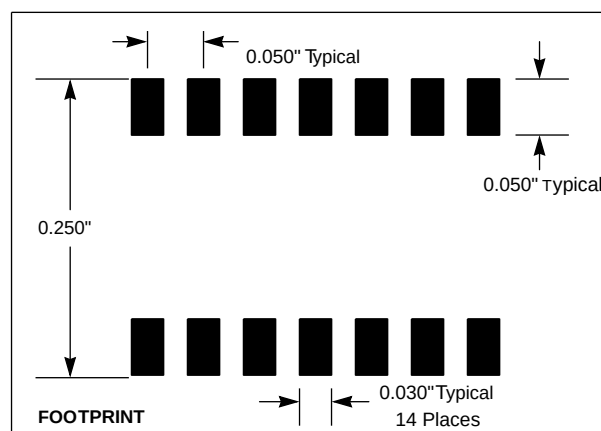
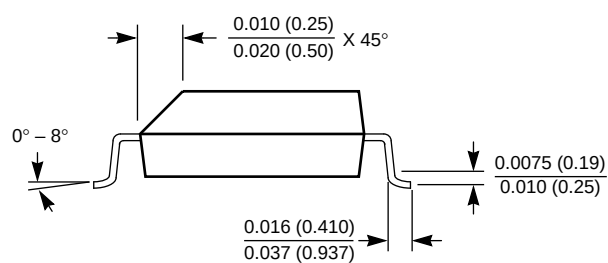
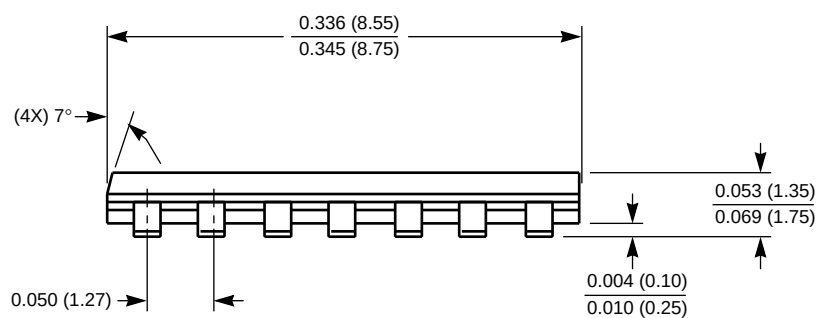
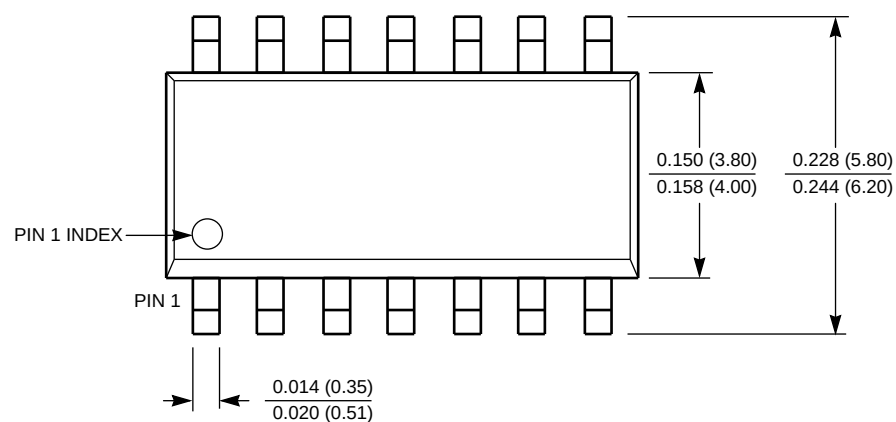
X25648/49

X25328/29

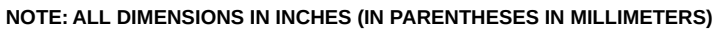
X25168/69

PACKAGING INFORMATION

14-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

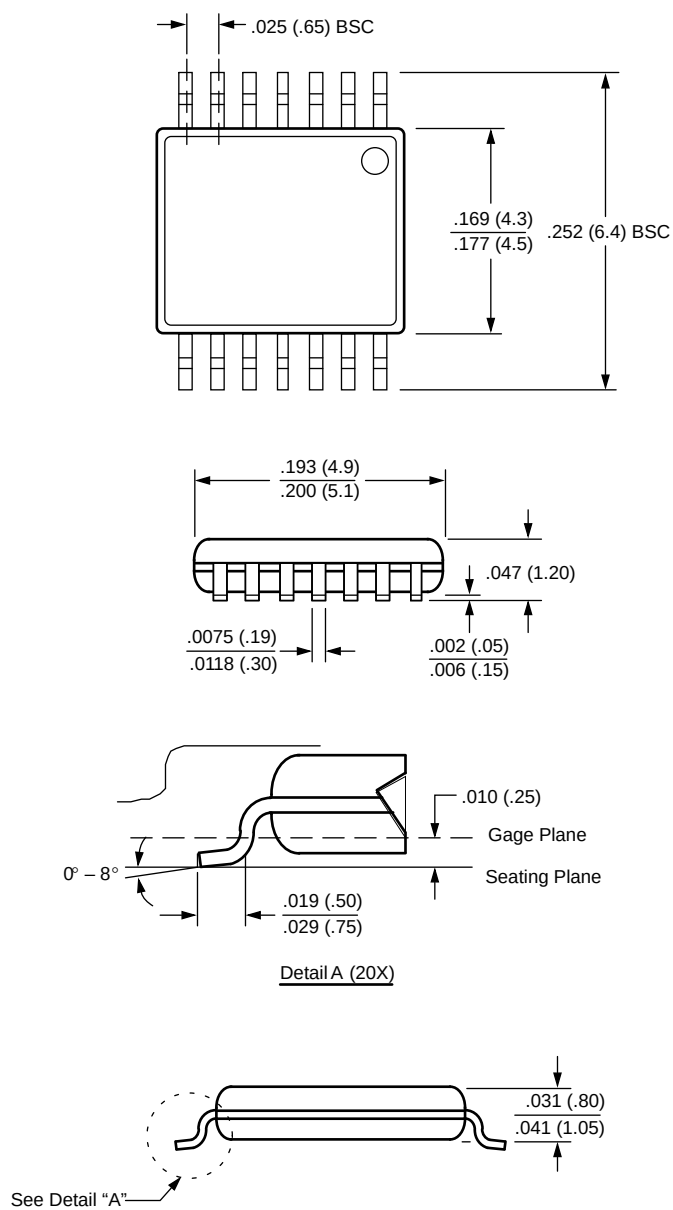


X25648/49

X25328/29

X25168/69

14-LEAD PLASTIC, TSSOP, PACKAGE TYPE V



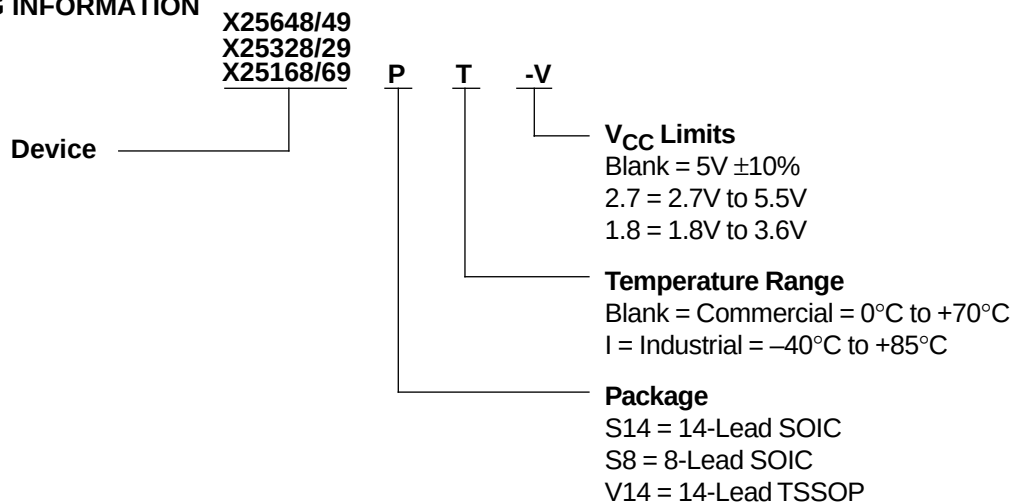
NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

X25648/49

X25328/29

X25168/69

ORDERING INFORMATION



Part Mark Convention

X25648/49 **X** — Blank = 14-Lead SOIC

X —
Blank = 5V ±10%, 0°C to +70°C
I = 5V ±10%, -40°C to +85°C
F = 2.7V to 5.5V, 0°C to +70°C
G = 2.7V to 5.5V, -40°C to +85°C
AG = 1.8V to 3.6V, 0°C to +70°C

X25328/29 **X** — Blank = 8-Lead SOIC
X25168/69 **V** = 14 Lead TSSOP

X —
Blank = 5V ±10%, 0°C to +70°C
I = 5V ±10%, -40°C to +85°C
F = 2.7V to 5.5V, 0°C to +70°C
G = 2.7V to 5.5V, -40°C to +85°C
AG = 1.8V to 3.6V, 0°C to +70°C

LIMITED WARRANTY

Devices sold by Xicor, Inc. are covered by the warranty and patent indemnification provisions appearing in its Terms of Sale only. Xicor, Inc. makes no warranty, express, statutory, implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. Xicor, Inc. makes no warranty of merchantability or fitness for any purpose. Xicor, Inc. reserves the right to discontinue production and change specifications and prices at any time and without notice.

Xicor, Inc. assumes no responsibility for the use of any circuitry other than circuitry embodied in a Xicor, Inc. product. No other circuits, patents, licenses are implied.

U.S. PATENTS

Xicor products are covered by one or more of the following U.S. Patents: 4,263,664; 4,274,012; 4,300,212; 4,314,265; 4,326,134; 4,393,481; 4,404,475; 4,450,402; 4,486,769; 4,488,060; 4,520,461; 4,533,846; 4,599,706; 4,617,652; 4,668,932; 4,752,912; 4,829, 482; 4,874, 967; 4,883, 976. Foreign patents and additional patents pending.

LIFE RELATED POLICY

In situations where semiconductor component failure may endanger life, system designers using this product should design the system with appropriate error detection and correction, redundancy and back-up features to prevent such an occurrence.

Xicor's products are not authorized for use in critical components in life support devices or systems.

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

X25648/49

X25328/29

X25168/69

NOTES

X25648/49

X25328/29

X25168/69

NOTES

X25648/49

X25328/29

X25168/69

NOTES

X25648/49 X25328/29 X25168/69

U.S. SALES OFFICES

Corporate Office

Xicor Inc.
1511 Buckeye Drive
Milpitas, CA 95035
Phone: 408/432-8888
Fax: 408/432-0640
E-mail: info@smtpgate.xicor.com

Northeast Region

Xicor Inc.
1344 Main Street
Waltham, MA 02154
Phone: 617/899-5510
Fax: 617/899-6808
E-mail: xicor-ne@smtpgate.xicor.com

Southeast Region

Xicor Inc.
100 E. Sybelia Ave.
Suite 355
Maitland, FL 32751
Phone: 407/740-8282
Fax: 407/740-8602
E-mail: xicor-se@smtpgate.xicor.com

Mid-Atlantic Region

Xicor Inc.
50 North Street
Danbury, CT 06810
Phone: 203/743-1701
Fax: 203/794-9501
E-mail: xicor-ma@smtpgate.xicor.com

North Central Region

Xicor Inc.
810 South Bartlett Road
Suite 103
Streamwood, IL 60107
Phone: 630/372-3200
Fax: 630/372-3210
E-mail: xicor-nc@smtpgate.xicor.com

South Central Region

Xicor Inc.
11884 Greenville Ave.
Suite 102
Dallas, TX 75243
Phone: 972/669-2022
Fax: 972/644-5835
E-mail: xicor-sc@smtpgate.xicor.com

Southwest Region

Xicor Inc.
4100 Newport Place Drive
Suite 710
Newport Beach, CA 92660
Phone: 714/752-8700
Fax: 714/752-8634
E-mail: xicor-sw@smtpgate.xicor.com

Northwest Region

Xicor Inc.
3333 Bowers Ave.
Suite 238
Santa Clara, CA 95054
Phone: 408/492-1966
Fax: 408/980-9478
E-mail: xicor-nw@smtpgate.xicor.com

INTERNATIONAL SALES OFFICES

EUROPE

Northern Europe

Xicor Ltd.
Grant Thornton House
Witan Way
Witney
Oxford OX8 6FE
UK
Phone: (44) 1933.700544
Fax: (44) 1933.700533
E-mail: xicor-uk@smtpgate.xicor.com

Central Europe

Xicor GmbH
Technopark Neukeferloh
Bretonischer Ring 15
85630 Grasbrunn bei Muenchen
Germany
Phone: (49) 8946.10080
Fax: (49) 8946.05472
E-mail: xicor-gm@smtpgate.xicor.com

ASIA/PACIFIC

Japan

Xicor Japan K.K.
Suzuki Building, 4th Floor
1-6-8 Shinjuku, Shinjuku-ku
Tokyo 160, Japan
Phone: (81) 3322.52004
Fax: (81) 3322.52319
E-mail: xicor-jp@smtpgate.xicor.com

Mainland China

Taiwan/Hong Kong

Xicor Inc.
4100 Newport Place Drive
Suite 710
Newport Beach, CA 92660
Phone: 714/752-8700
Fax: 714/752-8634
E-mail: xicor-sw@smtpgate.xicor.com

Singapore/Malaysia/India

Xicor Inc.
3333 Bowers Ave.
Suite 238
Santa Clara, CA 95054
Phone: 408/492-1966
Fax: 408/980-9478
E-mail: xicor-nw@smtpgate.xicor.com

Korea

Xicor Korea, Ltd.
27th Fl., Korea World Trade Ctr.
159, Samsung-dong
Kangnam Ku
Seoul 135-729
Korea
Phone: (82) 2.551.2750
Fax: (82) 2.551.2710
E-mail: xicor-ka@smtpgate.xicor.com

() = Country Code

Xicor product information is available at:

<http://www.xicor.com>