Quad DMOS Analog Switch Driver

"Improved Performance Over SD5000N and SD5400CY"

SD5300

FEATURES

- **Low Propagation Time 1ns**
- **Low On Resistance**
- **Low Insertion Loss**
- **Low Capacitance**
  - **Input (Gate). . . . . 3.6pF typ.**
  - **Output. . . . . 1.6pF typ.**
  - **Feedback . . . . . .6pF typ.**
- **Low Crosstalk . . . . . -107dB @ 4kHz**
- **Input Transient Protection**

APPLICATION

- **Analog Switch Driver**
- **Wide Band Dual Differential Amplifiers**

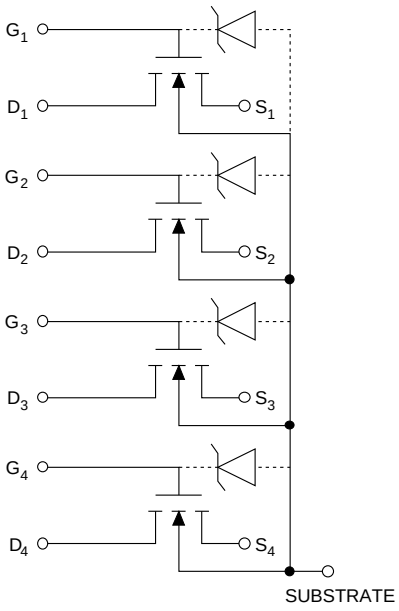
DESCRIPTION

The Calogic SD5300 is a monolithic array of 20V enhancement-mode DMOS FET analog switch drivers. The SD5300 is manufactured with implanted high-speed, high-voltage and low resistance double-diffused MOS (DMOS) process, and was designed to drive DMOS and other analog switches. The devices are available in 16-pin plastic DIP package and in a die form for hybrid applications. Custom devices based on SD5300 can also be ordered.

ORDERING INFORMATION

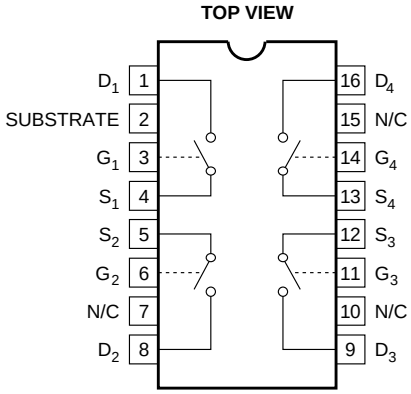
Part	Package	Temperature Range
SD5300Y	SOIC	-55°C to +125°C
SD5300N	Plastic DIP	-55°C to +125°C
XSD5300	Sorted Chips in Carriers	-55°C to +125°C

FUNCTIONAL BLOCK DIAGRAM

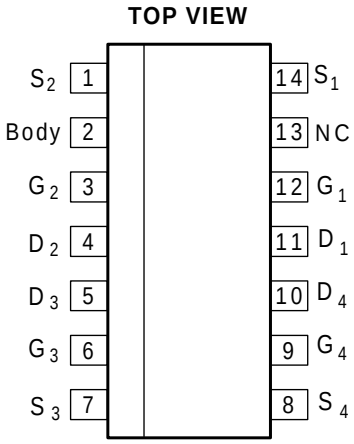


CD9

DUAL IN LINE PACKAGE PIN CONFIGURATION



SO PIN CONFIGURATION



calogic CORPORATION

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MAX. VALUE	UNITS
Breakdown Voltage			
Drain-Source	V_{DS}	20	V
Source-Drain	V_{SD}	20	
Drain-Substrate	V_{DB}	25	
Source-Substrate	V_{SB}	25	
Gate-Source	V_{GS}	25	
Gate-Substrate	V_{GB}	25/-.3	
Gate-Drain	V_{GD}	25	
Continuous Drain Current	I_D	50	mA

ABSOLUTE MAXIMUM

PARAMETER	SYMBOL	MAX. VALUE	UNITS
Drain Current	I_D	50	mA
Temperature Range			
Operating	T_J	-55 to +85	^oC
Storage	T_S	-55 to +150	
Power Dissipation			
Package	P_D	640 (Note 1)	mW
Each Device	P_D	300 (Note 2)	

Notes:
1. Linear Derating Factor – 10.7mW/^{o}C above 25^{o}C
2. Linear Derating Factor – 5.0mW/^{o}C above 25^{o}C

ELECTRICAL CHARACTERISTICS (T_A = 25^{o}C, unless otherwise noted)

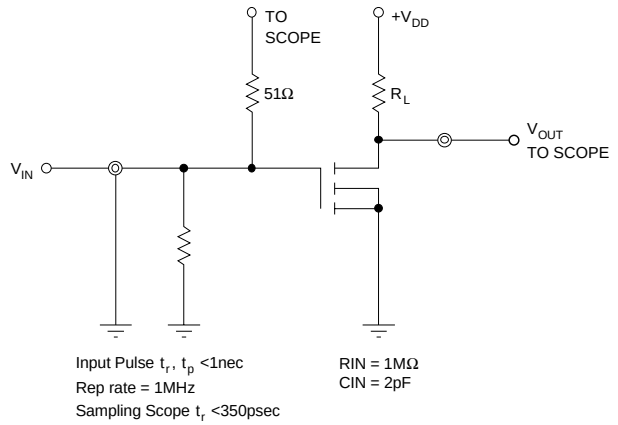
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
BV_{DS}	Drain-Source Breakdown Voltage	20	25		V	I_D = 10µA, V_{GS} = V_{BS} = 0
BV_{SB}	Source-Substrate Breakdown Voltage	20	25			I_S = 10µA, V_{GS} = 0, Drain Open
I_{GBS}	Gate-Body Leakage Current			1.0	µA	V_{GB} = 25V, V_{DB} = V_{SB} = 0
$V_{GS(th)}$	Gate-Source Threshold Voltage	0.5		2.0	V	V_{DS} = V_{GS}, I_D = 1.0µA, V_{SB} = 0
$r_{DS(on)}$	Drain-Source ON Resistance		40	45	ohms	V_{GS} = 5V, I_D = 1mA, V_{SB} = 0
			22	25		V_{GS} = 10V, I_D = 1mA, V_{SB} = 0
			17	20		V_{GS} = 15V, I_D = 1mA, V_{SB} = 0
			15	17		V_{GS} = 20V, I_D = 1mA, V_{SB} = 0
g_{fs}	Common-Source Forward Transconductance	10	12		mmhos	V_{DS} = 10V, I_D = 20mA, f = 1KHz, V_{SB} = 0
$c_{(ga+gd+gb)}$	Gate Node Capacitance		2.4	3.7	pF	f = 1MHz, V_{DS} = 10V, V_{GS} = V_{BS} = -15V
$c_{(gd+db)}$	Drain Node Capacitance		1.3	1.7		
$c_{(gs+sb)}$	Source Node Capacitance		3.5	4.5		
$c_{(dg)}$	Reverse Transfer Capacitance		0.3	.7		
C_T	Cross Talk		-107		dB	

SWITCHING CHARACTERISTICS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
$t_{d(on)}$	Turn-on Time		0.7	1.5	ns	R_L = 680Ω, R_G = 51
t_r	Rise Time		0.8	1.5		V_{DD} = 5V
t_{off} *	Turn-off Time		10.0			$V_{G(on)}$ = 10V

* t_{off} is dependent on R_L and C and does not depend on the device characteristics.

TEST CIRCUIT



SWITCHING WAVEFORM