XPressArray *0.18µ Hybrid Gate Array*

1.0 Key Features

- Next-generation 0.18µ hybrid gate array
- Platform for high-performance 1.8V ASICs and FPGA-to-ASIC conversions
- NRE and production cost savings
- Significant time-to-market advantages
- Drop-in replacement for cost-reducing Xilinx Virtex-E and Altera APEX-E designs
- 47K to 2.6M ASIC gates, 240K to 11M FPGA system gates
- 250MHz system, 350MHz local clock speeds
- Low power consumption (0.020µW/MHz/gate)
- 23Kbits to 1.4Mbits of embedded configurable memory
- Single-port/dual-port, RAM/CAM, initializable
- Flexible I/O technology
- Configurable signal, core and I/O power supply pad locations
- Supports LVTTL, LVCMOS, PCI, PCI-X, AGP-2X, HSTL, SSTL, GTL/+, LVPECL, LVDS, BLVDS
- 1.8V, 2.5V and 3.3V capable I/O
- True 3.3V and 5V tolerance with no external resistor necessary
- Up to 832 user I/Os
- Comprehensive clock management circuitry
- Up to 12 digital DLLs and 4 PLLs
- Variety of package options
- Integrated scan-test and JTAG support for high-fault coverage

2.0 Product Description

Targeted at medium-density, high-speed, 1.8V ASIC applications and high-density FPGA-to-ASIC conversions, the XPressArray 0.18µ hybrid gate array is an innovative next-generation technology platform that reduces time-to-market for system-on-chip (SoC) applications while delivering significant NRE and unit cost savings.

XPressArray offers a true drop-in replacement for Xilinx Virtex-E and Altera APEX-E FPGAs, making it the industry's lowest cost ASIC conversion solution. The result is a simplified route to cost reductions for OEMs looking to combine the flexibility of FPGA prototyping with a path to ASICs for final production.

Operating with system clock speeds up to 250MHz and local clocks up to 350MHz and available in a variety of package options, XPressArray 0.18µ devices deliver high-performance, low power ASIC solutions with densities to 2.6M ASIC gates.

Embedded configurable memory ranges from 23Kbits to 1.4Mbits, while flexible I/O technology includes support for a comprehensive array of common standards and compatibility with 1.8V, 2.5V, 3.3V and 5.0V I/O schemes. High fault coverage is provided through integrated scan-test and JTAG support.

For FPGA conversions rapid access to XPressArray technology can be achieved via AMI Semiconductor's NETRANS® FPGA-to-ASIC design flow. Alternatively, the availability of XPressArray synthesis libraries for leading commercial synthesizers allows conversion of FPGA designs to ASICs by simply re-targeting from an FPGA library to an XPressArray library.

Table 1: XPressArray 0.18µ Hybrid Gate Array Family

XPressArray Base	System Gates[1]	Usable ASIC Gates[2]	Usable RAM Bits[3]	DLL	PLL	Bond Pads[4]
XP164E	240K	44K	23K	4	2	164
XP220E	616K	136K	71K	4	2	220
XP270E	988K	226K	119K	4	2	270
XP368E	1972K	456K	240K	8	2	368
XP440E	3048K	718K	378K	8	2	440
XP560E	4970K	1181K	622K	8	4	560
XP704E	7942K	1895K	998K	12	4	704
XP832E	11100K	2664K	1403K	12	4	832[5]

(1) Equivalent FPGA system gates.
(2) Usable 2-NAND gate array equivalent gates, assumes full RAM utilization.
(3) Usable 2RW RAM bits, assumes full logic utilization.
(4) Total combined signal, power/ground and test bond pads.
(5) Flip-chip power pads not included in bond pad count.

Package offerings include traditional plastic TQFP/PQFP, as well as plastic and super BGA in 0.80mm, 1.00mm and 1.27mm pitches. Traditional wire-bond technology is used. Flip-chip technology is used on the largest array. Because XPressArray devices consume significantly less power than equivalent FPGAs, lower cost plastic packaging can be used in most cases. Table 2 shows the supported package configurations. Packaging options exist to optimize individual conversions.

Table 2: XPressArray Package Options

XPressArray Base	CS 144	F 144	T 144	Q 208	PQ/Q 240	FG 256	F 324	BG 352	B 356	BG 432	FG 456	F 484	BG 560	B 652	F 672	FG 676	FG 680	FG 860	FG 900	F 1020	F/CG 1156
XP164E	*	*	*	*	*																
XP220E	*	*	*	*	*	*	*	*	*												
XP270E	*	*	*	*	*	*	*	*	*												
XP368E							*	*	*	*	*	*									
XP440E							*		*	*	*	*	*	*	*	*			*		
XP560E												*	*	*	*	*	*	*	*	*	*
XP704E														*	*	*	*	*	*	*	*
XP832E																			*	*	*

* Supported package configuration
* Packaging option

3.0 The Advantages of XPressArray

FPGA devices are using ever smaller process geometries in the quest for higher density, higher performance and lower power. A consequence of this trend is that operating voltages have dropped with each new FPGA process introduction. To match operating voltage and still provide better performance and power consumption characteristics, an equivalent ASIC needs to be fabricated in a similar process technology. Another consequence of this process trend is that ASIC mask tooling costs have exploded. As a result, non-recurring engineering (NRE) charges for cell-based ASIC designs have priced out all but the highest volume applications.

The XPressArray architecture offers a unique solution to the challenges of maintaining FPGA process compatibility while delivering ASIC technology with reasonable NREs and low piece price. Compared to equivalent FPGAs, XPressArray devices operate at the same low voltage, offer higher densities, better performance and consume less power. Figure 1 compares volume pricing for FPGA, cell-based ASIC and XPressArray devices. Figure 2 compares power consumption of these devices.

XPressArray provides a FPGA conversion platform combining advanced process capability with virtually all the features of the Xilinx Virtex-E and Altera APEX-E devices. Support for a comprehensive array of I/O standards, abundant configurable memory, high-density logic and advanced high-performance clock management and frequency synthesis circuits round out the offering. XPressArray devices can be fabricated as pin-for-pin compatible FPGA drop-in replacements. Alternatively, multiple FPGAs can be combined into one XPressArray device, or die and package configurations can be optimized for specific requirements.

Access to XPressArray devices is via FPGA netlist conversion using AMI Semiconductor's NETRANS FPGA-to-ASIC flow. Or the re-synthesis route can be employed using AMI Semiconductors RTL hand-off flow.

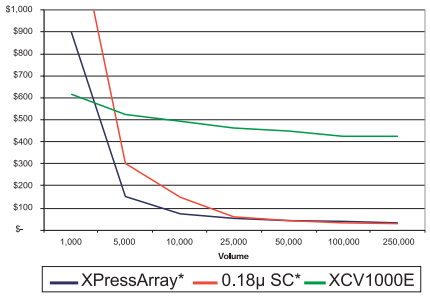


Fig. 1: Price vs. Volume (Amortized NRE)

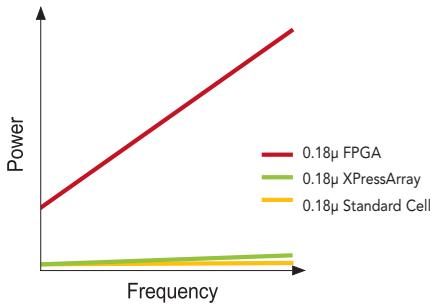
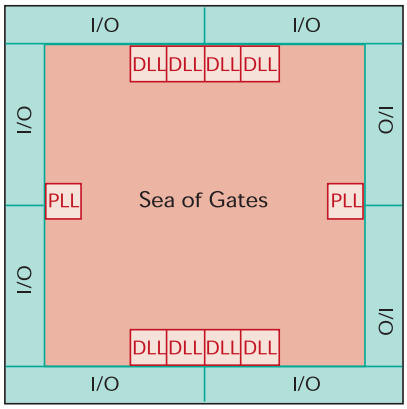


Fig. 2: XPressArray power consumption

4.0 XPressArray Architecture

Figure 3 shows the XPressArray device organization based around a sea-of-gates architecture with embedded RAM, DLLs, PLLs and support for a full compliment of I/O standards.

Fig. 3: XPressArray Architecture



5.0 I/O Description

The XPressArray I/O ring is composed of uniform I/O pad sites. Each pad site may be customized to operate as a signal pad, or a power supply pad for either the core or the I/O ring. The I/O power ring may be cut into virtually an unlimited number of segments. In most cases, the I/O power ring is divided into eight segments, making it compatible with the FPGA products and power supply rings built into the packages.

Signal pads are available for a wide variety of standards as listed in Table 3. Signal pads operate at 1.8V, 2.5V and 3.3V. In addition 3.3V and 5V tolerant pads are also available. Differential signaling standards typically require two pad sites. Signaling standards requiring a reference voltage typically share a common reference voltage within an I/O power ring segment, with the reference voltage being supplied through a pad from an off-chip source.

High-speed serial I/O operating at up to 622Mbps is supported with LVDS transceivers in conjunction with DLL/PLL clock management circuits and DDR (double data rate) circuitry.

Table 3: Supported I/O Standards

I/O Standards	Type[1]	VddIO	Notes
LVTTL	S	3.3	1-24mA, 5V-tolerant
LVCMOS33	S	3.3	1-24mA, 5V-tolerant
LVCMOS25	S	2.5	1-16mA, 3.3V/5V-tolerant (1-12mA)
LVCMOS18	S	1.8	1-24mA, 2.5V/3.3V-tolerant (1-8mA)
PCI33_33	S	3.3	Standard; 5V-tolerant requires external diode
PCI66	S	3.3	Standard; 5V-tolerant requires external diode
PCI-X	S	3.3	
AGP-2X	S	3.3	
ATA33	S	3.3	
GTL	V	N/A	
GTL+	V	N/A	
CTT	V	3.3	Contact factory for availability
SSTL-3 Type I	V	3.3	
SSTL-3 Type II	V	3.3	
SSTL-2 Type I	V	2.5	
SSTL-2 Type II	V	2.5	
HSTL Type I	V	1.5	
HSTL Type II	V	1.5	
HSTL Type III	V	1.5	
HSTL Type IV	V	1.5	
LVPECL33	V	3.3	
LVPECL25	V	2.5	
Xilinx LVDS	D	2.5	
LVDS33	D	3.3	
LVDS25	D	2.5	
LVDS18	D	1.8	Output only
Xilinx LVDS18	D	1.8	Input only; does not meet EIA/TAI LVDS spec
BLVDS33	D	3.3	
BLVDS25	D	2.5	

[1]I/O Types:
S: Single ended input and outputs.
V: Inputs are differential with respect to an external voltage reference, may share a reference pin. Outputs are single ended.
D: Fully differential input and output, requires two signal pins.

6.0 Memory Description

The XPressArray architecture supports abundant embedded RAM. Each RAM is individually port configurable as 512x1, 256x2, 128x4, 64x8 and 32x16 as shown in table 4. XPressArray embedded RAM blocks may be configured as single-port (1RW), dual-port (1R1W) or true dual-port (2RW). Synchronous and asynchronous modes are available. Synchronous-write asynchronous-read mode is supported for 1RW and 1R1W configurations. Each RAM bit is initializable by a late metal mask option.

The XPressArray memories also supports CAM by combining logic and embedded RAM functions together to form single-cycle, stackable binary or ternary 32x4 CAM blocks.

Table 4: Available RAM Configurations

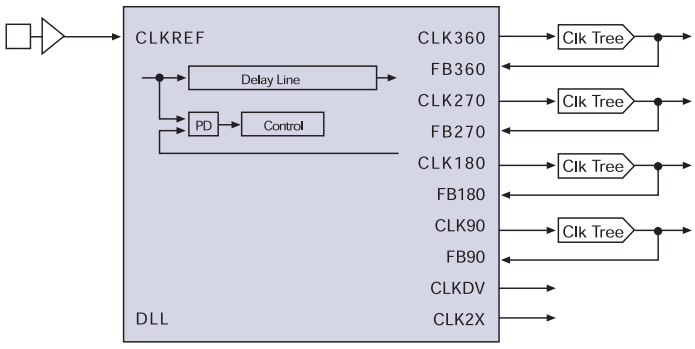
I/O Standard	Port A Width	Port B Width
RAM512X1_RW	1	N/A
RAM512X1_2RW	1	1
RAM512X1_256X2_2RW	1	2
RAM512X1_128X4_2RW	1	4
RAM512X1_64X8_2RW	1	8
RAM512X1_32X16_2RW	1	16
RAM256X2_1RW	2	N/A
RAM256X2_2RW	2	2
RAM256X2_128X4_2RW	2	4
RAM256X2_64X8_2RW	2	8
RAM256X3_32X16_2RW	2	16
RAM128X4_1RW	4	N/A
RAM128X4_2RW	4	4
RAM128X4_64X8_2RW	4	8
RAM128X4_32X16_2RW	4	16
RAM64X8_1RW	8	N/A
RAM64X8_2RW	8	8
RAM64X8_32X16_2RW	8	16
RAM32X16_2RW	16	N/A
RAM32X16_2RW	16	16

7.0 Delay-Locked Loop (DLL) Description

XPressArray devices employ clock tree synthesis to route a virtually unlimited number of clock and reset signals to the flip-flop groups. Synthesized clock trees deliver high speed clock signals with minimal skew and power.

DLLs are embedded into the XPressArray bases to minimize clock insertion delay, perform limited clock frequency synthesis and generate phase taps. Applications include double data rate (DDR) serial I/O and clock data recovery (CDR).

Fig. 4: DLL



8.0 Phase-Locked Loop (PLL) Description

PLLs are embedded into the XPressArray bases to perform advanced clock frequency synthesis operations, minimize clock insertion delay and generate phase taps. Applications include double data rate (DDR) serial I/O and clock data recovery (CDR). Each PLL can be configured as a general purpose or LVDS PLL.

Figure 5 shows the general purpose PLL configuration. All dividers have a range of 1 to 2049. In normal mode, the PLL performs classical "M over N" frequency synthesis application. When the output frequency is an integer multiple or division of the input frequency precise phase control allows fine adjustment of the phase relationship of the output to the

Fig. 5: General Purpose PLL

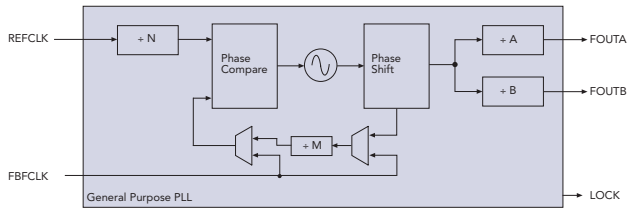
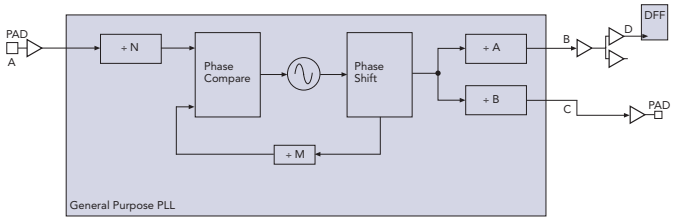


Fig. 6: General Purpose PLL in Normal Mode



input. In this example, locations B and C are phase controlled with respect to A. The phase relationship of A and D is inferred.

Figure 7 shows the general purpose PLL used in zero delay mode. This mode supports integer multiply or divide for both outputs. Locations A and B are phased matched.

Fig. 7: General Purpose PLL in Zero Delay Mode

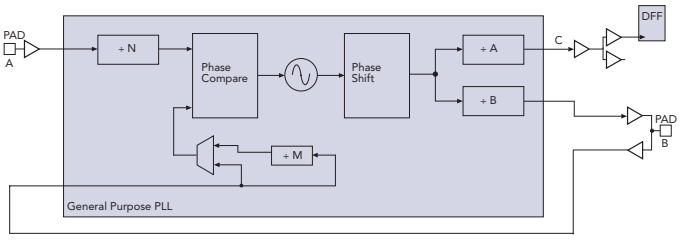


Figure 8 shows the general purpose PLL used in external feedback mode. This mode supports integer multiply or divide for both outputs. Locations A and B are phase matched.

Fig. 8: General Purpose PLL in External Feedback Mode

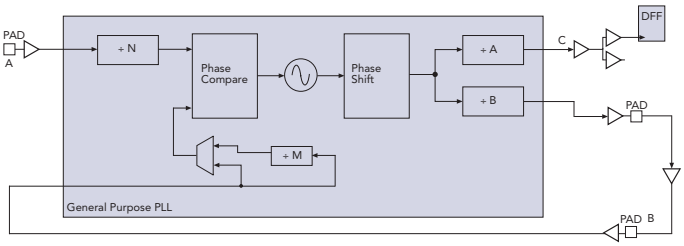


Figure 9 shows the general purpose PLL used in clock tree mode. This mode supports integer multiply or divide for both outputs. Locations A and B are phase matched, C is phase controlled with respect to D.

Fig. 9: General Purpose PLL in Clock Tree Mode

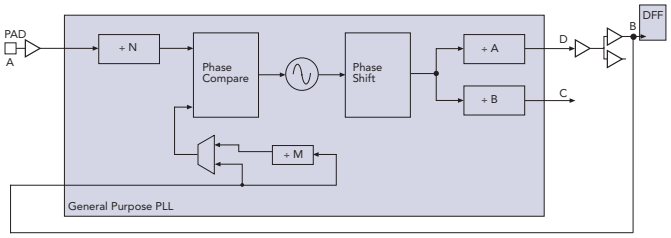
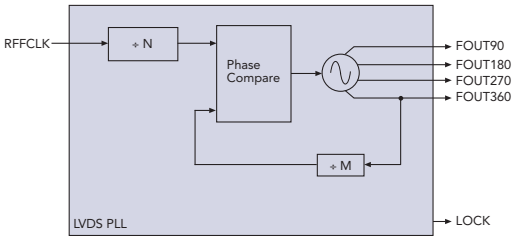


Figure 10 shows the LVDS PLL configuration which supports high-speed serial I/O applications. The reference divider supports a range of 1 to 2049 while the feedback divider is limited to a range of 1 to 33.

Fig. 10: LVDS PLL



The PLL contains integral test hardware to facilitate silicon testing and in-circuit PLL tuning. The PLL requires a dedicated power and ground pad pair.

9.0 NETRANS® Conversion Flow

XPressArray devices are fully supported by AMI Semiconductor's proven NETRANS flow. AMIS has over 15 years experience using NETRANS to convert over 1500 FPGA and third party ASIC designs to AMIS ASICs.

Inputs to the NETRANS flow include the FPGA or ASIC netlist, test benches and timing constraints. Over 70 different device types and netlist formats are supported.

Xilinx, Virtex and Altera APEX mapping libraries are fully verified by a process which includes formal verification of each primitive function. Support is also available for other FPGA device from Xilinx, Altera, Actel, Lattice, etc. Support for ASIC conversions from LSI, NEC, Toshiba, etc. to AMIS ASICs is available also.

10.0 RTL Hand-Off Flow

XPressArray synthesis libraries are available for leading commercial synthesizers, including Synplicity Synplify ASIC and Synopsys Design Compiler.

With the RTL Hand-Off flow, you can submit your RTL description, scripts and timing constraints to AMIS. AMIS will check, synthesize, layout and achieve timing closure on your design. Typically if Synplify Pro was used for the FPGA design, then Synplify ASIC will be used for the ASIC design. Likewise is FPGA Express was used, then Design Compiler is used for the ASIC re-synthesis.

11.0 Electrical Specifications

Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Units
V_{DDINT}	Internal Supply Voltage	-0.3	2.2	V
V_{DDIO}	I/O Supply Voltage	-0.3	4.0	V
V_{REF}	Input Reference Voltage	-0.3	4.0	V
V_{IN}, V_{OUT}	DC Input, Output	-0.3	4.0	V
T_J	Junction Temperature	-55	125	°C
T_L	Lead Temperature (Soldering 10s)		250	°C

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
V_{DDINT}	Internal Supply Voltage	1.62	1.98	V
V_{DDIO}	I/O Supply Voltage	1.2	3.6	V

DLL Specifications

Parameter	Value
Low Frequency Version	
Frequency Range	20-200MHz
Available Outputs	CLK90, CLK180, CLK270, CLK360, CLKDV, CLK2X
Clock Doubler Range	40-400MHz
Clock Divider Range	1.5-16 in 0.5 steps, 16-32 in 1.0 steps
High Frequency Version	
Frequency Range	200-350MHz
Available Outputs	CLK180, CLK360, CLKDV
Clock Divider Range	2-32 in 1.0 steps
Overall Characteristics	
Operating Voltage	1.8V ± 5%
Temperature	Commercial
Jitter	±85ps cycle-to-cycle
Phase offset between outputs	200ps estimated

DC Characteristics

Symbol	Parameter	Min.	Max.	Units
I_{CCINT}	Quiescent VDDINT supply current			µA
I_{CCIO}	Quiescent VDDIO supply current			µA
I_L	Input or output leakage current			µA
C_{IN}	Input capacitance			pF

PLL Specifications

Parameter	Value
General Purpose Operation	
Operating Modes	• Normal with Phase Shift • Zero Delay Buffer • External Feedback • Clock Tree
VCO Frequency Range	200-500MHz
PFD Frequency Range	1-50MHz
Max Input Frequency	500MHz
Reference Divider	1-2049
Feedback Divider	1-2049
Post Dividers	1-2049
Phase Shift Resolution	1/[FVCO*5]
Phase Shift Range	0-360O
Available Outputs	FOUTA, FOUTB
LVDS Operation	
VCO Frequency Range	200-800MHz
PFD Frequency Range	1-50MHz
Max Input Frequency	500MHz
Reference Divider	1-2049
Feedback Divider	1-33
Post Dividers	1, with 4 quadrature outputs
Available Outputs	FOUT90, FOUT180, FOUT270, FOUT360
Overall Characteristics	
Operating Voltage	1.8V +/- 5%
Temperature	Commercial
Jitter	+/-100ps peak-to-peak

12.0 FPGA Cross Reference

Xilinx Device	XPressArray Device
XCV50E-CS144	XP164E-CSP144 *
XCV50E-PQ240	XP270E-PQFP240
XCV50E-FG256	XP270E-PBGA256
XCV100E-CS144	XP164E-CSP144 *
XCV100E-PQ240	XP270E-PQFP240
XCV100E-FG256	XP270E-PBGA256
XCV100E-BG352	XP270E-SBGA352
XCV200E-CS144	XP164E-CSP144 *
XCV200E-PQ240	XP270E-PQFP240
XCV200E-FG256	XP270E-PBGA256
XCV200E-BG352	XP368E-SBGA352
XCV200E-FG456	XP440E-PBGA456
XCV300E-PQ240	XP270E-PQFP240
XCV300E-FG256	XP270E-PBGA256
XCV300E-BG352	XP368E-SBGA352
XCV300E-BG432	XP440E-PBGA432
XCV300E-FG456	XP440E-PBGA456
XCV400E-PQ240	XP270E-PQFP240
XCV400E-BG432	XP440E-PBGA432
XCV400E-BG560	XP560E-SBGA560
XCV400E-FG676	XP560E-PBGA676
XCV600E-HQ240	XP220E-PQFP240
XCV600E-BG432	XP440E-PBGA432
XCV600E-BG560	XP560E-SBGA560
XCV600E-FG676	XP704E-PBGA676
XCV600E-FG680	XP704E-FBGA680 *
XCV600E-FG900	XP560E-FBGA900 *
XCV1000E-HQ240	XP270E-PQFP240
XCV1000E-BG560	XP560E-SBGA560
XCV1000E-FG680	XP704E-FBGA680 *
XCV1000E-FG860	XP704E-FBGA860 *
XCV1000E-FG900	XP704E-FBGA900 *
XCV1000E-FG1156	XP704E-FBGA1156 *
XCV1600E-BG560	XP560E-SBGA560
XCV1600E-FG680	XP704E-FBGA680 *
XCV1600E-FG860	XP704E-FBGA860 *
XCV1600E-FG900	XP832E-FBGA900 *
XCV1600E-FG1156	XP832E-FBGA1156 *
XCV2000E-BG560	XP560E-SBGA560
XCV2000E-FG680	XP704E-FBGA680 *
XCV2000E-FG860	XP704E-FBGA860 *
XCV2000E-FG1156	XP832E-FBGA1156 *
XCV2600E-FG1156	XP832E-FBGA1156 *
XCV3200E-CG1156	XP832E-FBGA1156 *

* Consult factory.

Altera Device	XPressArray Device
EP20K30E-F144	XP164E-FBGA144 *
EP20K30E-T144	XP164E-LQFP144
EP20K30E-Q208	XP220E-PQFP208
EP20K30E-F324	XP220E-FBGA324 *
EP20K60E-F144	XP164E-FBGA144 *
EP20K60E-T144	XP164E-LQFP144
EP20K60E-Q208	XP220E-PQFP208
EP20K60E-Q240	XP220E-PQFP240
EP20K60E-F324	XP270E-FBGA324 *
EP20K60E-B356	XP270E-PBGA356
EP20K100E-F144	XP164E-FBGA144 *
EP20K100E-T144	XP164E-LQFP144
EP20K100E-Q208	XP220E-PQFP208
EP20K100E-Q240	XP270E-PQFP240
EP20K100E-F324	XP368E-FBGA324 *
EP20K100E-B356	XP368E-PBGA356
EP20K160E-T144	XP164E-LQFP144
EP20K160E-Q208	XP220E-PQFP208
EP20K160E-Q240	XP270E-PQFP240
EP20K160E-R240	XP270E-PQFP240
EP20K160E-B356	XP440E-PBGA356
EP20K160E-F484	XP440E-FBGA484 *
EP20K200E-Q208	XP220E-PQFP208
EP20K200E-Q240	XP270E-PQFP240
EP20K200E-B356	XP440E-PBGA356
EP20K200E-F484	XP560E-FBGA484 *
EP20K200E-B652	XP560E-PBGA652 *
EP20K200E-F672	XP560E-FBGA672 *
EP20K300E-Q240	XP270E-PQFP240
EP20K300E-B652	XP560E-PBGA652 *
EP20K300E-F672	XP560E-FBGA672 *
EP20K400E-B652	XP704E-PBGA652 *
EP20K400E-F672	XP704E-FBGA672 *
EP20K600E-B652	XP704E-PBGA652 *
EP20K600E-F672	XP704E-FBGA672 *
EP20K600E-F1020	XP704E-FBGA1020 *
EP20K1000E-B652	XP704E-PBGA652 *
EP20K1000E-F672	XP704E-FBGA672 *
EP20K1000E-F1020	XP832E-FBGA1020 *
EP20K1500E-B652	XP704E-PBGA652 *
EP20K1500E-F1020	XP832E-FBGA1020 *

* Consult factory.