- Input Voltage Range : 2.5V ~ 20V
- Output Voltage Range : 1.2V ~ 16.0V
- Oscillation Frequency Range : 100kHz ~ 600kHz
- Output Current : up to 3.0A
- Ceramic Capacitor Compatible
- MSOP-8A Package

APPLICATIONS

- Mobile phones, Cordless phones
- Palm top computers, PDAs
- Portable game
- Camera, Digital camera
- Note book computer

GENERAL DESCRIPTION

The XC9201 series are step-up multiple current and voltage feedback DC/DC controller ICs. Current sense, clock frequencies and amp feedback gain can all be externally regulated. A stable power supply is possible with output currents of up to 3.0A. With output voltage fixed internally, VOUT is selectable in 0.1V steps within a 1.2V - 16.0V range (± 2.5%).

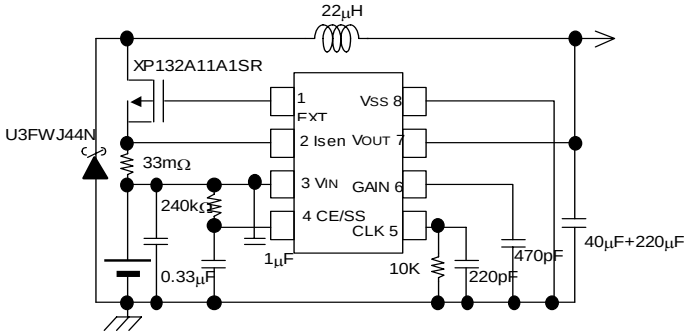
For output voltages outside this range, we recommend the FB version which has a 0.9V internal reference voltage. Using this version, the required output voltage can be set-up using 2 external resistors. Switching frequencies can also be set-up externally within a range of 100~600 kHz and therefore frequencies suited to your particular application can be selected.

With the current sense function, peak currents (which flow through the driver transistor and the coil) can be controlled. Soft-start time can be adjusted using external resistors and capacitors. During shutdown (CE pin =L), consumption current can be reduced to as little as 0.5μA (TYP.) or less and with U.V.L.O (Under Voltage Lock Out) built-in, the external transistor will be automatically shut off below the regulated voltage.

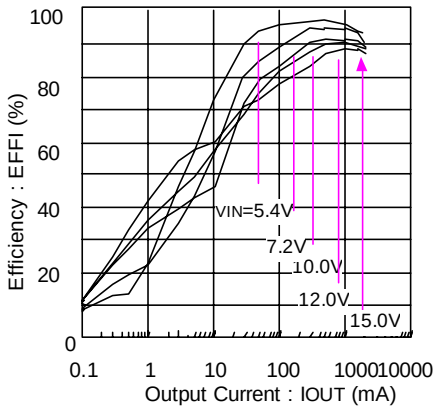
FEATURES

- Stable Operations via Current & Voltage Multiple Feedback
- Unlimited Options for Peripheral Selection
- Current Protection Circuit
- Ceramic Capacitor Compatible

TYPICAL APPLICATION CIRCUIT

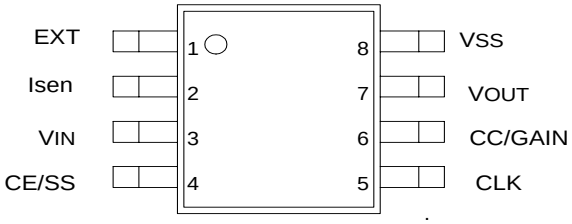


TYPICAL PERFORMANCE CHARACTERISTICS



TOREX Semiconductor Ltd.

■ PIN CONFIGURATION



MSOP-8A (TOP VIEW)

■ PIN ASSIGNMENT

PIN NUMBER	PIN NAME	FUNCTION
1	EXT	Driver
2	ISEN	Current Sense
3	VIN	Power Input
4	CE / SS	CE/Soft Start
5	CLK	Clock Input
6	CC / GAIN	Phase Compensation
7	VOUT / FB	Voltage Sense
8	VSS	Ground

■ PRODUCT CLASSIFICATION

● Ordering Information

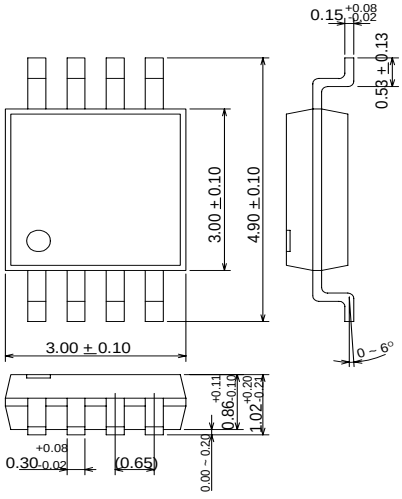
XC9201 ① ② ③ ④ ⑤ ⑥

DESIGNATOR	SYMBOL	DESCRIPTION	
①	C	VOUT	Soft-start externally set-up
	D	FB	Soft-start externally set-up
②③	Number	Output Voltage : For voltages above 10V, see below :	
		10=A, 11=B, 12=C, 13=D, 14=E, 15=F, 16=H	
		e.g. VOUT=2.3V → ②=2, ③=3 VOUT=13.5V → ②=D, ③=5	
		FB products → ②=0, ③=9 fixed	
④	A	Adjustable Frequency	
⑤	K	MSOP-8A	
⑥	R	Embossed tape. Standard Feed	
	L	Embossed tape. Reverse Feed	

The standard output voltages of the XC9201C series are 2.5V, 3.3V, and 5.0V.
Voltages other than those listed are semi-custom.

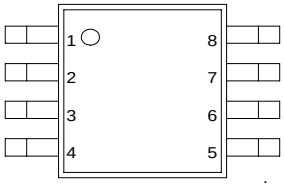
■ PACKAGING INFORMATION

❍ MSOP-8A



■ MARKING RULE

❍ MSOP-8A



MARK ① : Represents product series

SYMBOL	PART NUMBER
1	XC9201xxxAKx

MARK ② : Represents product type, DC/DC converter

SYMBOL	TYPE	PART NUMBER
C	VOUT, CE PIN	XC9201CxxAKx
D	FB, CE PIN	XC9201D09AKx

MARK ③ : Represents integral number of output voltage, or FB type

SYMBOL	VOLTAGE	TYPE	SYMBOL	VOLTAGE	TYPE
1	1. X	XC9201C1xAKx	A	10. X	XC9201CAxAKx
2	2. X	XC9201C2xAKx	B	11. X	XC9201CBxAKx
3	3. X	XC9201C3xAKx	C	12. X	XC9201CCxAKx
4	4. X	XC9201C4xAKx	D	13. X	XC9201CDxAKx
5	5. X	XC9201C5xAKx	E	14. X	XC9201CExAKx
6	6. X	XC9201C6xAKx	F	15. X	XC9201CFxAKx
7	7. X	XC9201C7xAKx	H	16. X	XC9201CHxAKx
8	8. X	XC9201C8xAKx			
9	9. X	XC9201C9xAKx			
0	FB products	XC9201D09AKx			

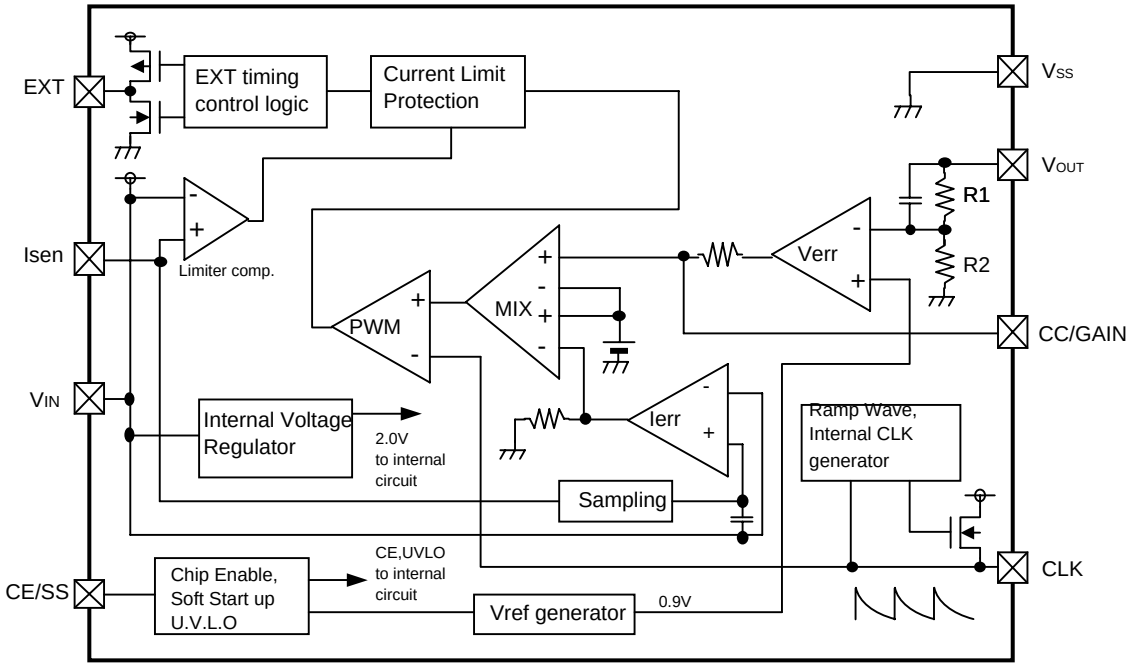
MARK ④ : Represents decimal point of output voltage

SYMBOL	VOLTAGE	PART NUMBER
0	X . 0	XC9201Cx0AKx
3	X . 3	XC9201Cx3AKx
9	FB products	XC9201D09AKx

MARK ⑤ : Represents oscillation frequency's control type

SYMBOL	TYPE	PART NUMBER
A	Adjustable Frequency	XC9201xxxAKx

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Ta = 25°C

PARAMETER	SYMBOL	RATINGS	UNITS
EXT Pin Voltage	VEXT	- 0.3 ~ VDD + 0.3	V
ISEN Pin Voltage	VISEN	- 0.3 ~ + 22	V
VIN Pin Voltage	VIN	- 0.3 ~ + 22	V
CE/SS Pin Voltage	VCE	- 0.3 ~ + 22	V
CLK Pin Voltage	VCLK	- 0.3 ~ VDD + 0.3	V
CC/GAIN Pin Voltage	VCC	- 0.3 ~ VDD + 0.3	V
VOUT/FB Pin Voltage	VOUT	- 0.3 ~ + 22	V
EXT Pin Current	IEXT	± 100	mA
Continuous Total Power Dissipation	Pd	150	mW
Operating Temperature Range	Topr	- 40 ~ + 85	°C
Storage Temperature Range	Tstg	- 55 ~ + 125	°C

■ ELECTRICAL CHARACTERISTICS

XC9201C25AKR Ta=25°C

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUITS
Output Voltage	VOUT	IOUT=300mA	2.438	2.500	2.562	V	①
Maximum Operating Voltage	VINmax		20	-	-	V	①
Minimum Operating Voltage	VINmin		-	-	2.200	V	①
U.V.L.O. Voltage	VUVLO	EXT voltage = High	1.0	1.400	2.0	V	⑤
Supply Current 1	IDD1	VIN = 3.75V, CE=VIN=VOUT		115	220	μA	②
Supply Current 2	IDD2	VIN=20.0V, CE=VIN, VOUT=VSS		130	235	μA	②
Stand-by Current	ISTB	VIN=3.75V, CE=VOUT=VSS		0.5	2.0	μA	②
CLK Oscillation Frequency	FOSC	RT=10.0kΩ, CT=220pF	280	330	380	kHz	③
Frequency Input Stability	$\frac{\Delta FOSC}{\Delta VIN \cdot FOSC}$	VIN=2.5V~20V		± 5		%	③
Frequency Temperature Fluctuation	$\frac{\Delta FOSC}{\Delta TOPR \cdot FOSC}$	VIN=3.75V , TOPR= - 40 ~ + 85°C		± 5		%	③
Maximum Duty Cycle	MAXDTY	VOUT=VSS	100			%	④
Minimum Duty Cycle	MINDTY	VOUT=VIN			0	%	⑥
Current Limiter Voltage	ILIM	VIN pin voltage - ISEN pin voltage	90	150	220	mV	⑥
ISEN Current	IISEN	VIN = 3.75V, ISEN = 3.75V	4.5	7	13	μA	⑥
CE "High" Current	ICEH	CE = VIN = 20.0V, VOUT = 0V	- 0.1	0	0.1	μA	⑤
CE "Low" Current	ICEL	CE = 0V, VIN = 20.0V, VOUT = 0V	- 0.1	0	0.1	μA	⑤
CE "High" Voltage	VCEH	Existence of CLK Oscillation, VOUT = 0V, CE : Voltage applied	0.6			V	⑤
CE "Low" Voltage	VCEL	Disappearance of CLK Oscillation, VOUT = 0V, CE : Voltage applied			0.2	V	⑤
EXT "High" ON Resistance	REXTH	EXT=VIN - 0.4V, CE=VOUT=VIN *1		27	40	Ω	④
EXT "Low" ON Resistance	REXTL	EXT=0.4V, CE=VIN, VOUT=VSS *1		24	33	Ω	④
Efficiency	EFFI			93		%	①
Soft-Start Time	TSS	Connect CSS and RSS, CE : 0V → 3.75V	5	10	20	mS	①
CC/GAIN Pin Output Impedance	RCCGAIN			400		kΩ	⑦

VIN = 3.75V unless specified

*1 : On resistance = 0.4V / measurement current

NOTE1 : EFFI = {[(Output Voltage) × (Output Current)] ÷ [(Input Voltage) × (Input Current)]} × 100

NOTE2 : The capacity range of the condenser used to set the external CLK frequency is 180 ~ 300pF

■ ELECTRICAL CHARACTERISTICS

XC9201C33AKR Ta=25°C

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUITS
Output Voltage	VOUT	IOUT=300mA	3.218	3.300	3.382	V	①
Maximum Operating Voltage	VINmax		20	-	-	V	①
Minimum Operating Voltage	VINmin		-	-	2.200	V	①
U.V.L.O. Voltage	VUVLO	EXT voltage = High	1.0	1.400	2.0	V	⑤
Supply Current 1	IDD1	VIN = 5.0V, CE=VIN=VOUT		115	220	μA	②
Supply Current 2	IDD2	VIN=20.0V, CE=VIN, VOUT=VSS		130	235	μA	②
Stand-by Current	ISTB	VIN=5.0V, CE=VOUT=VSS		0.5	2.0	μA	②
CLK Oscillation Frequency	FOSC	RT=10.0kΩ, CT=220pF	280	330	380	kHz	③
Frequency Input Stability	$\frac{\Delta FOSC}{\Delta VIN \cdot FOSC}$	VIN=2.5V~20V		± 5		%	③
Frequency Temperature Fluctuation	$\frac{\Delta FOSC}{\Delta TOPR \cdot FOSC}$	VIN=5.0V , TOPR= - 40 ~ + 85°C		± 5		%	③
Maximum Duty Cycle	MAXDTY	VOUT=VSS	100			%	④
Minimum Duty Cycle	MINDTY	VOUT=VIN			0	%	⑥
Current Limiter Voltage	ILIM	VIN pin voltage - ISEN pin voltage	90	150	220	mV	⑥
ISEN Current	IISEN	VIN = 5.0V, ISEN = 5.0V	4.5	7	13	μA	⑥
CE "High" Current	ICEH	CE = VIN = 20.0V, VOUT = 0V	- 0.1	0	0.1	μA	⑤
CE "Low" Current	ICEL	CE = 0V, VIN = 20.0V, VOUT = 0V	- 0.1	0	0.1	μA	⑤
CE "High" Voltage	VCEH	Existence of CLK Oscillation, VOUT = 0V, CE : Voltage applied	0.6			V	⑤
CE "Low" Voltage	VCEL	Disappearance of CLK Oscillation, VOUT = 0V, CE : Voltage applied			0.2	V	⑤
EXT "High" ON Resistance	REXTH	EXT=VIN - 0.4V, CE=VOUT=VIN *1		24	33	Ω	④
EXT "Low" ON Resistance	REXTL	EXT=0.4V, CE=VIN, VOUT=VSS *1		22	31	Ω	④
Efficiency	EFFI			93		%	①
Soft-Start Time	TSS	Connect CSS and RSS, CE : 0V → 5.0V	5	10	20	mS	①
CC/GAIN Pin Output Impedance	RCCGAIN			400		kΩ	⑦

VIN = 5.0V unless specified

*1 : On resistance = 0.4V / measurement current

NOTE1 : EFFI = {[(Output Voltage) × (Output Current)] ÷ [(Input Voltage) × (Input Current)]} × 100

NOTE2 : The capacity range of the condenser used to set the external CLK frequency is 180 ~ 300pF

■ ELECTRICAL CHARACTERISTICS

XC9201C50AKR Ta=25°C

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUITS
Output Voltage	VOUT	IOUT=300mA	4.875	5.000	5.125	V	①
Maximum Operating Voltage	VINmax		20	-	-	V	①
Minimum Operating Voltage	VINmin		-	-	2.200	V	①
U.V.L.O. Voltage	VUVLO	EXT voltage = High	1.0	1.400	2.0	V	⑤
Supply Current 1	IDD1	VIN = 7.5V, CE=VIN=VOUT		115	220	μA	②
Supply Current 2	IDD2	VIN=20.0V, CE=VIN, VOUT=VSS		130	235	μA	②
Stand-by Current	ISTB	VIN=7.5V, CE=VOUT=VSS		0.5	2.0	μA	②
CLK Oscillation Frequency	FOSC	RT=10.0kΩ, CT=220pF	280	330	380	kHz	③
Frequency Input Stability	$\frac{\Delta FOSC}{\Delta VIN \cdot FOSC}$	VIN=2.5V~20V		± 5		%	③
Frequency Temperature Fluctuation	$\frac{\Delta FOSC}{\Delta TOPR \cdot FOSC}$	VIN=7.5V , TOPR= - 40 ~ + 85°C		± 5		%	③
Maximum Duty Cycle	MAXDTY	VOUT=VSS	100			%	④
Minimum Duty Cycle	MINDTY	VOUT=VIN			0	%	⑥
Current Limiter Voltage	ILIM	VIN pin voltage - ISEN pin voltage	90	150	220	mV	⑥
ISEN Current	IISEN	VIN = 7.5V, ISEN = 7.5V	4.5	7	13	μA	⑥
CE "High" Current	ICEH	CE = VIN = 20.0V, VOUT = 0V	- 0.1	0	0.1	μA	⑤
CE "Low" Current	ICEL	CE = 0V, VIN = 20.0V, VOUT = 0V	- 0.1	0	0.1	μA	⑤
CE "High" Voltage	VCEH	Existence of CLK Oscillation, VOUT = 0V, CE : Voltage applied	0.6			V	⑤
CE "Low" Voltage	VCEL	Disappearance of CLK Oscillation, VOUT = 0V, CE : Voltage applied			0.2	V	⑤
EXT "High" ON Resistance	REXTH	VEXT=VIN - 0.4V, CE=VOUT=VIN *1		21	29	Ω	④
EXT "Low" ON Resistance	REXTL	VEXT=0.4V, CE=VIN, VOUT=VSS *1		20	27	Ω	④
Efficiency	EFFI			93		%	①
Soft-Start Time	TSS	Connect CSS and RSS, CE : 0V → 7.5V	5	10	20	mS	①
CC/GAIN Pin Output Impedance	RCCGAIN			400		kΩ	⑦

VIN = 7.5V unless specified

*1 : On resistance = 0.4V / measurement current

NOTE1 : EFFI = {[(Output Voltage) × (Output Current)] ÷ [(Input Voltage) × (Input Current)]} × 100

NOTE2 : The capacity range of the condenser used to set the external CLK frequency is 180 ~ 300pF

■ ELECTRICAL CHARACTERISTICS

XC9201C09AKR Ta=25°C

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUITS
FB Voltage	VFB	IOUT=300mA	0.8775	0.900	0.9225	V	①
Maximum Operating Voltage	VINmax		20	-	-	V	①
Minimum Operating Voltage	VINmin		-	-	2.200	V	①
U.V.L.O. Voltage	VUVLO	EXT voltage = High	1.0	1.400	2.0	V	⑤
Supply Current 1	IDD1	VIN = 4.0V, CE=VIN=FB		115	220	μA	②
Supply Current 2	IDD2	VIN=20.0V, CE=VIN, FB=VSS		130	235	μA	②
Stand-by Current	ISTB	VIN=4.0V, CE=FB=VSS		0.5	2.0	μA	②
CLK Oscillation Frequency	FOSC	RT=10.0kΩ, CT=220pF	280	330	380	kHz	③
Frequency Input Stability	$\frac{\Delta FOSC}{\Delta VIN \cdot FOSC}$	VIN=2.5V~20V		± 5		%	③
Frequency Temperature Fluctuation	$\frac{\Delta FOSC}{\Delta TOPR \cdot FOSC}$	VIN=4.0V , TOPR= - 40 ~ + 85°C		± 5		%	③
Maximum Duty Cycle	MAXDTY	FB=VSS	100			%	④
Minimum Duty Cycle	MINDTY	FB=VIN			0	%	⑥
Current Limiter Voltage	ILIM	VIN pin voltage - ISEN pin voltage	90	150	220	mV	⑥
ISEN Current	IISEN	VIN = 4.0V, ISEN = 4.0V	4.5	7	13	μA	⑥
CE "High" Current	ICEH	CE = VIN = 20.0V, FB = 0V	- 0.1	0	0.1	μA	⑤
CE "Low" Current	ICEL	CE = 0V, VIN = 20.0V, FB = 0V	- 0.1	0	0.1	μA	⑤
CE "High" Voltage	VCEH	Existence of CLK Oscillation, FB = 0V, CE : Voltage applied	0.6			V	⑤
CE "Low" Voltage	VCEL	Disappearance of CLK Oscillation, FB = 0V, CE : Voltage applied			0.2	V	⑤
EXT "High" ON Resistance	REXTH	EXT=VIN - 0.4V, CE=FB=VIN *1		27	40	Ω	④
EXT "Low" ON Resistance	REXTL	EXT=0.4V, CE=VIN, FB=VSS *1		24	34	Ω	④
Efficiency	EFFI			93		%	①
Soft-Start Time	TSS	Connect CSS and RSS, CE : 0V → 4.0V	5	10	20	mS	①
CC/GAIN Pin Output Impedance	RCCGAIN			400		kΩ	⑦

VIN = 4.0V unless specified

External components : RFB1=200kΩ, RFB2=100kΩ, CFB=82pF

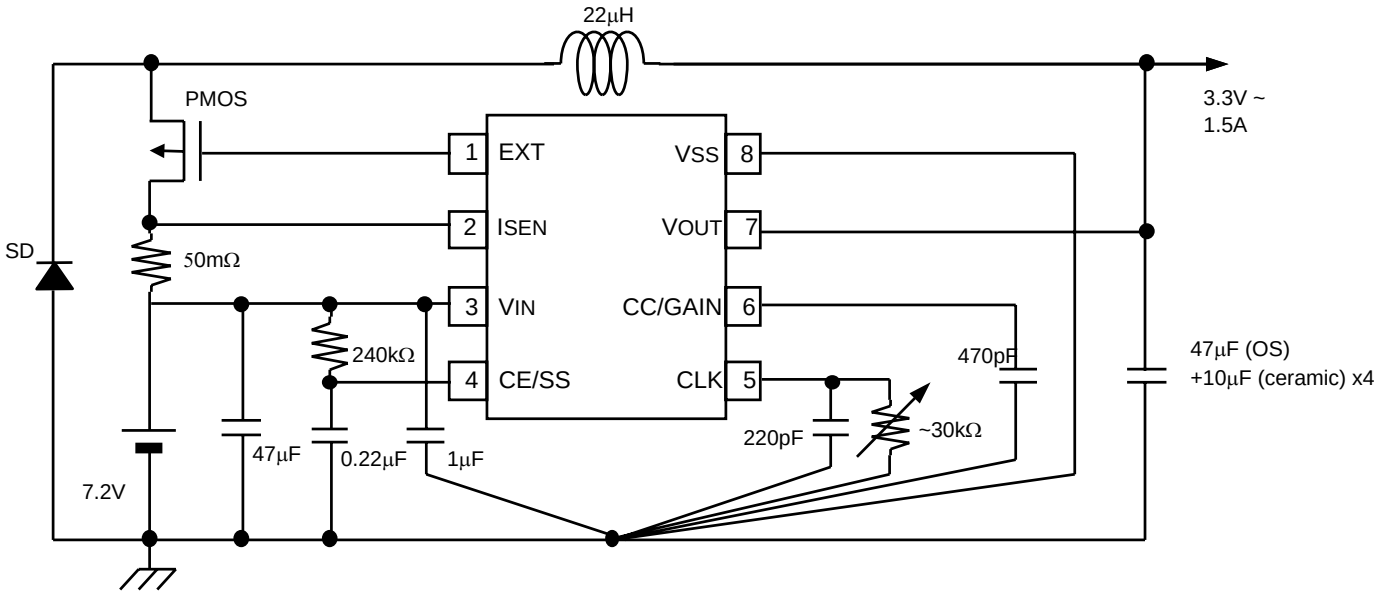
*1 : On resistance = 0.4V / measurement current

NOTE1 : EFFI = {[(Output Voltage) × (Output Current)] ÷ [(Input Voltage) × (Input Current)]} × 100

NOTE2 : The capacity range of the condenser used to set the external CLK frequency is 180 ~ 300pF

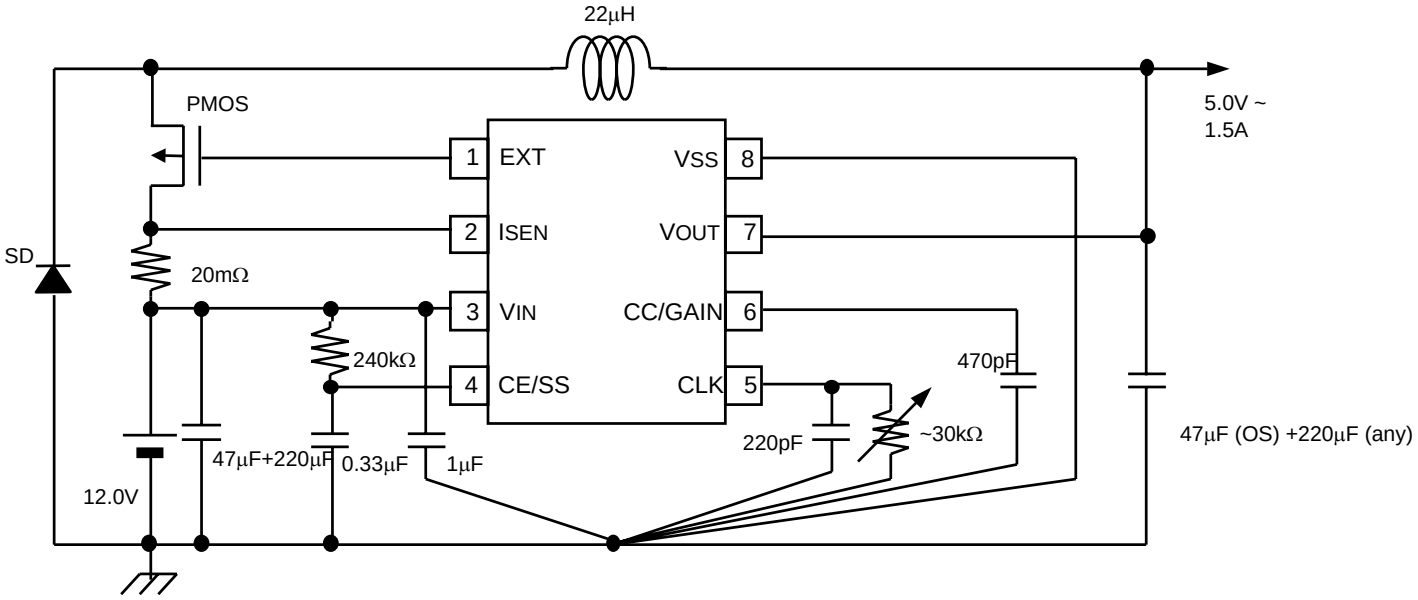
■ TYPICAL APPLICATION CIRCUIT

XC9201C33AKR



PMOS : XP132A11A1SR (TOREX)
Coil : 22μH (CR105 SUMIDA)
Resistor : 50mΩ for ISEN (NPR1 KOWA), 30kΩ (trimmer) for CLK, 240kΩ for SS
Capacitors : 220pF (ceramic) for CLK, 470pF (ceramic) for CC/GAIN, 0.22μF (ceramic) for SS, 1.0μF (ceramic) for Bypass
47μF (OS) or 10μF (ceramic) x 4 for CL, 47μF (tantalum) for CIN
SD : U3FWJ44N (TOSHIBA)

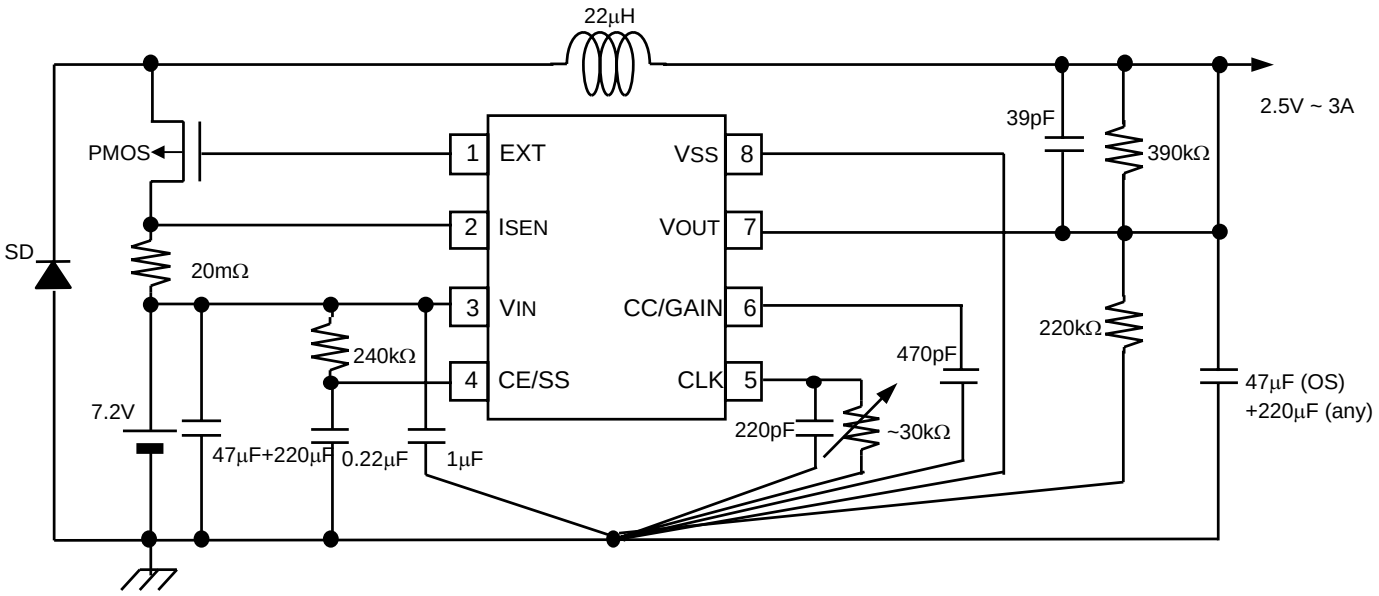
XC9201C50AKR



PMOS : XP132A11A1SR (TOREX)
Coil : 22μH (CDRH127 SUMIDA)
Resistor : 20mΩ for ISEN (NPR1 KOWA), 30kΩ (trimmer) for CLK, 240kΩ for SS
Capacitors : 220pF (ceramic) for CLK, 470pF (ceramic) for CC/GAIN, 0.33μF (any) for SS, 1.0μF (ceramic) for Bypass
47μF (OS) + 220μF (any) for CL, 47μF (tantalum) + 220μF (any) for CIN
SD : U3FWJ44N (TOSHIBA)

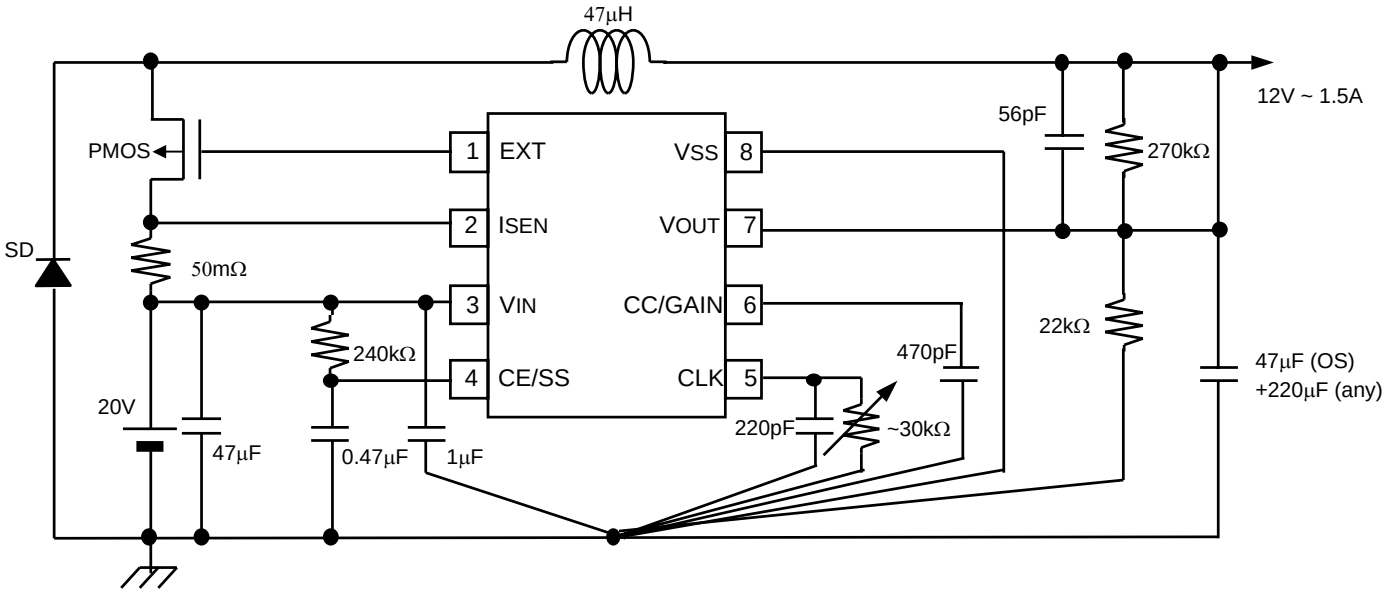
■ TYPICAL APPLICATION CIRCUIT (Continued)

XC9201D09AKR



PMOS : XP132A11A1SR (TOREX)
Coil : 22μH (CDRH127 SUMIDA)
Resistors : 20mΩ for ISEN (NPR1 KOWA), 30kΩ (trimmer) for CLK, 240kΩ for SS, 390kΩ for output voltage
220kΩ for output voltage
Capacitors : 220pF (ceramic) for CLK, 470pF (ceramic) for CC/GAIN, 0.22μF (any) for SS, 1.0μF (ceramic) for Bypass
39pF (ceramic) for FB, 47μF (OS) for CL, 47μF (tantalum) + 220μF (any) for CIN
SD : U3FWJ44N (TOSHIBA)

XC9201D09AKR



PMOS : XP132A11A1SR (TOREX)
Coil : 47μH (CR105 SUMIDA)
Resistors : 50mΩ for ISEN (NPR1 KOWA), 30kΩ (trimmer) for CLK, 240kΩ for SS, 270kΩ for output voltage
22kΩ (trimmer) for output voltage
Capacitors : 200pF (ceramic) for CLK, 470pF (ceramic) for CC/GAIN, 0.47μF (any) for SS, 1.0μF (ceramic) for Bypass
56pF (ceramic) for FB, 47μF (OS) + 220μF (any) for CL, 47μF (tantalum) + 220μF (any) for CIN
SD : U3FWJ44N (TOSHIBA)

OPERATIONAL EXPLANATION

Step-down DC/DC converter controllers of the XC9201series carry out pulse width modulation (PWM) according to the multiple feedback signals of the output voltage and coil current.

The internal circuits consist of different blocks that operate at VIN or the stabilized power (2.0 V) of the internal regulator. The output setting voltage of type C controller and the FB pin voltage (Vref = 0.9 V) of type D controller have been adjusted and set by laser-trimming.

<Clock>

With regard to clock pulses, a capacitor and resistor connected to the CLK pin generate ramp waveforms whose top and bottom are 0.7 V and 0.15 V, respectively. The frequency can be set within a range of 100 to 600 kHz externally (refer to the "Functional Settings" section for further information). The clock pulses are processed to generate a signal used for synchronizing internal sequence circuits.

<Verr amplifier>

The Verr amplifier is designed to monitor the output voltage. A fraction of the voltage applied to internal resistors R1, R2 in the case of a type C controller, and the voltage of the FB pin in the case of a type D controller, are fed back and compared with the reference voltage. In response to feedback of a voltage lower than the reference voltage, the output voltage of the Verr amplifier increases.

The output of the Verr amplifier enters the mixer via resistor (RVerr). This signal works as a pulse width control signal during PWM operations. By connecting an external capacitor and resistor through the CE/GAIN pin, it is possible to set the gain and frequency characteristics of Verr amplifier signals (refer to the "Functional Settings" section for further information)

<Ierr amplifier>

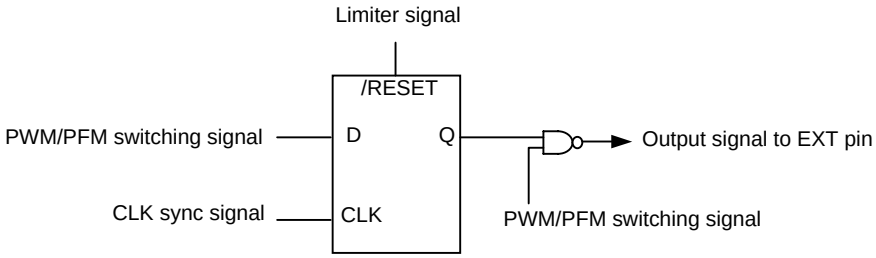
The Ierr amplifier monitors the coil current. The potential difference between the VIN and Isen pins is sampled at each switching operation. Then the potential difference is amplified or held, as necessary, and input to the mixer. The Ierr amplifier outputs a signal ensuring that the greater the potential difference between the VIN and Isen pins, the smaller the switching current. The gain and frequency characteristics of this amplifier are fixed internally.

<Mixer and PWM>

The mixer modulates the signal sent from Verr by the signal from Ierr. The modulated signal enters the PWM comparator for comparison with the sawtooth pulses generated at the CLK pin. If the signal is greater than the sawtooth waveforms, a signal is sent to the output circuit to turn on the external switch.

<Current Limiter>

The current flowing through the coil is monitored by the limiter comparator via the VIN and Isen pins. The limiter comparator outputs a signal when the potential difference between the VIN and Isen pins reaches 150 mV or more. This signal is converted to a logic signal and handled as a DFF reset signal for the internal limiter circuit. When a reset signal is input, a signal is output immediately at the EXT pin to turn off the MOS switch. When the limiter comparator sends a signal to enable data acceptance, a signal to turn on the MOS switch is output at the next clock pulse. If at this time the potential difference between the VIN and Isen pins is large, operation is repeated to turn off the MOS switch again. DFF operates in synchronization with the clock signal of the CLK pin.



<Soft Start>

The soft start function is made available by attaching a capacitor and resistor to the CE/SS pin. The Vref voltage applied to the Verr amplifier is restricted by the start-up voltage of the CE/SS pin. This ensures that the Verr amplifier operates with its two inputs in balance, thereby preventing the ON-TIME signal from becoming stronger than necessary. Consequently, soft start time needs to be set sufficiently longer than the time set to CLK. The start-up time of the CE/SS pin equals the time set for soft start (refer to the "Functional Settings" section for further information).
The soft start function operates when the voltage at the CE/SS pin is between 0V to 1.55V. If the voltage at the CE/SS pin doesn't start from 0V but from a mid level voltage when the power is switched on, the soft start function will become ineffective and the possibilities of large inrush currents and ripple voltages occurring will be increased.
Undervoltage Lock Out (U.V.L.O.) is also provided. This function is activated to turn off the MOS switch attached to the EXT pin when the input voltage (VIN) decreases to approximately 1.4 V or below. The purpose of this function is to keep the external MOS switch from turning on when a voltage at which the IC operates unstably is applied. U.V.L.O. also restricts signals during soft start so that the external MOS switch does not turn on until the internal circuitry becomes stable.

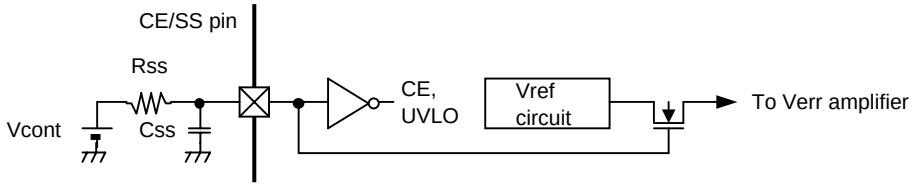
■ FUNCTIONAL SETTINGS

1. Soft Start

CE and soft start (SS) functions are commonly assigned to the CE/SS pin. The soft start function is effective until the voltage at the CE pin reaches approximately 1.55 V rising from 0 V. Soft start time is approximated by the equation below according to values of Vcont, RSS, and CSS.

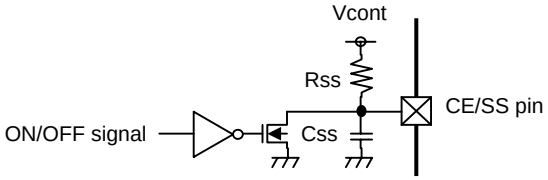
T = -CSS x RSS x ln ((Vcont - 1.55) / Vcont)

Example: When CSS = 0.1 μF, RSS = 470 kΩ, and Vcont = 5 V, T = -0.1 e^{-6} x 470 e^{3} x ln ((5 - 1.55) / 5) = 17.44 ms.

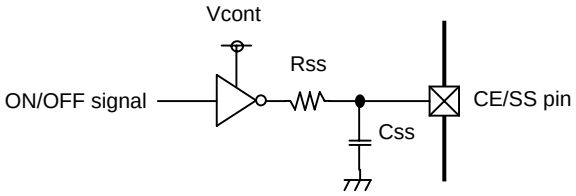


Set the soft start time to a value sufficiently longer than the period of a clock pulse.

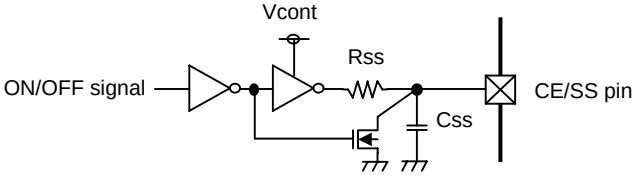
> Circuit example 1: Nch open drain



> Circuit example 2: CMOS logic (low current dissipation)



> Circuit example 3: CMOS logic (low current dissipation), quick off



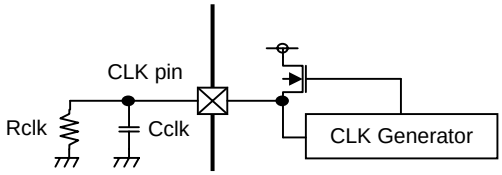
■ FUNCTIONAL SETTINGS (Continued)

2. Oscillation Frequency

The oscillation frequency of the internal clock generator is approximated by the following equation according to the values of the capacitor and resistor attached to the CLK pin. To stabilize the IC's operation, set the oscillation frequency within a range of 100kHz to 600kHz. Select a value for Cclk within a range of 180pF to 300pF and fix the frequency based on the value for Rclk.

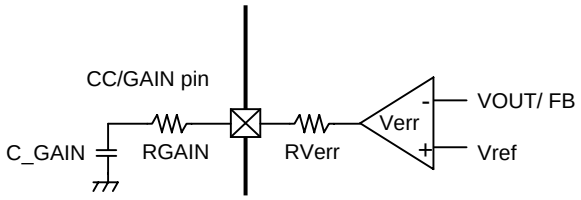
$$\mathbf{f = 1 / (-Cclk \times Rclk \times \ln 0.26)}$$

Example: When Cclk = 220 pF and Rclk = 10 kΩ, $f = 1/(-220e^{-12} \times 10e^{3} \times \ln(0.26)) = 337.43$ kHz.



3. Gain and Frequency Characteristics of the Verr Amplifier

The gain at output and frequency characteristics of the Verr amplifier are adjusted by the values of capacitor and resistor attached to the CC/GAIN pin. It is generally recommended to attach a C_GAIN of 220 to 1,000 pF without an R_GAIN. The greater the C_GAIN value, the more stable the phase and the slower the transient response. When using the IC with R_GAIN connected, it should be noted that if the R_GAIN resistance value is too high, abnormal oscillation may occur during transient response time. The size of R_GAIN should be carefully determined and connected.

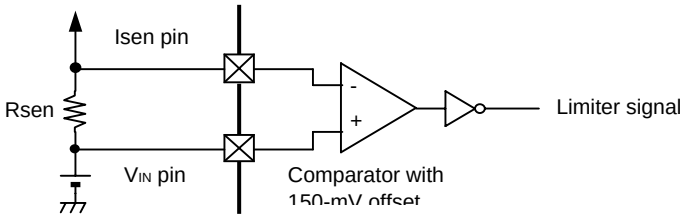


4. Current Limiting

The current limiting value is approximated by the following equation according to resistor RSEN inserted between the VIN and ISEN pins. Double function, current FB input and current limiting, is assigned to the ISEN pin. The current limiting value is approximated by the following equation according to the value for RSEN.

$$ILpeak\_limit = 0.15 / RSEN$$

Example: When RSEN = 100 mΩ, ILpeak_limit = 0.15 / 0.1 = 1.5 A



Because of the feedback at the internal error amp with this IC (which is brought about as a result of the phase compensation of the voltage generated at RSEN, which is in turn caused by current flowing through the coil when the PMOS is working.), should the value of the RSEN resistor be too large, the feedback signal will also increase and intermittent oscillation may occur. We therefore recommend that you carefully check the value for RSEN should you have a problem with oscillation. During normal operations, a voltage will be generated at RSEN as a result of the coil's peak current. Please ensure that this voltage is less than the current limit voltage which is 90mV (min.). For RSEN resistor's rated power, please refer to the note on the RSEN resistor on page 18.

■ FUNCTIONAL SETTINGS (Continued)

5. FB Voltage and Cfb

With regard to the XC9201D series, the output voltage is set by attaching externally divided resistors. The output voltage is determined by the equation shown below according to the values of Rfb1 and Rfb2. In general, the sum of Rfb1 and Rfb2 should be 1 MΩ or less.

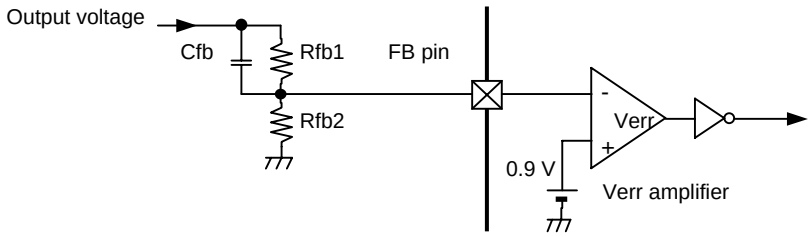
$$VOUT = 0.9 \times (Rfb1 + Rfb2)/Rfb2$$

The value of Cfb (phase compensation capacitor) is approximated by the following equation according to the values of Rfb1 and fzfb. The value of fzfb should be 10 kHz, as a general rule.

$$Cfb = 1/(2 \times \pi \times Rfb1 \times fzfb)$$

Example: When Rfb1 = 455 kΩ and Rfb2 = 100 kΩ : VOUT = 0.9 x (455 k + 100 k)/100 k = 4.995 V

:Cfb = 1/(2 x π x 455 k x 10 k) = 34.98 pF.



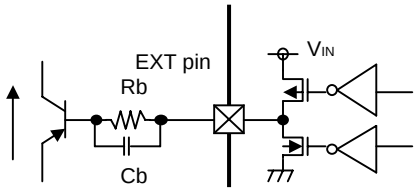
■ APPLICATION NOTES

1. The 9201 series are designed for use with an output ceramic capacitor. If, however, the potential difference between input and output is too large, a ceramic capacitor may fail to absorb the resulting high switching energy and oscillation could occur on the output side. If the input-output potential difference is large, connect an electrolytic capacitor in parallel to compensate for insufficient capacitance.

2. The EXT pin of the XC9201 series is designed to minimize the through current that occurs in the internal circuitry. However, the gate drive of external PMOS has a low impedance for the sake of speed. Therefore, if the input voltage is high and the bypass capacitor is attached away from the IC, the charge/discharge current to the external PMOS may lead to unstable operations due to switching operation of the EXT pin.

   As a solution to this problem, place the bypass capacitor as close to the IC as possible, so that voltage variations at the VIN and VSS pins caused by switching are minimized. If this is not effective, insert a resistor of several to several tens of ohms between the EXT pin and PMOS gate. Remember that the insertion of a resistor slows down the switching speed and may result in reduced efficiency.

3. A PNP transistor can be used in place of PMOS. If using a PNP transistor, insert a resistor (Rb) and capacitor (Cb) between the EXT pin and the base of the PNP transistor in order to limit the base current without slowing the switching speed. Adjust Rb in a range of 500Ω to 1kΩ according to the load and hFE of the transistor. Use a ceramic capacitor for Cb, complying with $Cb \leq 1/(2 \times \pi \times Rb \times Fosc \times 0.7)$, as a rule.



4. This IC incorporates a limit comparator to monitor the voltage produces across the RSEN resistor at the current peak of the coil. It functions as a limiter when, for example, the output is short-circuited. In such a case, the limit comparator senses that the voltage across the RSEN resistor has reached a current-limiting voltage (typically 150mV) and outputs a signal to turn off the external transistor. After sensing a current-limiting voltage, the limit comparator typically takes 200nsec before it turns off the external resistor. During this time, the voltage across the RSEN resistor can exceed the current-limiting voltage, especially when the difference between the input voltage and the output voltage is large and the coil inductance is small. Therefore, exercise great care in selecting absolute maximum ratings of the external transistor, coil, and Schottky diode.

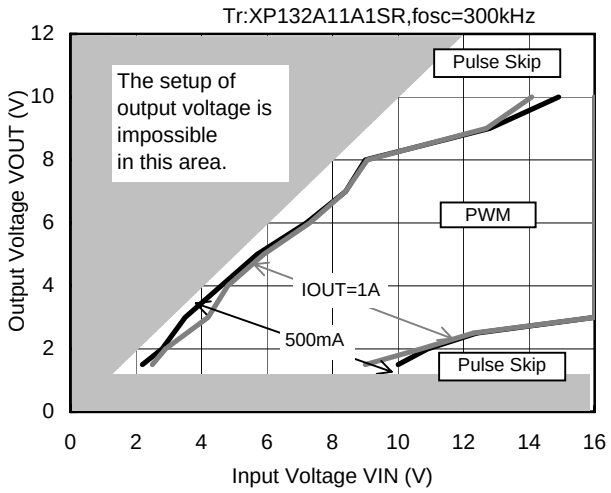
5. If the difference between the input voltage and the output voltage is large or small, the switching ON time or OFF time of this IC becomes short and actual operation can be critically influenced by values of peripheral components 'inductance of coil, resistance of CLK connection, capacitance of capacitor, etc.) Before use, it is recommended to evaluate this IC thoroughly with an actual unit.

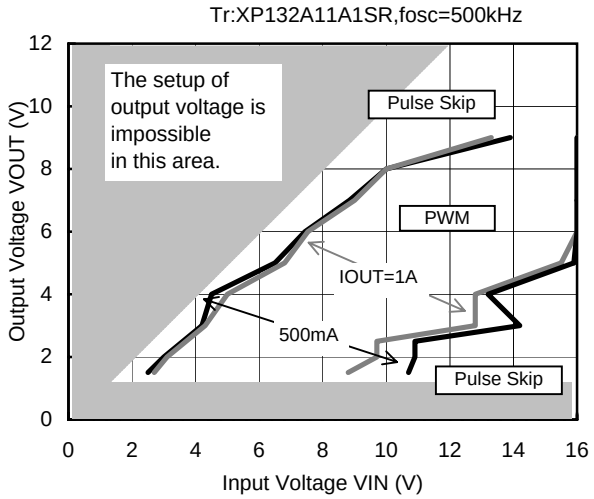
■ APPLICATION NOTES (Continued)

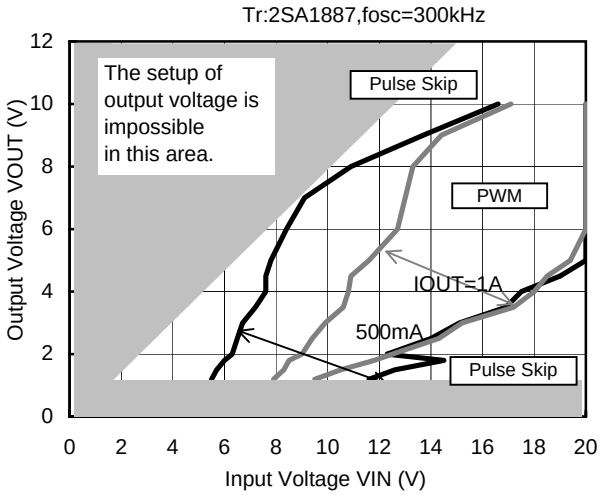
6. The series are designed to operate in PWM control. However, there is the possibility that some cycles may be skipped depending on the operational conditions. Please use the following output voltage vs. input voltage characteristics for reference. Verification using actual devices is recommended. It should be noted that when CCLK is connected to VIN, the influence of noise is lessened and the input and output voltage ranges as well as the output current range in which stable operation is possible is widened. It is recommended that you refer to the "Oscillation Frequency" Functional Settings (page 13) for setting up the oscillation frequency. If using a MOSFET, please pay particular attention to the gate breakdown voltage. In the following graphs, because the gate breakdown voltage of the MOSFET used was 20V, input voltages over 16V were not measured. Please use a bipolar transistor in applications where higher input voltages are required.

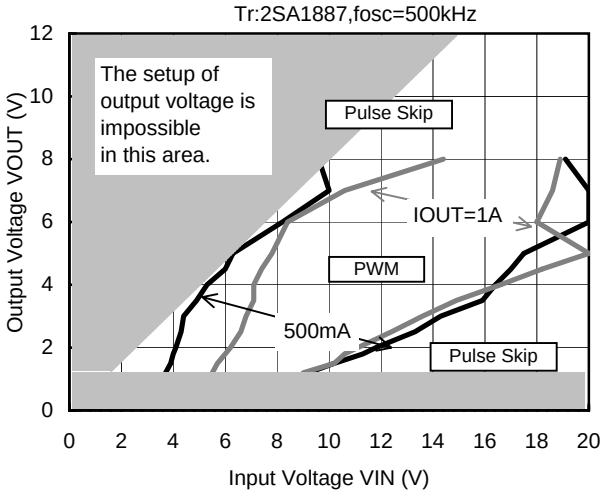
● Operational Control Characteristics

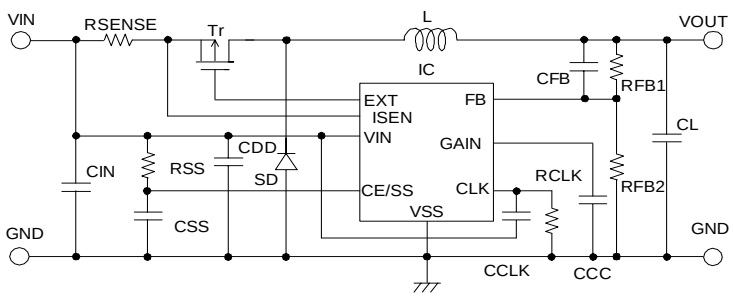
❍ XC9201D09AKR CCLK VIN Connection









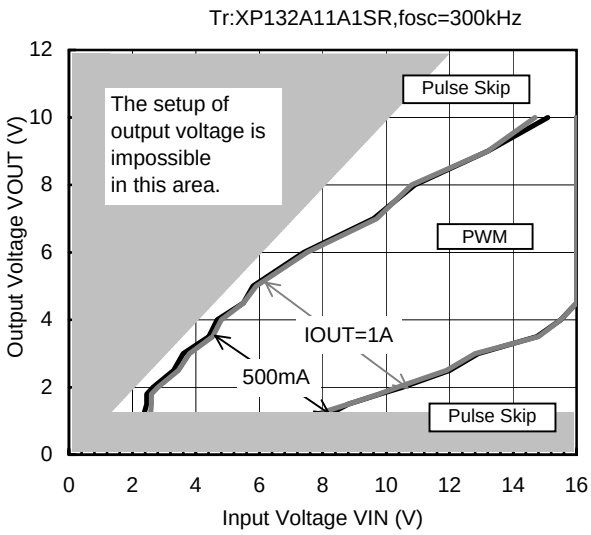


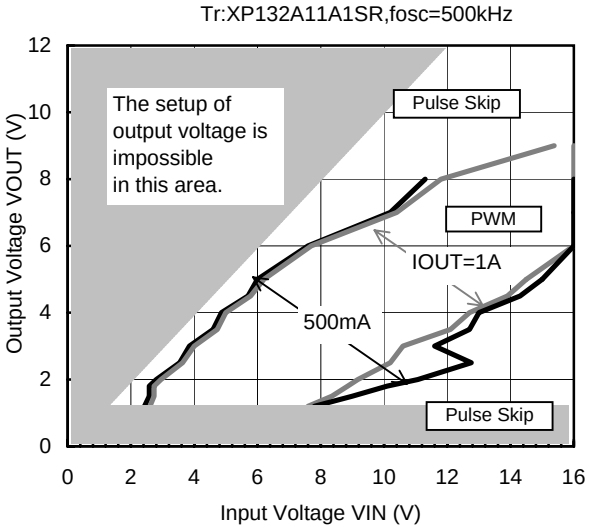
CCLK VIN Connection Circuit

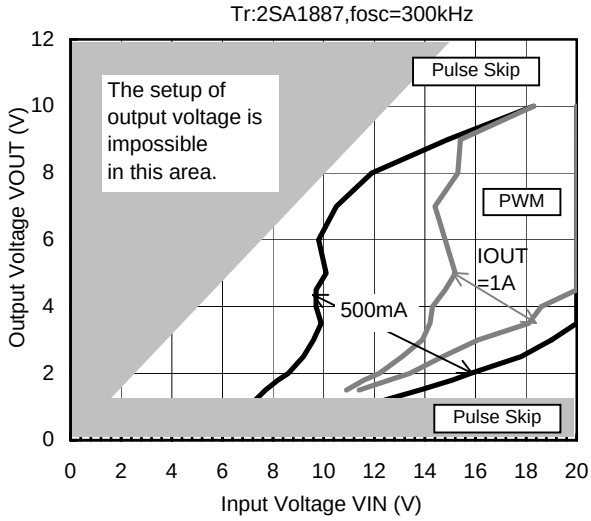
SD : D1FH3
L : CDRH127 / LD-220 (22uH)
CIN : TMK432BJ106KM (25V / 10uF) x 3
CL : JMK325BJ226MM (6.3V / 22uF) x 3
CDD : UMK325BJ105KH (50V / 1uF)
RSEN : 50mΩ
RCLK : 11kΩ (300kHz), 6.8KΩ (500kHz)
CCLK : 220pF
CCC : 330pF
RCC : 0Ω
RB (2SA1887) : 7kΩ (300kHz), 16kΩ (500kHz)
RSS : 1MΩ
CSS : 0.1uF
RFB1 : 330kΩ
CFB : 47pF

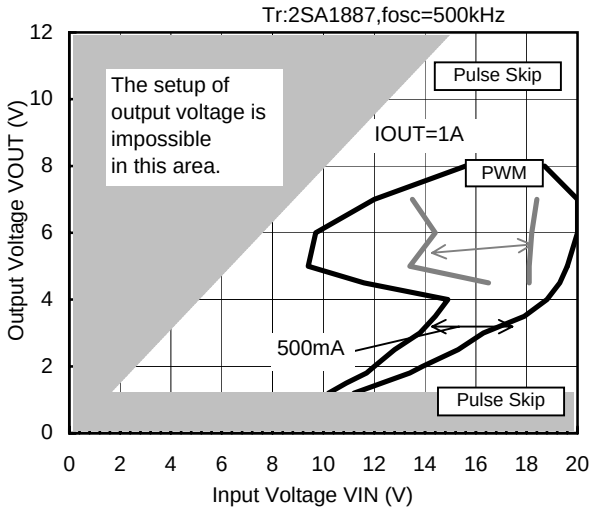
● Operational Control Characteristics (Continued)

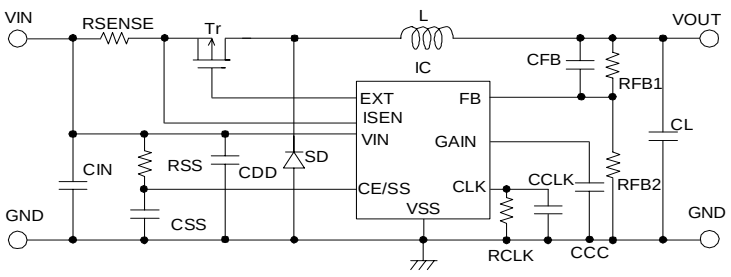
❍ XC9201D09AKR CCLK GND Connection











CCLK GND Connecton Circuit

SD : D1FH3
L : CDRH127 / LD-220 (22uH)
CIN : TMK432BJ106KM (25V / 10uF) x 3
CL : JMK325BJ226MM (6.3V / 22uF) x 3
CDD : UMK325BJ105KH (50V / 1uF)
RSEN : 50mΩ
RCLK : 11kΩ (300kHz), 6.8KΩ (500kHz)
CCLK : 220pF
CCC : 330pF
RCC : 0Ω
RB (2SA1887) : 7kΩ (300kHz), 16kΩ (500kHz)
RSS : 1MΩ
CSS : 0.1uF
RFB1 : 330kΩ
CFB : 47pF

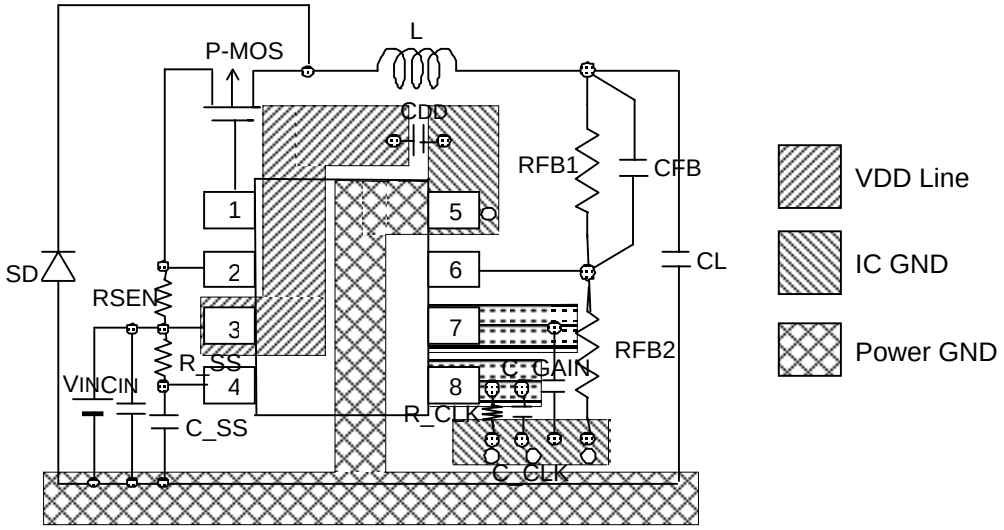
■ RECOMMENDED PATTERN LAYOUT

① In order to stabilize VDD's voltage level, we recommend that a by-pass condenser (CDD) be connected as close as possible to the VIN & VSS pins.

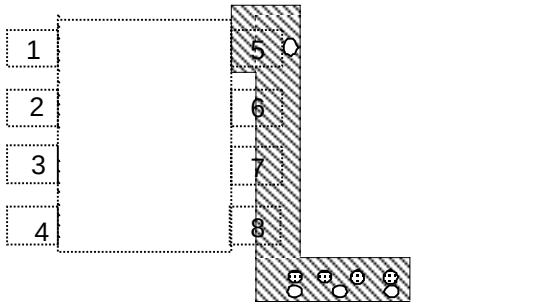
② In order to stabilize the GND voltage level which can fluctuate as a result of switching, we suggest that C_CLK's, R_CLK's & C_GAIN's GND be separated from Power GND and connected as close as possible to the VSS pin (by-pass condenser, CDD). Please use a multi layer board and check the wiring carefully.

Pattern Layout Examples XC9201D Series

2 layer Evaluation Board



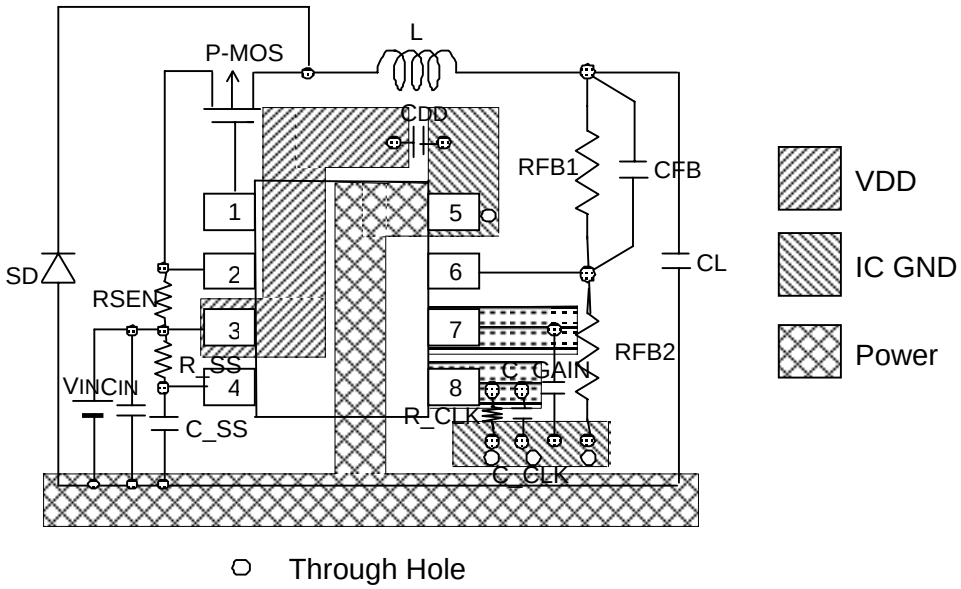
○ Through Hole



○ Through Hole

RECOMMENDED PATTERN LAYOUT (Continued)

1 layer Evaluation Board



Ensure that the absolute maximum ratings of the external components and the XC9201 DC/DC IC itself are not exceeded. We recommend that sufficient counter measures are put in place to eliminate the heat that may be generated by the external P-MOSFET as a result of switching losses.

Try to use a P-MOSFET with as small a gate capacitance as possible in order to avoid overly large output spike voltages that may occur (such spikes occur in proportion to gate capacitance). The performance of the XC9201 DC/DC converter is greatly influenced by not only its own characteristics, but also by those of the external components it is used with. We recommend that you refer to the specifications of each component to be used and take sufficient care when selecting components.

Wire external components as close to the IC as possible and use thick, short connecting wires to reduce wiring impedance. In particular, minimize the distance between the by-pass capacitor and the IC.

Make sure that the GND wiring is as strong as possible as variations in ground potential caused by ground current at the time of switching may result in unstable operation of the IC. Specifically, strengthen the ground wiring in the proximity of the VSS pin.

EXTERNAL COMPONENTS

RSENSE Resistor

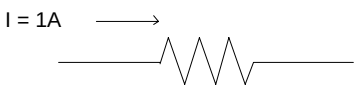
A low value resistor is defined as a resistor with a 10Ω value or lower. For RSENSE, the XC9201 series uses a resistor with a value of either 50mΩ or 100mΩ. Although resistors for RSENSE are classified as low resistance chip resistors or current limit resistors (which may give the impression that the RSENSE resistor is expensive), it is not necessary to use expensive low resistance chip resistors as general purpose chip resistors with values of 50mΩ or 100mΩ will do the job just as well.

When choosing the RSENSE resistor, it is important to confirm the resistor's power consumption which can be done using the following equation:

W (Power Consumption) =I (Current) x V (Voltage)
=I (Current) x I (Current) x R (Resistance)

It is recommended that a resistor which has a power rating of more than 3 times the power consumption of RSENSE be selected (refer to the example given below) :

(ex.) RSENSE = 100mΩ, I = 1A

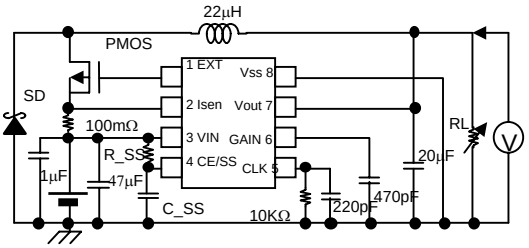


RSENSE = 100mΩ (0.1Ω)

Power supply W = 1 x 1 x 0.1 = 0.1 [W] 0.5Ω, 100mΩ resistor should be used

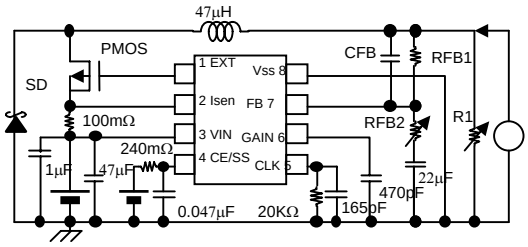
■ TEST CIRCUITS

Circuit ① (VOUT Type)

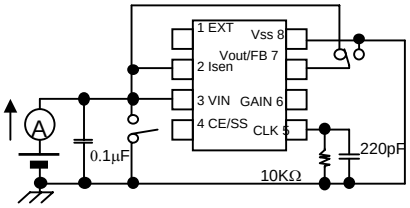


XC9201C25A	R_SS	: 188kΩ	C_SS	: 0.1μF
XC9201C33A	R_SS	: 270kΩ	C_SS	: 0.1μF
XC9201C50A	R_SS	: 430kΩ	C_SS	: 0.1μF

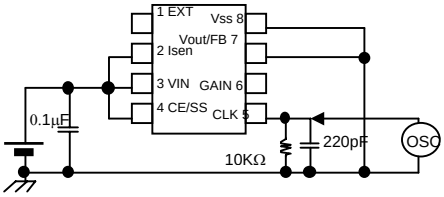
Circuit ① (FB Type)



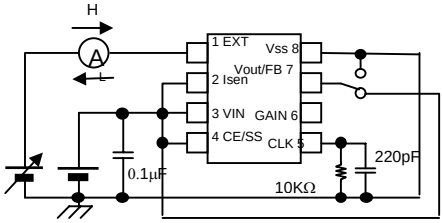
Circuit ②



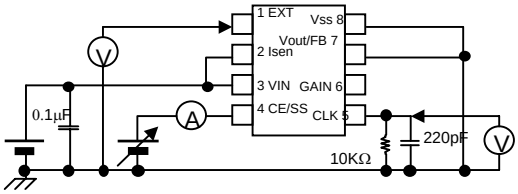
Circuit ③



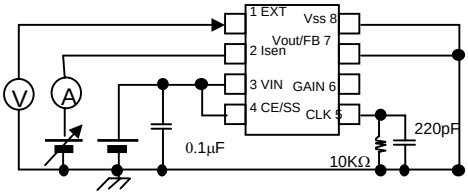
Circuit ④



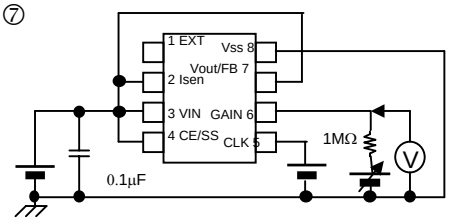
Circuit ⑤



Circuit ⑥



Circuit ⑦



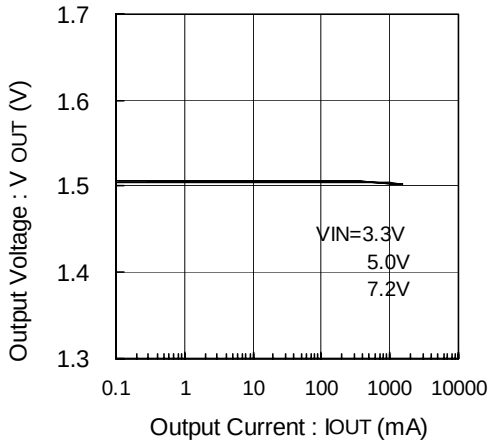
■ TYPICAL PERFORMANCE CHARACTERISTICS

XC9201D09AKR

(1) Output Voltage vs. Output Current

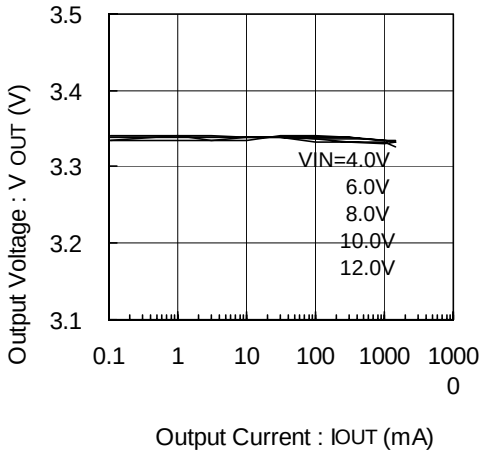
VOUT 1.5V, FOSC : 330kHz

L=22μH, CL=40μF (Ceramic), CIN=30μF (Ceramic)
RSEN=50mΩ, CDD=1μF (Ceramic), SD:U3FWJ44N
CGAIN=470pF (Ceramic), Tr:XP162A11C0PR



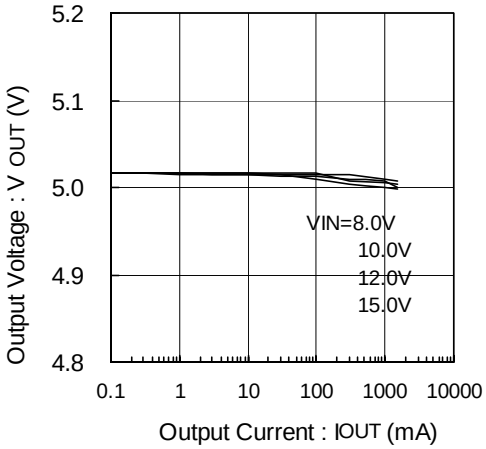
VOUT 3.3V, FOSC : 330kHz

L=22μH, CL=40μF (Ceramic), CIN=30μF (Ceramic)
RSEN=50mΩ, CDD=1μF (Ceramic), SD:U3FWJ44N
CGAIN=470pF (Ceramic), Tr:XP162A11C0PR



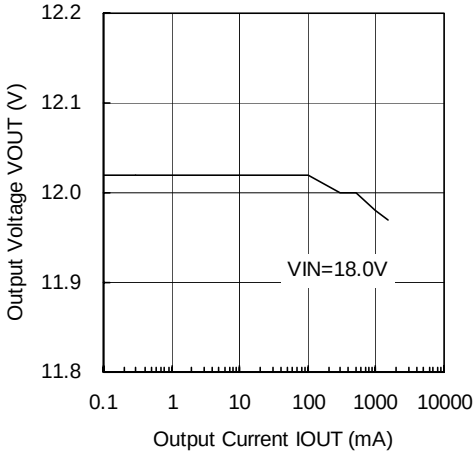
VOUT 5.0V, FOSC : 330kHz

L=22μH, CL=40μF (Ceramic), CIN=30μF (Ceramic)
RSEN=50mΩ, CDD=1μF (Ceramic), SD:U3FWJ44N
CGAIN=470pF (Ceramic), Tr:XP162A11C0PR



VOUT 12.0V, FOSC : 100kHz

L=68uH,CL=40uF(ceramic),CIN=30uF(ceramic)
RSEN=50mΩ,CDD=10uF(ceramic),SD:U3FWJ44N
CGAIN=470pF(ceramic),Tr:XP132A11A1SR



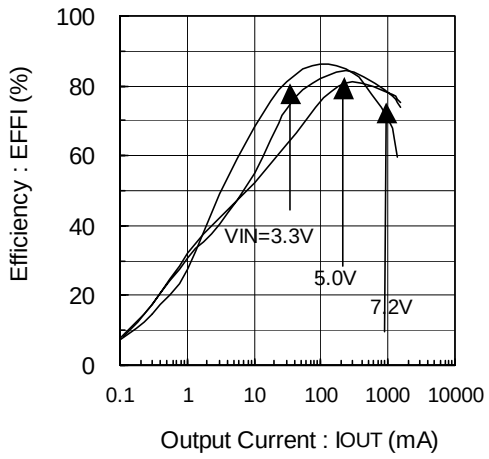
■ **TYPICAL PERFORMANCE CHARACTERISTICS (Continued)**

XC9201D09AKR

(2) Efficiency vs. Output Current

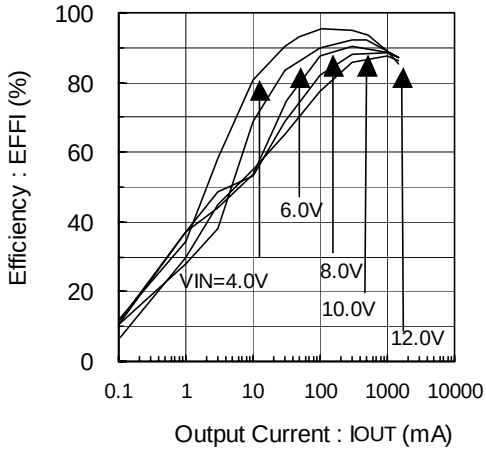
VOUT 1.5V, FOSC : 330kHz

L=22μH, CL=40μF (Ceramic), CIN=30μF (Ceramic)
RSEN=50mΩ, CDD=1μF (Ceramic), SD:U3FWJ44N
CGAIN=470pF (Ceramic), Tr:XP162A11C0PR



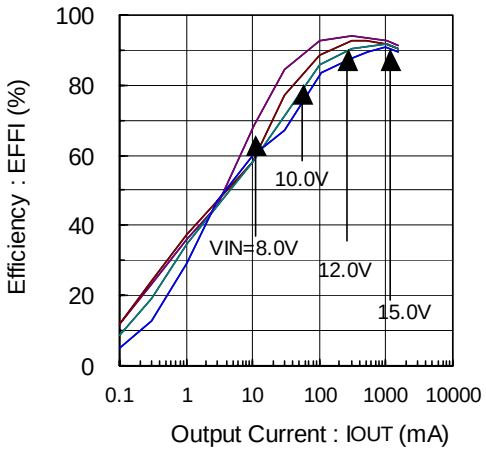
VOUT 3.3V, FOSC : 330kHz

L=22μH, CL=40μF (Ceramic), CIN=30μF (Ceramic)
RSEN=50mΩ, CDD=1μF (Ceramic), SD:U3FWJ44N
CGAIN=470pF (Ceramic), Tr:XP162A11C0PR



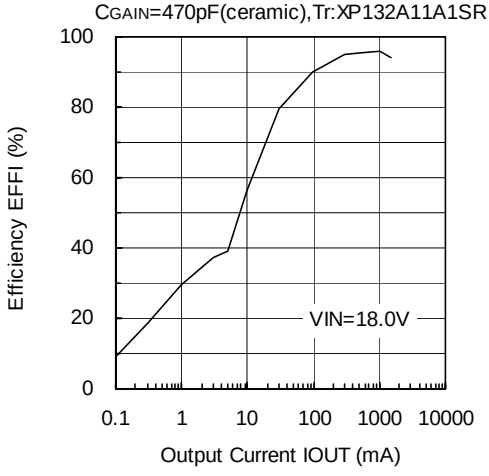
VOUT 5.0V, FOSC : 330kHz

L=22μH, CL=40μF (Ceramic), CIN=30μF (Ceramic)
RSEN=50mΩ, CDD=1μF (Ceramic), SD:U3FWJ44N
CGAIN=470pF (Ceramic), Tr:XP162A11C0PR



VOUT 12.0V, FOSC : 100kHz

L=68uH,CL=40uF(ceramic),CIN=30uF(ceramic)
RSEN=50mΩ,CDD=10uF(ceramic),SD:U3FWJ44N
CGAIN=470pF(ceramic),Tr:XP132A11A1SR



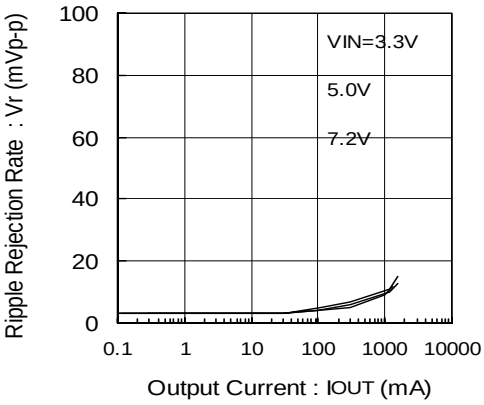
■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

XC9201D09AKR

(3) Ripple Rejection Rate vs. Output Current

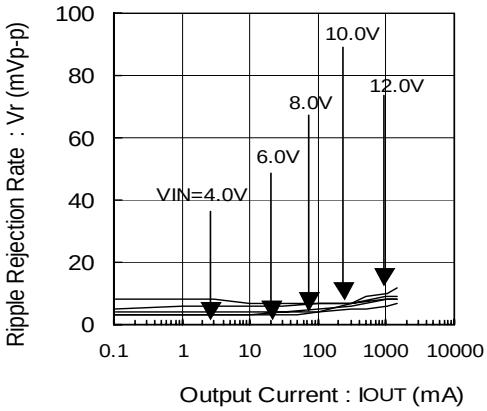
VOUT 1.5V, FOSC : 330kHz

L=22μH, CL=40μF (Ceramic), CIN=30μF (Ceramic)
RSEN=50mΩ, CDD=1μF (Ceramic), SD:U3FWJ44N
CGAIN=470pF (Ceramic), Tr:XP162A11C0PR



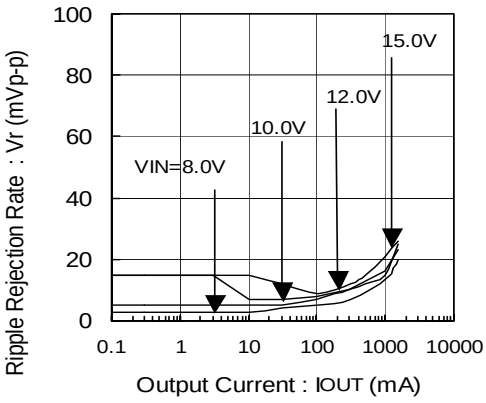
VOUT 3.3V, FOSC : 330kHz

L=22μH, CL=40μF (Ceramic), CIN=30μF (Ceramic)
RSEN=50mΩ, CDD=1μF (Ceramic), CD:U3FWJ44N
CGAIN=470pF (Ceramic), Tr:XP162A11C0PR



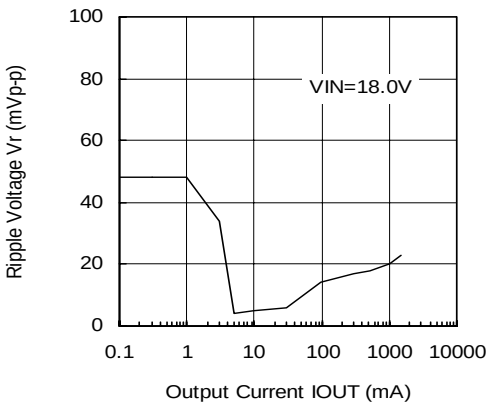
VOUT 5.0V, FOSC : 330kHz

L=22μH, CL=40μF (Ceramic), CIN=30μF (Ceramic)
RSEN=50mΩ, CDD=1μF (Ceramic), SD:U3FWJ44N
CGAIN=470pF (Ceramic), Tr:XP162A11C0PR



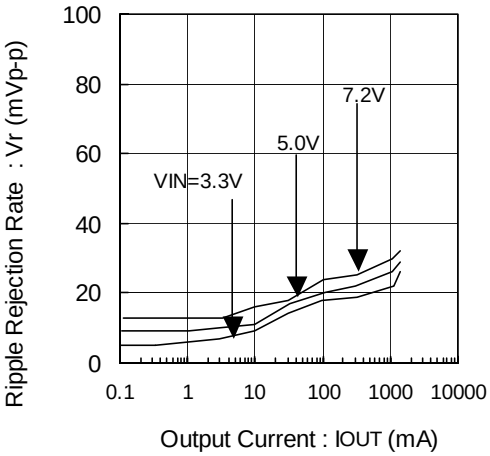
VOUT 12.0V, FOSC : 100kHz

L=68uH, CL=40uF(ceramic), CIN=30uF(ceramic)
RSEN=50mΩ, CDD=10uF(ceramic), SD:U3FWJ44N
CGAIN=470pF(ceramic), Tr:XP132A11A1SR



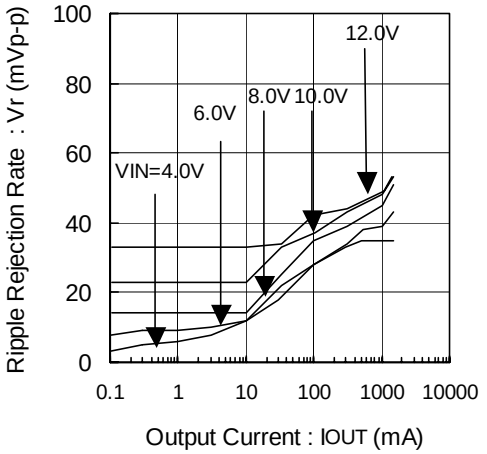
VOUT 1.5V, FOSC : 330kHz

L=22μH, CL=47μF (Tantalum), CIN=47μF (Tantalum)
RSEN=50mΩ, CDD=1μF (Ceramic), SD:U3FWJ44N
CGAIN=470pF (Ceramic), Tr:XP162A11C0PR



VOUT 3.3V, FOSC : 330kHz

L=22μH, CL=47μF (Tantalum), CIN=47μF (Tantalum)
RSEN=50mΩ, CDD=1μF (Ceramic), SD:U3FWJ44N
CGAIN=470pF (Ceramic), Tr:XP162A11C0PR



*Note: If the input and output voltage differential is large or small, the time of ON and Off switching will be shorten. This gives external components such as inductance value of coil, connecting a resistor to CLK, condenser, will critically influence the actual operation.