Application Note

AN2077/D
Rev. 1.2, 11/2001

Motorola RISC Microprocessor Design Checklist

Gary Milliorn
CPD Applications

This application note describes the generally recommended connections for new designs based on Motorola processors which implement the PowerPC architecture, as well as integrated embedded processors, and system controller logic for them. These devices include:

- MPC603, MPC603e, MPC603ev
- MPC740, MPC745, MPC750, MPC755
- MPC7400, MPC7410
- MPC7440, MPC7450
- MPC8240, MPC8241, MPC8245
- MPC107

The design checklist may also be applicable to bus- or footprint-compatible processors which may be introduced. It may also serve as a useful guide to debugging a newly-designed system, by highlighting those areas of a design which merit special attention during initial system startup.

The design checklist covers the following topics:

To locate any published errata or updates for this document, refer to the website at http://www.motorola.com/semiconductors.

1.1 Introduction

The Motorola processors that implement the PowerPC architecture, and the PCI bridge/memory controllers which operate with them, are all fairly easy to design to, as long as some simple rules are followed regarding connections and pullups.

For reference purposes, many designers may refer to the application notes and example/reference designs available on the Motorola website.

1.2 Connections

This section summarizes the connections and special conditions (such as pullups or pulldowns required) which may be needed for Motorola embedded/networking processors and corresponding system/memory controller logic (internal or external). Table 1 lists connections for the MPC603, MPC75x, MPC7400/MPC7410, MPC7450, and MPC824x microprocessors/microcontrollers, while Table 2 lists connections for the MPC8240, MPC8245 and MPC107 microcontrollers/system controllers. To keep the table compact, the cacheless variants (MPC740, MPC745 and MPC7440) are not listed in Table 1; instead, refer to the cache versions (MPC750, MPC755 and MPC7450) and ignore references to the L2 interface. The older MPC604 and MPC106 devices are also not listed; the MPC603 and MPC107 entries are very similar and can be used instead.

In the tables, if a connection to a specific signal is not named, it may be one of the following terms:

- xx-yyΩ OVDD — A pullup resistor to the OVDD power supply, with a value between xx and yy ohms. The choice of value may be selected by the designer, based upon system requirements such as noise immunity and the ability to share pullups.
- xx-yyΩ GND — A pulldown resistor to the ground power connection, with a value between xx and yy ohms. Again, the value may be specified by the designer.
- “open” — The signal may/should be left unconnected.
- “as needed” — The connection is determined principally by the system. It generally connects to the system controller logic, whether from Motorola or one of several third-parties who make such logic.

Lastly, some of the signals have a “critical” designation:

✋ — May cause complete failure; board will likely not operate if the signal is not properly connected.

This designator indicates signals which can cause system failure if not properly handled. If a new design is not running cycles (i.e., logic analyzer traces cannot be captured), the indicated signals should be checked first to narrow down possible problem sources. If these critical signals are not in the correct state, whether due to design or manufacturing error, the part may be improperly configured into a test mode and will not operate as desired.

As an example, consider transfer start ($\overline{TS}$). On an MPC107-based design, if a pullup is not present, $\overline{TS}$ may float low. Each device will wait for the (false) cycle to complete. A simple pullup insures that all devices sees an idle bus. Pullups or pulldowns may also be added to other signals without harm; it is not an error if a design has more pullups than might be minimally required. On several Motorola reference designs, pullups are added to some non-critical signals ($\overline{GBL}$, $\overline{TBST}$) in order to help logic analyzers present a more coherent picture of bus activity.

Table 1. Processor Connections

Critical	Signal	MPC603	MPC750	MPC755	MPC74X0	MPC745X	MPC824X	Connection		Notes
								if used	if not used	
	A[0:31]	✓	✓	✓	✓			as needed		Address bus may be pulled up to minimize sleep-mode power consumption; otherwise, pullups may be omitted. 74x0 in address bus drive mode (see EMODE) does not need pullups in either case.
	A[0:3]					✓		as needed	100-1KΩ GND	Extended address (MSBs). When not used (as with 32-bit logic), connect to pulldowns.
	A[4:35]					✓		to corresponding address pins		When used with 32-bit system bus logic (e.g. MPC107), connect CPU A(4:35) to device A(0:32).
✋	$\overline{\text{AACK}}$	✓	✓	✓	✓	✓		1K-5KΩ OVDD		Pullup needed to insure initial startup.
✋	$\overline{\text{ABB}}$	✓	✓	✓				1K-5KΩ OVDD		Not needed for MPC10x-based systems.
	$\overline{\text{ABB}}$/AMON0				✓			as needed	open	$\overline{\text{ABB}}$ is an output-only pin on the MPC74xx family. A pullup may be used where MPC75x/MPC74x0 footprint compatibility is needed.
	AP[0]					✓		as needed	1KΩ GND	If MPC7450 is operated in 32-bit address mode, AP0 is unused and should be pulled down to ground.
	AP[0:3] AP[1:4]	✓	✓	✓	✓	✓		as needed	1K-5KΩ OVDD	Address parity may be pulled up if unused to minimize sleep-mode power consumption; otherwise, pullups may be omitted.
	$\overline{\text{APE}}$	✓	✓	✓				1K-10KΩ OVDD	open	Open-drain output; pullup only if needed.
	$\overline{\text{ARTRY}}$	✓	✓	✓	✓	✓		1K-5KΩ OVDD		Pullup needed to insure initial startup.
✋	AVDD	✓	✓	✓	✓	✓	✓	filtered VDD		Must be connected to core voltage (VDD), not I/O (OVDD) through a 10 ohm resistor, with (2) 2.2uF ceramic caps on the AVDD pin. Trace lengths should be short, but do not need to be thick (~15mW typical). Avoid routing near noisy traces.
	$\overline{\text{BG}}$	✓	✓	✓	✓	✓		as needed	100-1KΩ GND	Pullup recommended for initial startup, or pulldown for permanently parked address bus.
✋	BMODE[0:1]					✓		as needed		Selects bus mode, address-bus-driven mode, and processor ID.
✋	$\overline{\text{BR}}$	✓	✓	✓	✓	✓		100-1KΩ OVDD		Pullup needed to insure initial startup.
✋	BVSEL				✓	✓		GND, $\overline{\text{HRESET}}$, OVDD		Connect BVSEL to: MPC755/7400/7410 — MPC745X GND — 1.8V OVDD — 1.8V OVDD HRESET — 2.5V OVDD — 2.5V OVDD OVDD — 3.3V OVDD — 2.5V OVDD or as described in the hardware specification.

Table 1. Processor Connections (Continued)

Critical	Signal	MPC603	MPC750	MPC755	MPC74X0	MPC745X	MPC824X	Connection		Notes
								if used	if not used	
	$\overline{\text{CHK}}$				✓			$\overline{\text{HRESET}}$	1K-5KΩ OVDD	Connect to $\overline{\text{HRESET}}$ to trigger a post-reset self-test. Usually not needed.
	$\overline{\text{CI}}$	✓	✓	✓	✓	✓		as needed	1K-5KΩ OVDD	$\overline{\text{CI}}$ may be pulled up to minimize sleep-mode power consumption; otherwise, pullup may be omitted.
✋	$\overline{\text{CKSTP\_IN}}$	✓	✓	✓	✓	✓	✓	1K-5KΩ OVDD		If $\overline{\text{CKSTP\_IN}}$ is not pulled up, the CPU will halt immediately. The $\overline{\text{CKSTP\_IN}}$ pullup may be shared with others if not used.
	$\overline{\text{CKSTP\_OUT}}$	✓	✓	✓	✓			1K-5KΩ OVDD	open	$\overline{\text{CKSTP\_OUT}}$ is an open-drain output.
	CLK_OUT	✓	✓	✓	✓	✓	✓	to testpoint	open	CLK_OUT is useful only for debugging, it cannot be used as a clock source.
	CSE[0:1]	✓						as needed	open	Output-only debug status; rarely used, connect to logic analyzer or float.
	$\overline{\text{DBB}}$	✓	✓	✓				1K-10KΩ OVDD		Not needed for MPC10x-based systems.
	$\overline{\text{DBB}}$/DMON0				✓					$\overline{\text{DBB}}$ is an output-only pin on the MPC74xx family. A pullup may be used where MPC75x/MPC74x0 footprint compatibility is needed.
	$\overline{\text{DBG}}$	✓	✓	✓	✓			as needed	100-1KΩ GND	Pullup recommended for initial startup, or pulldown for permanently parked data bus.
✋	$\overline{\text{DBDIS}}$	✓	✓	✓				1K-5KΩ OVDD		Rarely used signal; must be pulled up. Can be shared with other pullups.
✋	$\overline{\text{DBWO}}$	✓	✓	✓				1K-5KΩ OVDD		Rarely used signal; must be pulled up. Can be shared with other pullups.
	D[0:63] or DH[0:31] DL[0:31]	✓	✓	✓	✓	✓		as needed	open	Connect only to other CPUs, local-bus I/O and bridge devices. Memory is typically on an independent data bus (MDH/MDL). For 32-bit bus mode, if supported, DL(0:31) may be left open with no pullups required.
	DP[0:7]	✓	✓	✓	✓			as needed	open	Pullups are not needed if parity is unused.
	$\overline{\text{DPE}}$	✓	✓	✓				1K-5KΩ OVDD	open	Open-drain output; pullup only if needed.
	$\overline{\text{DRDY}}$				✓	✓		as needed	open	MPX bus mode output only.
✋	$\overline{\text{DRTRY}}$	✓	✓	✓				1-5KΩ OVDD	tie to HRESET	Tie $\overline{\text{DRTRY}}$ to $\overline{\text{HRESET}}$ to set NO-DRTRY mode. NO-DRTRY mode improves performance by eliminating an idle bus clock cycle after data transfers. $\overline{\text{DRTRY}}$ must not be tied to ground to enable NO-DRTRY mode.
	DTI[0:2] DTI[0:3]				✓	✓		as needed	100-1KΩ GND	MPX bus mode signals only; pulldowns insure strict ordering when in 60X bus mode.

Table 1. Processor Connections (Continued)

Critical	Signal	MPC603	MPC750	MPC755	MPC74X0	MPC745X	MPC824X	Connection		Notes
								if used	if not used	
	EMODE				✓			as needed	1K-5KΩ OVDD	Connect as follows: GND MPX bus mode with address bus drive mode. $\overline{\text{HRESET}}$ MPX bus mode OVDD 60X bus mode
	EXT_QUAL					✓		0-100Ω GND		$\overline{\text{Connect/pulldown to ground.}}$
	$\overline{\text{GBL}}$	✓	✓	✓	✓	✓		as needed + 200-500Ω OVDD		$\overline{\text{GBL}}$ should be strongly pulled up.
	$\overline{\text{HIT}}$				✓	✓		as needed	open	MPX bus mode output only.
✋	$\overline{\text{HRESET}}$ $\overline{\text{HRST\_CPU}}$	✓	✓	✓	✓	✓	✓	assert >= 255 bus clocks		A longer interval is acceptable, and may be needed for other devices such as the MPC10X.
✋	$\overline{\text{HRST\_CTRL}}$						✓	as needed		$\overline{\text{HRST\_CTRL}}$ should be tied to $\overline{\text{HRST\_CPU}}$.
	$\overline{\text{INT}}$	✓	✓	✓	✓	✓		1K-5KΩ OVDD		Pullup may be shared with others if $\overline{\text{INT}}$ not used.
✋	L1_TSTCLK	✓	✓	✓	✓				100 - 1KΩ OVDD	Use a strong pullup to keep noise from coupling to this pin. Do not share with other input-only pullups since asserting L1_TSTCLK during $\overline{\text{HRESET}}$ may be needed to correct errata on some devices.
						✓			100 - 1KΩ GND	Unlike other parts the MPC745X L1_TSTCLK must be connected to ground, or L3 will not work.
	L2ADDR[16:0]		✓	✓	✓			SRAM A[16:0]	open	The L2ADDR bus is little-endian, connect to similarly named SRAM address pins.
	L2ADDR17			✓	✓			SRAM A[17]	open	L2ADDR17 can be used for larger SRAM
	L2ASPARE				✓			SRAM A[18]	open	L2ASPARE may be used for larger SRAM
✋	L2AVDD		✓	✓	✓			filtered VDD		Must be connected to core voltage (VDD), not I/O (OVDD), through a 10 ohm resistor, with two 2.2uF ceramic caps on the AVDD pin. Trace lengths should be short and noise-free, but do not need to be thick (~15mW typical).
	$\overline{\text{L2CE}}$		✓	✓	✓			SRAM $\overline{\text{SE1}}$	open	Directly drives SRAM $\overline{\text{SE1}}$ pin. SE2 is typically tied high and $\overline{\text{SE3}}$ tied low.
	L2CLK_OUTA L2CLK_OUTB		✓	✓	✓			SRAM CLK	open	Traces must be point-to-point and equal length, equal to other SRAM trace lengths. For differential mode route using a split-T configuration.
	L2DATA[0:63]		✓	✓	✓			SRAM D[0:63]	open	L2 data bits can be rearranged to make routing better.
	L2DP[0:7]		✓	✓	✓			SRAM DP[0:7]	open	L2DP data bits can be rearranged to make routing better.

Table 1. Processor Connections (Continued)

Critical	Signal	MPC603	MPC750	MPC755	MPC74X0	MPC745X	MPC824X	Connection		Notes
								if used	if not used	
	L2SYNC_IN L2SYNC_OUT		✓	✓	✓			feedback		Connect L2SYNC_IN to L2SYNC_OUT with a trace length equal to that of the L2CLK_OUTA. If L2 is not used, the feedback loop is still required.
	L2VSEL				✓			GND, $\overline{\text{HRESET}}$, OVDD		Connect L2VSEL to: MPC755/7400/7410 GND 1.8V L2OVDD $\overline{\text{HRESET}}$ 2.5V L2OVDD OVDD 3.3V L2OVDD or as described in the hardware specification.
	L2_TSTCLK	✓	✓	✓	✓				100-1KΩ OVDD	Factory test pin only (has nothing to do with L2 interface).
						✓			to $\overline{\text{HRESET}}$	May also connect to pullup or pulldown.
	$\overline{\text{L2WE}}$		✓	✓	✓			SRAM $\overline{\text{SGW}}$	open	Directly drives SRAM $\overline{\text{SGW}}$ (global write) pin. $\overline{\text{SBW(AD)}}$ and $\overline{\text{SW}}$ are typically grounded.
	L2ZZ		✓	✓	✓			SRAM ZZ	open	Directly drives SRAM ZZ pin.
	L3VSEL					✓		GND, $\overline{\text{HRESET}}$, OVDD		Connect L3VSEL to: MPC745X GND 1.8V OVDD $\overline{\text{HRESET}}$ 2.5V OVDD OVDD 2.5V OVDD or as described in the hardware specification.
	L3ADDR[17:0]					✓		SRAM A[17:0]	open	The L3ADDR bus is little-endian, connect to similarly named SRAM address pins.
	L3_CLK[0:1]					✓		DDRSRAM: CK PBSRAM: K	open	One clock per SRAM device.
	$\overline{\text{L3\_CNTL0}}$					✓		DDRSRAM: B1 PBSRAM: $\overline{\text{SE1}}$	open	Function depends on SRAM type used.
	$\overline{\text{L3\_CNTL1}}$					✓		DDRSRAM: B2 PBSRAM: $\overline{\text{SGW}}$	open	Function depends on SRAM type used.
	L3DATA[0:63]					✓		SRAM D[0:63]	open	L3DATA[0:31] data bits may be rearranged to make routing more optimal, as may L3DATA[32:63]. Preserve the association between L3_ECHO_CLK[0:1] and L3DATA[0:31], and L3_ECHO_CLK[2:3] and L3DATA[32:63].

Table 1. Processor Connections (Continued)

Critical	Signal	MPC603	MPC750	MPC755	MPC74X0	MPC745X	MPC824X	Connection		Notes
								if used	if not used	
	L3DP[0:7]					✓		SRAM DP[0:7]	open	L3DP[0:3] and L3DP[4:7] data bits can be rearranged to make routing more optimal.
	L3_ECHO_ CLK[0:1]					✓		DDRSRAM: CQ PBSRAM: loop	open	For PBSRAM, connect L3_ECHO_CLK0 to L3_ECHO_CLK1, and match the trace length of L3_CLK0.
	L3_ECHO_ CLK[2:3]					✓		DDRSRAM: CQ PBSRAM: loop	open	For PBSRAM, connect L3_ECHO_CLK2 to L3_ECHO_CLK3, and match the trace length of L3_CLK1.
✋	$\overline{\text{LSSD\_MODE}}$	✓	✓	✓	✓	✓			100-1KΩ OVDD	Use a strong pullup to keep noise from coupling to this pin.
	$\overline{\text{MCP}}$	✓	✓	✓	✓	✓	✓	as needed	1K-5KΩ OVDD	Pullup may be shared with others if $\overline{\text{MCP}}$ not used.
✋	NC	✓	✓	✓	✓	✓	✓	open	open	Never connect anything to a NC pin unless it is defined on an upwardly compatible footprint (for upgrade purposes). For example, L2ADDR17 is NC on some BGA360 footprints; it is acceptable to connect this NC pad to an SRAM address line.
	PCI_SYNC_IN						✓	as needed		Clock input traces should match those for other PCI devices. Connect to PCICLK if PCI clock tree is not used.
✋	PLL_CFG[0:3]	✓	✓	✓	✓	✓		as needed		Pullups and pulldowns, jumpers to OVDD and GND, or digital logic may be used.
✋	PLL_CFG[0:4]						✓	as needed		Only pullups and pulldowns should be used. Jumpers to OVDD and GND, or digital logic, may be used only if debug mode is NEVER enabled.
✋	PLL_EXT					✓		as needed		Pullups and pulldowns, jumpers to OVDD and GND, or digital logic may be used. PLL_EXT is essentially the MSB of a 5-bit PLL encoding, or PLL_CFG[-1]. An alternate numbering scheme is to relabel the set {PLL_EXT, PLL_CFG[0:3]} as {PLL_CFG[0:4]} in that order.
	$\overline{\text{PMON\_IN}}$					✓		to event	1K-5KΩ OVDD	Performance monitor signal can be connected to any signal to measure.
	$\overline{\text{PMON\_OUT}}$					✓		as needed	open	Application-dependant.
	$\overline{\text{QACK}}$	✓	✓	✓	✓	✓	✓	1KΩ GND; or merge with $\overline{\text{HRESET}}$ logic	100-1KΩ GND	COP emulators require $\overline{\text{QACK}}$ asserted to single-step. 603 devices require $\overline{\text{QACK}}$ asserted during $\overline{\text{HRESET}}$ to prevent reduced-bus mode.
	$\overline{\text{QREQ}}$	✓	✓	✓	✓	✓		as needed	open	Output typically used only with MPC10X and/or COP interface.
	$\overline{\text{RSRV}}$	✓	✓	✓	✓			as needed	open	$\overline{\text{RSRV}}$ is a little-used output-only pin.
	SCK						✓	1K-3KΩ OVDD	open	SCK is open drain.

Table 1. Processor Connections (Continued)

Critical	Signal	MPC603	MPC750	MPC755	MPC74X0	MPC745X	MPC824X	Connection		Notes
								if used	if not used	
	SDA						✓	1K-3KΩ OVDD	open	SDA is open drain.
	$\overline{\text{SHD}}$[0:1]				✓	✓		1K-5KΩ OVDD		In 60X mode, $\overline{\text{SHD}}$ pins are ignored; pullup in all cases.
	$\overline{\text{SMI}}$	✓	✓	✓	✓	✓	✓	1K-5KΩ OVDD		Pullup may be shared with others if $\overline{\text{SMI}}$ not used.
	$\overline{\text{SRESET}}$	✓	✓	✓	✓	✓	✓	as needed	1K-5KΩ OVDD	$\overline{\text{SRESET}}$ need not be asserted during power-up reset.
✋	SYSCLK	✓	✓	✓	✓	✓		as needed		Clock input traces should match those for other PowerPC-bus devices.
✋	$\overline{\text{TA}}$	✓	✓	✓	✓	✓		1K-5KΩ OVDD		Pullup needed for initial startup.
	$\overline{\text{TBEN}}$	✓	✓	✓	✓	✓	✓	as needed	1K-5KΩ OVDD	May be pulled down to disable TBU/TBL/DEC registers (rarely useful).
	$\overline{\text{TBST}}$	✓	✓	✓	✓	✓		1K-5KΩ OVDD		Pullup needed for initial startup.
	TC[0:1]	✓						as needed	open	TC outputs indicate data vs. instruction cycles for 603 only. Often used for logic analyzer headers (compare with $\overline{\text{WT}}$ for 75x/745x processors and TT[0] for 74x0 processors).
	TCK	✓	✓	✓	✓	✓	✓	as needed	open	TCK has a weak (>=20KΩ) internal pullup to OVDD.
	TDI	✓	✓	✓	✓	✓	✓	as needed	open	TDI has a weak (>=20KΩ) internal pullup to OVD.
	TDO	✓	✓	✓	✓	✓	✓	as needed	open	TDO has a weak (>=20KΩ) internal pullup to OVD.
✋	$\overline{\text{TEA}}$	✓	✓	✓	✓	✓		1K-5KΩ OVDD		Pullup needed for initial startup.
✋	$\overline{\text{TEST0}}$						✓		100-1KΩ OVDD	Use a strong pullup to keep noise from coupling to this pin.
✋	$\overline{\text{TEST[0:5]}}$					✓			100-1KΩ OVDD	Use a strong pullup to keep noise from coupling to this pin.
✋	$\overline{\text{TEST6}}$					✓			0-100Ω GND	Use a strong pulldown to keep noise from coupling to this pin.
	$\overline{\text{TLBISYNC}}$	✓	✓	✓				assert during HRESET if needed	1K-5KΩ OVDD	$\overline{\text{TLBISYNC}}$ selects 32-bit bus mode on 60X devices; assert during $\overline{\text{HRESET}}$ if needed. $\overline{\text{TLBISYNC}}$ must be pulled up on the MPC750. $\overline{\text{TLBISYNC}}$ on the MPC7400 is not supported, so pull it up.
	TMS	✓	✓	✓	✓	✓	✓	as needed	open	TMS has a weak (>=20KΩ) internal pullup.
✋	$\overline{\text{TRST}}$	✓	✓	✓	✓	✓	✓	actively drive with $\overline{\text{HRESET}}$, logically OR'ed with COP $\overline{\text{TRST}}$, if any		While $\overline{\text{TRST}}$ has a weak (>=20KΩ) internal pullup, do **not** leave it floating or pulled up. $\overline{\text{TRST}}$ must be asserted to initialize the boundary scan chain. If COP is not used, a pulldown is sufficient. If COP is used, use discrete logic to merge the COP $\overline{\text{TRST}}$ source and the target system $\overline{\text{HRESET}}$.
✋	$\overline{\text{TS}}$	✓	✓	✓	✓	✓		1K-5KΩ OVDD		Pullup needed for initial startup.

Table 1. Processor Connections (Continued)

Critical	Signal	MPC603	MPC750	MPC755	MPC74X0	MPC745X	MPC824X	Connection		Notes
								if used	if not used	
	TSIZ[0:2]	✓	✓	✓	✓	✓		as needed		TSIZ bus may be pulled up to minimize sleep-mode power consumption; otherwise, pullups may be omitted.
	TT[0:4]	✓	✓	✓	✓	✓		as needed		TT bus may be pulled up to minimize sleep-mode power consumption; otherwise, pullups may be omitted. TT0 indicates instruction vs. data information for debugging on MPC74x0.
	VOLTDET	✓	✓	✓				as needed	open	VOLTDET definition varies by device; may be connected to GND, OVDD, or VDD (core) depending on device and mask revision.
	$\overline{WT}$	✓	✓	✓	✓	✓		as needed	1K-5KΩ OVDD	$\overline{WT}$ may be pulled up to minimize sleep-mode power consumption; otherwise, pullup may be omitted. $\overline{WT}$ distinguishes instruction vs. data reads, for debugging on MPC7xxx series.

Table 2 lists only the memory/PCI/system controller signals of the devices, not the 60X bus signals (if any). For example, the MPC107 does not have an entry for the $\overline{TS}$ signal, since $\overline{TS}$ should already have been properly connected as described in Table 1, when the (required) PowerPC CPU is connected.

Table 2. Memory/PCI/System Controller Connections

Critical	Signal	MPC107	MPC8240	MPC8245	Connection		Notes
					if used	if not used	
	AD[31:0]	✓	✓	✓	as needed 1K-5KΩ LVDD	1K-5KΩ LVDD	Should be pulled up on a PCI motherboard or private PCI bus, but not on a plug-in peripheral card. If the PCI port is not used, the bus must be pulled up or the PCI bus parked.
	AVDD	✓	✓	✓	filtered VDD		Connect to core voltage (VDD not OVDD) through a 10 ohm resistor, with (2) 2.2uF ceramic capacitors. Trace lengths should be short, but do not need to be thick (~15mW typical).
	AVDD2		✓	✓	filtered VDD		Connect to core voltage (VDD not OVDD) through a 10 ohm resistor, with (2) 2.2uF ceramic capacitors. Trace lengths should be short, but do not need to be thick (~15mW typical).
	$\overline{C/BE[3:0]}$	✓	✓	✓	as needed 1K-5KΩ LVDD	1K-5KΩ LVDD	Should be pulled up on a PCI motherboard or private PCI bus, but not on a plug-in peripheral card. If PCI is not used, pull up (or park the PCI bus).
	CKE	✓	✓	✓	SDRAM CKE	open	Standard SDRAM control signal. If low-power is not a concern, CKE can be wired to '1' at the SDRAM device and the CKE can be left open.

Table 2. Memory/PCI/System Controller Connections (Continued)

Critical	Signal	MPC107	MPC8240	MPC8245	Connection		Notes
					if used	if not used	
✋	CPU_CLK[0:2]	✓			as needed	open	CPU_CLK signals must have trace length added to match any delay on the SDRAM_SYNC_OUT to SDRAM_SYNC_IN feedback path. Refer to the MPC107 Design Guide (AN1849) for details.
	$\overline{\text{CS}}$[0:7]	✓	✓	✓	SDRAM $\overline{\text{CS}}$	open	Standard SDRAM control signal. Each $\overline{\text{CS}}$[0:7] pin must control one 64-bit (or 32-bit) array of memory. Each SODIMM or DIMM will have one or two arrays of memory on it with one, two or four usable chip-selects. Standard wiring is: SODIMM (64 only): One $\overline{\text{CS}}$[0:7] to $\overline{\text{CS0}}$, second $\overline{\text{CS}}$[0:7] to $\overline{\text{CS1}}$. DIMM (as 64-bits): One $\overline{\text{CS}}$[0:7] to $\overline{\text{CS0}}$ and $\overline{\text{CS2}}$, second $\overline{\text{CS}}$[0:7] to $\overline{\text{CS1}}$ and $\overline{\text{CS3}}$. DIMM (as 32-bits): One $\overline{\text{CS}}$[0:7] to $\overline{\text{CS0}}$, second $\overline{\text{CS}}$[0:7] to $\overline{\text{CS2}}$, third $\overline{\text{CS}}$[0:7] to $\overline{\text{CS1}}$, fourth $\overline{\text{CS}}$[0:7] to $\overline{\text{CS3}}$.
	CTS1			✓	RS232 receiver	1K-5KΩ OVDD	RS232 signal: Clear to send.
	$\overline{\text{DEVSEL}}$	✓	✓	✓	as needed 1K-5KΩ LVDD	1K-5KΩ LVDD	Should be pulled up on a PCI motherboard or private PCI bus, but not on a plug-in peripheral card. If PCI is not used, pull up (or park the PCI bus).
	DQM[0:7]	✓	✓	✓	SDRAM DQ[0:7]	open	Each DQM must be associated with corresponding MDH/MDL byte lanes: DQM0⮜-⮞MDH[0:7] DQM1⮜-⮞MDH[8:15] DQM2⮜-⮞MDH[16:23] DQM3⮜-⮞MDH[24:31] DQM4⮜-⮞MDL[0:7] DQM5⮜-⮞MDH[8:15] DQM6⮜-⮞MDH[16:23] DQM7⮜-⮞MDH[24:31] If an 8-bit SDRAM device is attached to MDH[0:7], then DQM0 should be connected to the DQM pin, and so forth. Any parity SDRAM devices can use any DQM[0:7] signal (it will have to share).
	$\overline{\text{FOE}}$	✓	✓	✓	as needed	open	$\overline{\text{FOE}}$ is not needed if non-writable devices (PROM) is used for the boot code (or if the boot code is on PCI).
	$\overline{\text{FRAME}}$	✓	✓	✓	as needed 1K-5KΩ LVDD	1K-5K LVDD	Should be pulled up on a PCI motherboard or private PCI bus, but not on a plug-in peripheral card. If PCI is not used, pull up (or park the PCI bus).
	$\overline{\text{GNT}}$[4:0]	✓	✓	✓	as needed	GNT0: 1K-5KΩ LVDD, others open	If the arbiter is disabled, $\overline{\text{GNT0}}$ becomes “REQ” and should be pulled up on a PCI motherboard or private PCI bus.

Table 2. Memory/PCI/System Controller Connections (Continued)

Critical	Signal	MPC107	MPC8240	MPC8245	Connection		Notes
					if used	if not used	
✋	IDSEL	✓	✓	✓	one of AD[31:0]	GND	IDSEL should be connected to GND for host systems and to one address line of AD[31:0] for agent systems. If the PCI port is not used, it should be grounded.
	$\overline{\text{INTA}}$				as needed	open	In agent mode, $\overline{\text{INTA}}$ typically connects to a central interrupt controller. In host mode, $\overline{\text{INTA}}$ may be used to assert interrupts to other devices, such as a second processor.
	$\overline{\text{IRDY}}$	✓	✓	✓	as needed 1K-5KΩ LVDD	1K-5KΩ LVDD	Should be pulled up on a PCI motherboard or private PCI bus, but not on a plug-in peripheral card. If PCI is not used, pull up (or park the PCI bus).
	$\overline{\text{IRQ(0:4)}}$	✓	✓	✓	as needed 1K-5KΩ LVDD	1K-5KΩ LVDD	$\overline{\text{INT[0:4]}}$ should be pulled up on a PCI motherboard or private PCI bus, but not on a plug-in peripheral card.
✋	LAVDD	✓			filtered VDD		Connect to core voltage (VDD not OVDD) through a 10 ohm resistor, with (2) 2.2uF ceramic capacitors. Trace lengths should be short, but do not need to be thick (~15mW typical).
			✓	✓		open or AVDD	Internally connected to AVDD (pin C17).
	$\overline{\text{LOCK}}$	✓	✓	✓	as needed 1K-5KΩ LVDD	1K-5KΩ LVDD	Should be pulled up on a PCI motherboard or private PCI bus, but not on a plug-in peripheral card. If PCI is not used, pull up (or park the PCI bus).
	MAA[0:2]		✓	✓	to logic analyzer	open	MAA assists logic analyzers in recovering addressing information
	MDH[0:31] MDL[0:31]	✓	✓	✓	as needed		All flash, SDRAM/DRAM, and PortX I/O devices connect to MDH/MDL, not to the DH/DL processor data bus (if any).
	$\overline{\text{MIV}}$		✓	✓	to logic analyzer	open	$\overline{\text{MIV}}$ assists logic analyzers in recovering addressing information.
	OSC_IN	✓	✓	✓	PCI clock source	1K-5KΩ OVDD	OSC_IN recommended only for embedded host systems, not for PCI agent cards due to clock skew.
	PAR(0:7)	✓	✓	✓	as needed	open	All flash, SDRAM/DRAM, and I/O devices connect to PAR[0:7], not to the DH/DL processor data bus (if visible). For Flash and I/O, PAR[0:7] is used for addressing, not flash or I/O parity.
	PAR	✓	✓	✓	as needed 1K-5KΩ LVDD	1K-5K LVDD	PAR should be pulled up on a PCI motherboard or private PCI bus, but not on a plug-in peripheral card. If PCI is not used, pull up (or park the PCI bus).
	PCI_CLK[0:4]	✓	✓	✓	as needed	open	PCI clocks to target PCI devices should have equal lengths. If not used, disable clock drivers in the CDCR register.

Table 2. Memory/PCI/System Controller Connections (Continued)

Critical	Signal	MPC107	MPC8240	MPC8245	Connection		Notes
					if used	if not used	
✋	PCI_SYNC_IN	✓	✓	✓	3.3V PCICLK, local clock source or PCI_SYNC_OUT		PCI_SYNC_IN is the primary clock input for the chip, (OSC_IN is just a clock buffer). If the buffer is not used, the PCI clock "CLK" connects to PCI_SYNC_IN with the same consideration any other PCI clock gets: max of 2.0 ns skew on a motherboard, max 2.5" trace length on a plug-in card. If PCI_SYNC_IN is connected to a PCI backplane, the clock source must be 3.3V or restricted (pin is not 5V PCI compatible).
	PCI_SYNC_OUT	✓	✓	✓	PCI_SYNC_IN	open	PCI feedback path should have a trace length to PCI_SYNC_IN of equal lengths to other PCI device clocks.
	$\overline{\text{PERR}}$	✓	✓	✓	as needed 1K-5KΩ LVDD	1K-5KΩ LVDD	Should be pulled up on a PCI motherboard or private PCI bus, but not on a plug-in peripheral card. If PCI is not used, pull up (or park the PCI bus).
	PMAA[0:2]		✓	✓	to logic analyzer	open	PMAA assists logic analyzers in recovering addressing information
	$\overline{\text{RCS0}}$	✓	✓	✓	to boot ROM or 100-1KΩ pulldown	open	$\overline{\text{RCS0}}$ is used for reset startup code. A pulldown on RCS0 selects PCI boot mode.
	$\overline{\text{RCS1}}$	✓	✓	✓	as needed	open	Local ROM or PortX chip select.
	$\overline{\text{RCS[2:3]}}$	✓		✓	as needed	open	Local ROM or PortX chip select.
	$\overline{\text{REQ[4:0]}}$	✓	✓	✓	as needed 1K-10KΩ LVDD	1K-5KΩ LVDD	If the arbiter is enabled, $\overline{\text{REQ[4:0]}}$ should be pulled up on a PCI motherboard or private PCI bus. If PCI is not used, ground $\overline{\text{REQ0}}$ (which becomes $\overline{\text{GNT}}$) to park the PCI bus and maintain valid PCI state.
	RFC (RTC)			✓	to LF oscillator	open	Refresh clock is independent of all other clocks.
	RTS1			✓	RS232 driver	open	RS232 Request-To-Send output
	SCK	✓	✓	✓	1K-3KΩ OVDD	open	SCK is open drain.
	SDA	✓	✓	✓	1K-3KΩ OVDD	open	SDA is open drain.
	SDBA0	✓	✓	✓		open	Standard SDRAM address signal.
	SDBA1	✓	✓	✓		open	Standard SDRAM address signal.
	SDCAS	✓	✓	✓	SDRAM CKE	open	Standard SDRAM control signal.
	SDMA12/ SDBA1		✓		SDRAM A12 and/or SDBA1	open	Standard SDRAM address signal. Connects to SDBA1 or A12, depending on SDRAM size. For modules, connect to both A12 and SDBA1 pins.

Table 2. Memory/PCI/System Controller Connections (Continued)

Critical	Signal	MPC107	MPC8240	MPC8245	Connection		Notes
					if used	if not used	
	SDMA[11:0]	✓	✓	✓	SDRAM A[11:0]	open	Standard SDRAM address signal.
	SDMA[13:12]	✓		✓	SDRAM A[13:12]	open	Standard SDRAM address signal.
	SDMA14			✓	SDRAM A14	open	Standard SDRAM address signal.
✋	SDRAM_CLK [0:3]	✓	✓	✓	SDRAM CLK	open	Standard SDRAM clock signal. Clocks to the SDRAM should have equal-length traces, and generally match the trace length of the SDRAM.
✋	SDRAM_ SYNC_IN	✓	✓	✓	SDRAM_ SYNC_OUT		Connects to SDRAM_SYNC_OUT usually, except when zero-delay buffers are inserted between feedback path.
✋	SDRAM_ SYNC_OUT	✓	✓	✓	SDRAM_ SYNC_IN		SDRAM feedback path should have a trace length at least equal to that of SDRAM_CLK to SDRAM clock pin path lengths. Additional delay can be added to increase hold time for SDRAM modules (usually required).
	$\overline{\text{SDRAS}}$	✓	✓	✓	SDRAM CKE	open	Standard SDRAM control signal.
	$\overline{\text{SERR}}$	✓	✓	✓	as needed 1K-5KΩ LVDD	1K-5KΩ LVDD	Should be pulled up on a PCI motherboard or private PCI bus, but not on a plug-in peripheral card. If PCI is not used, pull up (or park the PCI bus).
	SIN1			✓	RS232 receiver	open	RS232 Received data.
	SOUT1			✓	RS232 driver	open	RS232 Transmitted data.
	$\overline{\text{STOP}}$	✓	✓	✓	as needed 1K-5KΩ LVDD	1K-5KΩ LVDD	Should be pulled up on a PCI motherboard or private PCI bus, but not on a plug-in peripheral card. If PCI is not used, pull up (or park the PCI bus).
✋	$\overline{\text{SUSPEND}}$	✓			1K-5KΩ OVDD		$\overline{\text{SUSPEND}}$ requires a pullup.
	$\overline{\text{TRDY}}$	✓	✓	✓	as needed 1K-5KΩ LVDD	1K-5KΩ LVDD	Should be pulled up on a PCI motherboard or private PCI bus, but not on a plug-in peripheral card. If PCI is not used, pull up (or park the PCI bus).
	TRIG_IN	✓		✓	TRIG_OUT	1K-5KΩ OVDD	TRIG_IN is usually connected to TRIG_OUT, or a logic analyzer.
	TRIG_OUT	✓		✓	TRIG_IN or CKSTP_IN	open	TRIG_OUT is usually connected to TRIG_IN, CKSTP_IN, or a logic analyzer.
	$\overline{\text{WE}}$	✓	✓	✓	as needed	open	$\overline{\text{WE}}$ is not needed if non-writable devices (PROM) is used for the boot code (or if the boot code is on PCI).

1.3 L2 Cache Pipelined/Late-Write SRAM Connections

The MPC750, MPC755 and MPC74X0 processors support a “backside” L2 cache on a private cache bus. For some devices this bus can act as a private memory area. The L2 interface uses standard synchronous pipelined-burst or late-write SRAM devices in a non-pipelined manner. The connections are shown in Table 3.

Table 3. L2 Cache SRAM Connections

SRAM Signal	Connection	Notes
A[16:0]	L2ADDR[16:0]	Connect buses; order is not important since burst mode is not used.
A17	L2ADDR17	If present and/or needed. For forward compatibility, tie to a weak (1K-5KΩ pulldown) since LA17 = $\overline{CE3}$ on some SRAM devices.
A18	L2ASPARE	If present and/or needed.
$\overline{ADV}$	L2OVDD	Deasserted since burst mode not used.
$\overline{ADSC}$	GND	Asserted to continually accept addresses.
$\overline{ADSP}$	L2OVDD	Deasserted since burst mode not used.
DQ[0:63]	L2DATA[0:63]	Connect buses; order is not important since byte access modes are not used. DP bits may be intermixed with DQ bits if and only if parity-capable SRAMs are always used; otherwise, connect DP only to DP.
DP[0:7]	L2DP[0:7]	Connect buses; order is not important since byte access modes are not used. DP bits may be intermixed with DQ bits if and only if parity-capable SRAMs are always used; otherwise, connect DP only to DP.
$\overline{G}$ $\overline{OE}$	GND	Since the L2 is chip-select-controlled, it is normally in output mode unless being written to. $\overline{OE}$ may tied low.
CK K	L2CLK_OUTA L2CLK_OUTB	For single-ended clocks, tie one clock to each of two SRAMs without sharing. Keep trace lengths matching other L2 traces. For differential clocks, tie “A” to the active high clocks and “B” to the active low clocks. Route the clocks in a “Y” manner so the stubs have the same, minimal, length.
$\overline{LBO}$	GND or VCC	GND is for PowerPC bursts order; however, burst mode is not used so may be tied high or low.
$\overline{SB[A:D]}$	GND or L2OVDD	Byte write modes are not used.
$\overline{SGW}$	$\overline{L2WE}$	Write cause global writes.
$\overline{SW}$	L2OVDD	Byte write modes are not used.
$\overline{SE1}$	$\overline{L2CE}$	Connect SRAM chip select.
SE2	L2OVDD	Second chip-select not used.
$\overline{SE3}$	GND	Third chip-select not used.
ZZ	L2ZZ or GND	Optional; not all SRAMs have ZZ.

In addition, the L2SYNC_OUT pin should be connected to the L2SYNC_IN pin using a trace length equal to the ones used on the L2CLK_OUT[A:B] traces.

1.4 L3 Cache DDR SRAM Connections

The MPC745x processors support a “backside” L3 cache on a private cache bus. The L3 interface supports double-data rate SRAM (DDRSRAM) devices of the MSUG2 and PCDDR types. The connections are shown in Table 4.

Table 4. L3 Cache DDRSRAM Connections

SRAM Signal	Connection	Notes
A[17:0]	L3ADDR[17:0]	Connect buses; order is not important since burst mode is not used.
B1	L3CNTL0	Signal operates as load address strobe.
B2	L3CNTL1	Signal operates as read/write enable.
B3	GND	Signal operates as single/double rate selection (double-rate selected).
CK K	L3_CLK0 or L3_CLK1	Connect one clock to each of the SRAMs without sharing. Keep trace lengths matching other L3_ECHO_CLK feedback traces.
$\overline{CK}$ $\overline{K}$	GVDD/2	Connect to a resistor divider or power supply set to the L3 cache power supply. Two 250Ω resistors are sufficient current.
CQ1	L3ECHO_CLK0 or L3ECHO_CLK2	L3ECHO_CLK0 is paired with DQ[0:15] and L3DP[0:1]. L3ECHO_CLK2 is paired with DQ[32:47] and L3DP[4:5].
CQ2	L3ECHO_CLK1 or L3ECHO_CLK3	L3ECHO_CLK1 is paired with DQ[16:31] and L3DP[2:3]. L3ECHO_CLK3 is paired with DQ[48:63] and L3DP[6:7].
$\overline{CQ1}$ $\overline{CQ2}$	NC	No connection.
DQ[0:15] DQP[0:1]	L3DATA[0:15] L3DP[0:1]	Connect buses; order is not important since byte access modes are not used. DQ bits may be reordered. DQP bits may be reordered. DQ and DQP bits may be intermixed within this pairing only, if and only if parity-capable SRAMs are always used, otherwise connect only DQ to DQ and DQP to DQP.
DQ[16:31] DQP[2:3]	L3DATA[16:31] L3DP[2:3]	
DQ[32:47] DQP[4:5]	L3DATA[32:47] L3DP[4:5]	Connect buses; order is not important since byte access modes are not used. DQ bits may be reordered. DQP bits may be reordered. DQ and DQP bits may be intermixed within this pairing only, if and only if parity-capable SRAMs are always used, otherwise connect only DQ to DQ and DQP to DQP.
DQ[48:63] DQP[6:7]	L3DATA[48:63] L3DP[6:7]	
$\overline{G}$ $\overline{OE}$	GND	The L3 is chip-select-controlled, so it is normally in output mode unless being written to. $\overline{G}$ may tied low.
$\overline{LBO}$	GND	Selects linear burst order.
ZQ	GVDD/2	Connect to a resistor divider or power supply set to the L3 cache power supply. Two 250Ω resistors are sufficient current.

1.5 L3 Cache Pipelined/Late-Write SRAM Connections

The MPC745x processors also support pipelined burst SRAM (PBSRAM) or late-write SRAM (LWSRAM) devices in a non-pipelined manner. Refer to the processor connection table for non-SRAM-specific connections (such as L3_ECHO_CLK). The PB/LWSRAM connections are shown in Table 5.

Table 5. L3 Cache PBSRAM/LWSRAM Connections

SRAM Signal	Connection	Notes
A[17:0]	L3ADDR[17:0]	Connect buses; order is not important since burst mode is not used.
$\overline{\text{ADV}}$	GVDD	Deasserted since burst mode not used.
$\overline{\text{ADSC}}$	GND	Asserted to continually accept addresses.
$\overline{\text{ADSP}}$	GVDD	Deasserted since burst mode not used.
CK K	L3_CLK0 or L3_CLK1	Connect one clock to each of the SRAMs without sharing. Keep trace lengths matching other L3_ECHO_CLK feedback traces.
$\overline{\text{CK}}$ $\overline{\text{K}}$	GVDD/2	Connect to a resistor divider or power supply set to the L3 cache power supply. Two 250Ω resistors are sufficient current.
DQ[0:31] DQP[0:3]	L3DATA[0:31] L3DP[0:3]	Connect buses; order is not important since byte access modes are not used. DQ bits may be reordered. DQP bits may be reordered. DQ and DQP bits may be intermixed within this pairing only, if and only if parity-capable SRAMs are always used, otherwise connect only DQ to DQ and DQP to DQP.
DQ[32:63] DQP[4:7]	L3DATA[32:63] L3DP[4:7]	
$\overline{\text{G}}$ $\overline{\text{OE}}$	GND	The L3 is chip-select-controlled, so it is normally in output mode unless being written to. $\overline{\text{G}}$ may tied low.
$\overline{\text{LBO}}$	GND	Selects linear burst order.
$\overline{\text{SBW[A:D]}}$	GVDD	Byte write modes are not used.
$\overline{\text{SE1}}$	L3CNTL0	Signal operates as SRAM chip select.
SE2	GVDD	Second active-high chip-select not used.
$\overline{\text{SE3}}$	GND	Third active-low chip-select not used.
$\overline{\text{SGW}}$	L3CNTL1	Signal operates as global write enable.
$\overline{\text{SW}}$	GVDD	Byte write modes are not used.
ZZ	GND	Optional; not all SRAMs have ZZ.

1.6 Power

Motorola processor specifications state restrictions on the amount of time any power pin can be at a non-standard voltage in relation to another power pin. Typically these event occur during power-up and power-down. When the restrictions are not met, if the amount of time exceeds approximately 50 mS, damage to the part may occur.

If the power supply can sequence all the I/O voltage (OVDD), L2 I/O voltage (L2OVDD), and core voltage (VDD) within the specification limits, or stabilize within 50 mS, then no further design work is needed.

Otherwise, power supply sequencing assistance is needed. The easiest way is to apply a diode voltage sourcing network as shown in the hardware specifications, but other means such as MOSFETs configured as a linear regulator would be suitable as well. The diode solution supplies just under the targeted operating voltage, but within the differential allowances in the hardware specification. Each device has slightly different allowances, so refer to the hardware specifications for particular examples of diode networks for each device.

Note that the diode network is needed for each non-compliant power supply. However, it is not needed between all power supplies, only between those which are too slow. Thus, if OVDD (typically 3.3V) is stable first and last, the others can be derived from it alone.

1.7 Clocks

All clocks should be carefully routed to be of equal lengths within similar domains (processor system bus, cache bus, memory bus, or PCI bus). Devices with integrated clock drivers make this relatively easy; see the corresponding hardware specifications, or the MPC107 Design Guide for further details.

1.8 References

The reference materials shown in Table may be useful to the designer. To locate the documents, go to http://www.motorola.com/ and search for the document title.

Table 6. Reference Material

Description	Document
MPC107 Design Guide	AN1849/D
MPC603e™ Hardware Specifications (PID6)	MPC603EEC/D R2
MPC603e Hardware Specifications (PID7t)	MPC603E7TEC/D R3
MPC750A Hardware Specification	MPC750EC/D
MPC7400 Hardware Specifications	MPC7400EC/D
MPC7410 Hardware Specifications	MPC7410EC/D
MPC7450 Hardware Specification	MPC7450EC/D
MPC107 Hardware Specification	MPC107EC/D
MPC8240 Integrated Processor Hardware Specifications	MPC8240EC/D
MPC8245 Integrated Processor Hardware Specifications	MPC8240EC/D

1.9 Revision History

Table 7 provides a revision history of this document.

Table 7. Document History

Revision Number	Changes
Rev 1.1	Added MPC7450 Support.
Rev 1.2	Corrected AP0 data; changed OVDD pullup recommendations, Motorola processor references.

HOW TO REACH US:

USA/EUROPE/LOCATIONS NOT LISTED:

Motorola Literature Distribution;
P.O. Box 5405, Denver, Colorado 80217
1-303-675-2140 or 1-800-441-2447

JAPAN:

Motorola Japan Ltd.; SPS, Technical Information Center,
3-20-1, Minami-Azabu Minato-ku, Tokyo 106-8573 Japan
81-3-3440-3569

ASIA/PACIFIC:

Motorola Semiconductors H.K. Ltd.; Silicon Harbour Centre, 2 Dai King Street, Tai Po Industrial Estate,
Tai Po, N.T., Hong Kong
852-26668334

TECHNICAL INFORMATION CENTER:

1-800-521-6274

HOME PAGE:

http://www.motorola.com/semiconductors

DOCUMENT COMMENTS:

FAX (512) 933-2625,
Attn: RISC Applications Engineering

xxxxxxxx/D