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Product Brief

MPC821 PowerPC™ Portable Systems Microprocessor

The MPC821 microprocessor is a versatile, one-chip integrated microprocessor and peripheral combination that can be used in a variety of portable electronics applications. It particularly excels in low power, portable, computing systems, and personal communications products. The MPC821 microprocessor integrates a high performance Embedded PowerPC™ Core with a Communication Processor Module (CPM) that utilizes a specialized RISC processor for communications. The CPM can perform embedded signal processing functions and supports six serial channels: two serial communication controllers (SCCs), two serial management controllers (SMCs), one serial peripheral interface (SPI), and one interprocessor-integrated communications (I^2C) controller. This two-processor architecture provides better power consumption for operations performed (performance) than traditional architectures because the CPM off-loads peripheral tasks from the PowerPC core.

MPC821 Microprocessor Key Features

The following list summarizes the key MPC821 microprocessor features:

- Embedded PowerPC™ Core provides 53 MIPS (using Dhrystone 2.1) or 90K Dhrystones 2.1 at 40 MHz and 32 MIPS (using Dhrystone 2.1) or 53K Dhrystones 2.1 at 25 MHz
  - — Single Issue, 32-Bit Version of the PowerPC Core with 32 x 32-Bit Fixed Point Registers
  - — Performs Branch Folding, Branch Prediction with Conditional Pre-Fetch, without Conditional Execution
  - — 4 Kbyte Data Cache and 4 Kbyte Instruction Cache
  - — Instruction and Data Caches are Two Way, Set-Associative, Physical Address, 4-Word Line Burst, LRU Replacement Algorithm, Lockable on Line Granularity
  - — MMUs with 32-Entry TLBs, Fully Associative Instruction and Data TLBs
  - — MMUs Supports Multiple Page Sizes of 4 Kbyte, 16 Kbyte, 512 Kbyte and 8 Mbyte (1 Kbyte Protection Granularity at the 4K Page Size); 16 Virtual Address Spaces and 8 Protection Groups
  - — Advanced On-Chip Emulation Debug Mode
- Data Bus Dynamic Bus Sizing for 8-, 16-, and 32-Bit busses
  - — Support Traditional 68K Big-Endian, Traditional x86 Little-Endian, and PowerPC Little-Endian Memory Systems
- Completely Static Design (0–40 MHz Operation)
- Communications Processor Module (CPM)
  - — 32-Bit, Harvard Architecture, Scalar RISC Controller
  - — Communication Specific Commands (e.g., Graceful Stop Transmit, Close Receive Buffer Descriptor, RxBD)
  - — Up to 320 Buffer Descriptors

— Supports Continuous Mode Transmission and Reception on All Serial Channels
— 5 Kbytes of Dual-Port RAM
— 12 Serial DMA (SDMA) Channels
— Three Parallel I/O Registers with Open-Drain Capability
— Each Serial Channel Can Have Its Own Pins (Non-Multiplexed Serial Interface Mode)
— 16 x 16-Bit Multiply Accumulate Hardware (MAC)
  — One Operation per Clock (Two Clock Latency, One Clock Blockage)
  — MAC Operates Concurrently with Other Instructions
  — Uses DMA Controller to Burst Data Directly Into Register File Without Interaction from the PowerPC core

- Four Baud Rate Generators
  — Independent (Can Be Connected to Any SCC or SMC)
  — Allow Changes During Operation
  — Autobaud Support Option
- Two SCCs (Serial Communication Controllers)
  — Ethernet/IEEE 802.3 Optional on SCC1 (Full 10-Mbps Support) (Available only on Specially Programmed Devices)
  — HDLC/SDLC™ (All Channels Supported at 4 Mbps)
  — HDLC Bus (Implements an HDLC-Based Local Area Network (LAN))
  — AppleTalk®
  — Universal Asynchronous Receiver Transmitter (UART)
  — Synchronous UART
  — Serial Infrared (IrDA)
  — Binary Synchronous Communication (BISYNC)
  — Totally Transparent (Bit Streams)
  — Totally Transparent (Frame Based with Optional Cyclical Redundancy Check (CRC))
  — Maximum Serial Data Rate of 22 Mbps
- Two SMCs (Serial Management Channels)
  — UART
  — Transparent
  — General Circuit Interface (GCI) Controller
  — Can Be Connected to the Time-Division Multiplexed (TDM) Channels
- One SPI (Serial Peripheral Interface)
  — Supports Master and Slave Modes
  — Supports Multimaster Operation on the Same Bus
- One I^2C (Interprocessor-Integrated Communications) Port
  — Supports Master and Slave Modes
  — Supports Multimaster Environment
- Time-Slot Assigner
  — Allows SCCs and SMCs to be used in Multiplexed and/or Non-Multiplexed Operation
  — Supports T1, CEPT, PCM Highway, ISDN Basic Rate, ISDN Primary Rate, User Defined
  — 1- or 8-Bit Resolution
  — Allows Independent Transmit and Receive Routing, Frame Syncs, Clocking
  — Allows Dynamic Changes
  — Can Be Internally Connected to Four Serial Channels (Two SCCs and Two SMCs)
- Parallel Interface Port
  — Centronics™ Interface Support

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- General-Purpose Timers
  - Four 16-Bit Timers or Two 32-Bit Timers
  - Gate Mode Can Enable/Disable Counting
  - Interrupt Can Be Masked on Reference Match and Event Capture
- Interrupts
  - Seven External Interrupt Request (IRQ) Lines
  - 12 Port Pins with Interrupt Capability
  - 16 Internal Interrupt Sources
  - Programmable Priority Between SCCs
  - Programmable Highest Priority Request
- Memory Controller (Eight Banks)
  - Programmable Memory Controller Can Be Programmed to Support Almost Any Memory Interface for Glueless Interface to DRAM Single In-Line Memory Modules (SIMMs), Static Random-Access Memory (SRAM), Electrically Programmable Read-Only Memory (EPROM), Flash EPROM, etc.
  - 8 Memory Banks; Each Bank Can Be a Chip Select or Support a DRAM Bank
  - Up to 15 Wait States Programmable per Memory Bank
  - Four CAS lines, Four WE lines, One OE line
  - Boot Chip Select Available at Reset (Options for 8-, 16-, or 32-Bit Memory)
  - Variable Block Sizes, 32 Kbyte to 256 Mbyte
  - Selectable Write Protection
  - On-Chip Bus Arbitration Supports External Bus Master
  - Special Features for Burst Mode Support
- System Interface Unit (SIU)
  - Bus Monitor
  - Spurious Interrupt Monitor
  - Software Watchdog
  - Periodic Interrupt Timer
  - Low Power Stop Mode
  - Clock Synthesizer
  - PowerPC Decrementer
  - PowerPC Time Base and RTC
  - Reset Controller
  - IEEE 1149.1 Test Access Port (JTAG)
- LCD Interface Controller
  - Monochrome, 4/16-Level Grey Scale
  - 16 Color Thin Film Transistor (TFT), 9 Bits, 3 x 3 RGB
  - Passive Color, 4/8-Bit Data
  - Configuration Programmable for Frame Rate, Pixels per Line, Lines per Frame
  - Panel Voltage Control
- PCMCIA Controller
  - Master Interface, Release 2.1 Compliant
  - Supports Two Independent PCMCIA Sockets
  - 8 Memory or I/O Windows Can Be Allocated Between Sockets
  - RTC, LCD and CPM in Low Power Standby
- Low Power Support
  - Full On - All Units Fully Powered
  - Doze - Core Functional Units Disabled Except Time Base Decrementer, PLL, Memory Controller, Sleep - All Units Disabled Except RTC and PIT, PLL Active for Fast Wake-up
  - Deep Sleep - All Units Disabled including PLL Except RTC and PIT
  - Low Power STOP

— Separate Power Supply Input to Operate Internal Logic at 2.2V When Operating at or Below 25 MHz

- Debug Interface
  - — Eight Comparators: Four Operate on Instruction Address, Two Operate on Data Address, and Two Operate on Data
  - — Supports Conditions: = ≠ < >.
  - — Each Watchpoint can Generate a Breakpoint Internally
- 3.3V Operation with TTL Compatibility on I/O Pins
- 357-Pin Ball Grid Array (BGA)

ARCHITECTURE OVERVIEW

The MPC821 microprocessor integrates a high-performance Embedded PowerPC Core with high-performance, low-power peripherals and extends the Motorola family of microprocessors into the handheld, portable communications and consumer markets.

The MPC821 microprocessor is comprised of three modules: the Embedded PowerPC Core, the System Interface Unit (SIU), and the Communication Processor Module (CPM). Each module interfaces to the 32-bit internal bus. The MPC821 microprocessor block diagram is shown in Figure 1.

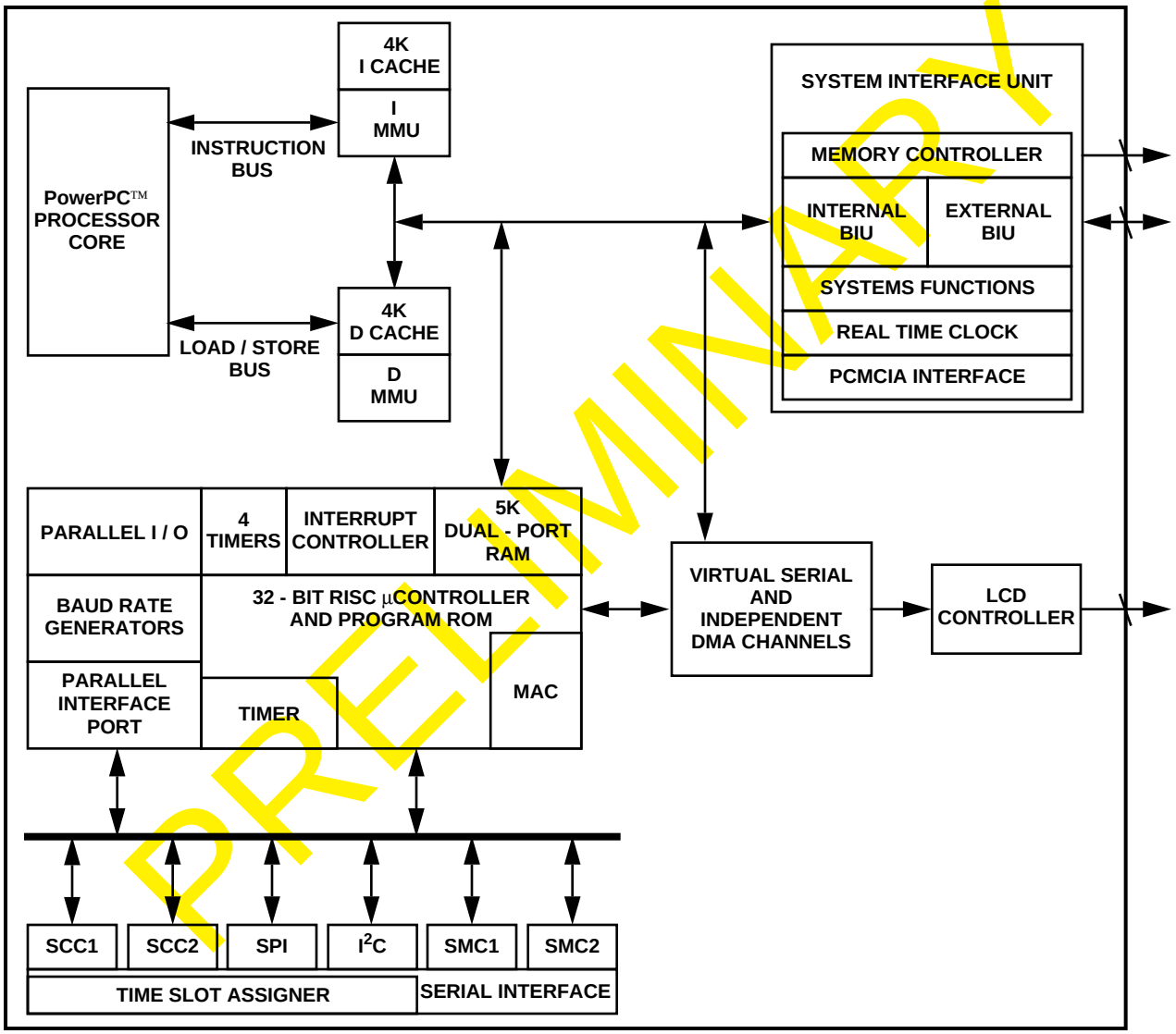

Figure 1. MPC821 Microprocessor Block Diagram

Architectural Approach

The MPC821 microprocessor adopts a dual-processor architectural approach. This design philosophy provides a high-performance, general-purpose RISC integer processor, the Embedded PowerPC Core, for application programming use. The design also provides a special purpose RISC communications processor, the Communication Processor Module (CPM), for personal communications needs. The CPM performs embedded signal processing functions for communications and user interface enhancements as well as providing I/O support for high speed digital communications.

Embedded PowerPC Core

The PowerPC core is a fully static design that consists of three functional blocks; the integer block, a hardware multiplier/divider and the load/store block. It executes all integer and load/store operations directly on the hardware. The core supports integer operations on a 32-bit internal data path and 32-bit arithmetic hardware. Its interface to the internal and external buses is 32 bits. The PowerPC core uses a 2 instruction Load/Store Queue, 4 instruction Pre-Fetch Queue, and a 6 instruction history buffer. The core does Branch Folding and Branch Prediction with conditional Pre-Fetch but without conditional execution. The PowerPC core can operate on 32-bit external operands with one bus cycle.

The PowerPC integer block supports 32 x 32-bit fixed point general purpose registers. It can execute one integer instruction each clock cycle. Each element in the integer block is clocked only when valid data is present in the data queue ready for operation. This reduces the power consumption of the device to the minimum required to perform an operation.

The PowerPC microprocessor is integrated with MMUs, and 4 Kbyte Instruction and Data Caches. The MMUs provide a 32-entry, fully-associative instruction and data TLB, with multiple page sizes of: 4 Kbyte (1 Kbyte protection), 16 Kbyte, 512 Kbyte, and 8 Mbyte. It will support 16 virtual address spaces with 8 protection groups. Three special registers are available as scratch registers to support software table walk and update.

The Instruction Cache is 4 Kbytes, two-way, set-associative with physical addressing. It allows single cycle access on HIT with no added latency for MISS. It has four words per line, and supports burst line fill using an LRU replacement algorithm. The cache can be locked on a line basis for application critical routines.

The Data Cache is 4 Kbytes, two-way, set-associative with physical addressing. It allows single cycle access on HIT with one added clock latency for MISS. It has four words per line, supports burst line fill using an LRU replacement algorithm. The cache can be locked on a line basis for application critical routines. The Data Cache can be programmed to support Copy-Back or Write-Through via the MMU. The inhibit mode can be programmed per MMU page.

The PowerPC microprocessor with its Instruction and Data Caches can deliver approximately 53 MIPS at 40 MHz (using Dhrystone 2.1) or 90K Dhrystones and 32 MIPS at 25 MHz (using Dhrystone 2.1) or 53K Dhrystones. This is based on the assumption that it is issuing one instruction per cycle with a cache hit rate of 94%.

Communications Processor Module (CPM)

The CPM contains features that allow the MPC821 microprocessor to excel in low power, personal communications and control applications. These features may be divided into three sub-groups:

- Communications Processor (CP)
- Twelve Independent DMA (IDMA) Controllers
- Four General-Purpose Timers

The CPM provides the communication features of the MPC821 microprocessor. Included are a RISC processor with multiply accumulate hardware (MAC), two serial communication controllers (SCCs), two serial management controllers (SMCs), one serial peripheral interface (SPI), one interprocessor-integrated communications (I^2C) controller, 5 Kbytes of dual-port RAM, an interrupt controller, a time slot assigner, three parallel ports, a parallel interface port, and four independent baud rate generators.

Twelve serial DMA channels support the SCCs, SMCs, and SPIs. The IDMAs provide two channels of general-purpose DMA capability for each communications channel. They offer high-speed transfers, 32-bit data movement, buffer chaining, and independent request and acknowledge logic. The RISC controller may access the IDMA registers directly in the buffer chaining modes.

The four general-purpose timers on the CPM are functionally similar to the two general-purpose timers found on the MC68360 Quad Integrated Communications Controller (QUICC). However, they offer some minor enhancements, such as the internal cascading of two timers to form a 32-bit timer. The MPC821 microprocessor also contains a periodic interval timer in the SIU, bringing the total of on-chip timers to five.

System Interface Unit (SIU)

Although the PowerPC core is always a 32-bit device internally, it may be configured to operate with an 8-, 16- or 32-bit data bus. Regardless of the choice of system bus size, dynamic bus sizing is supported. Bus sizing allows 8-, 16-, and 32-bit peripherals and memory to coexist on the 32-bit system bus.

The SIU provides support to interface to traditional 68K Big-Endian memory systems, traditional x86 Little-Endian memory systems, and PowerPC Little-Endian memory systems.

The SIU also provides power management functions, Reset control, PowerPC decrementer, PowerPC time base and Real Time Clock.

The memory controller will support up to eight memory banks with glueless interfaces to DRAM, SRAM, PSRAM, EPROM, Flash EPROM, SRDRAM, EDO and other peripherals with two-clock initial access to external SRAM and bursting support. It provides variable block sizes from 32 Kbytes to 256 Mbytes. The memory controller will provide 0 to 15 wait states for each bank of memory and can use address type matching to qualify each memory bank access. It provides four byte enable signals for varying width devices, one output enable signal and one Boot chip select available at reset.

The DRAM interface supports ports of 8-, 16-, and 32-bits. The DRAM interface uses a programmable state machine to support almost any memory interface. Memory banks can be defined in depths of 256K, 512K, 1M, 2M, 4M, 8M, 16M, 32M, or 64M for all port sizes. In addition, the memory depth can be defined as 64K and 128K for 8-bit memory or 128M and 256M for 32-bit memory. The DRAM controller supports Page Mode access for successive transfers within bursts. The MPC821 microprocessor will support a glueless interface to one bank of DRAM, while external buffers are required for additional memory banks. The refresh unit provides CAS before RAS, a programmable refresh timer, refresh active during external reset, disable refresh modes, and stacking for up to 7 refresh cycles.

LCD Controller

The LCD controller on the MPC821 microprocessor supports a versatile interface. It provides Monochrome or 4/16-level grey scale, Color TFT (9 bits, 3 x 3 RGB), and passive color (xSTN) 4/8-bit data. The controller supports 4-bit non-split, 8-bit non-split, 2+2-bit split, or 4+4-bit split. It is programmable for frame rate, number of pixels per line, and number of lines per frame. The panel voltage is programmable through duty cycle, for contrast adjustments implemented in the CPM module program. Display data is stored in user memory space and is transferred into the controller using the DMA channels.

PCMCIA Controller

The PCMCIA interface is a Master controller and is compliant with release 2.1. The interface will support up to two independent PCMCIA sockets with external transceivers/buffers required. The interface provides 8 memory or I/O windows where each window can be allocated to each socket. If only one PCMCIA port is being used, the unused PCMCIA port can be used as general purpose input with interrupt capability.

Power Management

The MPC821 microprocessor supports a wide range of power management features including Full On, Doze, Sleep, Deep Sleep, and Low Power Stop. In Full On mode, the MPC821 microprocessor is fully powered with all internal units operating at the full speed of the processor. There is a Gear mode that is determined by a clock divider that allows the operating system to reduce the operational frequency of the processor. Doze mode disables core functional units except the time base decrementer, PLL, memory controller, RTC, and LCD controller, and places the CPM in low power standby mode. Sleep mode is the next lower power mode that disables everything else except the RTC and PIT, leaving the PLL active for quick wake-up. The Deep Sleep mode then disables the PLL for lower power but slower wake-up. Low Power Stop disables all logic in the processor except the minimum logic required to restart the device, and provides the lowest power consumption but requires the longest wake-up time.

The MPC821 microprocessor also provides a separate set of power pins for the internal logic in the device. These power pins can be used to provide the device with a 2.2V power source that can be used when the processor is operating at 25 MHz or less. This capability reduces the power consumption of the device by an additional 30%.

System Debug Support

The MPC821 microprocessor contains an advanced debug interface that provides superior debug capabilities without causing any degradation in the speed of operation. It supports six watchpoint pins that can be combined with eight internal comparators, four of which operate on the address on the Instruction bus. The other four comparators are split: two comparators operate on the address on the Load/Store bus, and two comparators operate on the data on the Load/Store bus. The MPC821 microprocessor can compare using =, ≠, <, > conditions to generate watchpoints. Each watchpoint can then generate a breakpoint that can be programmed to trigger in a programmable number of events.

MPC821 GLUELESS SYSTEM DESIGN

A fundamental design goal of the MPC821 microprocessor was ease of interface to other system components. Figure 2 shows a system configuration that offers one EPROM, one flash EPROM, and supports two DRAM SIMMs. Depending on the capacitance on the system bus, external buffers may be required as they are for the dual DRAM-bank design shown. From a logic standpoint, however, a glueless system is maintained and buffers would not be required for single DRAM-bank systems.

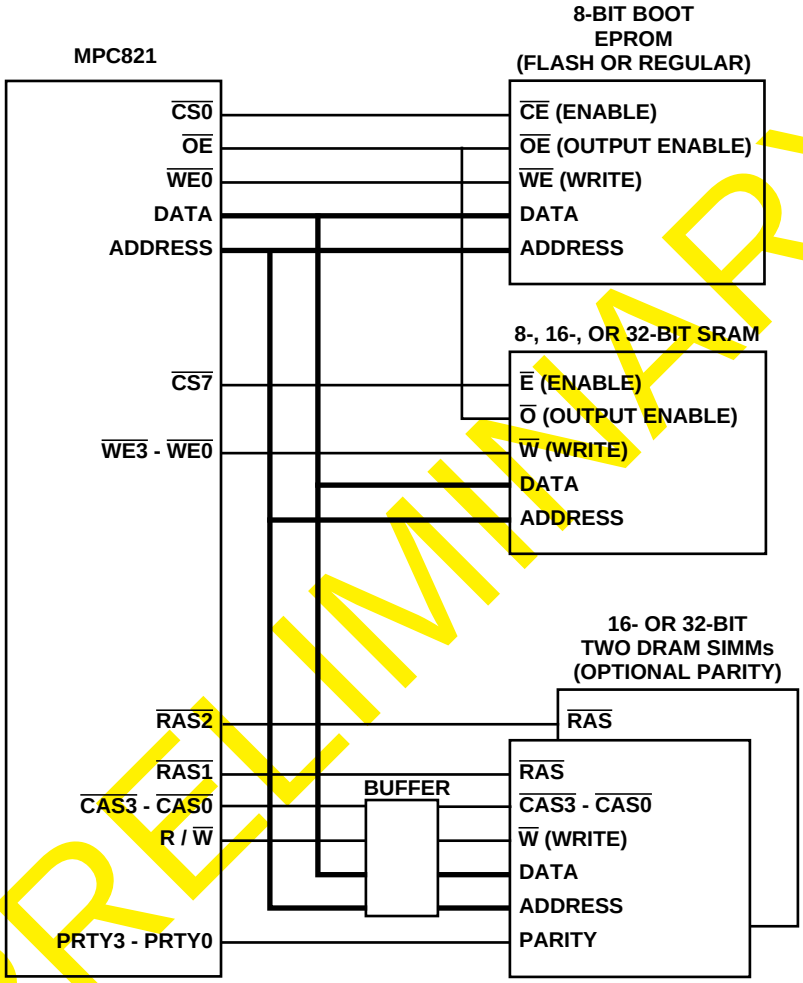

Figure 2. MPC821 System Configuration

The following table identifies the packages and operating frequencies available for the MPC821.

Table 1. MPC821 Package/Frequency Availability

Package Type	Frequency (MHz)	Temperature	Order Number
Ball Grid Array (BGSuffix)	0-25	0˚ C to 70˚ C	XPC821ZP25
Ball Grid Array (BGSuffix	0-40	0˚ C to 70˚ C	XPC821ZP40
	TBD	-40˚ C to 85˚ C	TBD

The documents listed in the following table contain detailed information on the MPC821. These documents may be obtained from the Literature Distribution Centers at the addresses listed at the bottom of this page.

Table 2. Related Documentation

Document Title	Order Number	Contents
MPC821 User's Manual	MPC821UM/AD	Detailed Information for Design
Product Brief	MPC821/D	Overview of Product Features
PowerPC™ Microprocessors Family: The Programming Environment	MPCFPE/AC	PowerPC™ Instruction Set
The Embedded PowerPC™ Source	TBD	Independent Vendor Listing Supporting Software and Development Tools

Literature Distribution Centers:

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