MPC860PTS/D
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PowerPC™

Advance Information

MPC860P PowerQUICC™ Technical Summary

The MPC860 Plus (MPC860P) is a pin-compatible enhanced version of the MPC860 PowerQUICC™ microprocessor that increases the instruction cache size from 4 to 16 Kbytes and the data cache from 4 to 8 Kbytes. Dual-port RAM is increased from 5 to 8 Kbytes, extending the flexibility and capabilities of the communications processor module (CPM). The MPC860P is also capable of system clock rates of 80 MHz and faster.

The MPC860P is a versatile, one-chip integrated microprocessor and peripheral combination that can be used in a variety of controller applications, excelling particularly in communications and networking products. The MPC860P has two processing blocks, the embedded PowerPC core and the CPM. The CPM supports four serial communications controllers (SCCs); however, there are actually eight serial channels—four SCCs, two serial management controllers (SMCs), one serial peripheral interface (SPI) and one I^2C interface. This dual-processor architecture provides lower power consumption than traditional architectures because the CPM off-loads peripheral tasks from the core.

As a superset of the MPC860SR and the MPC860T (revision D), the MPC860P supports ATM features including the UTOPIA interface, 10/100 base-T (Fast) Ethernet, and QMC microcode for multichannel HDLC support.

The MPC860DP, a version of the MPC860P with only two SCCs, is also available.

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1.1 Key Features

The MPC860P integrates the PowerPC core with high performance, low-power peripherals to extend the Motorola networking and communications family of embedded processors even farther into high-end communications and networking products.

The MPC860P is comprised of three modules which all use the 32-bit internal bus—the PowerPC core, the system interface unit (SIU), and the communications processor module (CPM). The MPC860P block diagram is shown in Figure 1.

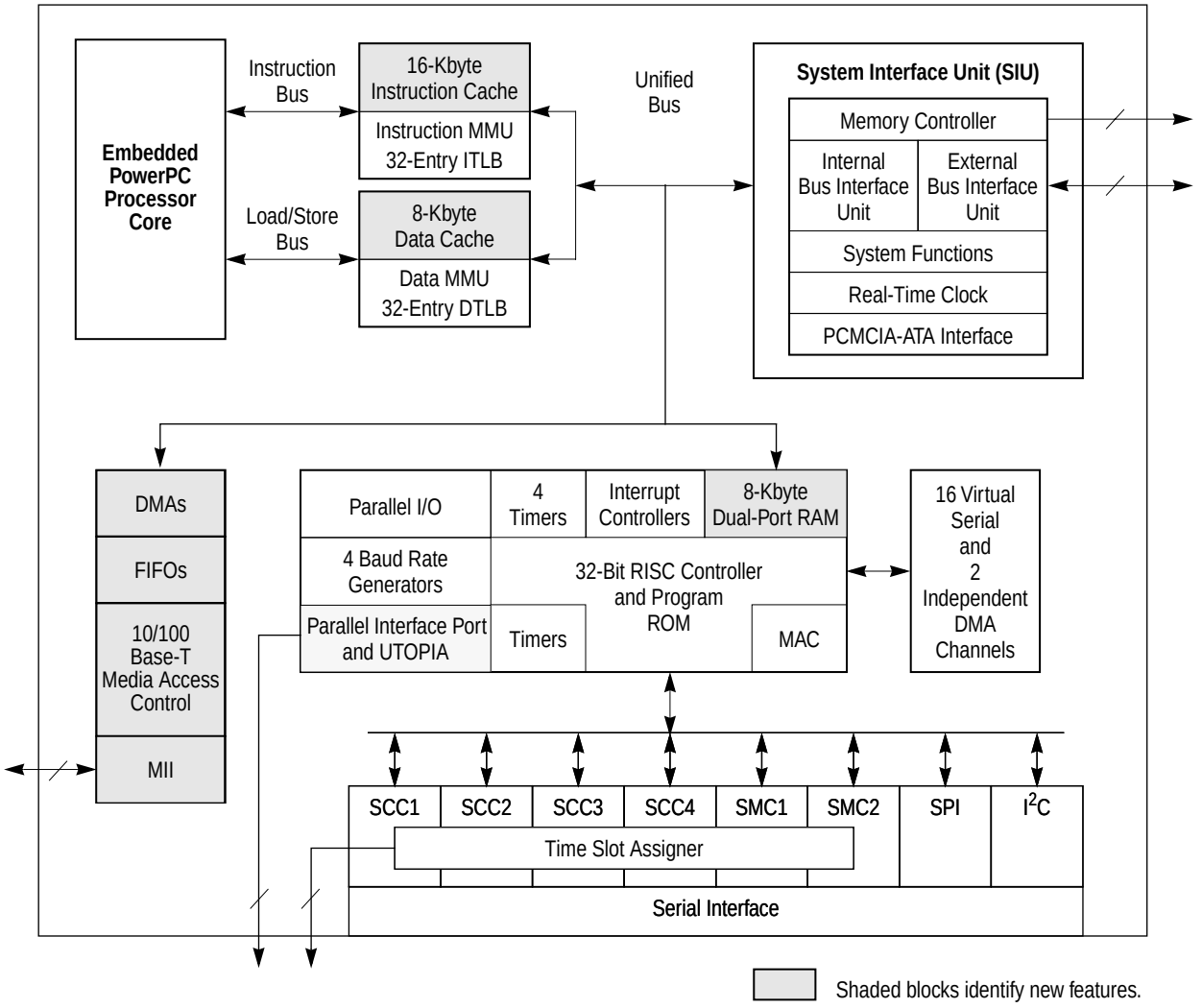

Figure 1. MPC860P Block Diagram

The following list summarizes key MPC860P features:

- Embedded PowerPC core with 106 MIPS at 80 MHz (using Dhrystone 2.1)
- Single-issue, 32-bit version of the PowerPC core (fully compatible with the PowerPC user instruction set architecture (UISA) with 32 32-bit general-purpose registers (GPRs)
  - — PowerPC core performs branch folding, branch prediction with conditional pre-fetch, without conditional execution
  - — 8-Kbyte data cache and 16-Kbyte instruction cache

  - — Instruction cache is four-way, set-associative; data cache is two-way, set-associative. Both are physically addressed, four-word line burst, least recently used (LRU) replacement algorithm, lockable on-line granularity.
  - — MMUs with 32-entry translation lookaside buffers (TLBs), fully-associative instruction and data TLBs
  - — MMUs support multiple page sizes of 4 Kbyte, 16 Kbyte, 512 Kbyte and 8 Mbyte; 16 virtual address spaces and 16 protection groups
  - — Advanced on-chip emulation debug mode
- Up to 32-bit data bus (dynamic bus sizing for 8, 16, and 32 bits)
- 32 address lines
- Complete static design (0–80 MHz operation)
- Memory controller (eight banks)
  - — Contains complete dynamic random-access memory (DRAM) controller
  - — Each bank can be a chip select or $\overline{\text{RAS}}$ to support a DRAM bank
  - — Up to 15 wait states programmable per memory bank
  - — Glueless interface to DRAM single in-line memory modules (SIMMs), static random-access memory (SRAM), electrically programmable read-only memory (EPROM), flash EPROM and synchronous DRAM (SDRAM).
  - — DRAM controller programmable to support most size and speed memory interfaces
  - — Four $\overline{\text{CAS}}$ lines, four $\overline{\text{WE}}$ lines, one $\overline{\text{OE}}$ line
  - — Boot chip select available at reset (options for 8-, 16-, or 32-bit memory)
  - — Variable block sizes, 32 Kbyte to 256 Mbyte
  - — Selectable write protection
  - — On-chip bus arbitration logic
- General-purpose timers
  - — Four 16-bit timers or two 32-bit timers
  - — Gate mode can enable/disable counting
  - — Interrupt can be masked on reference match and event capture
- System interface unit (SIU)
  - — Bus monitor
  - — Software watchdog
  - — Periodic interrupt timer
  - — Low power stop mode
  - — Clock synthesizer
  - — PowerPC decrementer
  - — Real-time clock (RTC) and PowerPC time base
  - — Reset controller
  - — IEEE 1149.1 test access port (JTAG)
- Interrupts
  - — Seven external interrupt request (IRQ) lines
  - — 12 port pins with interrupt capability
  - — 23 internal interrupt sources
  - — Programmable priority between SCCs
  - — Programmable highest priority request

- Communications processor module (CPM)
  - RISC communications processor (CP)
  - Communication-specific commands (for example, GRACEFUL STOP TRANSMIT, CLOSE RECEIVE BUFFER DESCRIPTOR)
  - Supports continuous mode transmission and reception on all serial channels
  - 8 Kbytes of dual-port RAM
  - 16 serial DMA (SDMA) channels
  - Three parallel I/O registers with open-drain capability
- On-chip 16 x 16 multiply accumulate controller (MAC)
  - One operation per clock (two-clock latency, one-clock blockage)
  - MAC operates concurrently with other instructions
  - FIR loop: four clocks per four multiplies
- Four baud-rate generators
  - Independent (can be connected to any SCC or SMC)
  - Allow changes during operation
  - Autobaud support option
- Four serial communications controllers (SCCs)
  - Ethernet/IEEE 802.3 optional on SCC1–SCC4, supporting full 10-Mbps operation (available on specially programmed devices)
  - HDLC/SDLC™ (all channels supported at 2 Mbps)
  - HDLC bus (implements an HDLC-based local area network (LAN))
  - Asynchronous HDLC to support point-to-point protocol (PPP)
  - AppleTalk®
  - Universal asynchronous receiver transmitter (UART)
  - Synchronous UART
  - Serial Infrared (IrDA)
  - Binary synchronous communication (BISYNC)
  - Totally transparent
    - bit streams
    - frame based with optional cyclic redundancy check (CRC)
- ATM support
  - Compliant with ATM forum UNI 4.0 specification
  - Cell processing up to 50–70 Mbps at 50-MHz system clock
  - Cell multiplexing/demultiplexing
  - Support of AAL5 and AAL0 protocols on a per-VC basis
  - AAL0 support enables OAM and software implementation of other protocols
  - ATM pace control (APC) scheduler, providing:
    - Direct support of constant bit rate (CBR)
    - Direct support of unspecified bit rate (UBR)
    - Control mechanisms enabling software support of available bit rate (ABR)
    - Support for two types of physical interfaces
    - UTOPIA
    - Byte-aligned serial (for example, T1/E1/ADSL)

- UTOPIA-mode ATM supports:
  - UTOPIA level 1 master with cell-level handshake
  - Multi-PHY (up to 4 physical layer devices)
  - Connection to 25 Mbps, 51 Mbps, or 155 Mbps framers
  - UTOPIA clock rates of 1:2 or 1:3 system clock rates
- Serial-mode ATM connection supports:
  - Transmission convergence (TC) function for T1/E1/ADSL lines
  - Cell delineation
  - Cell payload scrambling/descrambling
  - Automatic idle/unassigned cell insertion/stripping
  - Header error control (HEC) generation, checking, and statistics
  - Glueless interface to Motorola CopperGold ADSL transceiver
- Receive VP/VC connection lookup mechanisms, including:
  - Internal sequential lookup table supporting up to 32 connections
  - Support for up to 64K connections using external memory via address compression or content-addressable memory (CAM)
- Independent transmit/receive buffer descriptor ring data structures for each connection
- Interrupt report per channel using exception queue
- Supports 53-byte or up to 64-byte (expanded) ATM cells
- AAL5 segmentation and reassembly (SAR) features for segmentation
  - Segment CPCS_PDU directly from system memory
  - CPCS_PDU padding
  - CRC32 generation
  - Automatic last cell marking (in PTI field of cell header)
  - Automatic CS_UU, CPI, and LENGTH insertion in last cell
- AAL5 segmentation and reassembly (SAR) features for reassembly:
  - Reassembles CPCS_PDU directly into system memory
  - Removes CPCS_PDU padding
  - CRC32 checking
  - CS_UU, CPI, and LENGTH reporting
  - CLP and congestion reporting
  - Interrupts per buffer or per message
  - Error reporting, including CRC, length mismatch, message abort
- AAL0 features for transmit include the following:
  - Transmits user-defined cell from transmit memory buffer
  - Automatic HEC generation
  - Optional CRC10 insertion
- AAL0 features for receive include the following:
  - Copies entire cell into receive memory buffer
  - Provides interrupt per cell
  - Optional CRC10 checking

- Fast Ethernet support
  - 10/100 base-T support
    - Full compliance with the IEEE 802.3u standard for 10/100 base-T
    - Support for three different physical interfaces: 100-Mbps 802.3 media-independent interface (MII), 10-Mbps 802.3 MII, and 10-Mbps 7-wire interface
    - Large on-chip transmit and receive FIFOs to support a variety of bus latencies
    - Retransmission from transmit FIFO following a collision
    - Automatic internal flushing of the receive FIFO for runts and collisions
    - Off-chip buffer descriptor tables of user-definable size allow nearly unlimited flexibility in management of transmit and receive buffer memory
  - 10/100 media access control (MAC) features
    - Address recognition for broadcast, single station address, promiscuous mode, and multicast hashing
    - Full support of media-independent interface (MII)
    - Interrupts supported per frame or per buffer (Selectable buffer interrupt functionality using the I-bit is not supported however.)
    - Automatic interrupt vector generation for receive and transmit events (Tx interrupts, Rx interrupts, and non-time critical interrupts)
    - Ethernet channel bursts data to/from external memory
- Two SMCs (serial management channels)
  - UART
  - Transparent
  - General circuit interface (GCI) controller
  - Can be connected to the time-division multiplexed (TDM) channels
- One SPI (serial peripheral interface)
  - Supports master and slave modes
  - Supports multi-master operation on the same bus
- One I^2C (inter-integrated circuit) port
  - Supports master and slave modes
  - Multi-master environment support
- Time-slot assigner
  - Allows SCCs and SMCs to run in multiplexed and/or non-multiplexed operation
  - Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user-defined
  - 1- or 8-bit resolution
  - Allows independent transmit and receive routing, frame syncs, clocking
  - Allows dynamic changes
  - Can be connected internally to six serial channels (four SCCs and two SMCs)
- Parallel interface port
  - Centronics® interface support
  - Supports fast connection between compatible ports on MPC860 or MC68360
- PCMCIA Interface
  - Master (socket) interface, release 2.1 compliant
  - Supports two independent PCMCIA sockets
  - 8 memory or I/O windows supported

- Low-power support
  - — Full-on—All units fully powered
  - — Doze—Core functional units disabled except time base decrementer, PLL, memory controller, RTC, and CPM in low-power standby
  - — Sleep—All units disabled except RTC and PIT, PLL active for fast wake-up
  - — Deep sleep—All units disabled including PLL except RTC and PIT
  - — Power-down mode– All units powered down except PLL, RTC, PIT, time base, and decrementer
- Debug interface
  - — Eight comparators:
    - – four operate on instruction address,
    - – two operate on data address, and
    - – two operate on data
  - — Supports conditions: = ≠ < >
  - — Each watchpoint can generate a breakpoint internally
- 3.3-V operation with 5-V TTL compatibility
- 357-pin ball grid array (BGA) package

1.2 Embedded PowerPC Core

The core complies with the PowerPC user instruction set architecture (UISA). The PowerPC core is a fully static design that consists of two functional blocks; the integer block and the load/store block. It executes all integer and load/store operations directly on the hardware. The core supports integer operations on a 32-bit internal data path and 32-bit arithmetic hardware. The core interface to the internal and external buses is 32 bits. The core uses a two instruction load/store queue, a four instruction prefetch queue, and a six instruction history buffer. The core does branch folding and branch prediction with conditional prefetching but without conditional execution. The PowerPC core can operate on 32-bit external operands with one bus cycle.

The core supports thirty-two 32-bit general purpose registers (GPRs) defined by the UISA which provides source and destination operands for the integer unit (IU). The IU can typically execute one integer instruction each clock cycle.

The PowerPC core is integrated with instruction and data caches and MMUs. Each MMU provides a 32-entry, fully associative instruction and data TLB, with multiple page sizes of 4 Kbyte, 16 Kbyte, 512 Kbyte, and 8 Mbyte. It supports 16 virtual address spaces with 16 protection groups. Three special registers are available as scratch registers to support software tablewalk and update.

The 16-Kbyte instruction cache is four-way, set associative with physical addressing. It allows single-cycle access on hit with no added latency for miss. It has four words per line, supporting burst line fill using least recently used (LRU) replacement. The cache can be locked on a per line basis for application critical routines. The cache inhibit mode can be programmed per MMU page.

The 8 Kbyte data cache is two-way, set associative with physical addressing. It allows single-cycle access on hit with one added clock latency for miss. It has four words per line, supporting burst line fill using LRU replacement. The cache can be locked on a per line basis for application critical data. The data cache can be programmed to support copy-back or write-through via the MMU. The cache-inhibit mode can be programmed per MMU page.

The PowerPC core with its instruction and data caches delivers approximately 106 MIPS at 80 MHz, using Dhrystone 2.1

The PowerPC core contains a much improved debug interface that provides superior debug capabilities without causing any degradation in the speed of operation. This interface supports six watchpoint pins that are used to detect software events. Internally it has eight comparators, four of which operate on the effective address on the address bus. The remaining four comparators are split, with two comparators operating on the effective address on the data address bus, and two comparators operating on the data bus. The PowerPC core can compare using =, ≠, <, > conditions to generate watchpoints. Each watchpoint can then generate a breakpoint that can be programmed to trigger in a programmable number of events.

1.3 System Interface Unit (SIU)

The SIU integrates general-purpose features useful in almost any 32-bit processor system, enhancing the performance provided by the system integration module (SIM) on the MC68360 QUICC™ device.

Dynamic bus sizing, allowing 8-, 16-, and 32-bit peripherals and memory to exist in the 32-bit system bus mode, is supported.

The SIU also provides power management functions, reset control, PowerPC decrementer, PowerPC time base and the real-time clock.

The memory controller supports up to eight memory banks with glueless interfaces to DRAM, SRAM, SSRAM, EPROM, Flash EPROM, SDRAM, EDO and other peripherals with two-clock access to external SRAM and bursting support. It provides variable block sizes from 32 Kbytes to 256 Mbytes. The memory controller provides 0–30 wait states for each bank of memory and can use address type matching to qualify each memory bank access. It provides four byte enable signals, one output enable signal and one boot chip select available at reset.

The DRAM interface supports port sizes of 8, 16, and 32 bits. Memory banks can be defined in depths of 256 or 512 Kbytes or 1, 2, 4, 8, 16, 32, or 64 Mbytes for all port sizes. In addition, the memory depth can be defined as 64 or 128 Kbytes for 8-bit memory or 128 or 256 Mbytes for 32-bit memory. The DRAM controller supports page mode access for successive transfers within bursts. The MPC860P supports a glueless interface to one bank of DRAM while external buffers are required for additional memory banks. The refresh unit provides $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$, a programmable refresh timer, refresh active during external reset, disable refresh mode, and stacking up to seven refresh cycles. The DRAM interface uses a programmable state machine to support almost any memory interface.

1.4 PCMCIA Controller

The PCMCIA interface is a master (socket) controller and is compliant with release 2.1. The interface supports up to two independent PCMCIA sockets requiring only external transceivers/buffers. The interface provides 8 memory or I/O windows in which each window can be allocated to a particular socket. If only one PCMCIA port is being used, the unused PCMCIA port may be used as general-purpose input with interrupt capability.

1.5 Power Management

The MPC860P supports a wide range of power management features including full-on, doze, sleep, deep sleep, and low-power stop.

- In full-on mode the MPC860P processor is fully powered with all internal units operating at the full speed of the processor. A gear mode is provided which is determined by a clock divider, allowing the operating system to reduce the operational frequency of the processor.
- Doze mode disables core functional units other than the time base decrementer, PLL, memory controller, RTC, and then places the CPM in low-power standby mode.
- Sleep mode disables everything except the RTC and PIT, leaving the PLL active for quick wake-up.
- Deep sleep mode disables the PLL for lower power but slower wake-up.
- Low-power stop disables all logic in the processor except the minimum logic required to restart the device, providing the lowest power consumption but requiring the longest wake-up time.

1.6 Communications Processor Module (CPM)

The CPM provides a flexible and integrated approach to communications-intensive environments. To reduce system frequency and save power, the CPM has its own independent RISC communications processor (CP) that is optimized for serial communications. The CP services several integrated communications controllers, performing low-level protocol processing and controlling DMA.

The CPM supports multiple communications channels and protocols, and it has flexible firmware programmability. The CPM frees the core of many computational tasks in the following ways:

- By reducing the interrupt rate. The core is interrupted only upon frame reception or transmission, instead of on a per-character basis.
- By implementing some of the OSI layer-2 processing, which provides more core bandwidth for higher layer processing.
- By supporting multibuffer memory data structures that are convenient for software handling.

The CPM in the MPC860P is derived from the CPM in the MC68360 QUICC; see the *MC68360 Quad Integrated Communications Controller (QUICC) User's Manual*. The MPC860P maintains the best features of the MC68360 QUICC, while making changes required to provide for the increased flexibility, integration, and performance requested by customers demanding the performance of the PowerPC architecture.

The following lists the CPM's main features:

- Communications processor (CP)
  - — 8 Kbytes of dual-port RAM
  - — Internal ROM
  - — Two physical serial DMA (SDMA) controllers implement sixteen SDMA channels, which provide two channels each for the communications controllers.
  - — Two independent DMA (IDMA) channels offer high-speed, 32-bit data movement with buffer chaining.
    - – Memory-to-memory transfers
    - – Interfacing external peripherals with independent request and acknowledge logic
  - — RISC timer tables
- MAC (multiply-and-accumulate) function enables various modem and DSP applications
- Four full-duplex serial communications controllers (SCCs)
- Two full-duplex serial management controllers (SMCs)
- Serial peripheral interface (SPI) support for master or slave modes
- Inter-integrated circuit (I^2C) bus controller
- A serial interface (SI) with a time-slot assigner (TSA) that supports time-division multiplexing of data from the SCCs and SMCs
- Parallel interface port (PIP)
- Four independent baud rate generators (BRGs)
- Four general-purpose 16-bit timers or two 32-bit timers
- CPM interrupt controller (CPIC)
- General-purpose I/O ports

1.7 Glueless System Design

Figure 2 shows the glueless connection of the MPC860P serial channels and UTOPIA interface to physical layer framers and transceivers.

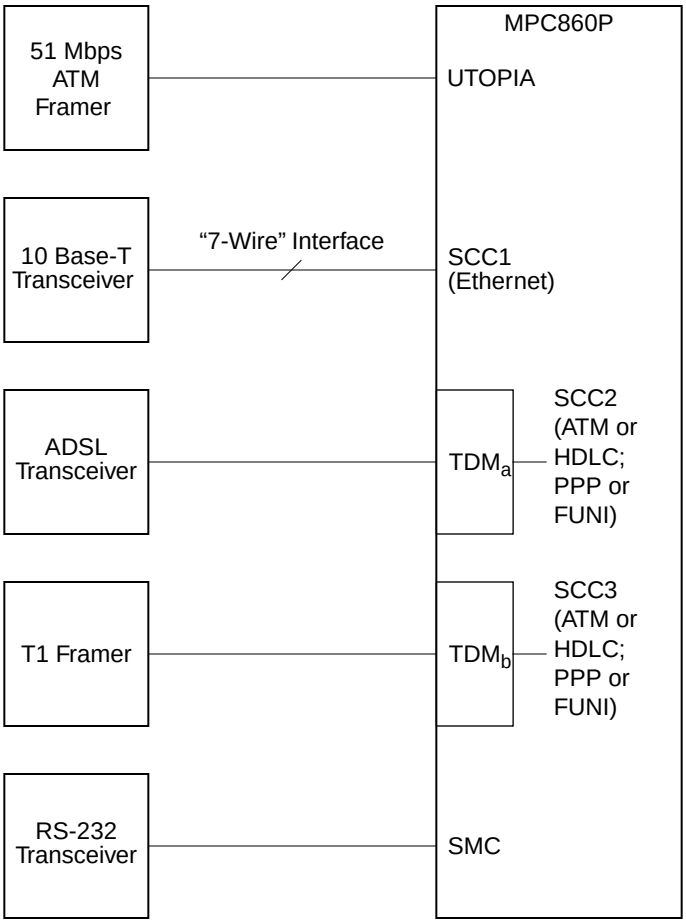

Figure 2. MPC860P System Configuration

1.8 Ordering Information

The following Motorola part numbers can be used for ordering purposes:

- XPC860PZP50D
- XPC860PZP66D
- XPC860PZP80D
- XPC860DPZP50D
- XPC860DPZP66D
- XPC860DPZP80D

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