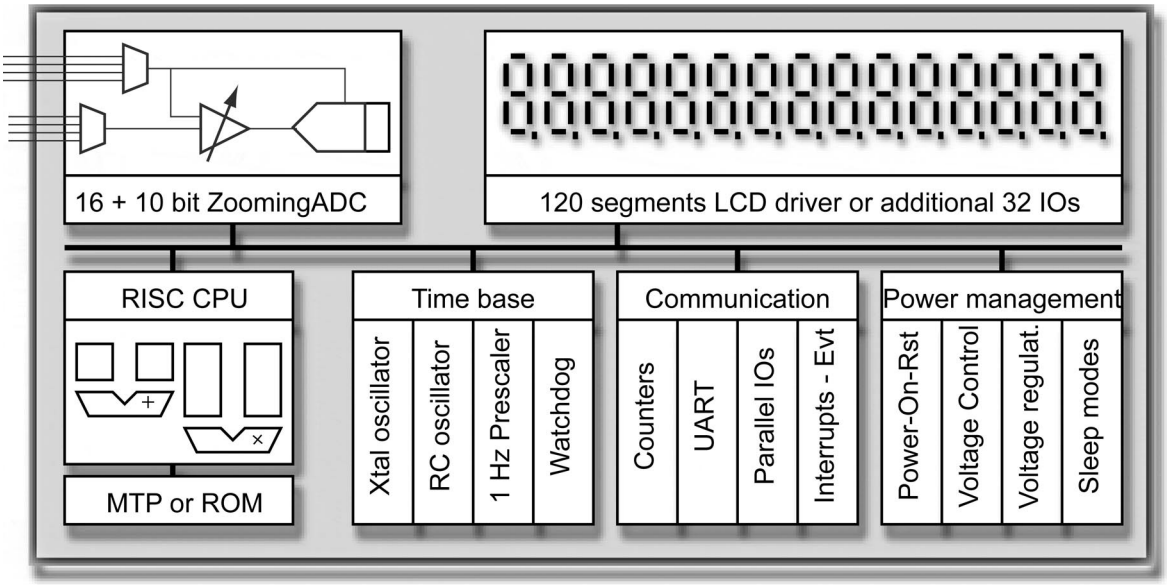
XEMICS

XE88LC02
Data Sheet
Preliminary



XE88LC02 Sensing Machine

Data Acquisition MCU with 16 + 10 bit ZoomingADC and LCD driver

General Description

- The XE88LC02 is a data acquisition ultra low-power low-voltage microcontroller unit (MCU) with extremely high efficiency, allowing for 1 MIPS at 300uA and 2.4 V, and 8 x 8 bits multiplying in one clock cycle at 1.2 V.
- XE88LC02 includes a high resolution acquisition path with the 16+10 bits ZoomingADC and an LCD driver for up to 120 segments. The LCD lines can be used as additional IOs.
- XE88LC02 is available with on chip ROM or Multi-ple-Time-Programmable (MTP) program memory.

Applications

- Portable, battery operated instruments
- RF system supervisor
- Remote control
- HVAC control
- Metering
- Sports watches, wrist instruments

Key product Features

- Low-power, high resolution ZoomingADC
  - 0.5 to 1000 gain with offset cancellation
  - up to 16 bits ADC
  - up to 13 input multiplexer
- 4 low power comparators
- Low-voltage low-power controller operation
  - 4 MIPS at 2.4 V to 5.5 V supply voltage
  - 300 µA at 1 MIPS, 2.4 V to 5.5 V supply
- 22 kByte (8 kInstruction) MTP, 1032 Byte RAM
- RC and crystal oscillators
- 5 reset, 24 interrupt, 16 event sources
- 120 segments LCD driver, can be used for IOs

Ordering Information

- **ES** identifies engineering samples
- **XX** identifies pre-production products
- **XE** identifies qualified products

Product	Temperature range	Memory type	Package
XE88LC02MI000	-40°C to 85 °C	MTP	die
XE88LC02MI035	-40°C to 85 °C	MTP	LQFP100

XEMICS SA, Switzerland. Tel: +41 32 720 5511 Fax: +41 32 720 5770 email: info@xemics.com web: www.xemics.com

2 Detailed Pin Description

3 Absolute maximum ratings

Stresses beyond these listed in this chapter may cause permanent damage to the device. No functional operation is implied at or beyond these conditions. Exposure to these conditions for an extended period may affect the device reliability.

Parameter	Valéue
VBAT with respect to VSS	-0.3V to 6.0V
Input voltage on any input pin	VSS-0.3V to VBAT+0.3V
Storage temperature	-55°C to 125°C
Storage temperature for programmed MTP devices	-40°C to 85°C

Table 3.1: Absolute maximum ratings

These devices are ESD sensitive. Although these devices feature proprietary ESD protection structures, permanent damage may occur on devices subjected to high energy electrostatic discharges. Proper ESD precautions have to be taken to avoid performance degradation or loss of functionality.

4 Electrical Characteristics

All specification are -40°C to 85°C unless otherwise noted. ROM operates up to 125°C.

Operation conditions		min	typ	max	Unit	Remarks
Power supply	ROM version	2.4		5.5	V	
	MTP version	2.4		5.5	V	
Operating speed	2.4 V to 5.5 V	0.032		4	MHz	
Instruction cycle	any instruction		250		ns	7
Current requirement	CPU running at 1 MIPS			310	uA	1
	CPU running at 32 kHz on Xtal, RC off			10	uA	1
	CPU halt, timer on Xtal, RC off			1	uA	1
	CPU halt, timer on Xtal, RC ready			1.7	uA	1
	CPU halt, Xtal off timer on RC at 100 kHz			1.4	uA	1
Current requirement	CPU halt, ADC 16 bits at 4 kHz		190		uA	4,6
	CPU halt, ADC 12 bits at 4 kHz, PGA gain 100		460		uA	4,6
	CPU at 1 MIPS, ADC 12 bits at 4 kHz		670		uA	3,4,6
	CPU at 1 MIPS, ADC 12 bits at 4 kHz, PGA gain 10		790		uA	3,4,6
	CPU at 1 MIPS, ADC 12 bits at 4 kHz, PGA gain 100		940		uA	3,4,6
	CPU at 1 MIPS, ADC 12 bits at 4 kHz, PGA gain 1000		1100		uA	3,4,6
	Voltage level detection			15	uA	
MTP Flash instruction memory	Prog. voltage	10.3		10.8	V	
	Erase time	0.2		1	s	8
	Write/Erase cycles	10	100			5
	Data retention	10			year	2

Table 4.1: Specifications and current requirement of the XE88LC02

Note:
1) Power supply: 2.4 V - 5.5 V, temperature is 27°C.
2) Temperature < 85°C, < 10 erase cycles.
3) Output not loaded.
4) Current requirement can be divided by a factor of 2 or 4 by reducing the speed accordingly.
5) More cycles possible during development, with restraint retention
6) Power supply: 3.0V, at 27°C; see chapter Power Consumption on page 22 for variation of current with voltage and clock speed variation
7) With 4 MHz clock, all instructions are using exactly 1 clock cycle
8) Longer erase time may degrade retention

5 CPU

The XE88LC02 CPU is a low power RISC core. It has 16 internal registers for efficient implementation of the C compiler. Its instruction set is made of 35 generic instructions, all coded on 22 bits, with 8 addressing modes. All instructions are executed in one clock cycle, including conditional jumps and 8x8 multiplication.

A complete tool suite for development is available from XEMICS, including programmer, C-compiler, assembler, simulator, linker, all integrated in a modern and efficient graphical user interface.

6 Memory organisation

The CPU uses a Harvard architecture, so that memory is organised in two separated fields: program memory and data memory. As both memory are separated, the central processing unit can read/write data at the same time it loads an instruction. Peripherals and system control registers are mapped on data memory space.

Program memory is made in one page. Data is made of several 256 bytes pages.

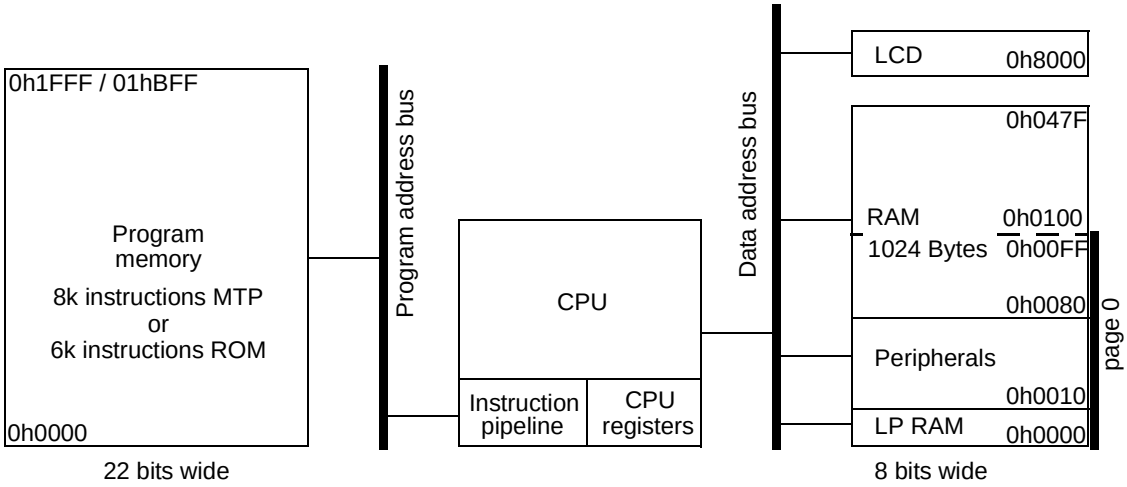


Figure 6.1: Memory organization

6.1 Program memory

The program memory is implemented as Multiple Time Programmable (MTP) Flash memory. The power consumption of MTP memory is linear with the access frequency (no significant static current).

- Size of the MTP Flash memory is 8192 x 22 bits (= 22 kBytes)
- Size of the ROM memory is 6144 x 22 bits (= 17 kBytes)

block	size	address
MTP	8192 x 22	H0000 - H1FFF
ROM	6144 x 22	H0000 - H1BFF

Table 6.1: Program addresses for MTP or ROM memory

6.2 Data memory

The data memory is implemented as static Random-Access Memory (RAM). The RAM size is 512 x 8 bits plus 8 low power RAM bytes that require very low current when addressed. Programs using the low-power RAM instead of RAM will use even less current.

block	size	address
LP RAM	8 x 8	H0000 - H0007
RAM	1024 x 8	H0080 - H047F

Table 6.2: RAM addresses

6.3 Peripherals mapping

block	size	address	Page
LP RAM	8x8	H0000-H0007	Page 0
System control	16x8	H0010-H001F	
Port A	8x8	H0020-H0027	
Port B	8x8	H0028-H002F	
Port C	4x8	H0030-H0033	
Port D	4x8	H0034-H0037	
MTP	4x8	H0038-H003B	
Event	4x8	H003C-H003F	
Interrupts control	8x8	H0040-H0047	
reserved	8x8	H0048-H004F	
UART	8x8	H0050-H0057	
Counters	8x8	H0058-H005F	
Zooming ADC	8x8	H0060-H0067	
SPI	8x8	H0068-H006F	
Reserved	12x8	H0070-H007B	
Other (VLD)	4x8	H007C-H007F	
RAM1	128x8	H0080 - H00FF	
RAM2	256x8	H0100 - H01FF	
RAM3	256x8	H0200 - H02FF	
RAM4	256x8	H0300 - H03FF	
RAM5	128x8	H0400 - H047F	
LCD	32x8	H8000-H803F	

Table 6.3: Peripherals addresses

7 Peripherals

The XE88LC02 includes usual microcontroller peripherals and some other blocks more specific to low-voltage or mixed-signal operation. They are 3 parallel ports, one input port (A), one IO and analog port (B) with analog switching capabilities and one general purpose IO port (C). A watchdog is available, connected to a prescaler. Four 8-bit counters, with capture, PWM and chaining capabilities are available. The UART can handle transmission speeds as high as 115kbaud.

Low-power low-voltage blocks include a voltage level detector, two oscillators (one internal 0.1-4 MHz RC oscillator and a 32 kHz crystal oscillator) and a specific regulation scheme that largely uncouples current requirement from external power supply (usual CMOS ASICs require much more current at 5.5 V than they need at 2.4 V. This is not the case for the XE88LC02).

Analog blocks (ZoomingADC (acquisition path)) are defined below. All these blocks operate on 2.4 - 5.5 V power supply range.

7.1 Counters

- 4 8-bit counters
- Daisy chain on 16 bits
- PWM on 8-16 bits
- Capture - compare on 16 bits
- Events and interrupts generation

7.2 Prescaler

- Interrupt generated with 1 second period for ultra low power hibernation mode

7.3 Watchdog

- 2 seconds watchdog

7.4 UART

- full duplex operation with buffered receiver and transmitter.
- Internal baudrate generator with programmable baudrate (300 - 115000 bauds).
- 7 or 8 bits word length.
- even, odd, or no-parity bit generation and detection
- 1 stop bit
- error receive detection : Start, Parity, Frame and Overrun
- receiver echo mode
- 2 interrupts (receive full and transmit empty)
- enable receive and/or transmit
- invert pad Rx and/or Tx

7.5 SPI

- dedicated lines for hardware SPI interface.

7.6 Xtal clock

The Xtal Oscillator operates with an external crystal of 32’768 Hz.

symbol	description	min	typ	max	unit	comments
f_clk32k	nominal frequency		32768		Hz	
st_x32k	oscillator start-up time		1	2	s	for full precision
duty_clk32k	duty cycle on the digital output	30	50	70	%	
fstab_1	relative frequency deviation from nominal, for a crystal with CL=8.2 pF and temperature between -40° and +85°C	-100		+300	ppm	not included: crystal frequency tolerance and aging crystal frequency - temperature dependence

Table 7.1: Xtal oscillator specifications.

Note: Board layout recommendations for safer crystal oscillation and lower current consumption:
Keep lines xtal_in and xtal_out short and insert a VSS line between them.
Connect package of the crystal to VSS.
No noisy or digital lines near xtal_in and xtal_out.
Insert guards at VSS where needed.

7.7 RC oscillator

The RC Oscillator is always turned on at power-on reset and can be turned off after the optional Xtal oscillator has been started. The RC oscillator has two frequency ranges: sub-MHz (100KHz to 1MHz) and above-MHz (1MHz to max MCU frequency). Inside a range, the frequency can be tuned by software for coarse and fine adjustment.

Note: No external component is required for the RC oscillator.

The RC oscillator can be in 3 modes. In mode 1(RC on), the RC oscillator and its bias are on. In mode 2 (RC ready), the RC oscillator is off and the bias is on. In mode 3 (RC off), the RC oscillator and the bias are off. RC ready mode is a compromise between power consumption and start-up time.

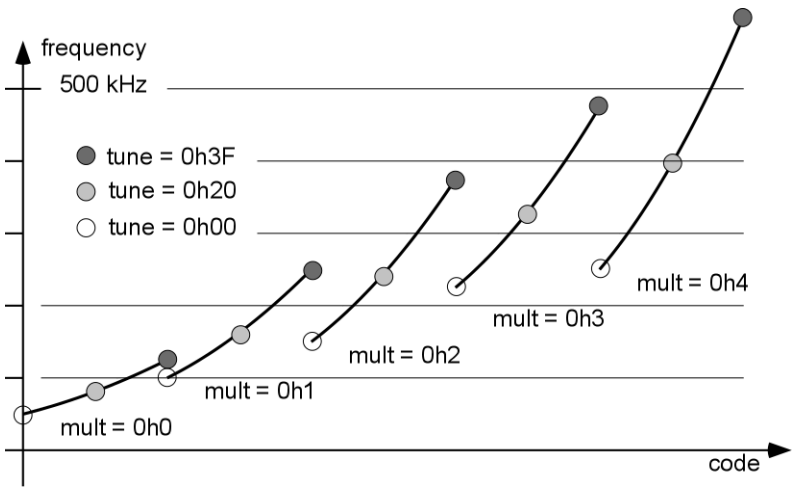


Figure 7.1: RC frequencies programming example for low range (typical values)

symbol	description	min	typ	max	unit	comments
F_{st}	frequency at start-up	40	80	120	kHz	
range	range selection	1		10		multiplies F_{st}

Table 7.2: RC specifications

symbol	description	min	typ	max	unit	comments
mult[3:0]	coarse tuning range	1		16		4 bits, multiplies F_{st} * range
tune[5:0]	fine tuning range	0.65		1.5		6 bits, multiplies F_{st} * range * mult
	fine tuning step		1.4	2	%	
T_{st}	start-up time		30	50	µs	bias current is off (RC off)
O_{st}	overshoot at start-up			50	%	bias current is off (RC off)
T_{wu}	wakeup time		3	5	µs	bias current is on (RC ready)
O_{wu}	overshoot at wakeup			50	%	bias current is on (RC ready)
jit	jitter rms		2		$^{o}/_{oo}$	

Table 7.2: RC specifications

7.8 Parallel IO ports

- up to 68 IO lines:
- 8 bit input port A with interrupt, reset and event generation.
- 8 bit input-output-analog port B with analog switching capabilities.
- 2 x 8 bit input-output port C.
- 32 lines from LCD driver can be used as additional IOs.
- 4 lines from SPI interface can be used as additional IOs.

sym	description	condition	min	typ	max	unit	Comments
	Port A: low threshold limit	Vbat = 1.2 V				V	
	Port A: high threshold limit					V	
	output drop when sinking 1 mA				0.4	V	
	output drop when sourcing 1 mA				0.4	V	
	Port A: low threshold limit	Vbat = 2.4 V		1		V	
	Port A: high threshold limit			1.5		V	
	output drop when sinking 1 mA					V	
	output drop when sinking 8 mA				0.4	V	
	output drop when sourcing 1 mA					V	
	output drop when sourcing 8 mA				0.4	V	
	Port A: low threshold limit	Vbat = 5.0 V		2		V	
	Port A: high threshold limit			3		V	
	output drop when sinking 1 mA					V	
	output drop when sinking 8 mA				0.4	V	
	output drop when sourcing 1 mA					V	
	output drop when sourcing 8 mA				0.4	V	
	pull-up, pull-down resistor		50		150	kohm	

Table 7.3: IO pins performances

7.9 Voltage level detector

- Can be switched off, on or simultaneously with CPU activities
- Generates an interrupt if power supply is below a pre-determined level

The Voltage Level Detector monitors the state of the system battery. It returns a logical high value (an interrupt) in the status register if the supplied voltage drops below the user defined level.

symbol	description	min	typ	max	unit	comments	
Vth	Threshold voltage	Note 1			V	trimming values:	
						VldRange	VldT
			1.53			0	00
			1.44			0	00
			1.36			0	01
			1.29			0	01
			1.22			0	10
			1.16			0	10
			1.11			0	11
			1.06			0	11
			3.06			1	00
			2.88			1	00
			2.72			1	01
			2.57			1	01
			2.44			1	10
			2.33			1	10
			2.22			1	11
			2.13			1	11
T_{EOM}	duration of measurement		2.0	2.5	ms	Note 2	
T_{PW}	Minimum pulse width detected		875	1350	us	Note 2	

Table 7.4: Voltage level detector operation

Note: **1)** Absolute precision of the threshold voltage is ±10%.
2) This timing is respected in case the internal RC or crystal oscillators are selected. Refer to the clock block documentation in case the external clock is used.

8 ZoomingADC

The fully differential acquisition chain is formed of a programmable gain (0.5 - 1000) and offset amplifier and a programmable speed and resolution ADC (example: 12 bits at 4 kHz, 16 bits at 1 kHz). It can handle inputs with very low full scale signal and large offsets.

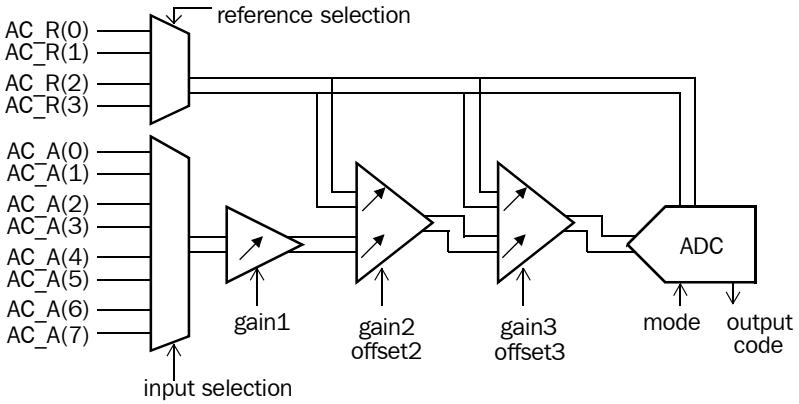


Figure 8.1: Acquisition channel block diagram

Input selection is made from 1 of 4 differential pair or 1 of seven single signal versus AC_A(0). Reference is chosen from the 2 differential references. Acquisition path offset can be suppressed by inverting input polarity.

The gain of each amplifier is programmed individually. Each amplifier is powered on and off on command to minimize the total current requirement. All blocks can be set to low frequency operation and lower their current requirement by a factor 2 or 4.

The ADC can run continuously (end of conversion signalled by an interrupt, event or by pooling the ready bit), or it can be started on request.

8.1 PGA 1

symbol	description	min	typ	max	unit	Comments
GD1	PGA1 Signal Gain	1		10	-	GD1 = 1 or 10
GD_preci	Precision on gain settings	-5		+5	%	
GD_TC	Temperature dependency of gain settings	-5		+5	ppm/°C	
fs	input sampling frequency			512	kHz	
Zin1	Input impedance	150			kΩ	1
Zin1p	Input impedance for gain 1	1500			kΩ	1
VN1	Input referred noise		18		nV/ sqrt(Hz)	2

Table 8.1: PGA1 Performances

Note: 1) Measured with block connected to inputs through AMUX block. Normalized input sampling frequency for input impedance is 512 kHz. This figure has to be multiplied by 2 for fs = 256 kHz and 4 for fs = 128 kHz.
2) Input referred rms noise is 10 uV per input sample. This corresponds to 18 nV/sqrt(Hz) for fs = 512 kHz.

8.2 PGA2

sym	description	min	typ	max	unit	Comments
GD2	PGA2 Signal Gain	1		10	-	GD2 = 1, 2, 5 or 10
GDoff2	PGA2 Offset Gain	-1		1	FS	
GDoff2_step	GDoff2(code+1) – GDoff2(code)	0.18	0.2	0.22	-	
GD_preci	Precision on gain settings	-5		+5	%	valid for GD2 and GDoff2
GD_TC	Temperature dependency of gain settings	-5		+5	ppm/°C	
fs	Input sampling frequency			512	kHz	
Zin2	Input impedance	150			kΩ	1
VN2	Input referred noise		36		nV/ sqrt(Hz)	2

Table 8.2: PGA2 Performances

Note: 1) Measured with block connected to inputs through AMUX block. Normalized input sampling frequency for input impedance is 512 kHz. This figure has to be multiplied by 2 for fs = 256 kHz and 4 for fs = 128 kHz.
2) Input referred rms noise is 26uV per sample.This corresponds to 36 nV/sqrt(Hz) max for fs = 512 kHz.

8.3 PGA3

sym	description	min	typ	max	unit	Comments
GD3	PGA3 Signal Gain	0		10	-	
GDoff3	PGA3 Offset Gain	-5		5	FS	
GD3_step	GD3(code+1) - GD3(code)	0.075	0.08	0.085	-	
GDoff3_step	GDoff2(code+1) – GDoff2(code)	0.075	0.08	0.085	-	
GD_preci	Precision on gain settings	-5		+5	%	valid for GD3 and GDoff3
GD_TC	Temperature dependency of gain settings	-5		+5	ppm/°C	
fs	Input sampling frequency			512	kHz	
Zin3	Input impedance	150			kΩ	1
VN3	Input referred noise		36		nV/ sqrt(Hz)	2

Table 8.3: PGA3 Performances

Note: 1) Measured with block connected to inputs through AMUX block. Normalized input sampling frequency for input impedance is 512 kHz. This figure has to be multiplied by 2 for fs = 256 kHz and 4 for fs = 128 kHz.
2) Input referred rms noise is 26uV per sample. This corresponds to 36 nV/sqrt(Hz) max for fs = 512 kHz.

8.4 Analog to digital converter (ADC)

The wholeanalog to digital conversion sequence is basically made of an initialisation, a set of Nelconv elementary incremental conversions and finally a termination phase(**N_{umCONV}** is set by 2 bits on **RegACCfg0**). The result is a mean of the results of the elementary conversions.

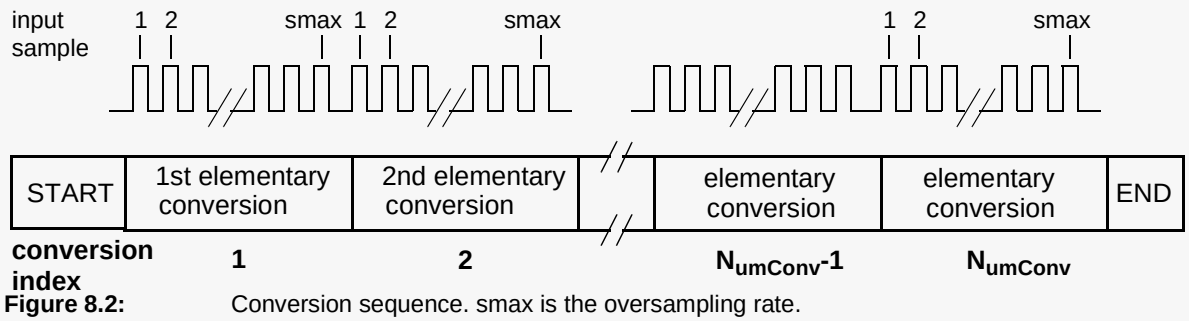


Figure 8.2: Conversion sequence. smax is the oversampling rate.

Note: **N_{umCONV}** elementary conversions are performed, each elementary conversion being made of smax input samples.

$N_{umCONV} = 2^{NELCONV}$

$smax = 8*2^{OSR}$

During the elementary conversions, the operation of the converter is the same as in a sigma delta modulator. During one conversion sequence, the elementary conversions are alternatively performed with direct and crossed PGA-ADC differential inputs, so that when two elementary conversions or more are performed, the offset of the converter is cancelled.

Some additional clock cycles (N_{INIT}+N_{END}) clock cycles are used to initiate and terminate the conversion properly.

8.5 ADC performances

sym	description	min	typ	max	unit	Comments
VINR	Input range	-0.5		0.5	Vref	
Resol	Resolution	6		16	bits	
NResol	Numerical resolution			16	bits	3
DNL	Differential non-linearity	-0.1		0.1	LSB	LSB at 16 bits
INL	Integral non-linearity	-3		2	LSB	2, LSB at 16 bits
fs	sampling frequency	10		512	kHz	
smax	Oversampling Ratio	8		1024	-	1
N_{UMCONV}	Number of elementary conversions in incremental mode	1		8	-	1
Ninit	Number of periods for incremental conversion initialization			5	-	
Nend	Number of periods for incremental conversion termination			5	-	

Table 8.4: ADC Performances

Note: 1) Only powers of 2
2) INL is defined as the deviation of the DC transfer curve from the best fit straight line. This specification holds over 100% of the full scale.
3) NResol is the maximal readable resolution of the digital filter.

8.6

resolution	conditions	input frequency.	convertion time.	output frequency.
6	oversampling per convertion = 8 1 conversion (no offset rejection)	512 kHz	40 us	25 kHz
8	oversampling per convertion = 16 1 conversion (no offset rejection)	512 kHz	50 us	20 kHz
12	oversampling per convertion = 64 1 conversion (no offset rejection)	512 kHz	150 us	6.7 kHz
13	oversampling per convertion = 64 2 convertions (offset rejection)	512 kHz	275 us	3.6 kHz
16	oversampling per convertion = 256 1 convertion (no offset rejection)	512 kHz	500 us	2 kHz
16	oversampling per convertion = 256 2 convertions (offset rejection)	512 kHz	1 ms	1 kHz
16	oversampling per convertion = 1024 8 convertions (offset rejection)	512 kHz	16.5 ms	60 Hz

Table 8.5: ADC performances examples

8.7 Linearity

To quantify linearity errors, Integral Non-Linearity (INL) and Differential Non-Linearity (DNL) were measured for the ADC alone and for gains of 1, 5, 10, 20, 100, 1000, and a resolution of 12 bits and 16 bits.

INL is defined as the deviation (in LSB) of the DC transfer curve of each individual code from the best-fit straight line. This specification holds over the full scale.

DNL is defined as the difference (in LSB) between the ideal (1 LSB) and measured code transitions for successive codes. INL and DNL are specified after gain and offset errors have been removed.

8.8 Integral Non-Linearity (INL) and Differential Non-Linearity (DNL) for <u>12-bit resolution</u>

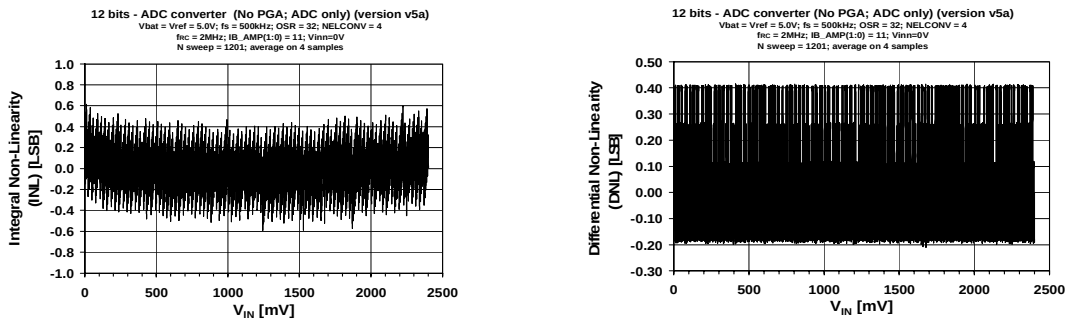


Figure 8.3: NO GAIN (ONLY ADC), 12 bit ADC setting

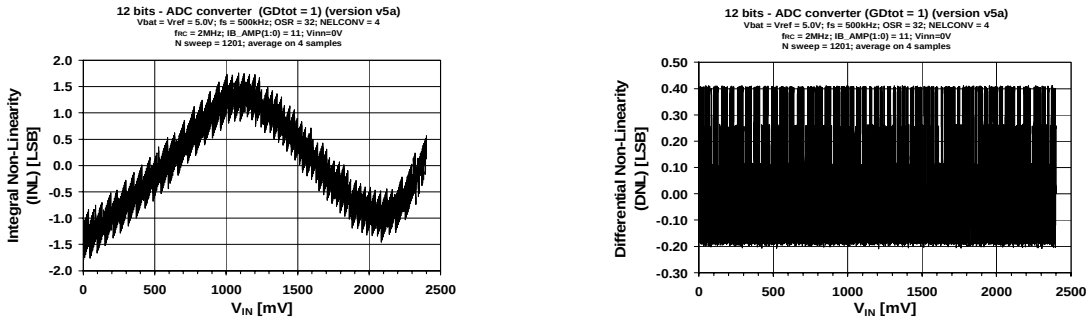


Figure 8.4: GAIN=1, 12 bit ADC setting

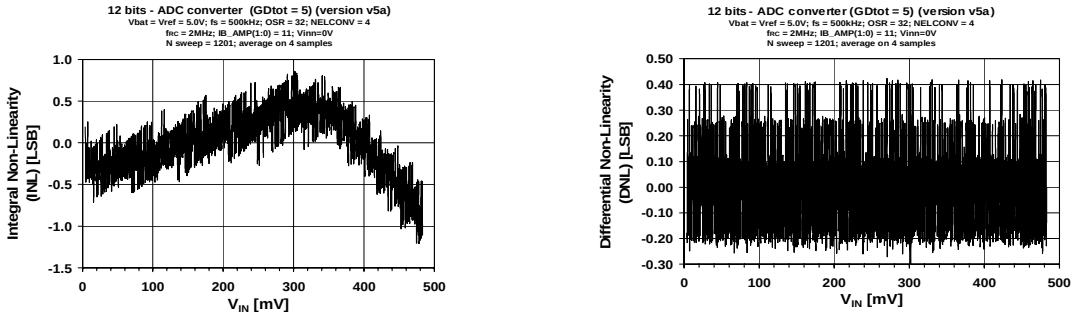


Figure 8.5: GAIN=5, 12 bit ADC setting

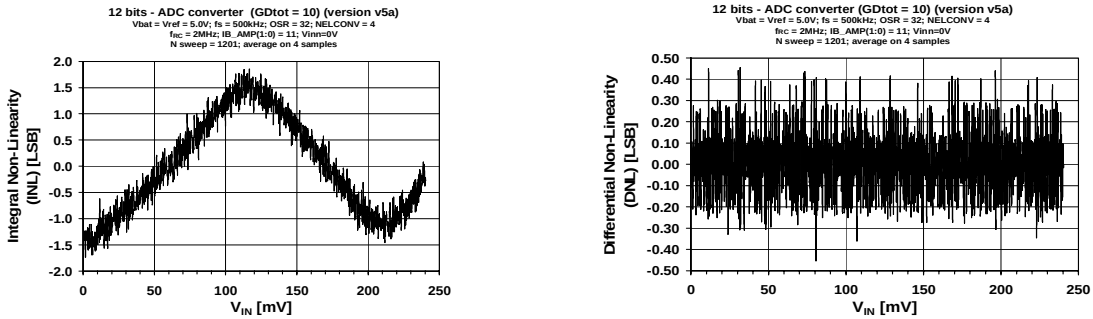
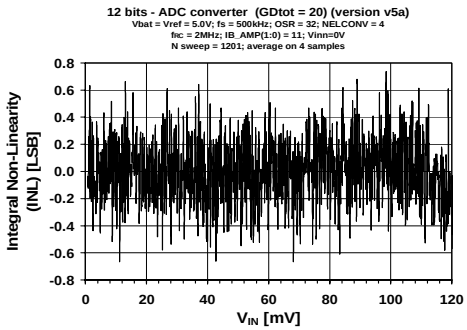


Figure 8.6: GAIN=10, 12 bit ADC setting



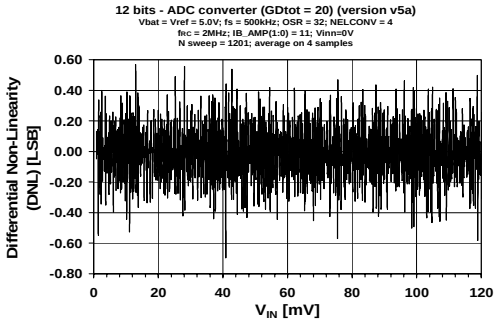
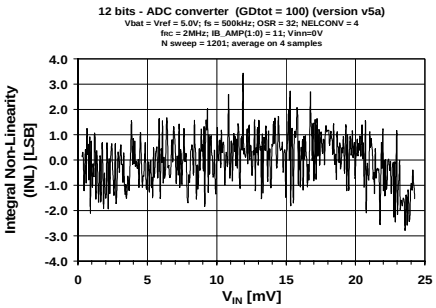


Figure 8.7: GAIN=20, 12 bit ADC setting



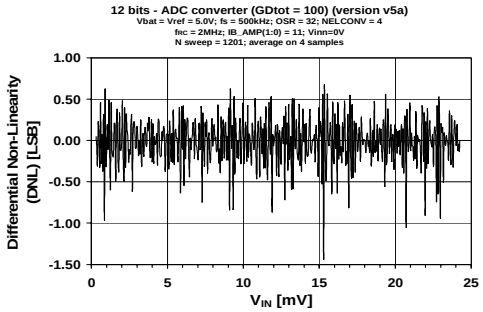
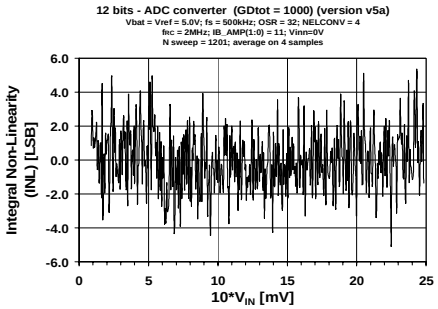


Figure 8.8: GAIN=100, 12 bit ADC setting



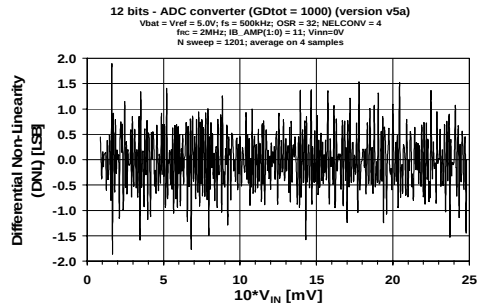


Figure 8.9: GAIN=1000, 12 bit ADC setting

8.9 Integral Non-Linearity (INL) and Differential Non-Linearity (DNL) for 16-bit resolution

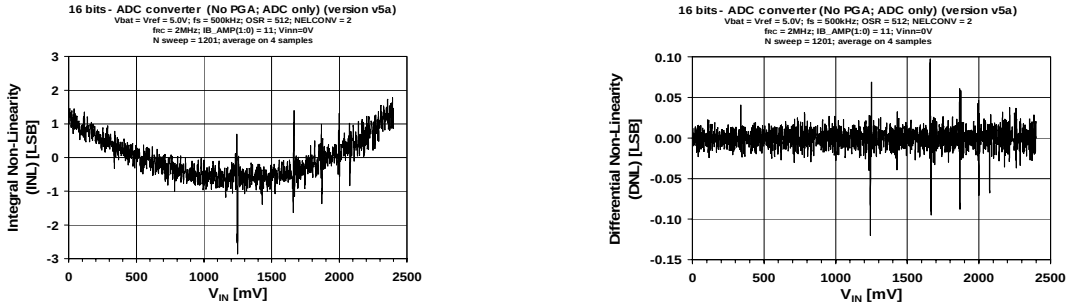


Figure 8.10: NO GAIN (ONLY ADC), 16 bit ADC setting

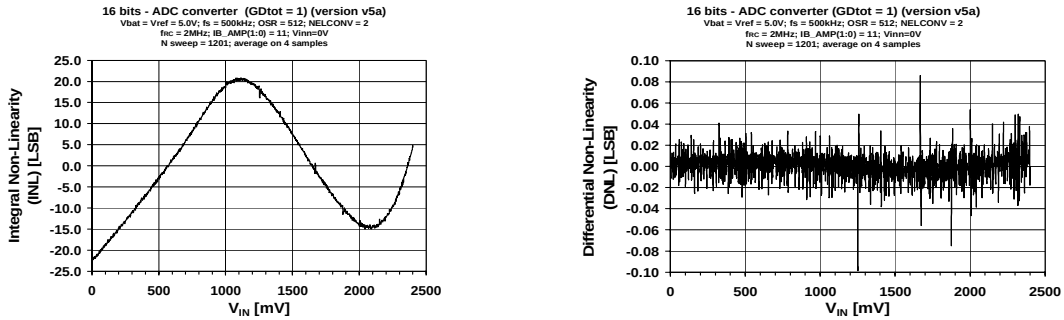


Figure 8.11: GAIN=1, 16 bit ADC setting

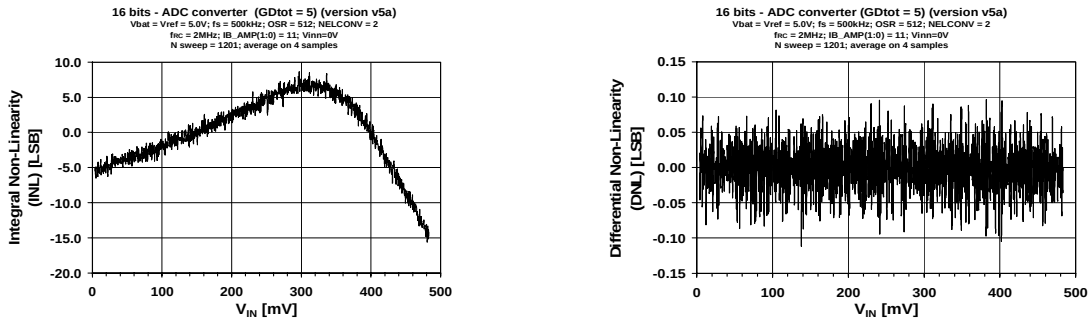


Figure 8.12: GAIN=5, 16 bit ADC setting

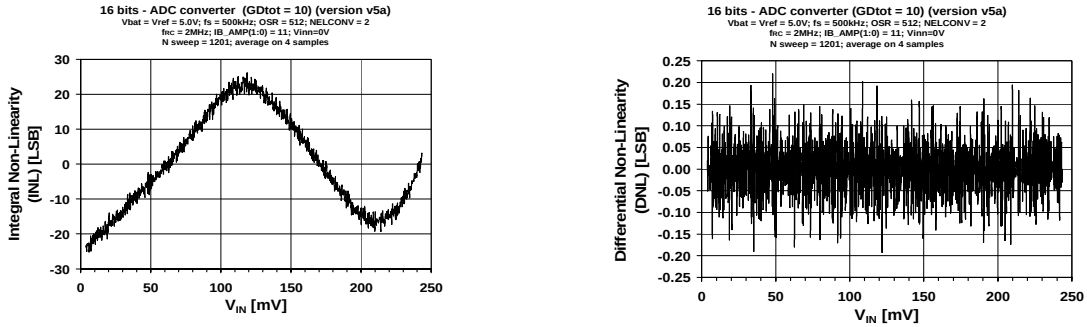


Figure 8.13: GAIN=10, 16 bit ADC setting

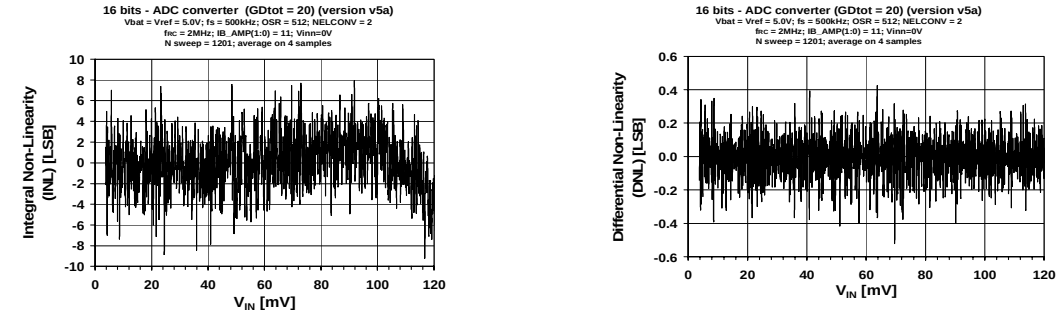


Figure 8.14: GAIN=20, 16 bit ADC setting

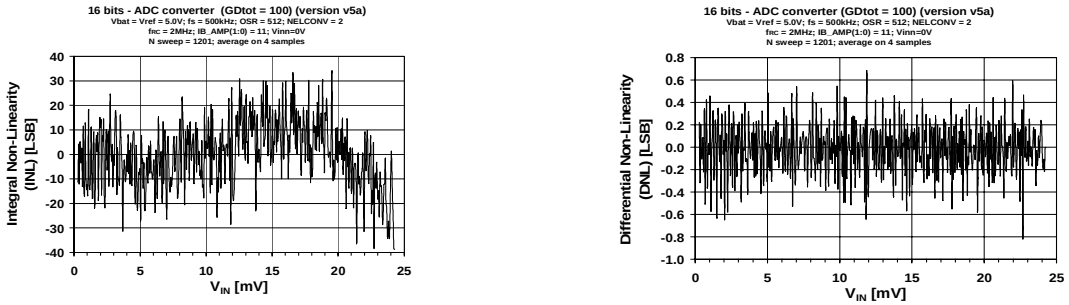


Figure 8.15: GAIN=100, 16 bit ADC setting

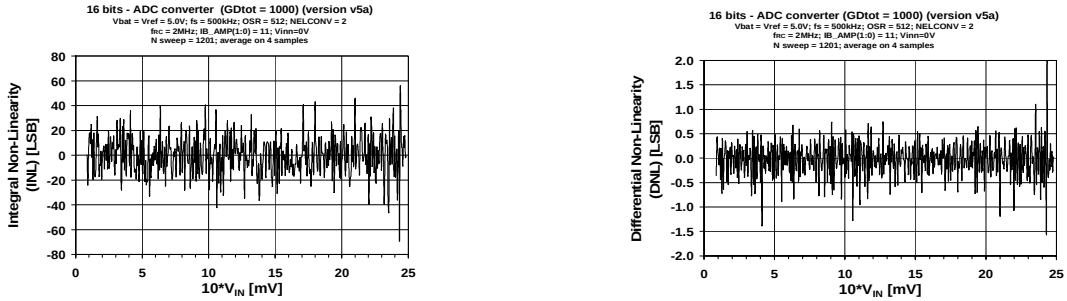


Figure 8.16: GAIN=1000, 16 bit ADC setting

The gain settings of each PGA stage for the plots of above figure are those of the table below.

PGA Gain GD_{TOT} (V/V)	PGA1 Gain GD1 (V/V)	PGA2 Gain GD2 (V/V)	PGA3 Gain GD3 (V/V)
1	1	bypassed	bypassed
5	1	5	bypassed
10	10	bypassed	bypassed
20	10	2	bypassed
100	10	10	bypassed
1000	10	10	10

Table 8.6: Individual PGA gains for INL & DNL measurements

Table 8.7:

Noise

Ideally, a constant input voltage V_{IN} should result in a constant output code. However, because of circuit noise, the output code may vary for a fixed input voltage. The figure shows the distribution for the ADC alone (PGA1, 2, and 3 bypassed) and of several configurations of the PGAs. Quantization noise is dominant in this case of ADC only, and, thus, the ADC thermal noise is negligible.

One has to considere two points when computing final noise of the acquisition chain:

- this is a type of amplifier (switched-cap with constant capacitive load) that maintains its output noise when changing the gain. Therefore input refered noise is lowered when the gain of an amplifier is increased.
- the ADC is oversampled, and the number of samples taken lowers the thermal noise

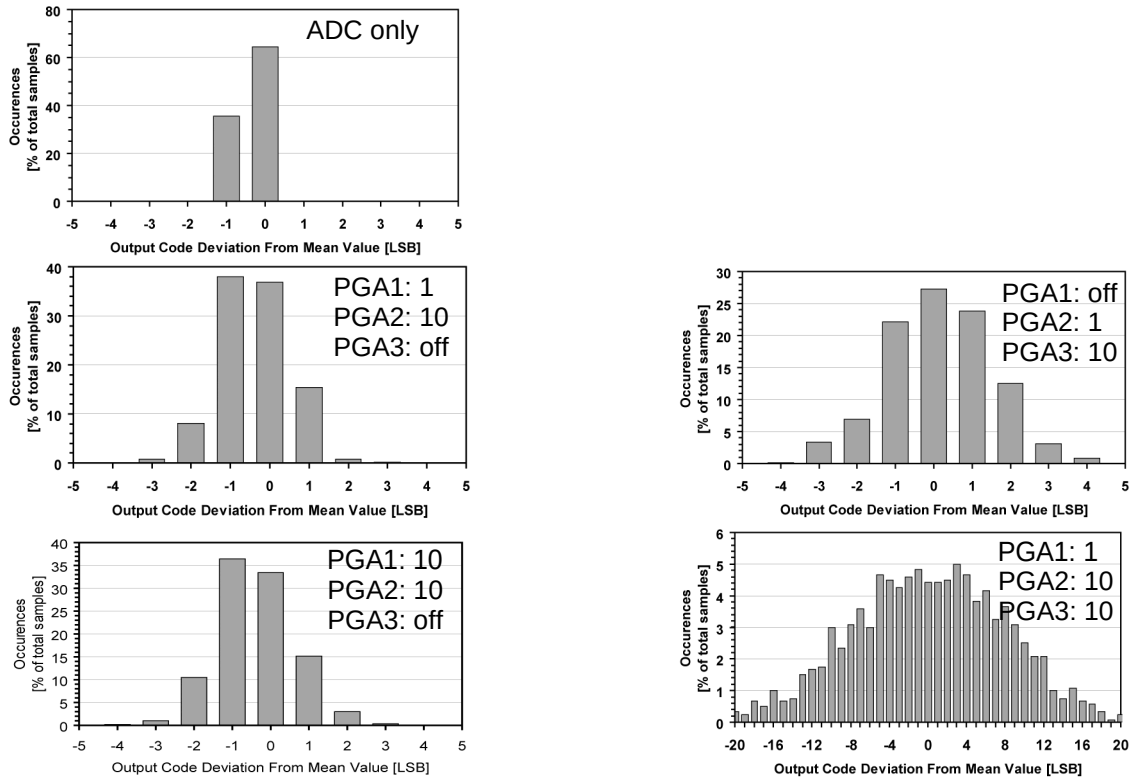
Total input refered noise can be computed using the following equation:

$$V^2_{n,\,in} = \frac{\left(\frac{V_{n,\,out1}}{gain1}\right)^2 + \left(\frac{V_{n,\,out2}}{gain1 \cdot gain2}\right)^2 + \left(\frac{V_{n,\,out3}}{gain1 \cdot gain2 \cdot gain3}\right)^2}{numconv \cdot smax}$$

Where $V_{n,outx}$ is the rms output noise of amplifier x.

Amplifier	Symbol	Typical output noise per over-sample	Unit
PGA1	$V_{n,out1}$	205	uVrms
PGA2	$V_{n,out2}$	340	uVrms
PGA3	$V_{n,out3}$	365	uVrms

Typical output noise of ZoomingADC preamplifiers



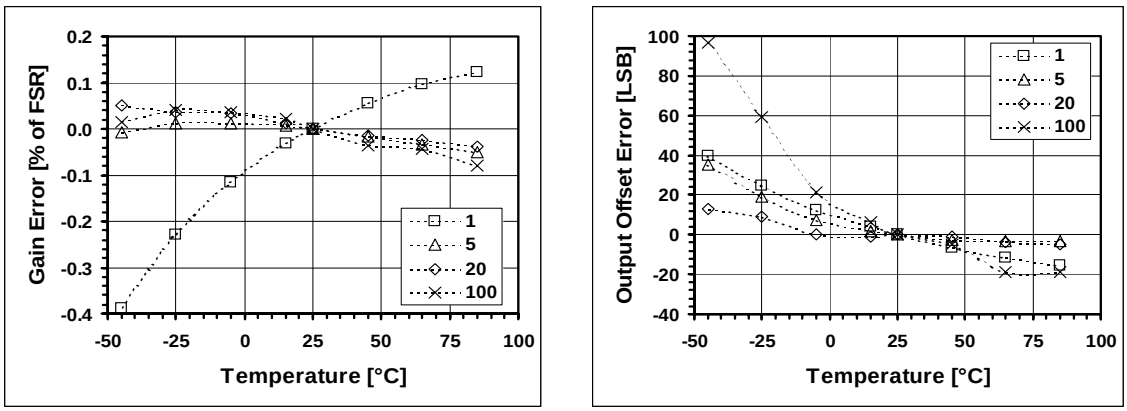
Noise measured at the output of the ZoomingADC

As one can see on the figures above, increase the gain of the first amplifier lowers the output noise for constant global gain. It also lowers sensitivity to temperature drift as offset is better compensated on first amplifier.

Gain Error and Offset Error

Gain error is defined as the amount of deviation between the ideal transfer function and the measured transfer function (with the offset error removed). The left figure shows gain error vs. temperature for different PGA gains. The curves are expressed in% of Full-Scale Range (FSR) normalized to 25°C.

Offset error is defined as the output code error for a zero volt input (ideally, output code = 0). The measured offset errors vs. temperature curves for different PGA gains are depicted in the right figure below. The output offset error, expressed in (LSB), is normalized to 25°C.



Gain and offset error vs temperature for several gains, normalized to 25°C, offset cancellation disabled. When the offset cancellation is enabled, the offset of PGA1 and ADC remains below the LSB in all temperature situations.

8.10 Power Consumption

Left figure below plots the variation of quiescent current consumption with supply voltage V_{DD}, as well as the distribution between the 3 PGA stages and the ADC. As shown in the right figure, quiescent current consumption is not greatly affected by sampling frequency. It can be seen that the quiescent current varies by about 20% between 100kHz and 2MHz. Quiescent current consumption vs. temperature is shown in the second set of figures, showing a relative increase of nearly 40% between -45 and +85°C.

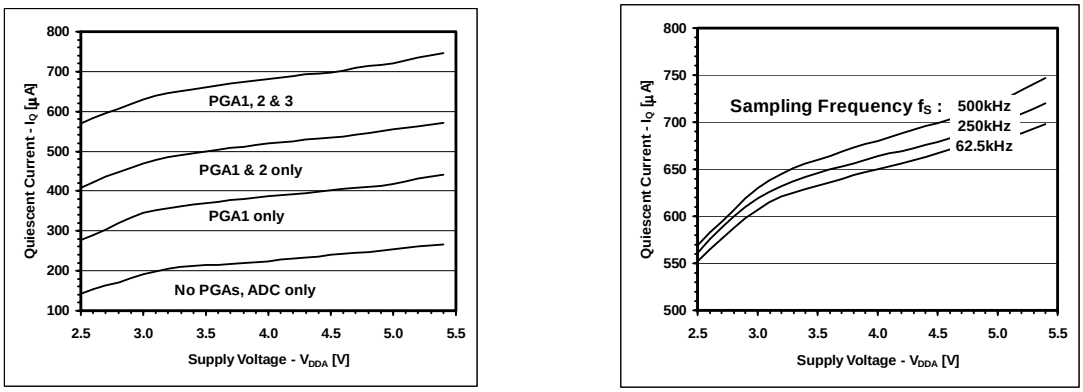


Figure 8.17: Quiescent current versus supply voltage for different gains and clock speed (not using the PGA and ADC low power modes)

Supply	ADC	PGA1	PGA2	PGA3	TOTAL	Unit
V_{DD} = 5V	250	165	130	175	720	µA
V_{DD} = 3V	190	150	120	160	620	µA

Table 8.8: Typical quiescent current distributions in acquisition chain (n = 16 bits, f_S = 500kHz)

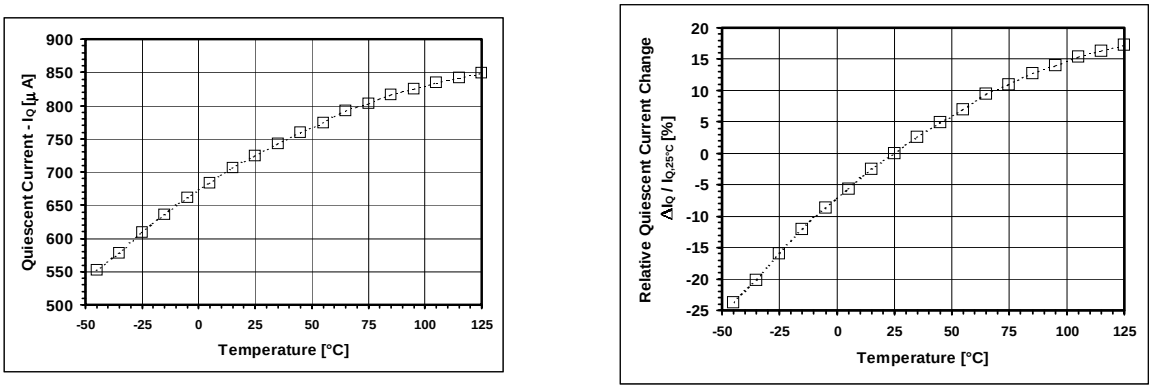


Figure 8.18: Absolute and (b) relative change in quiescent current consumption vs. temperature

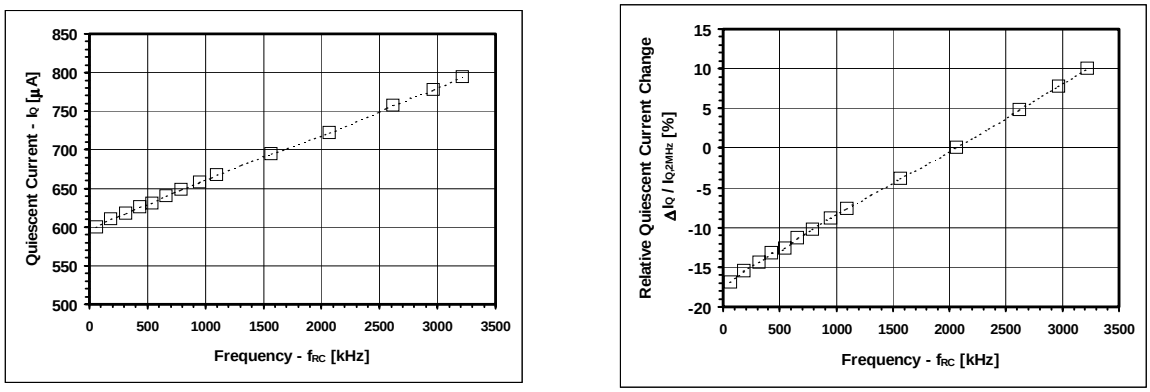


Figure 8.19: Absolute and (b) relative change in quiescent current consumption vs. clock speed

8.11 Power Supply Rejection Ratio

Figure below shows power supply rejection ratio (PSRR) at 3V and 5V supply voltage, and for various PGA gains. PSRR is defined as the ratio (in dB) of voltage supply change (in V) to the change in the converter output (in V). PSRR depends on both PGA gain and supply voltage V_{DD}.

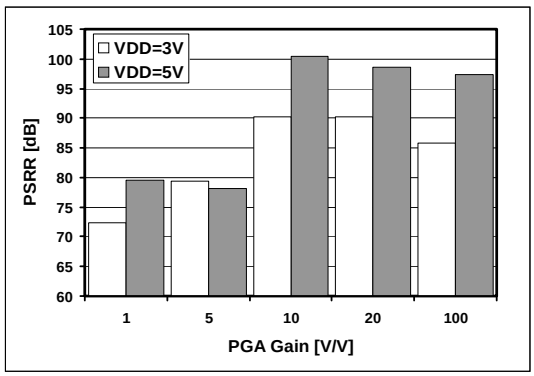


Figure 8.20: Power supply rejection ratio (PSRR)

Supply	GAIN = 1	GAIN =5	GAIN = 10	GAIN = 20	GAIN =100	Unit
V_{DD} = 5V	79	78	100	99	97	dB
V_{DD} = 3V	72	79	90	90	86	dB

Table 8.9: PSRR (n = 16 bits, $V_{IN} = V_{REF}$ = 2.5V, f_S = 500kHz)

8.12 Frequency Response

The incremental ADC of the XE88LC02 is an over-sampled converter with two main blocks: an analog modulator and a low-pass digital filter. The main function of the digital filter is to remove the quantization noise introduced by the modulator. As shown below, this filter determines the frequency response of the transfer function between the output of the ADC and the analog input V_{IN}. Notice that the frequency axes are normalized to one elementary conversion period OSR/f_S. The plots below also show that the frequency response changes with the number of elementary conversions N_{ELCONV} performed. In particular, notches appear for $N_{ELCONV} \geq 2$. These notches occur at:

$$f_{NOTCH}(i) = \frac{i \cdot f_S}{OSR \cdot N_{ELCONV}} \text{ (Hz)} \quad \text{for} \quad i = 1,2,...,(N_{ELCONV} - 1)$$

and are repeated every f_S/OSR.

Information on the location of these notches is particularly useful when specific frequencies must be filtered out by the acquisition system. For example, consider a 5Hz-bandwidth, 16-bit sensing system where 50Hz line rejection is needed. Using the above equation and the plots below, we set the 4th notch for N_{ELCONV} = 4 to 50Hz, i.e. $1.25 \cdot f_S/OSR$ = 50Hz. The sampling frequency is then calculated as f_S = 20.48kHz for OSR = 512. Notice that this choice yields also good attenuation of 50Hz harmonics.

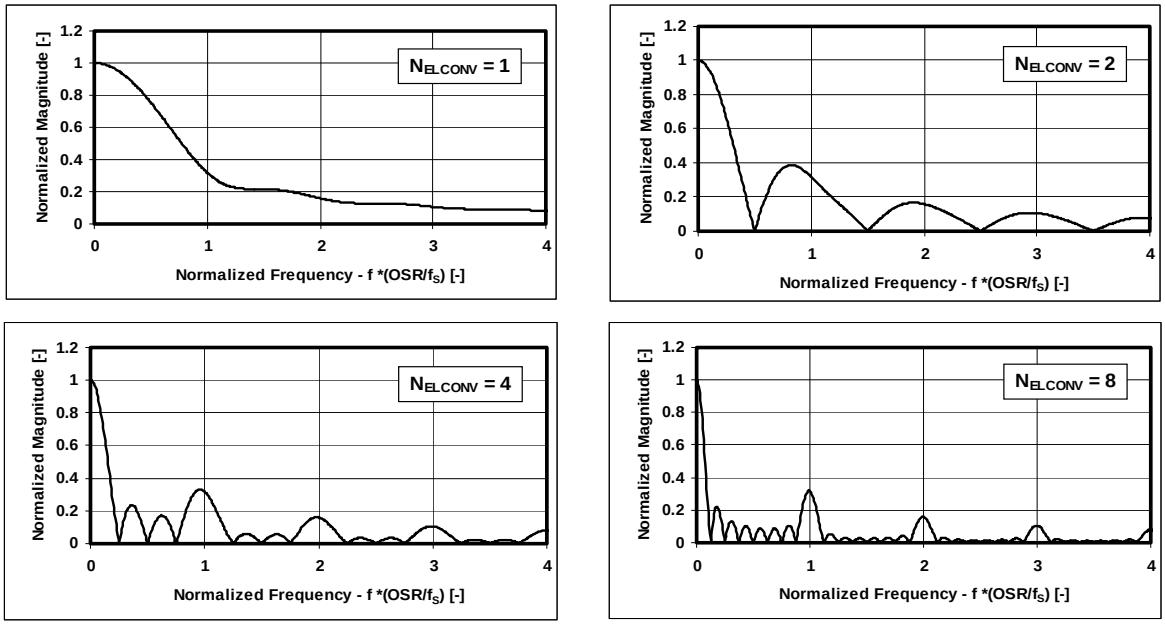


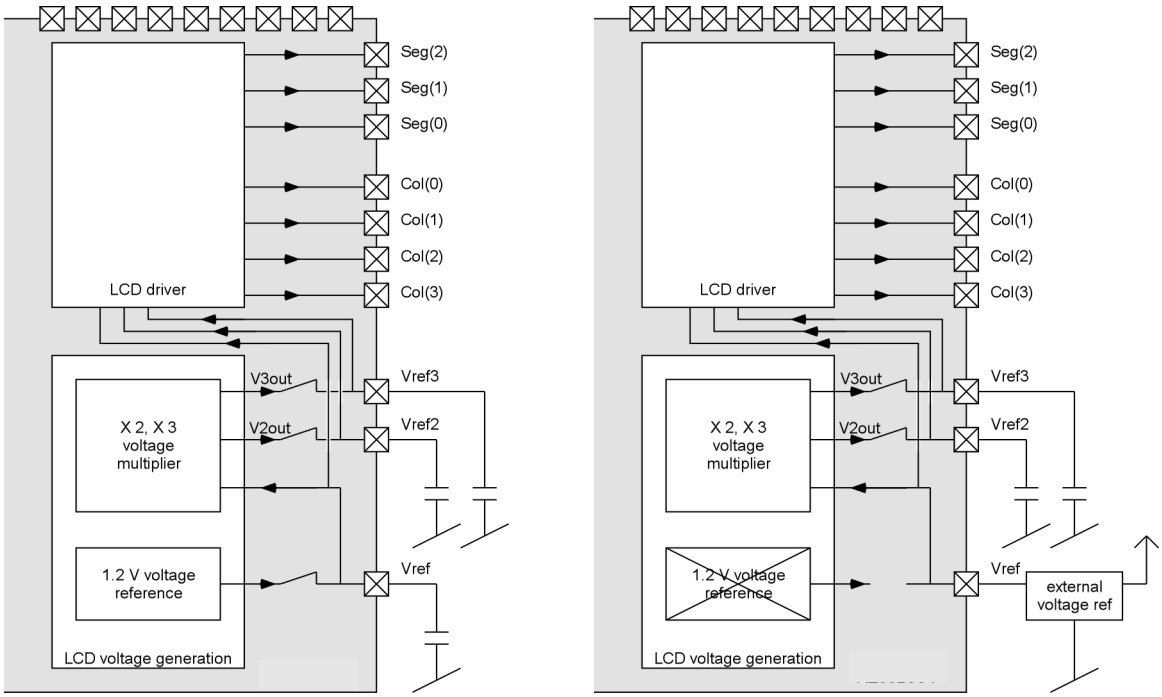
Figure 8.21: Frequency response: normalized magnitude vs. frequency for different N_{ELCONV}

9 LCD drivers

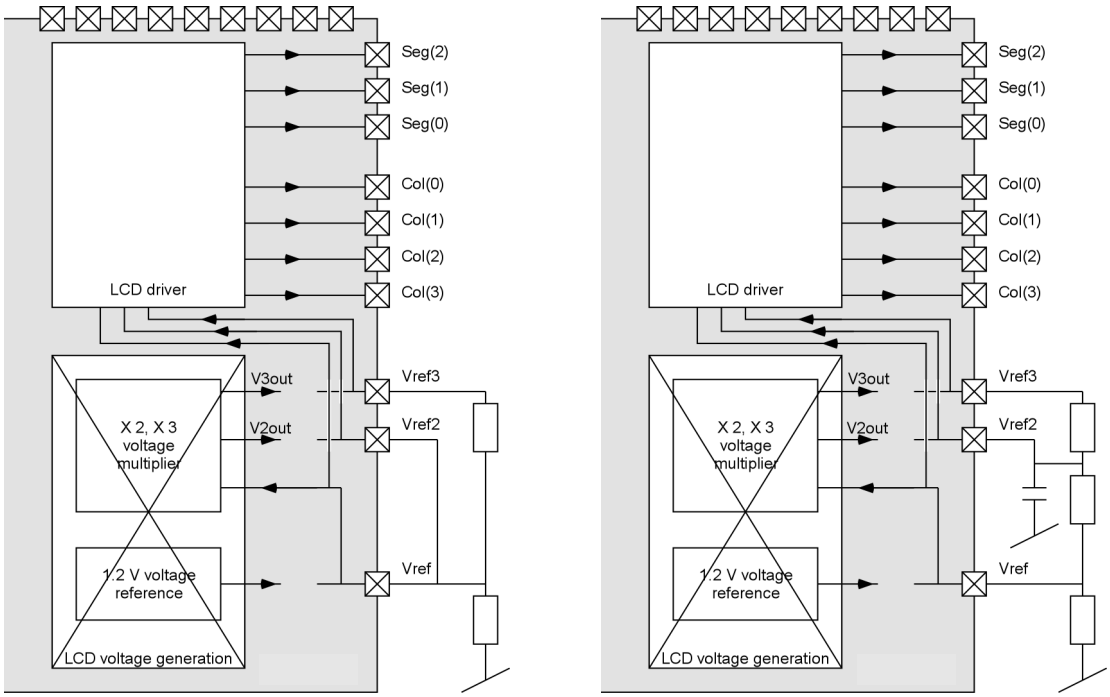
The XE88LC02 includes LCD drivers for up to 120 segments. Multiplex can be chosen between 1 and 4. Intermediate voltages for multiplex signals can be generated on chip, even at very low power supply, thanks to a 1.2 V voltage reference and to 2 voltage multipliers.

The voltage generator of the XE88LC02 can be used in a multitude of ways: for generating absolute voltages (above or below Vbat), for generating voltages relative to Vbat, or for generating voltages relative to an external reference. This great variety of possibilities make possible to have devices compensated for temperature, or to operate LCD with good contrast even with limited voltage supply.

Pads can be shared between LCD and IO mode. This is done in goups of 4 pads when Vbat is equal to Vref3. It is made in 2 packets of 4 and 8 pins when Vbat is different from Vref3.



igure 9.1: Generating absolute voltages for the LCD driver, either with internal reference (left) or



igure 9.2: Using voltages proportional to Vbat (power supply) for multiplex by two (left) or three or four

10 Physical description

10.1 LQFP100 package

Figure 10.1:

10.2 LQFP80 package

Figure 10.2:

11 Contacting XEMICS

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You will find more information about the XE88LC02 and other XEMICS products, as well as the addresses of our representatives and distributors for your region on www.xemics.com.