Preliminary

XR-T7234

E3 UNI (User Network Interface) IC for ATM

December 1997–1

FEATURES

- Compliant with UTOPIA Level 2 Interface Specification
- Supports 8 or 16 Bit UTOPIA Bus Operating at 25MHz or 33MHz or 50MHz
- User Programmable Cell Filter
- OAM Cell and GFC Field Extraction and Insertion
- Receive UTOPIA Interface Contains 4 Cell Deep FIFO
- Transmit UTOPIA Interface Contains up to 16 Cell Deep FIFO (Variable Depth)
- 52, 53 and 54 Byte Cell Formats Supported
- Programmable Idle Cell Generation
- Microprocessor Interface Compliant with Motorola and Intel
- Microprocessor Interface Supports Burst Mode Access
- LAPD Processor for Data Link Messages
- Identical Pinout with XR-T7245, DS3 ATM UNI
- 160 and 100 Pin PQFP

APPLICATIONS

- ATM Switches
- ATM Routers and Bridges
- ATM Concentrators

GENERAL DESCRIPTION

The XR-T7234 E3 ATM User Network Interface (UNI) device is designed to provide the ATM Physical Layer (Physical Medium Dependent and Transmission Convergence sub-layers) interface for the public and private networks at E3 rates. This device provides full-duplex data flow between two ATM layer devices (e.g., such as ATM switch) over an E3 transport medium.

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
XR-7234A	100 Lead PQFP (14mm x 20mm)	-40°C to +85°C
XR-7234B	160 Lead PQFP (28mm x 28mm)	-40°C to +85°C

EXAR Corporation, 48720 Kato Road, Fremont, CA 94538 ◆ (510) 668-7000 ◆ FAX (510) 668-7017

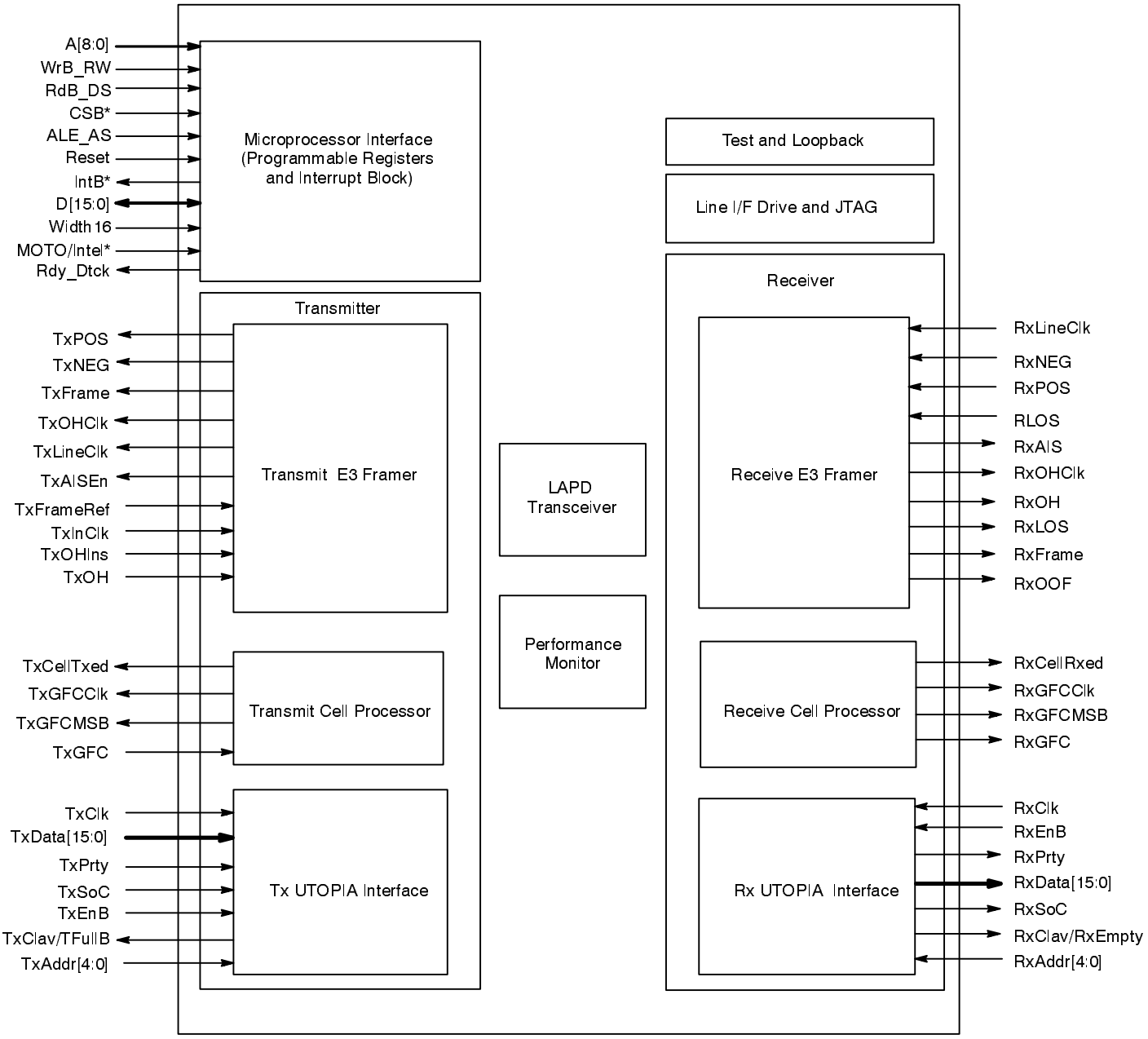


Figure 1. Block Diagram of the XR-T7234 E3 ATM UNI

SYSTEM DESCRIPTION

The Receive Section

The purpose of the Receiver section within the XR-T7234 E3 ATM UNI device is to allow a local ATM Layer (or ATM Adaptation Layer) processor to receive ATM cell data from a remote terminal via a public or leased E3 transport medium.

In the Receive Direction, the UNI device will:

The Receive E3 Framer will synchronize to the incoming E3 data stream and remove or process the E3 Framing/Overhead Bits. This procedure will result in extracting ATM Cell data, from the incoming E3 data stream. The Receive E3 Framer includes an on-chip LAPD Receiver that supports path maintenance data link messages.

Note:
The Receive E3 Framer supports the ITU-T G.832 Framing Format.

The Receive Cell Processor will perform the following functions:

- Cell Delineation
- HEC byte verification of incoming cells (optional)
- Cell-payload de-scrambling (optional)
- Idle cell detection and removal (optional)
- User and OAM Cell Filtering (optional)

The XR-T7234 provides 54 bytes of on-chip RAM that allows for the reception and processing of selected OAM cells.

- The Receive UTOPIA Interface will write the ATM cells to the Receive FIFO (within the Receive UTOPIA Block) where they can be read by the ATM Layer device, over the UTOPIA Bus.

The Transmit Section

The purpose of the Transmit section of the XR-T7234 E3 ATM UNI device is to allow a local ATM Layer (or ATM Adaptation Layer) processor to transmit ATM Cell data to a remote piece of equipment via a public or leased E3 transport medium.

In the Transmit Direction, the UNI device will:

- Allow the ATM Layer processor to write ATM cells into the Transmit FIFO (within the Transmit UTOPIA block).
- The Transmit Cell Processor will retrieve these cells from the Transmit FIFO (if available). If no cell is available in the Transmit FIFO, then the Transmit Cell Processor will automatically generate an Idle cell. The UNI is equipped with on-chip registers to allow for the generation of customized Idle cells.
- The UNI provides 54 bytes of on-chip RAM that allows for the generation and transmission of customized OAM cells. The Transmit Cell Processor will transmit these OAM cells upon software command.
- The Transmit Cell Processor will optionally scramble the Cell Payload and optionally compute and insert the HEC (Header Error Check) byte. This HEC byte will be inserted into the fifth octet of each cell prior to being transferred to the Transmit E3 Framer. These ATM cells will be inserted into the payload portion of an outbound E3 Frame; for transmission to the "far–end" terminal, by the Transmit E3 Frame. The Transmit E3 Framer can transmit PMDL (Path Maintenance Data Link) messages to the "far-end " terminal via the on-chip (LAPD) transceiver.

FEATURES

UTOPIA Interface

- Compliant with UTOPIA Level 2 Interface Specification (e.g., supports Single-PHY or Multi-PHY operation).
- Supports 8 or 16 bit UTOPIA Data Bus operation in the Transmit and Receive Directions.
- The UTOPIA Data Bus run at clock rates of 25MHz, 33MHz or 50MHz.
- Supports Octet-Level and Cell-Level Handshaking between UNI and ATM Layer processor.
- Performs parity checking of input ATM cell data from ATM Layer processor. Will optionally discard errored cells.
- Contains on-chip 16 cell FIFO in the Transmit Direction (TxFIFO).
- Contains on-chip 4 cell FIFO in the Receive Direction (RxFIFO).

Transmit Cell Processor

- Optionally computes and inserts HEC byte into all cells (user, OAM and Idle).
- Optionally scrambles the payload of each cell.
- Idle cells are automatically generated when no user cells are available in the TxFIFO.
- UNI contains on-chip registers that support the generation/transmission of default or custom Idle cells.
- UNI contains on-chip buffer (54 bytes) that allows the generation of custom or default OAM cells.
- OAM cells are transmitted upon software command.
- Performs data path integrity check on cell data from the ATM Layer processor.
- Provides a serial port to allow the user to insert the GFC (Generic Flow Control) field externally into the GFC nibble field of an outbound (Transmit) ATM Cell.

Receive Cell Processor

- Performs cell delineation.
- Verifies the HEC bytes of incoming cells and corrects most cells with single bit errors.
- Cells with multi-bit errors are optionally discarded.
- Performs filtering of Idle Cells.
- Performs filtering of User cells.
- UNI contains on-chip buffer space that allows for the reception and processing of selected OAM cells.
- Optionally de-scrambles the payload of each cell.
- Provides a serial port that allows the user to read the GFC value of an incoming (Receive) ATM Cell.
- Supports Data Path Integrity Checking.

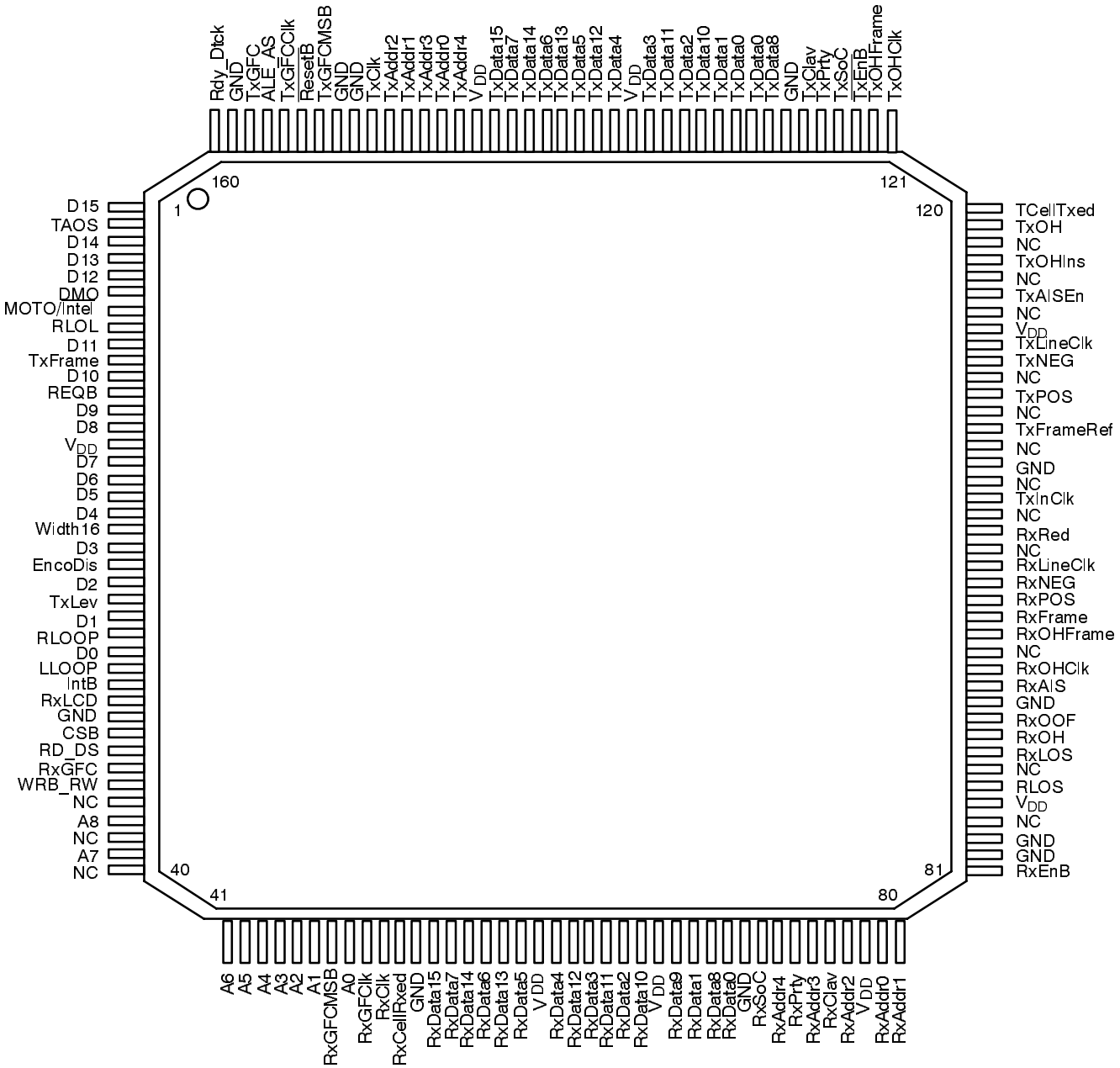
Transmit/Receive E3 Framer

- ITU-T .832 Framing Format is supported.
- Transmit and Receive E3 Framers can transmit/receive data in Unipolar or Bipolar (AMI or HDB3 line codes) format.
- Provides a serial port that allows the user to insert his/her own values for the Transmit E3 Frame Overhead bytes.
- Provides a serial port that allows the user access to the values of the incoming (Receive) E3 Frame Overhead bytes.
- The Receive E3 Framer can be configured to sample the incoming E3 data (at the RxPOS and RxNEG input pins) via the rising edge or falling edge of the Receive Line Clock (RxLineClk) input.
- The Transmit E3 Framer can be configured to update the outgoing E3 data (at the TxPOS and TxNEG output pins) at the rising edge or falling edge of the Transmit Line Clock (TxLineClk) output.
- XR-T7234 includes on-chip RAM space to support the transmission/reception of path maintenance data link (PMDL) messages via an on-chip LAPD Transceiver.
- Contains on-chip LAPD Transceiver

Miscellaneous

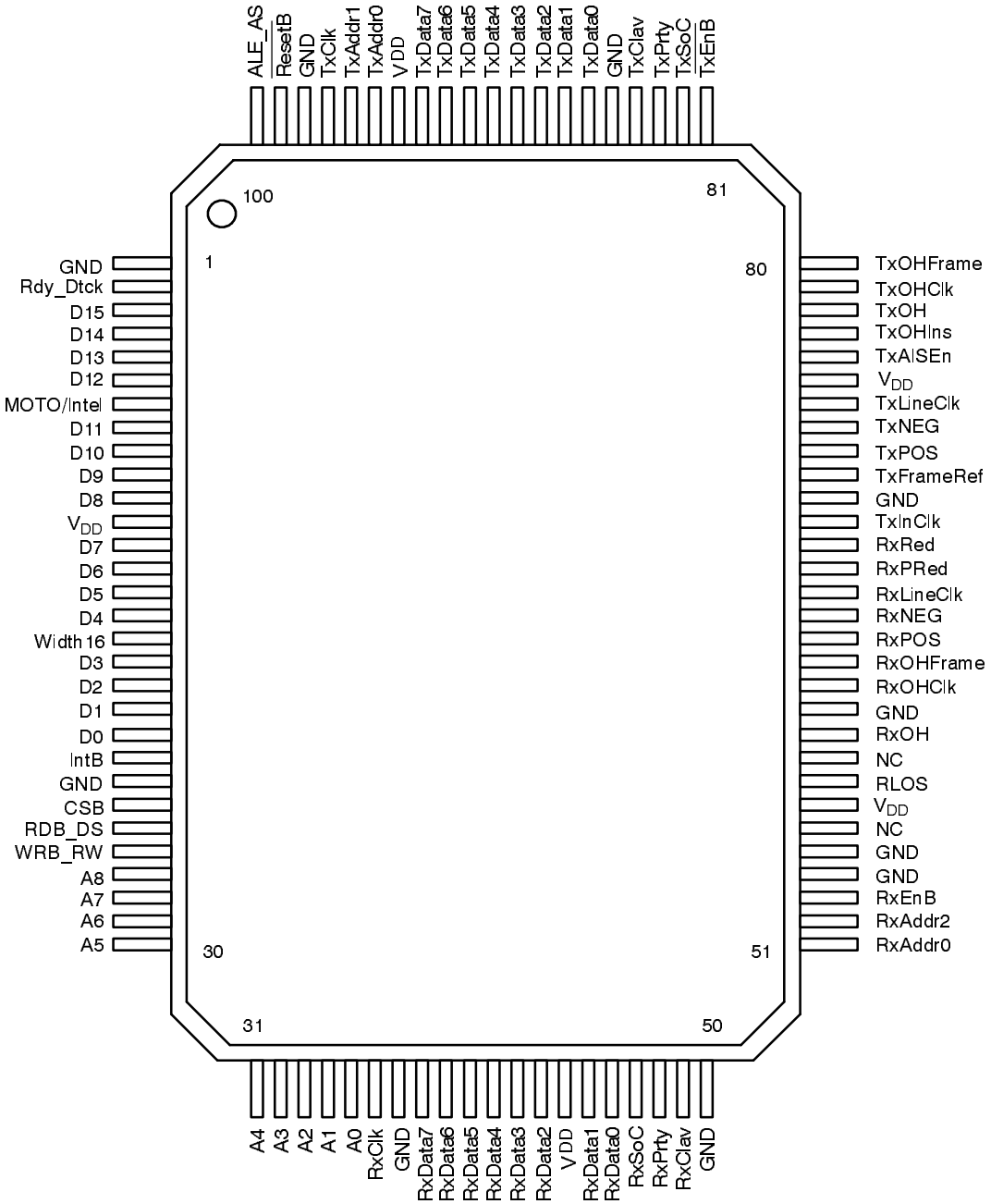
- Supports Line and Cell Loop-back Modes.
- Can be interfaced to Motorola or Intel type of microprocessors/microcontrollers.
- Supports polled or interrupt driven environments.
- +5V Power Supply, CMOS Technology.
- Available in either 160 pin or 100 pin PQFP Packages.
- Pin-for-pin compatible with the XR-T7245 DS3 UNI Device.

PIN CONFIGURATION



160 Lead PQFP

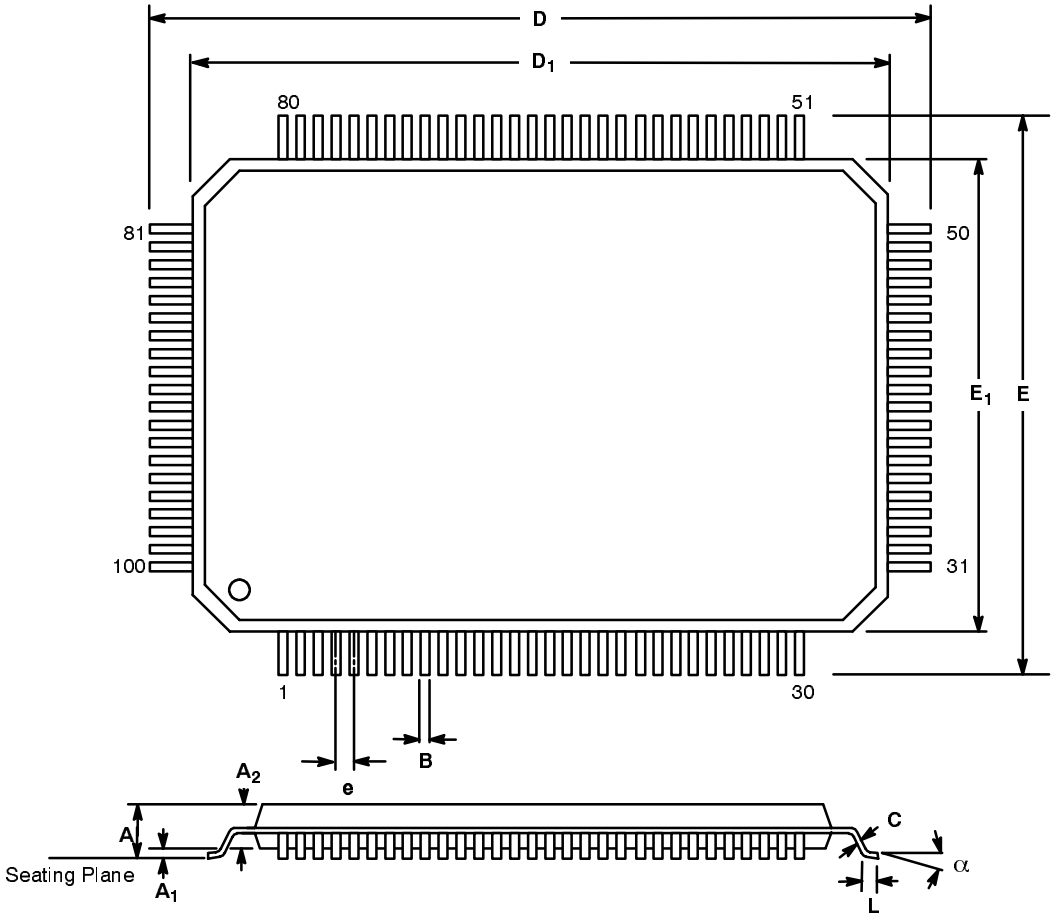
PIN CONFIGURATION



100 Lead PQFP

100 LEAD PLASTIC QUAD FLAT PACK (14 mm x 20 mm, QFP)

Rev. 2.00

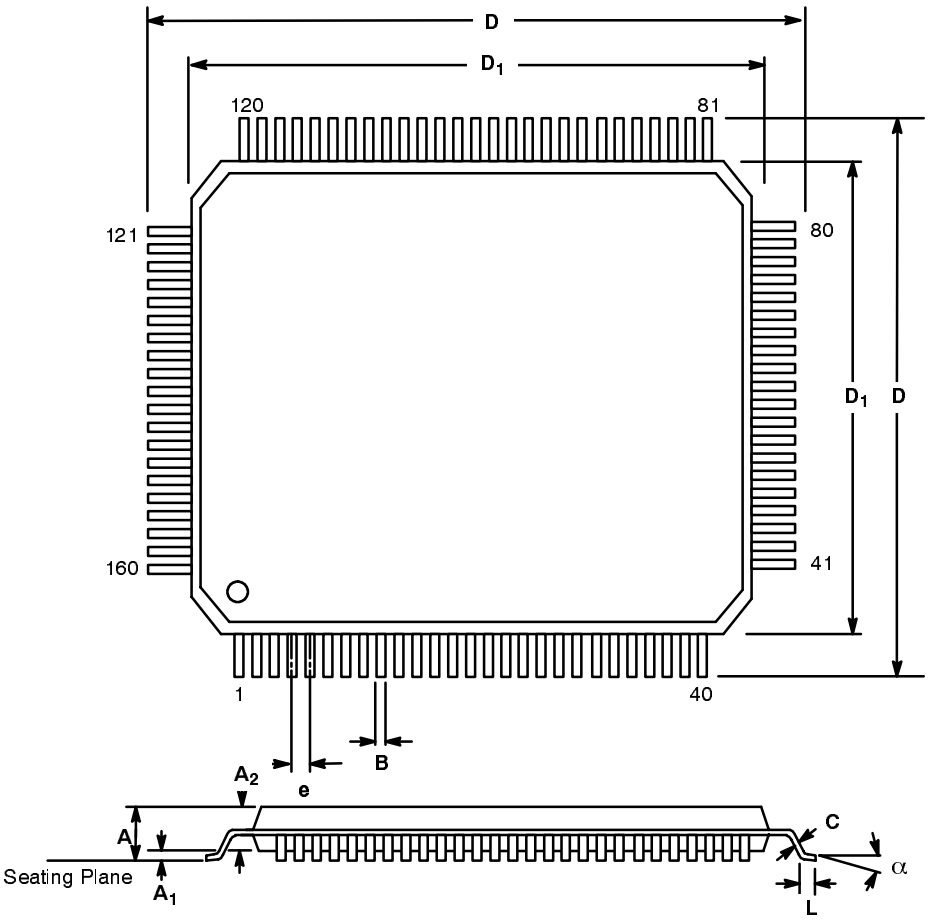


	1.6 mm Form				1.95 mm Form			
	INCHES		MILLIMETERS		INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	0.102	0.130	2.60	3.30	0.102	0.134	2.60	3.40
A_1	0.002	0.010	0.05	0.25	0.002	0.014	0.05	0.35
A_2	0.100	0.120	2.55	3.05	0.100	0.120	2.55	3.05
B	0.009	0.015	0.22	0.38	0.009	0.015	0.22	0.38
C	0.005	0.009	0.13	0.23	0.005	0.009	0.13	0.23
D	0.904	0.923	22.95	23.45	0.931	0.951	23.65	24.15
D_1	0.783	0.791	19.90	20.10	0.783	0.791	19.90	20.10
E	0.667	0.687	16.95	17.45	0.695	0.715	17.65	18.15
E_1	0.547	0.555	13.90	14.10	0.547	0.555	13.90	14.10
e	0.0256 BSC		0.65 BSC		0.0256 BSC		0.65 BSC	
L	0.029	0.040	0.73	1.03	0.026	0.037	0.65	0.95
α	0°	7°	0°	7°	0°	7°	0°	7°

Note: The control dimension is the millimeter column

160 LEAD PLASTIC QUAD FLAT PACK (28 mm x 28 mm, QFP)

Rev. 1.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.127	0.160	3.22	4.07
A_1	0.002	0.016	0.05	0.40
A_2	0.125	0.144	3.17	3.67
B	0.009	0.015	0.22	0.38
C	0.005	0.009	0.13	0.23
D	1.218	1.238	30.95	31.45
D_1	1.098	1.106	27.90	28.10
e	0.0256 BSC		0.65 BSC	
L	0.029	0.040	0.73	1.03
α	0°	7°	0°	7°

Note: The control dimension is the millimeter column

Notes

Notes

Notes

NOTICE

EXAR Corporation reserves the right to make changes to the products contained in this publication in order to improve design, performance or reliability. EXAR Corporation assumes no responsibility for the use of any circuits described herein, conveys no license under any patent or other right, and makes no representation that the circuits are free of patent infringement. Charts and schedules contained here in are only for illustration purposes and may vary depending upon a user's specific application. While the information in this publication has been carefully checked; no responsibility, however, is assumed for inaccuracies.

EXAR Corporation does not recommend the use of any of its products in life support applications where the failure or malfunction of the product can reasonably be expected to cause failure of the life support system or to significantly affect its safety or effectiveness. Products are not authorized for use in such applications unless EXAR Corporation receives, in writing, assurances to its satisfaction that: (a) the risk of injury or damage has been minimized; (b) the user assumes all such risks; (c) potential liability of EXAR Corporation is adequately protected under the circumstances.

Datasheet December 1997