MOTOROLA
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PowerPC™

Application Note

MPC860 Revision D PLL Considerations

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NCSG Applications

The capacitor value of XFC depends on the voltage controlled oscillator (VCO) frequency and the resulting multiplication factor. The larger the capacitor value, the slower the feedback loop. The MPC860 User's Manual (MPC860UM/AD Rev. 1) recommends XFC values depending on the multiplication factor (MF). If the XFC value is below the recommended range, the jitter of the VCO output increases. If the XFC value is larger than the recommended range, the PLL may never achieve lock after system startup.

1.1 Device Nomenclature and Current XFC Table

The formula in table 15-2 on page 15-8 in the MPC860 Users Manual is valid for all revision C silicon and eariler. The revision of the silicon can be derived from last 2 digits of the part number, e.g. XPC860ENZP66C1 is a C revision silicon. XPC860PZP80D4 is a revision D silicon.

1.2 Revision D XFC Implementation

Due to the change of manufacturing technology used for revision D silicon, a revised set of formula must be used to calculate the appropriate XFC value. The XFC values are larger for revision D compared to revision C formula to obtain lower jitter. For systems which are migrating from revision C to revision D, the XFC capacitor value may need to change, to fit within the new calculation ranges. It may be possible to go from a revision C to a revision D MPC860 without changing the XFC value. However, the system must have timing margins of at least 2.0 ns on all propogation delay values of the bus signals, especially of

SDRAM signals. Table 1 shows the revised XFC formula for revision D silicon and later.

Table 1 XFC Capacitor Value for Revision D Silicon and later Based on PLPRCR[MF].

MF Range	Minimum Capacitance	Maximum Capacitance	Unit
1 <= (MF+1) <= 4	XFC = [(MF+1) x 580] - 100	XFC = [(MF+1) x 780] - 140	pF
(MF+1) > 4	XFC = (MF+1) x 830	XFC = (MF+1) x 1470	pF

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