X1202

2-Wire™ RTC

Real Time Clock/Calendar/Alarms/CPU Supervisor

FEATURES

- **Selectable watchdog timer (0.25s, 0.75s, 1.75s, off)**
- **Power on reset (250ms)**
- **Programmable low voltage reset**
- **2 polled alarms**
  - **—Settable on the second, minute, hour, day, month, or day of the week**
- **2-wire interface interoperable with I^2C**
  - **—400kHz data transfer rate**
- **Secondary power supply input with internal switch-over circuitry**
- **Low power CMOS**
  - **—<1µA operating current**
  - **—<3mA active current during program**
  - **—<400µA active current during data read**
- **Single byte write capability**
- **Typical nonvolatile write cycle time: 5ms**
- **High reliability**
- **Small package options**
  - **—8-lead SOIC package, 8-lead TSSOP package**

DESCRIPTION

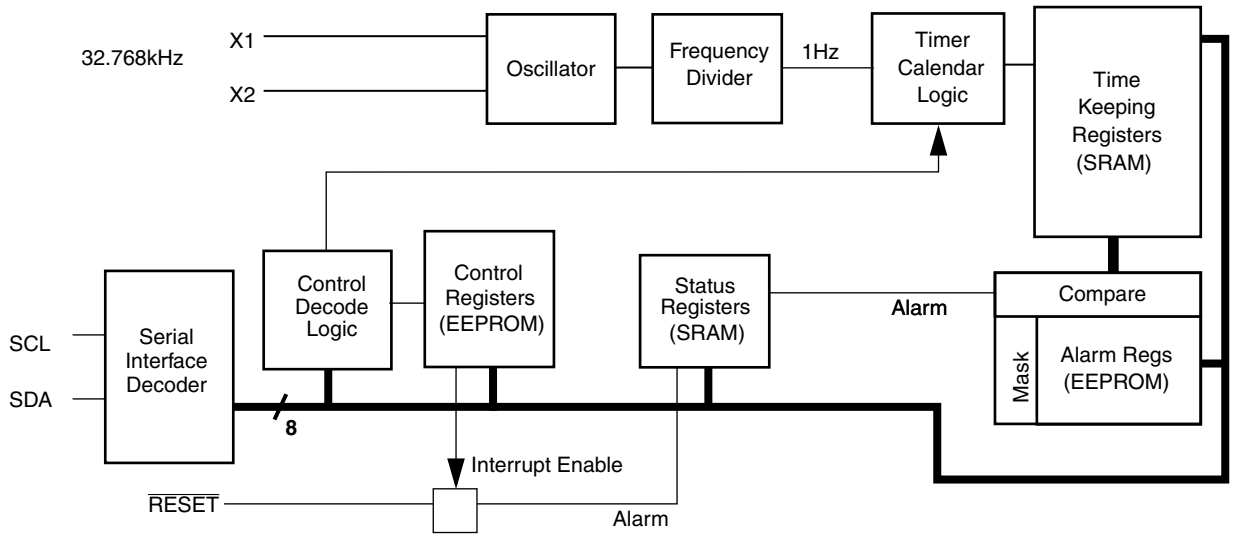
The X1202 is a Real Time Clock with Clock/Calendar/CPU Supervisor circuits and two polled alarms. The dual port clock and alarm registers allow the clock to operate, without loss of accuracy, even during read and write operations.

The clock/calendar provides functionality that is controllable and readable through a set of registers. The clock, using a low-cost 32.768kHz crystal input, accurately tracks the time in seconds, minutes, hours, date, day, month and years. It has leap year correction and automatic adjustment for months with less than 31 days.

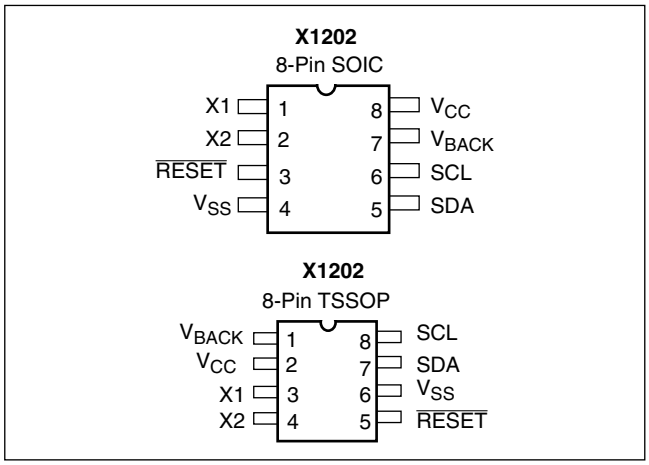
The X1202 provides a watchdog timer with 3 selectable time out periods and off. The watchdog activates a RESET pin when it expires. The reset also goes active when V_{CC} drops below a fixed trip point. There are two alarms where a match is monitored by polling status bits.

The device offers a backup power input pin. This V_{BACK} pin allows the device to be backed up by a non-rechargeable battery. The RTC is fully operational from 1.8 to 5.5 volts.

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTIONS

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device. The input buffer on this pin is always active (not gated).

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It has an open drain output and may be wire ORed with other open drain or open collector outputs. The input buffer is always active (not gated).

An open drain output requires the use of a pull-up resistor. The output circuitry controls the fall time of the output signal with the use of a slope controlled pull-down. The circuit is designed for 400kHz 2-wire interface speeds.

V_{BACK}

This input provides a backup supply voltage to the device. V_{BACK} supplies power to the device in the event the V_{CC} supply fails.

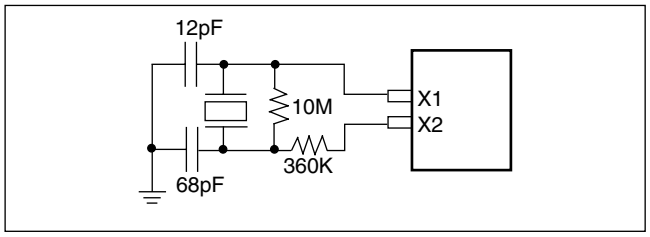
RESET Output—$\overline{RESET}$

This is a reset signal output. This signal notifies a host processor that the watchdog time period has expired or that the supply voltage V_{CC} has dropped below a fixed V_{TRIP} threshold. It is an open drain active LOW output.

X1, X2

The X1 and X2 pins are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator. A 32.768kHz quartz crystal is used. Recommended crystal is a Citizen CFS-206. The crystal supplies a timebase for a clock/oscillator. The internal clock can be driven by an external signal on X1, with X2 left unconnected.

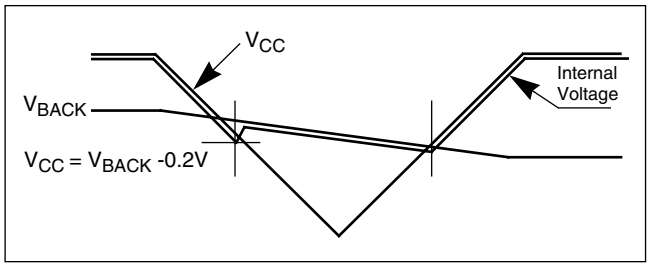
Figure 1. Recommended Crystal Connection



POWER CONTROL OPERATION

The Power control circuit accepts a V_{CC} and a V_{BACK} input. The power control circuit will switch to V_{BACK} when $V_{CC} < V_{BACK} - 0.2V$. It will switch back to V_{CC} when V_{CC} exceeds V_{BACK}.

Figure 2. Power Control



REAL TIME CLOCK OPERATION

The Real Time Clock (RTC) uses an external, 32.768kHz quartz crystal to maintain an accurate internal representation of the year, month, day, date, hour, minute, and seconds. The RTC has leap-year correction and century byte. The clock also corrects for months having fewer than 31 days and has a bit that controls 24-hour or AM/PM format. When the X1202 powers up after the loss of both V_{CC} and V_{BACK}, the clock will not increment until at least one byte is written to the clock register.

Reading the Real Time Clock

The RTC is read by initiating a Read command and specifying the address corresponding to the register of the real time clock. The RTC Registers can then be read in a Sequential Read Mode. Since the clock runs continuously and a read takes a finite amount of time, there is the possibility that the clock could change during the course of a read operation. In this device, the

time is latched by the read command (falling edge of the clock on the ACK bit prior to RTC data output) into a separate latch to avoid time changes during the read operation. The clock continues to run. Alarms occurring during a read are unaffected by the read operation.

Writing to the Real Time Clock

The time and date may be set by writing to the RTC registers. To avoid changing the current time by an uncompleted write operation, the current time value is loaded into a separate buffer at the falling edge of the clock on the ACK bit before the RTC data input bytes, the clock continues to run. The new serial input data replaces the values in the buffer. This new RTC value is loaded back into the RTC register by a stop bit at the end of a valid write sequence. An invalid write operation aborts the time update procedure and the contents of the buffer are discarded. After a valid write operation the RTC will reflect the newly loaded data beginning with the first “one second” clock cycle after the stop bit. The RTC continues to update the time while an RTC register write is in progress and the RTC continues to run during any nonvolatile write sequences. A single byte may be written to the RTC without affecting the other bytes.

CLOCK/CONTROL REGISTERS (CCR)

The Control/Clock Registers are located in an area separate from the EEPROM array and are only accessible following a slave byte of “1101111x” and reads or writes to addresses [0000h:003Fh].

CCR Access

The contents of the CCR can be modified by performing a byte or a page write operation directly to any address in the CCR. Prior to writing to the CCR (except the status register), however, the WEL and RWEL bits must be set using a two step process (See section “Writing to the Clock/Control Registers.”)

The CCR is divided into 5 sections. These are:

1. Alarm 0 (8 bytes)
2. Alarm 1 (8 bytes)
3. Control (1 byte)
4. Real Time Clock (8 bytes)
5. Status (1 byte)

Sections 1) through 3) are nonvolatile and Sections 4) and 5) are volatile. Each register is read and written through buffers. The nonvolatile portion (or the counter portion of the RTC) is updated only if RWEL is set and only after a valid write operation and stop bit. A sequential read or page write operation provides access to the contents of only one section of the CCR per operation. Access to another section requires a new operation. Continued reads or writes, once reaching the end of a section, will wrap around to the start of the section. A read or page write can begin at any address in the CCR.

Section 5) is a volatile register. It is not necessary to set the RWEL bit prior to writing the status register. Section 5) supports a single byte read or write only. Continued reads or writes from this section terminates the operation.

The state of the CCR can be read by performing a random read at any address in the CCR at any time. This returns the contents of that register location. Additional registers are read by performing a sequential read. The read instruction latches all clock registers into a buffer, so an update of the clock does not change the time being read. At the end of a read, the master supplies a stop condition to end the operation and free the bus. After a read of the CCR, the address remains at the previous address +1 so the user can execute a current address read of the CCR and continue reading the next Register.

ALARM REGISTERS

There are two alarm registers whose contents mimic the contents of the RTC register, but add enable bits and exclude the 24-hour time selection bit. The enable bits specify which registers to use in the comparison between the Alarm and real time registers. For example:

– The user can set the X1202 to alarm every Wednesday at 8:00AM by setting the EDWn, the EHRn and EMNn enable bits to ‘1’ and setting the DWAn, HRAn and MNAn Alarm registers to 8:00AM Wednesday.

– A daily alarm for 9:30PM results when the EHRn and EMNn enable bits are set to ‘1’ and the HRAn and MNAn registers set 9:30PM.

– Setting the EMOn bit in combination with other enable bits and a specific alarm time, the user can establish an alarm that triggers at the same time once a year.

When there is a match, an alarm flag is set. The occurrence of an alarm can only be determined by polling the AL0 and AL1 bits.

The alarm enable bits are located in the MSB of the particular register. When all enable bits are set to ‘0’, there are no alarms.

Table 1. Clock/Control Memory Map

Addr.	Type	Reg Name	Bit								Range	Factory Setting
			7	6	5	4	3	2	1	0 (optional)		
003F	Status	SR	BAT	AL1	AL0	0	0	RWEL	WEL	RTCF		01h
0037	RTC (SRAM)	Y2K	0	0	Y2K21	Y2K20	Y2K13	0	0	Y2K10	19/20	20h
0036		DW	0	0	0	0	0	DY2	DY1	DY0	0-6	00h
0035		YR	Y23	Y22	Y21	Y20	Y13	Y12	Y11	Y10	0-99	00h
0034		MO	0	0	0	G20	G13	G12	G11	G10	1-12	00h
0033		DT	0	0	D21	D20	D13	D12	D11	D10	1-31	00h
0032		HR	MIL	0	H21	H20	H13	H12	H11	H10	0-23	00h
0031		MN	0	M22	M21	M20	M13	M12	M11	M10	0-59	00h
0030		SC	0	S22	S21	S20	S13	S12	S11	S10	0-59	00h
0010	Control (EEPROM)	BL	0	0	0	WD1	WD0	0	0	0		00h
000F	Alarm1 (EEPROM)	Y2K0	0	0	A1Y2K21	A1Y2K20	A1Y2K13	0	0	A1Y2K10	19/20	20h
000E		DWA0	EDW1	0	0	0	0	DY2	DY1	DY0	0-6	00h
000D		YRA0	Unused - Default = RTC Year value									
000C		MOA0	EMO1	0	0	A1G20	A1G13	A1G12	A1G11	A1G10	1-12	00h
000B		DTA0	EDT1	0	A1D21	A1D20	A1D13	A1D12	A1D11	A1D10	1-31	00h
000A		HRA0	EHR1	0	A1H21	A1H20	A1H13	A1H12	A1H11	A1H10	0-23	00h
0009		MNA0	EMN1	A1M22	A1M21	A1M20	A1M13	A1M12	A1M11	A1M10	0-59	00h
0008		SCA0	ESC1	A1S22	A1S21	A1S20	A1S13	A1S12	A1S11	A1S10	0-59	00h
0007	Alarm0 (EEPROM)	Y2K1	0	0	A0Y2K21	A0Y2K20	A0Y2K13	0	0	A0Y2K10	19/20	20h
0006		DWA1	EDW0	0	0	0	0	DY2	DY1	DY0	0-6	00h
0005		YRA1	Unused - Default = RTC Year value									
0004		MOA1	EMO0	0	0	A0G20	A0G13	A0G12	A0G11	A0G10	1-12	00h
0003		DTA1	EDT0	0	A0D21	A0D20	A0D13	A0D12	A0D11	A0D10	1-31	00h
0002		HRA1	EHR0	0	A0H21	A0H20	A0H13	A0H12	A0H11	A0H10	0-23	00h
0001		MNA1	EMN0	A0M22	A0M21	A0M20	A0M13	A0M12	A0M11	A0M10	0-59	00h
0000		SCA1	ESC0	A0S22	A0S21	A0S20	A0S13	A0S12	A0S11	A0S10	0-59	00h

REAL TIME CLOCK REGISTERS

Year 2000 (Y2K)

The X1202 has a century byte that “rolls over” from 19 to 20 when the years byte changes from 99 to 00. The Y2K byte can contain only the values of 19 or 20.

Day of the Week Register (DW)

This register provides a Day of the Week status and uses three bits DY2 to DY0 to represent the seven days of the week. The counter advances in the cycle 0-1-2-3-4-5-6-0-1-2-... The assignment of a numerical value to a specific day of the week is arbitrary and may be decided by the system software designer. The Clock Default values define 0 = Sunday.

Clock/Calendar Register (YR, MO, DT, HR, MN, SC)

These registers depict BCD representations of the time. As such, SC (Seconds) and MN (Minutes) range from 0 to 59, HR (Hour) is 1 to 12 with an AM or PM indicator (H21 bit) or 0 to 23 (with MIL = 1), DT (Date) is 1 to 31, MO (Month) is 1 to 12, YR (Year) is 0 to 99.

24 Hour Time

If the MIL bit of the HR register is 1, the RTC uses a 24-hour format. If the MIL bit is 0, the RTC uses a 12-hour format and bit H21 functions as an AM/PM indicator with a '1' representing PM. The clock defaults to Standard Time with H21 = 0.

Leap Years

Leap years add the day February 29 and are defined as those years that are divisible by 4. Years divisible by 100 are not leap years, unless they are also divisible by 400. This means that the year 2000 is a leap year, the year 2100 is not. The X1202 does not correct for the leap year in the year 2100.

STATUS REGISTER (SR)

The Status Register is located in the RTC area at address 003Fh. This is a volatile register only and is used to control the WEL and RWEL write enable latches, read two power status and two alarm bits. This register is separate from both the array and the Clock/Control Registers (CCR).

Table 2. Status Register (SR)

Addr	7	6	5	4	3	2	1	0
003Fh	BAT	AL1	AL0	0	0	RWEL	WEL	RTCF
Default	0	0	0	0	0	0	0	1

BAT: Battery Supply—Volatile

This bit set to "1" indicates that the device is operating from V_{BACK}, not V_{CC}. It is a read only bit and is set/reset by hardware.

AL1, AL0: Alarm bits—Volatile

These bits announce if either alarm 1 or alarm 2 match the real time clock. If there is a match, the respective bit is set to '1'. The falling edge of the last data bit in a SR Read operation resets the flags.

Note: Only the AL bits that are set when an SR read starts will be reset. An alarm bit that is set by an alarm occurring during an SR read operation will remain set after the read operation is complete.

RWEL: Register Write Enable Latch—Volatile

This bit is a volatile latch that powers up in the LOW (disabled) state. The RWEL bit must be set to "1" prior to any writes to the Clock/Control Registers. Writes to RWEL bit do not cause a nonvolatile write cycle, so the device is ready for the next operation immediately after the stop condition. A write to the CCR requires both the RWEL and WEL bits to be set in a specific sequence. RWEL bit is reset after each high voltage or reset by sending 00h to status register.

WEL: Write Enable Latch—Volatile

The WEL bit controls the access to the CCR and memory array during a write operation. This bit is a volatile latch that powers up in the LOW (disabled) state. While the WEL bit is LOW, writes to the CCR or any array address will be ignored (no acknowledge will be issued after the Data Byte). The WEL bit is set by writing a "1" to the WEL bit and zeroes to the other bits of the Status Register. Once set, WEL remains set until either reset to "0" (by writing a "0" to the WEL bit and zeroes to the other bits of the Status Register) or until the part powers up again. Writes to WEL bit do not cause a nonvolatile write cycle, so the device is ready for the next operation immediately after the stop condition.

RTCF: Real Time Clock Fail Bit—Volatile

This bit is set to a '1' after a total power failure. This is a read only bit that is set by hardware when the device powers up after having lost all power to the device. The bit is set regardless of whether V_{CC} or V_{BACK} is applied first. The loss of one or the other supplies does not result in setting the RTCF bit. The first valid write to the RTC (writing one byte is sufficient) resets the RTCF bit to '0'.

Unused Bits

These devices do not use bits 3 or 4, but must have a zero in these bit positions. The Data Byte output during a SR read will contain zeros in these bit locations.

CONTROL REGISTER

Watchdog Timer Control Bits

The bits WD1 and WD0 control the period of the Watchdog Timer. See Table 3 for options.

Table 3. Watchdog Timer Time Out Options

WD1	WD0	Watchdog Time Out Period
0	0	1.75 seconds
0	1	750 milliseconds
1	0	250 milliseconds
1	1	disabled

WRITING TO THE CLOCK/CONTROL REGISTERS

Changing any of the nonvolatile bits of the clock/control register requires the following steps:

– Write a 02H to the status register to set the Write Enable Latch (WEL). This is a volatile operation, so there is no delay after the write. (Operation preceeded by a start and ended with a stop).

– Write a 06H to the status register to set both the Register Write Enable Latch (RWEL) and the WEL bit. This is also a volatile cycle. The zeros in the data byte are required. (Operation preceeded by a start and ended with a stop).

– Write one to 8 bytes to the clock/control registers with the desired clock, alarm, or control data. This sequence starts with a start bit, requires a slave byte of "11011110" and an address within the CCR and is terminated by a stop bit. A write to the CCR changes EEPROM values so these initiate a nonvolatile write cycle and will take up to 10ms to complete. Writes to undefined areas have no effect. The RWEL bit is reset by the completion of a nonvolatile write cycle, so the sequence must be repeated to again initiate another change to the CCR contents. If the sequence is not completed for any reason (by sending an incorrect number of bits or sending a start instead of a stop, for example) the RWEL bit is not reset and the device remains in an active mode.

– The RWEL and WEL bits can be reset by writing a 0 to the status register.

– A read operation occurring between any of the previous operations will not interrupt the register write operation.

POWER ON RESET

Application of power to the X1202 activates a power on reset circuit that pulls the $\overline{\text{RESET}}$ pin active. This signal provides several benefits.

– It prevents the system microprocessor from starting to operate with insufficient voltage.

– It prevents the processor from operating prior to stabilization of the oscillator.

– It allows time for an FPGA to download its configuration prior to initialization of the circuit.

When V_{CC} exceeds the device V_{TRIP} threshold value for 250ms the circuit releases $\overline{\text{RESET}}$, allowing the system to begin operation.

WATCHDOG TIMER OPERATION

The watchdog timer is selectable. By writing a value to WD1 and WD0, the watchdog timer can be set to 3 different time out periods or off. When the watchdog timer is set to off, the watchdog circuit is configured for low power operation.

Watchdog Timer Restart

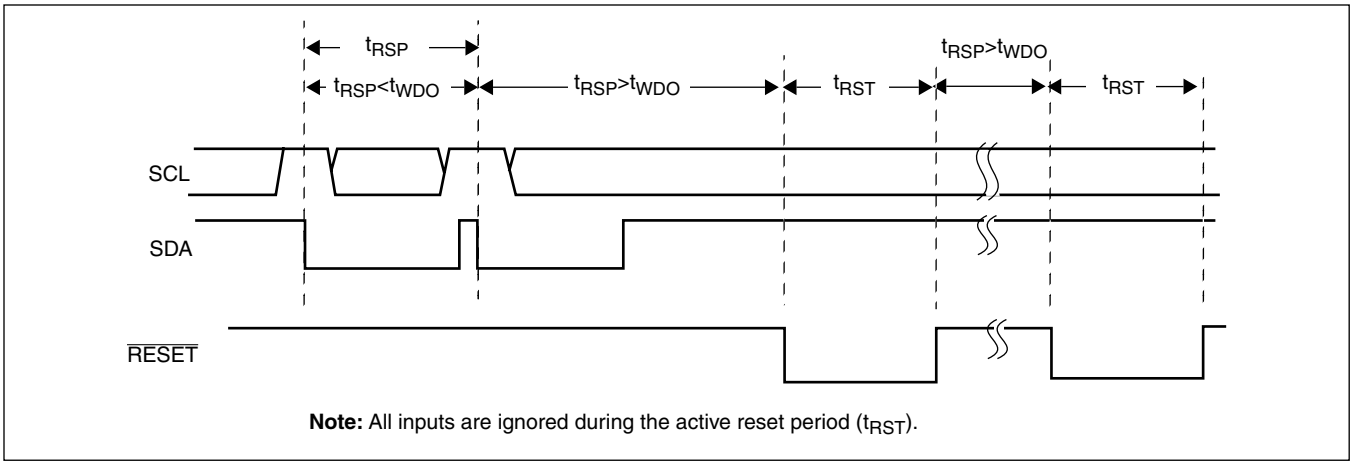
The Watchdog Timer is restarted by a falling edge of SDA when the SCL line is high. This is also referred to as start condition. The restart signal restarts the watchdog timer counter, resetting the period of the counter back to the maximum. If another start fails to be detected prior to the watchdog timer expiration, then the $\overline{\text{RESET}}$ pin becomes active. In the event that the restart signal occurs during a reset time out period, the restart will have no effect.

LOW VOLTAGE RESET OPERATION

When a power failure occurs, and the voltage to the part drops below a fixed V_{TRIP} voltage, a reset pulse is issued to the host microcontroller. The circuitry monitors the V_{CC} line with a voltage comparator which senses a preset threshold voltage. Power up and power down waveforms are shown in Figure 4. The low voltage reset circuit is to be designed so the $\overline{\text{RESET}}$ signal is valid down to 1.0V.

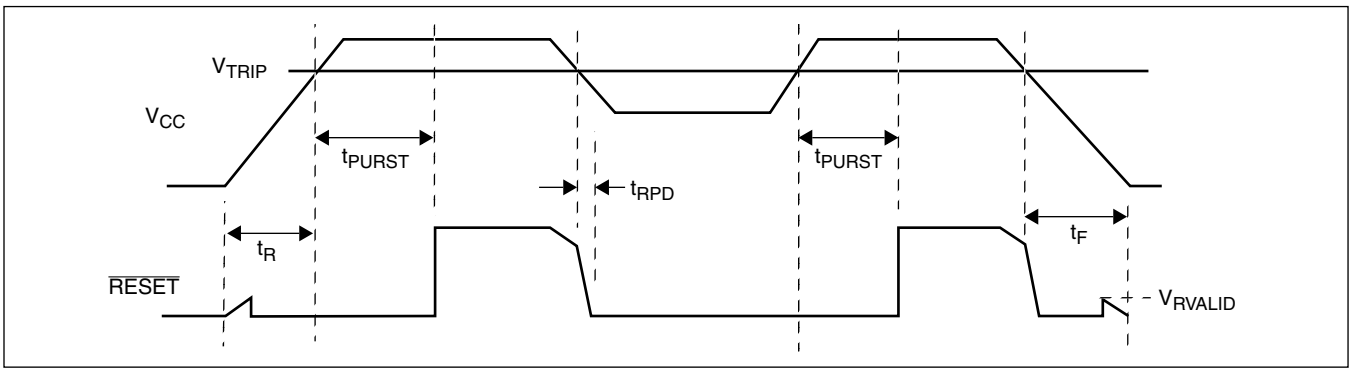
When the low voltage reset signal is active, the operation of any in-progress nonvolatile write cycle is unaffected, allowing a nonvolatile write to continue as long as possible (down to the power on reset voltage). The low voltage reset signal, when active, terminates in-progress communications to the device and prevents new commands, to reduce the likelihood of data corruption.

Figure 3. Watchdog Restart/Time Out



Note: All inputs are ignored during the active reset period (t_{RST}).

Figure 4. Power On Reset and Low Voltage Reset



V_{CC} THRESHOLD RESET PROCEDURE

The X1202 is shipped with a standard V_{CC} threshold (V_{TRIP}) voltage. This value will not change over normal operating and storage conditions. However, in applications where the standard V_{TRIP} is not exactly right, or if higher precision is needed in the V_{TRIP} value, the X1202 threshold may be adjusted. The procedure is described below, and uses the application of a nonvolatile write control signal.

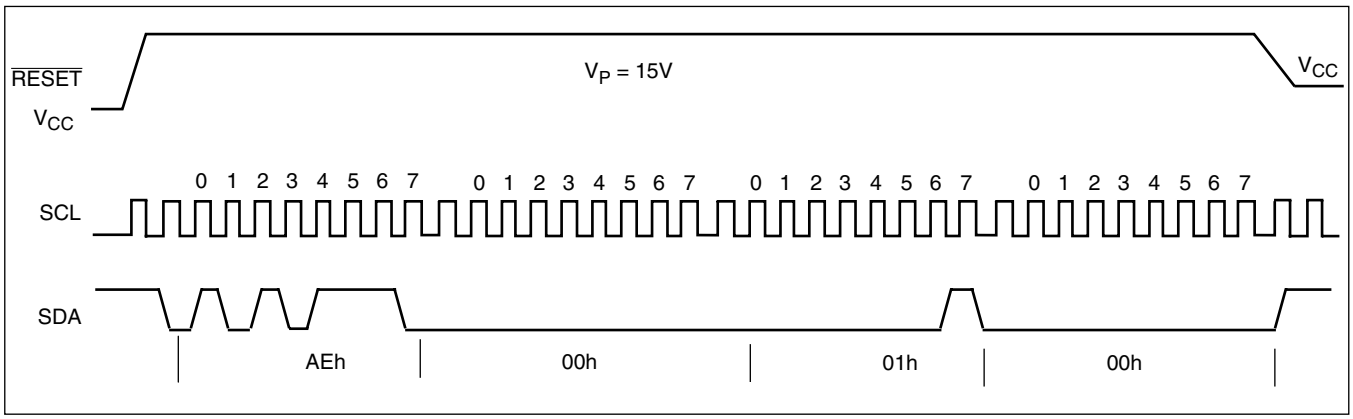
Setting the V_{TRIP} Voltage

This procedure is used to set the V_{TRIP} to a higher voltage value. It is necessary to reset the trip point before setting the new value.

To set the new V_{TRIP} voltage, apply the desired V_{TRIP} threshold voltage to the V_{CC} pin and tie the $\overline{RESET}$ pad pin to the programming voltage V_P. Then write data 00h to address 01h. The stop bit following a valid write operation initiates the V_{TRIP} programming sequence. Bring $\overline{RESET}$ to V_{CC} to complete the operation.

Note: This operation also writes 00h to address 01h of the EEPROM array.

Figure 5. Set V_{TRIP} Level Sequence (V_{CC} = desired V_{TRIP} value)



Resetting the V_{TRIP} Voltage

This procedure is used to set the V_{TRIP} to a "native" voltage level. For example, if the current V_{TRIP} is 4.4V and the new V_{TRIP} must be 4.0V, then the V_{TRIP} must be reset. When V_{TRIP} is reset, the new V_{TRIP} is less than 1.7V. This procedure must be used to set the voltage to a lower value.

To reset the new V_{TRIP} voltage, apply more than 3V to the V_{CC} pin and tie the $\overline{RESET}$ pin to the programming voltage V_P Then write 00h to address 03h. The stop bit of a valid write operation initiates the V_{TRIP} programming sequence. Bring $\overline{RESET}$ to complete the operation.

Note: This operation also writes 00h to address 03h of the EEPROM array.

Figure 6. Reset V_{TRIP} Level Sequence (V_{CC} > 3V)

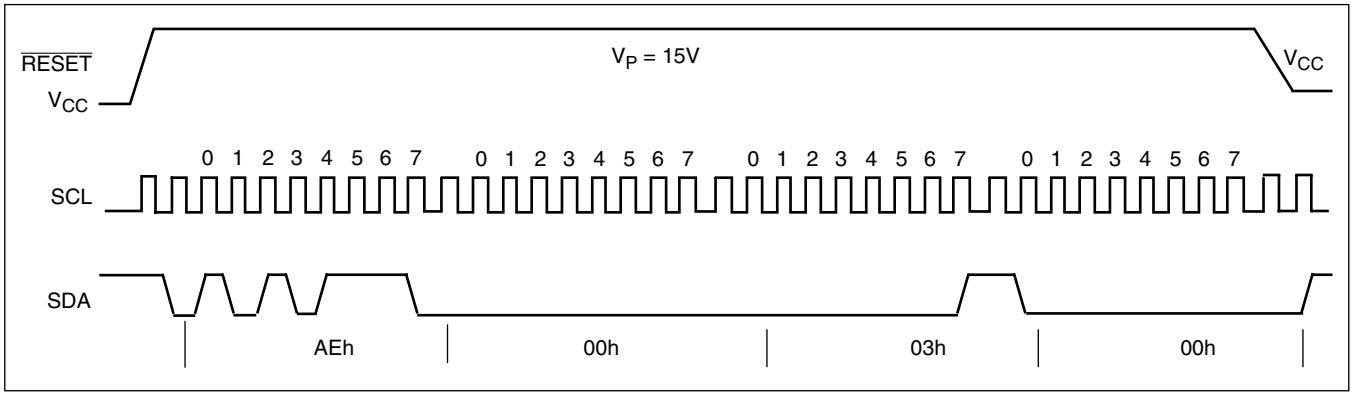
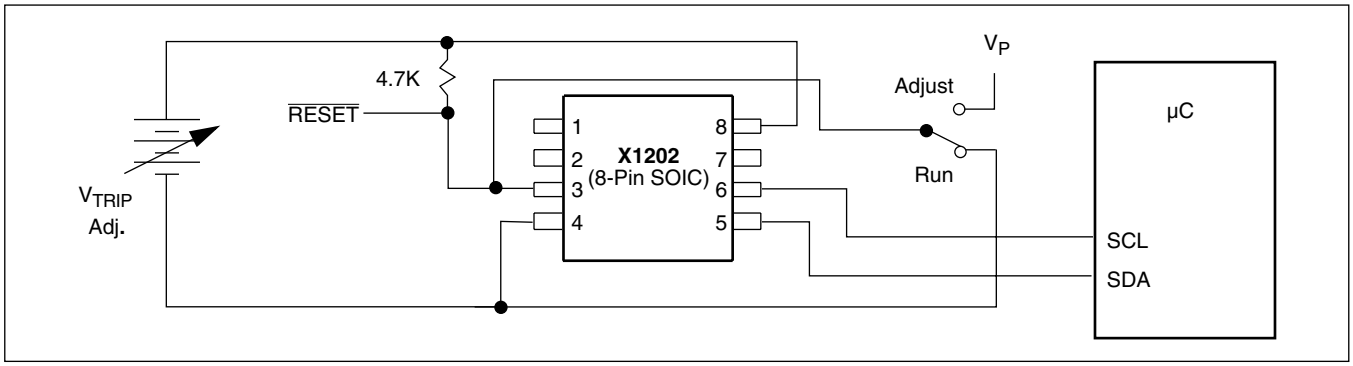


Figure 7. Sample V_{TRIP} Reset Circuit



SERIAL COMMUNICATION

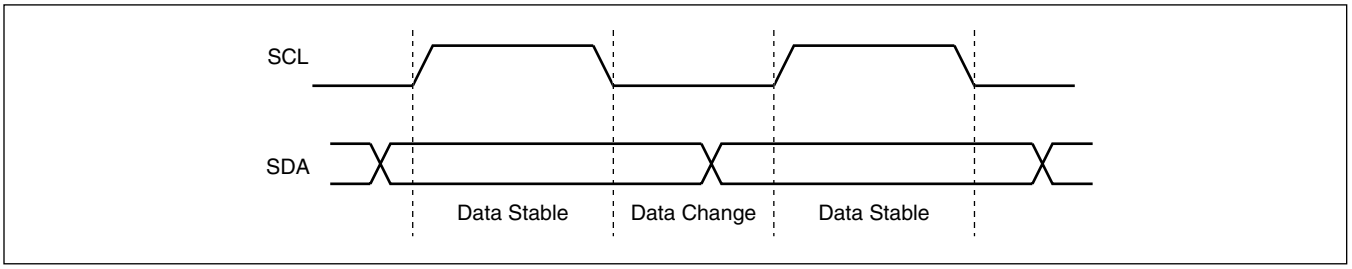
Interface Conventions

The device supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is called the master and the device being controlled is called the slave. The master always initiates data transfers, and provides the clock for both transmit and receive operations. Therefore, the devices in this family operate as slaves in all applications.

Clock and Data

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. See Figure 8.

Figure 8. Valid Data Changes on the SDA Bus



Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met. See Figure 9.

Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the device into the Standby power mode after a read sequence. A stop condition can only be issued after the transmitting device has released the bus. See Figure 8.

Acknowledge

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 10.

Figure 9. Valid Start and Stop Conditions

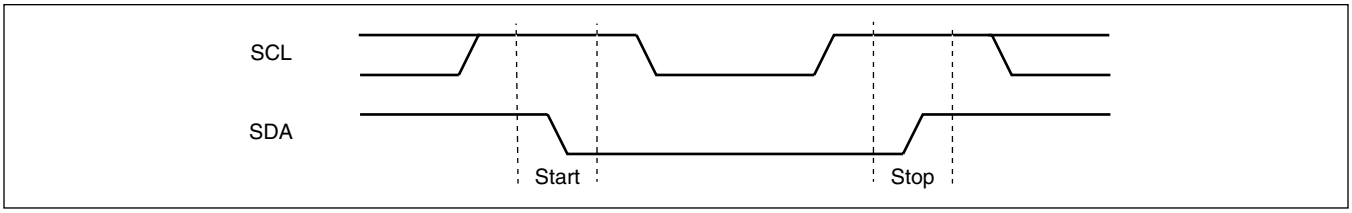
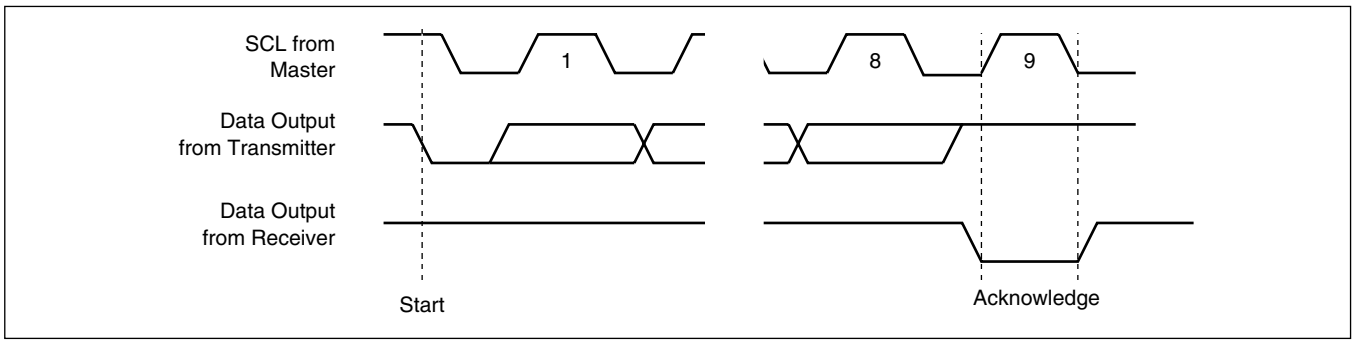


Figure 10. Acknowledge Response From Receiver



The device will respond with an acknowledge after recognition of a start condition and if the correct device identifier and select bits are contained in the slave address byte. If a write operation is selected, the device will respond with an acknowledge after the receipt of each subsequent eight bit word. The device will acknowledge all incoming data and address bytes, except for:

– The slave address byte when the device identifier and/or select bits are incorrect

– All data bytes of a write when the WEL in the write protect register is LOW

– The 2nd data byte of a status register write operation (only 1 data byte is allowed)

In the read mode, the device will transmit eight bits of data, release the SDA line, then monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the device will continue to transmit data. The device will terminate further data transmissions if an acknowledge is not detected. The master must then issue a stop condition to return the device to standby mode and place the device into a known state.

WRITE OPERATIONS

Byte Write

For a byte write operation, the device requires the slave address byte and the CCR address bytes. This gives the master access to any one of the words in the CCR. (**Note:** Prior to writing to the CCR, the master must write a 02h, then 06h to the status register in two preceeding operations to enable the write operation. See “Writing to the Clock/Control Registers” on page 6.) Upon receipt of each address byte, the X1202 responds with an acknowledge. After receiving both address bytes the X1202 awaits the eight bits of data. After receiving the 8 data bits, the X1202 again responds with an acknowledge. The master then terminates the transfer by generating a stop condition. The X1202 then begins an internal write cycle of the data to the nonvolatile memory. During the internal write cycle, the device inputs are disabled, so the device will not respond to any requests from the master. The SDA output is at high impedance. See Figure 11.

Page Write

The X1202 has a page write operation. It is initiated in the same manner as the byte write operation; but instead of terminating the write cycle after the first data byte is transferred, the master can transmit up to 7 more bytes to the clock/control registers.

Note: Prior to writing to the CCR, the master must write a 02h, then 06h to the status register in two preceeding operations to enable the write operation. See “Writing to the Clock/Control Registers” on page 6.)

Figure 11. Byte Write Sequence

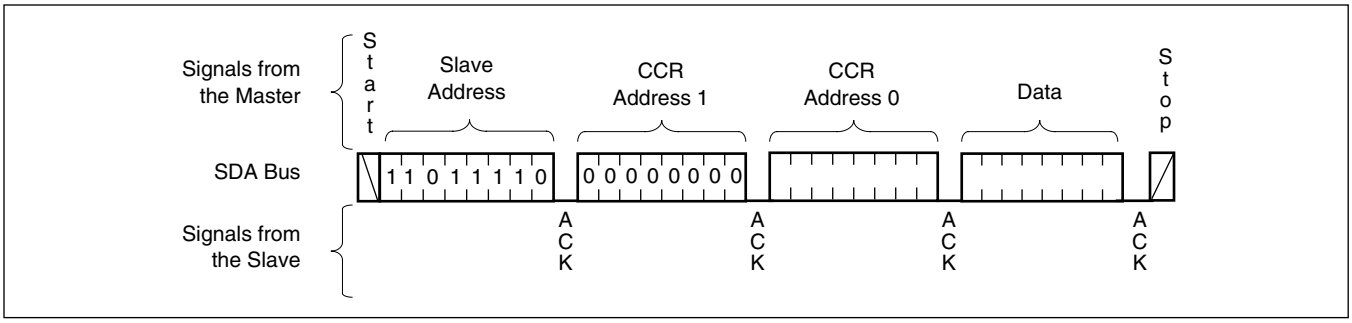
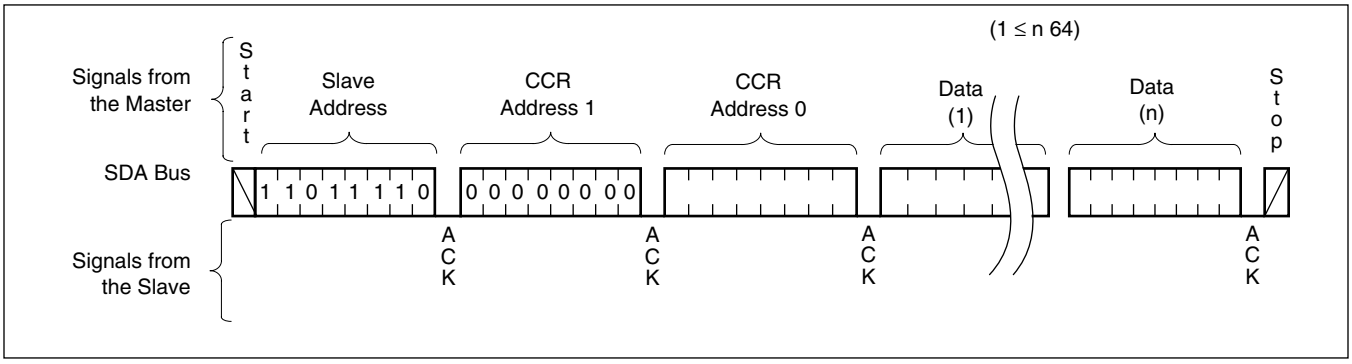


Figure 12. Page Write Sequence



After the receipt of each byte, the X1202 responds with an acknowledge, and the address is internally incriminated by one. When the counter reaches the end of the page, it “rolls over” and goes back to the first address on the same page. If the master supplies more than 8 bytes of data, then the previously loaded data is over written by the new data, one byte at a time. The master terminates the data byte loading by issuing a stop condition, which causes the device to begin the non volatile write cycle. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to Figure 12 for the address, acknowledge, and data transfer sequence.

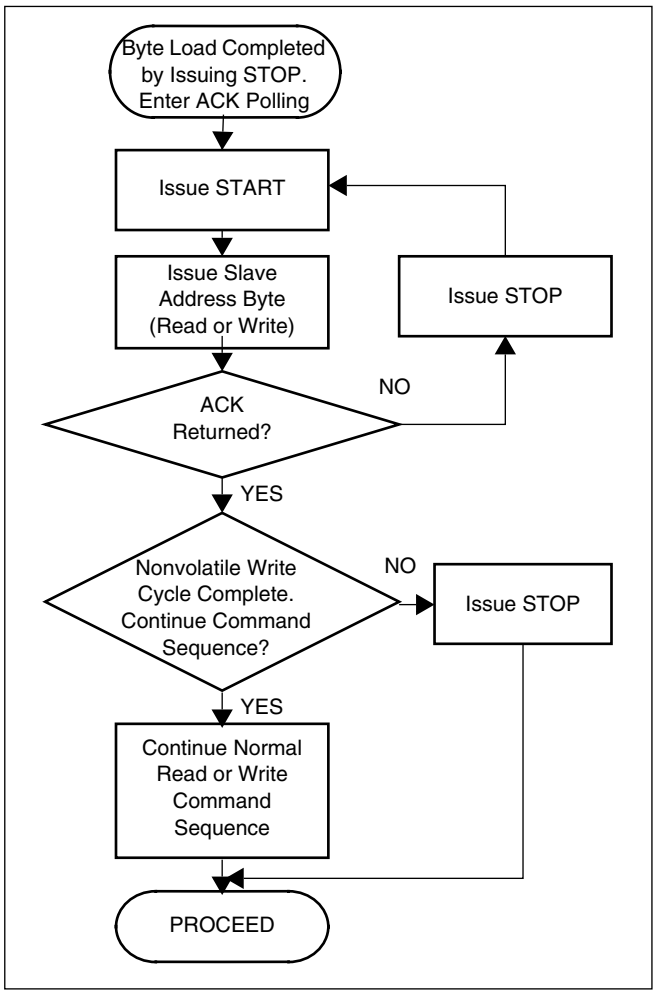
Stops and Write Modes

Stop conditions that terminate write operations must be sent by the master after sending at least 1 full data byte and its associated ACK signal. If a stop is issued in the middle of a data byte, or before 1 full data byte + ACK is sent, then the device will reset itself without performing the write. The contents of the array will not be affected.

Acknowledge Polling

The disabling of the inputs during non volatile write cycles can be used to take advantage of the typical 5ms write cycle time. Once the stop condition is issued to indicate the end of the master’s byte load operation, the device initiates the internal non volatile write cycle. Acknowledge polling can be initiated immediately. To do this, the master issues a start condition followed by the slave address byte for a write or read operation. If the device is still busy with the non volatile write cycle then no ACK will be returned. If the device has completed the write operation, an ACK will be returned and the host can then proceed with the read or write operation. Refer to the flow chart in Figure 13.

Figure 13. Acknowledge Polling Sequence



READ OPERATIONS

There are three basic read operations: Current Address Read, Random Read, and Sequential Read.

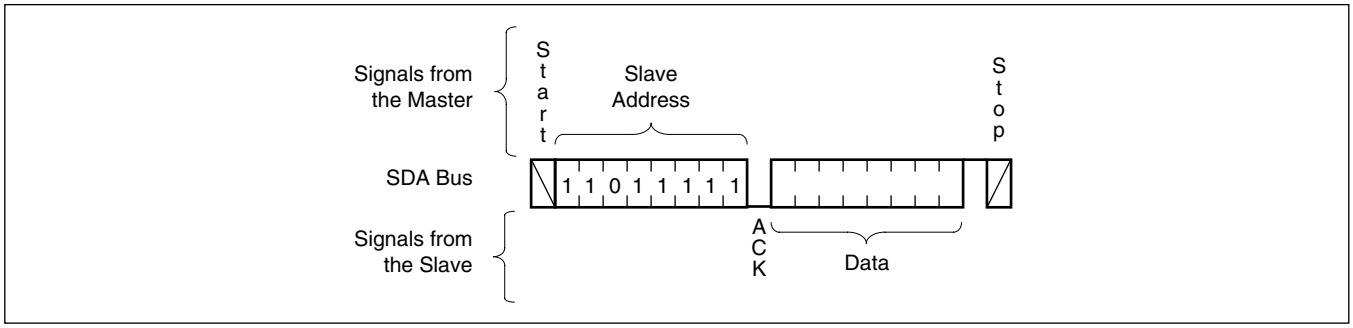
Current Address Read

Internally the device contains an address counter that maintains the address of the last word read incriminated by one. Therefore, if the last read was to address n, the next read operation would access data from address n + 1.

Upon receipt of the slave address byte with the R/$\overline{W}$ bit set to one, the device issues an acknowledge and then transmits the eight bits of the data byte. The master terminates the read operation when it does not respond with an acknowledge during the ninth clock and then issues a stop condition. Refer to Figure 14 for the address, acknowledge, and data transfer sequence.

It should be noted that the ninth clock cycle of the read operation is not a “don’t care.” To terminate a read operation, the master must either issue a stop condition during the ninth cycle or hold SDA HIGH during the ninth clock cycle and then issue a stop condition.

Figure 14. Current Address Read Sequence



Random Read

Random read operation allows the master to access any memory location in the array. Prior to issuing the slave address byte with the R/$\overline{W}$ bit set to one, the master must first perform a “dummy” write operation. The master issues the start condition and the slave address byte, receives an acknowledge, then issues the CCR address bytes. After acknowledging receipt of the CCR address bytes, the master immediately issues another start condition and the slave address byte with the R/$\overline{W}$ bit set to one. This is followed by an acknowledge from the device and then by the eight bit word. The master terminates the read operation by not responding with an acknowledge and then issuing a stop condition. Refer to Figure 15 for the address, acknowledge, and data transfer sequence.

In a similar operation called “Set Current Address,” the device sets the address if a stop is issued instead of the second start shown in Figure 16. The X1202 then goes into standby mode after the stop and all bus activity will be ignored until a start is detected. This operation loads the new address into the address counter. The next current address read operation will read from the newly loaded address. This operation could be useful if the master knows the next address it needs to read, but is not ready for the data.

Figure 15. Random Address Read Sequence

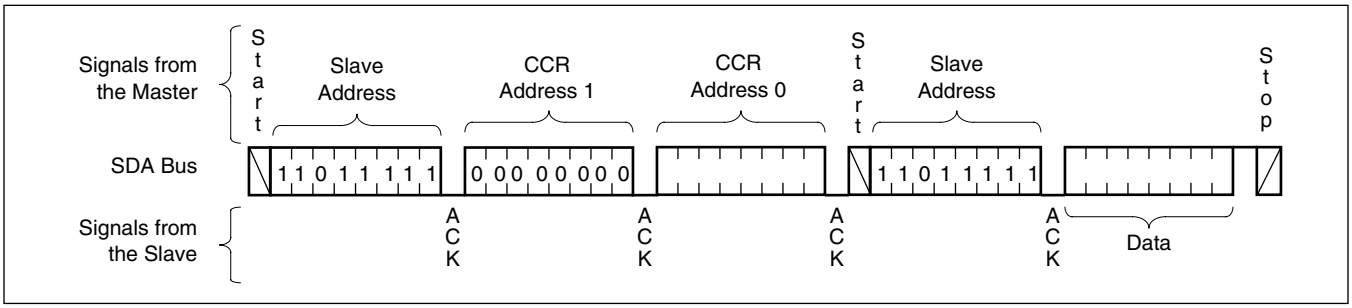
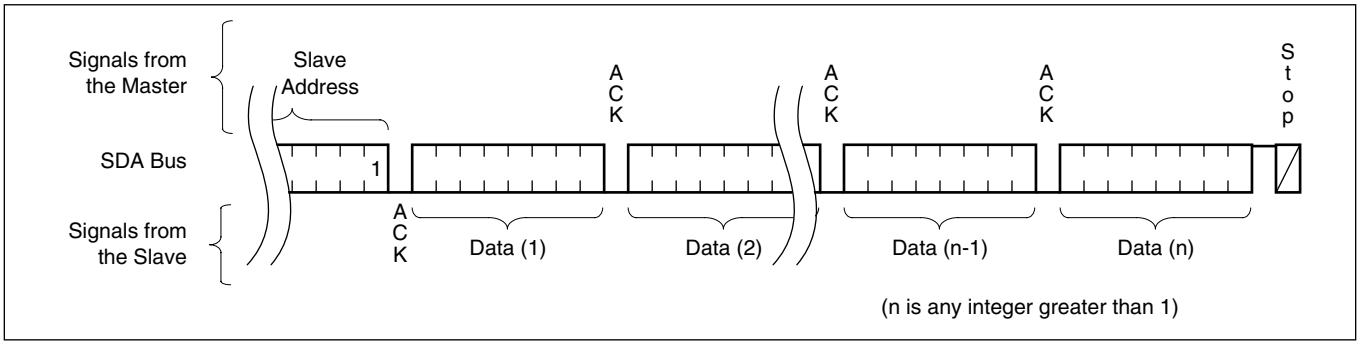


Figure 16. Sequential Read Sequence



Sequential Read

Sequential reads can be initiated as either a current address read or random address read. The first data byte is transmitted as with the other modes; however, the master now responds with an acknowledge, indicating it requires additional data. The device continues to output data for each acknowledge received. The master terminates the read operation by not responding with an acknowledge and then issuing a stop condition.

The data output is sequential, with the data from address n followed by the data from address n + 1. The address counter for read operations increments automatically, allowing the entire register contents to be serially read during one operation. At the end of the register space the counter “rolls over” to the first location in the register and the device continues to output data for each acknowledge received. Refer to Figure 18 for the acknowledge and data transfer sequence.

DEVICE ADDRESSING

Following a start condition, the master must output a slave address byte. The first four bits of the Slave Address Byte specify access to the CCR. Slave bits 1101 access the CCR.

Bit 3 through Bit 1 of the slave byte specify the device select bits. These are set to 111.

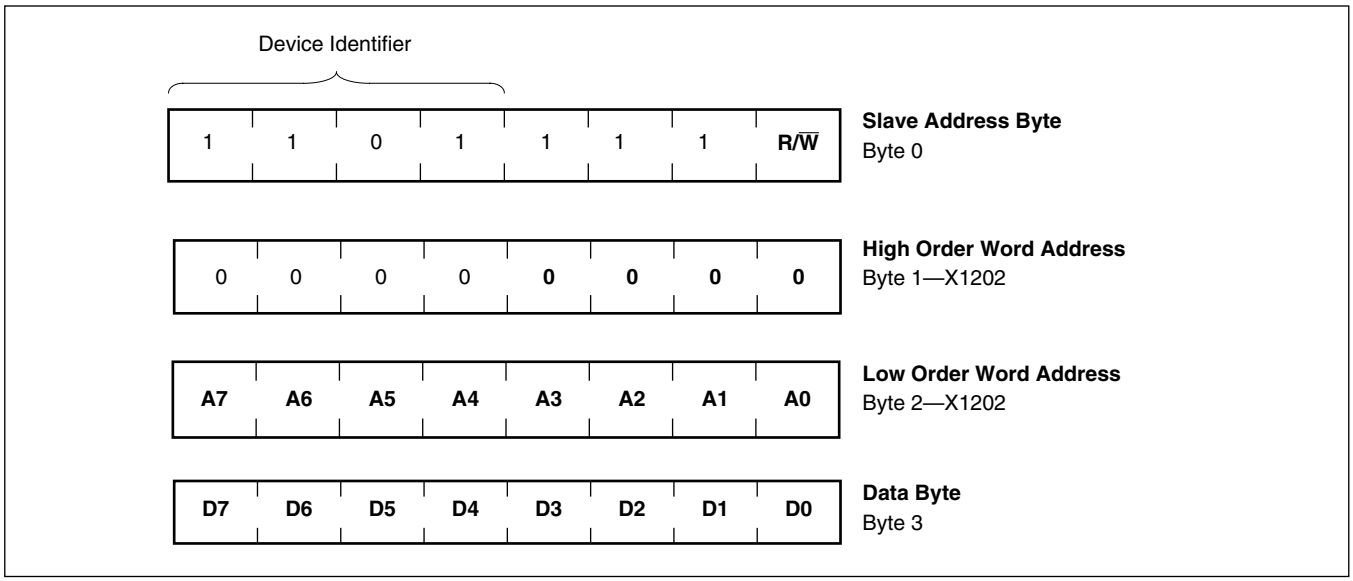
The last bit of the slave address byte defines the operation to be performed. When this R/$\overline{W}$ bit is a one, then a read operation is selected. A zero selects a write operation. Refer to Figure 18.

After loading the entire slave address byte from the SDA bus, the device compares the device identifier and device select bits with 1101111. Upon a correct compare, the device outputs an acknowledge on the SDA line.

Following the slave byte is a two byte CCR address. The CCR address is either supplied by the master device or obtained from an internal counter.

In a random read operation, the slave byte in the "dummy write" portion must match the slave byte in the "read" section. That is, for a random read of the clock/control registers, the slave byte must be 1101111x in both places.

Figure 17. Slave Address, Word Address, and Data Bytes (64 Byte pages)



ABSOLUTE MAXIMUM RATINGS

Temperature under bias ..... -65 to +135°C
Storage temperature ..... -65 to +150°C
Voltage on any pin (respect to ground)....-1.0V to 7.0V
DC output current..... 5 mA
Lead temperature (soldering, 10 sec) ..... 300°C

COMMENTS

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; the functional operation of the device (at these or any other conditions above those indicated in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC OPERATING CHARACTERISTICS (Temperature = -40°C to +85°C, unless otherwise stated.)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit	Notes
V_{CC}	Main Power Supply		2.7		5.5	V	
V_{BACK}	Backup Power Supply		1.8		5.5	V	
V_{CB}	Switch to Backup Supply		V_{BACK} - 0.2		V_{BACK} - 0.1	V	17
V_{BC}	Switch to Main Supply		V_{BACK}		V_{BACK} + 0.1	V	17
I_{CC1}	Active Supply Current	V_{CC} = 2.7V			1.2	µA	5, 8, 15
		V_{CC} = 5.5V			1.7	µA	
I_{CC2}	Program Supply Current (nonvolatile)	V_{CC} = 2.7V			1.5	µA	5, 8, 16, 17
		V_{CC} = 5.5V			3.0	µA	
I_{CC3}	Main Timekeeping Current	V_{CC} = 2.7V			2.0	µA	5, 7, 16, 17
		V_{CC} = 5.5V			2.5	µA	
I_{BACK1}	Backup Timekeeping Current	V_{BACK} = 1.8V			1.0	µA	7, 10, 16, 17
		V_{BACK} = 5.5V			1.5	µA	
I_{BACK2}	Backup Supply Current (External crystal network)	V_{BACK} = 1.8V		1.6	2	µA	7, 10, 16, 17
		V_{BACK} = 5.5V		7.5	10	µA	
I_{LI}	Input Leakage Current				10	µA	11
I_{LO}	Output Leakage Current				10	µA	11
V_{IL}	Input LOW Voltage		-0.5		V_{CC} x 0.2 or V_{BACK} x 0.2	V	5, 14
V_{IH}	Input HIGH Voltage		V_{CC} x 0.7 or V_{BACK} x 0.7		V_{CC} + 0.5 V_{BACK} + 0.5	V	5, 14
V_{HYS}	Schmitt Trigger Input Hysteresis	V_{CC} related level	.05 x V_{CC} or .05 x V_{BACK}			V	14
V_{OL}	Output LOW Voltage	V_{CC} = 2.7V			0.4	V	12
		V_{CC} = 5.5V			0.4		
V_{OH}	Output HIGH Voltage	V_{CC} = 2.7V	1.6			V	13
		V_{CC} = 5.5V	2.4				

Notes: (1) The device enters the active state after any start, and remains active: for 9 clock cycles if the device select bits in the slave address byte are incorrect or until 200ns after a stop ending a read or write operation.
(2) The device enters the program state 200ns after a stop ending a write operation and continues for t_{WC}.
(3) The device goes into the timekeeping state 200ns after any stop, except those that initiate a nonvolatile write cycle; t_{WC} after a stop that initiates a nonvolatile write cycle; or 9 clock cycles after any start that is not followed by the correct device select bits in the slave address byte.
(4) For reference only and not tested.
(5) $V_{IL} = V_{CC} \times 0.1$, $V_{IH} = V_{CC} \times 0.9$, f_{SCL} = 400kHz, SDA = open
(6) $V_{IL} = V_{CC} \times 0.1$, $V_{IH} = V_{CC} \times 0.9$, f_{SCL} = 400kHz, f_{SDA} = 400kHz, $V_{CC} = 1.22 \times V_{CC}$ Min
(7) V_{CC} = 0V
(8) V_{BACK} = 0V
(9) $V_{SDA} = V_{SCL} = V_{CC}$, Others = GND or V_{CC}
(10) $V_{SDA} = V_{SCL} = V_{BACK}$, Others = GND or V_{BACK}
(11) V_{SDA} = GND to V_{CC}, V_{CLK} = GND or V_{CC}
(12) I_{OL} = 3.0mA at 5V, 1.5mA at 2.7V
(13) I_{OH} = -1.0mA at 5V, -0.4mA at 2.7V
(14) Threshold voltages based on the higher of V_{CC} or V_{BACK}.
(15) Driven by external 32.768kHz square wave oscillator on X1, X2 open.
(16) Using recommended crystal and oscillator network applied to X1 and X2 (25°C).
(17) Periodically sampled and not 100% tested

CAPACITANCE T_A = 25°C, F = 1.0 MHZ, V_{CC} = 5V

Symbol	Parameter	Max.	Unit	Test Condition
C_{OUT}(1)	Output capacitance (SDA, $\overline{RESET}$)	8	pF	V_{OUT} = 0V
C_{IN}(1)	Input capacitance (SCL)	6	pF	V_{IN} = 0V

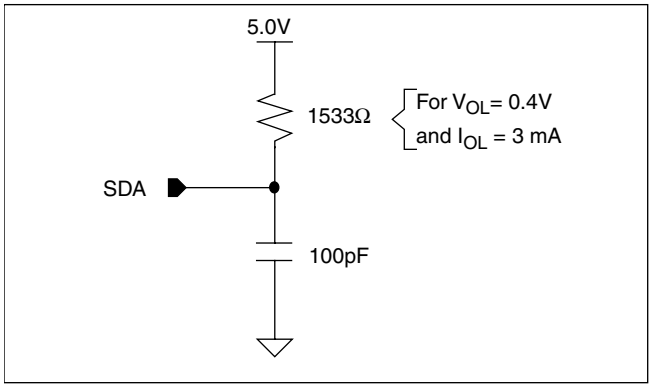
Note: (1) This parameter is periodically sampled and not 100% tested.

AC CHARACTERISTICS

AC Test Conditions

Input pulse levels	$V_{CC} \times 0.1$ to $V_{CC} \times 0.9$
Input rise and fall times	10ns
Input and output timing levels	$V_{CC} \times 0.5$
Output load	Standard output load

EQUIVALENT AC OUTPUT LOAD CIRCUIT FOR V_{CC} = 5V (standard output load for testing the device with V_{CC} = 5.0V)



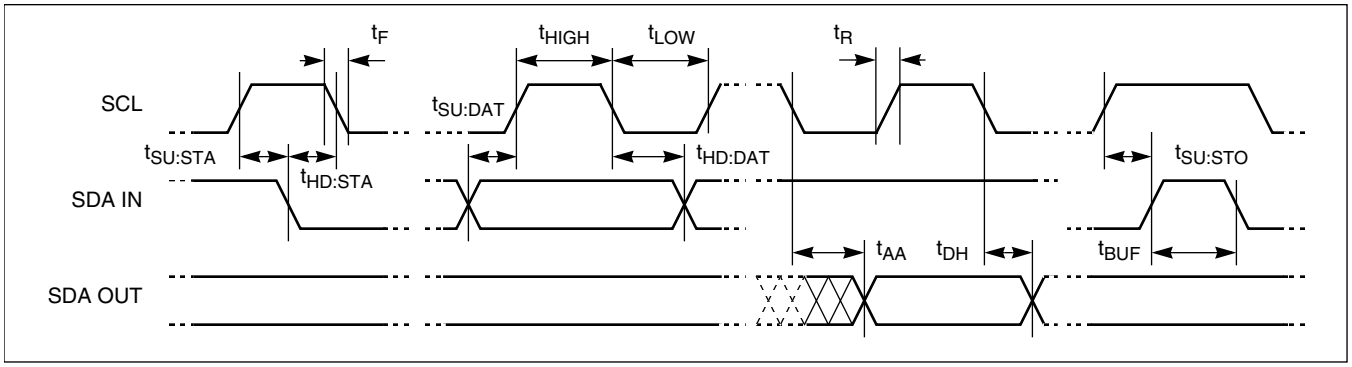
AC SPECIFICATIONS (T_A = -40°C to +85°C, V_{CC} = +2.7V to +5.5V, unless otherwise specified.)

Symbol	Parameter	Min.	Max.	Unit
f_{SCL}	SCL clock frequency	0	400	kHz
t_{IN}	Pulse width suppression time at inputs	50		ns
t_{AA}	SCL LOW to SDA data out valid	0.1	0.9	µs
t_{BUF}	Time the bus must be free before a new transmission can start	1.3		µs
t_{LOW}	Clock LOW time	1.3		µs
t_{HIGH}	Clock HIGH time	0.6		µs
$t_{SU:STA}$	Start condition setup time	0.6		µs
$t_{HD:STA}$	Start condition hold time	0.6		µs
$t_{SU:DAT}$	Data in setup time	100		ns
$t_{HD:DAT}$	Data in hold time	0		µs
$t_{SU:STO}$	Stop condition setup time	0.6		µs
t_{DH}	Data output hold time	50		ns
t_R	SDA and SCL rise time	20 +.1Cb(3)	300	ns
t_F	SDA and SCL fall time	20 +.1Cb(3)	300	ns
Cb	Capacitive load for each bus line		400	pF

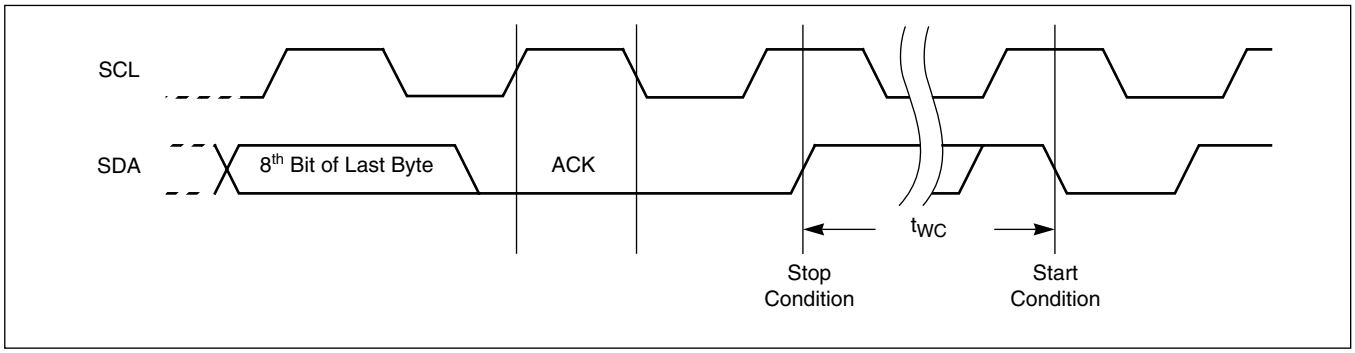
Notes: (1) Typical values are for T_A = 25°C and V_{CC} = 5.0V
(2) This parameter is periodically sampled and not 100% tested.
(3) Cb = total capacitance of one bus line in pF.

TIMING DIAGRAMS

Bus Timing



Write Cycle Timing



Power Up Timing

Symbol	Parameter	Min.	Typ.(2)	Max.	Unit
t_{PUR}(1)	Time from power up to read			1	ms
t_{PUW}(1)	Time from power up to write			5	ms

Notes: (1) Delays are measured from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.
(2) Typical values are for T_A = 25°C and V_{CC} = 5.0V

Nonvolatile Write Cycle Timing

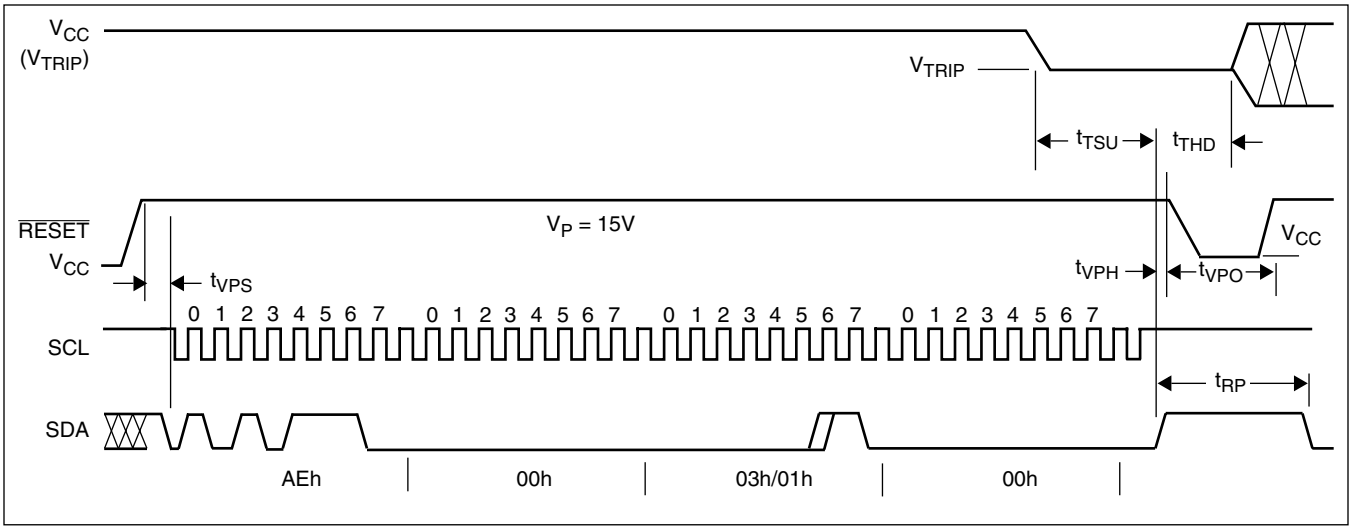
Symbol	Parameter	Min.	Typ.(1)	Max.	Unit
t_{WC}(1)	Write cycle time		5	10	ms

Note: (1) t_{WC} is the time from a valid stop condition at the end of a write sequence to the end of the self-timed internal nonvolatile write cycle. It is the minimum cycle time to be allowed for any nonvolatile write by the user, unless Acknowledge Polling is used.

WATCHDOG TIMER/LOW VOLTAGE RESET OPERATING CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{PTRIP}	Pre-programmed reset trip voltage				
	X1202-4.5A	4.49	4.63	4.77	
	X1202	4.25	4.38	4.51	V
	X1202-2.7A	2.76	2.85	2.94	
	X1202-2.7	2.57	2.65	2.73	
t_{RPD}	V_{CC} detect to $\overline{RESET}$ LOW			500	ns
t_{PURST1}	Power up reset time out delay	100	200	400	ms
t_F	V_{CC} fall time	10			µs
t_R	V_{CC} rise time	10			µs
t_{WDO}	Watchdog timer period:				
	WD1 = 0, WD0 = 0	1.7	1.75	1.8	s
	WD1 = 0, WD0 = 1	725	750	775	ms
	WD1 = 1, WD0 = 0	225	250	275	ms
t_{RST1}	Watchdog reset time out delay	225	250	275	ms
t_{RSP}	2-wire interface	1			µs
V_{RVALID}	Reset valid V_{CC}	1.0			V

V_{TRIP} Programming Timing Diagram



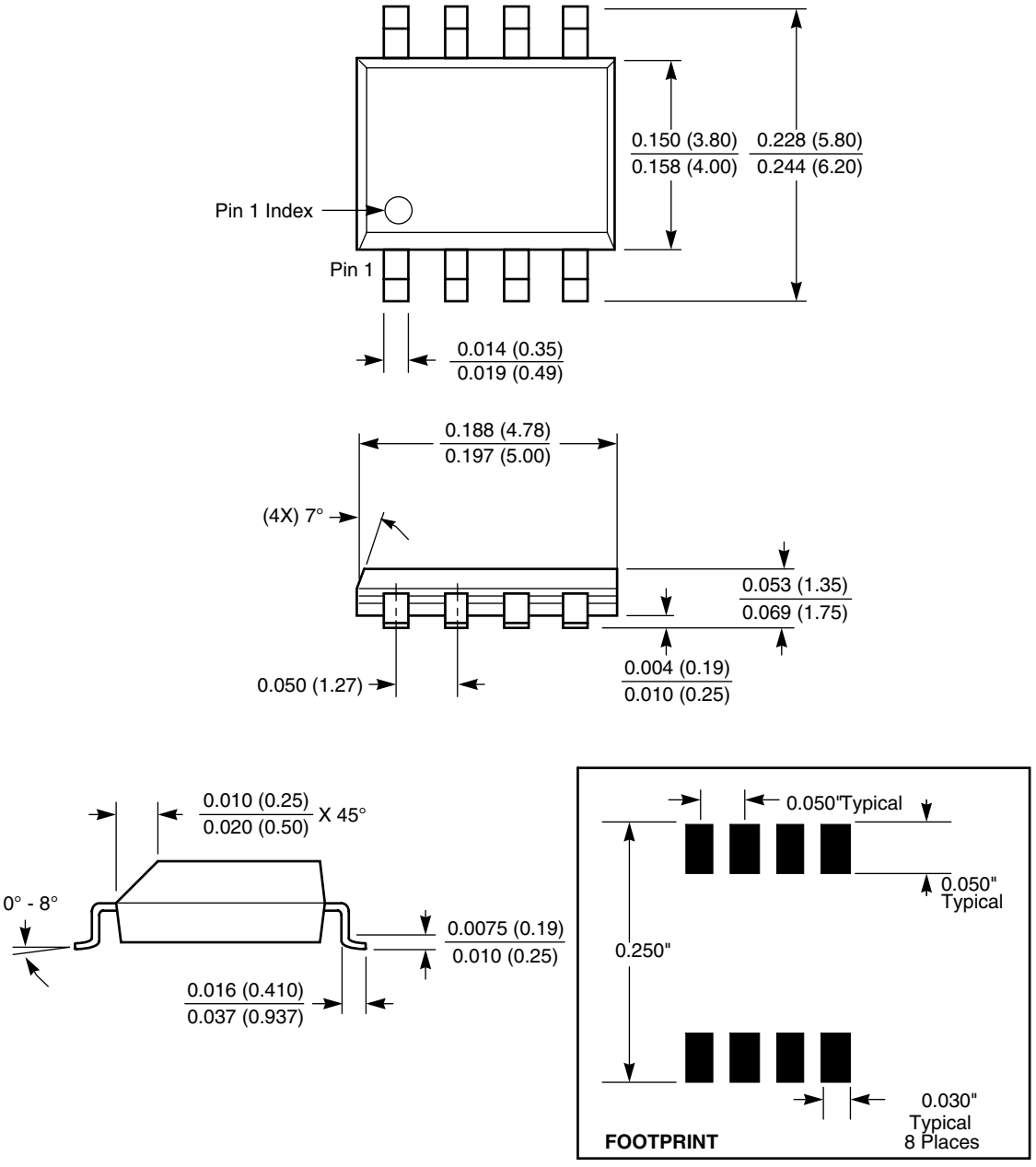
V_{TRIP} Programming Parameters

Parameter	Description	Min.	Max.	Unit
t_{VPS}	V_{TRIP} program enable voltage setup time	1		µs
t_{VPH}	V_{TRIP} program enable voltage hold time	1		µs
t_{TSU}	V_{TRIP} setup time	1		µs
t_{THD}	V_{TRIP} hold (stable) time	10		ms
t_{WC}	V_{TRIP} write cycle time		10	ms
t_{VPO}	V_{TRIP} program enable voltage off time (between successive adjustments)	0		µs
t_{RP}	V_{TRIP} program recovery period (between successive adjustments)	10		ms
V_P	Programming voltage	14	15	V
V_{TRAN}	V_{TRIP} programmed voltage range	1.7	5.0	V
V_{ta1}	Initial V_{TRIP} program voltage accuracy (V_{CC} applied–V_{TRIP}) (programmed at 25°C)	-0.1	+0.4	V
V_{ta2}	Subsequent V_{TRIP} program voltage accuracy [(V_{CC} applied–V_{ta1})—V_{TRIP}. Programmed at 25°C.)	-25	+25	mV
V_{tr}	V_{TRIP} program voltage repeatability (Successive program operations. Programmed at 25°C.)	-25	+25	mV
V_{tv}	V_{TRIP} program variation after programming (0–75°C). (programmed at 25°C)	-25	+25	mV

V_{TRIP} programming parameters are periodically sampled and are not 100% tested.

PACKAGING INFORMATION

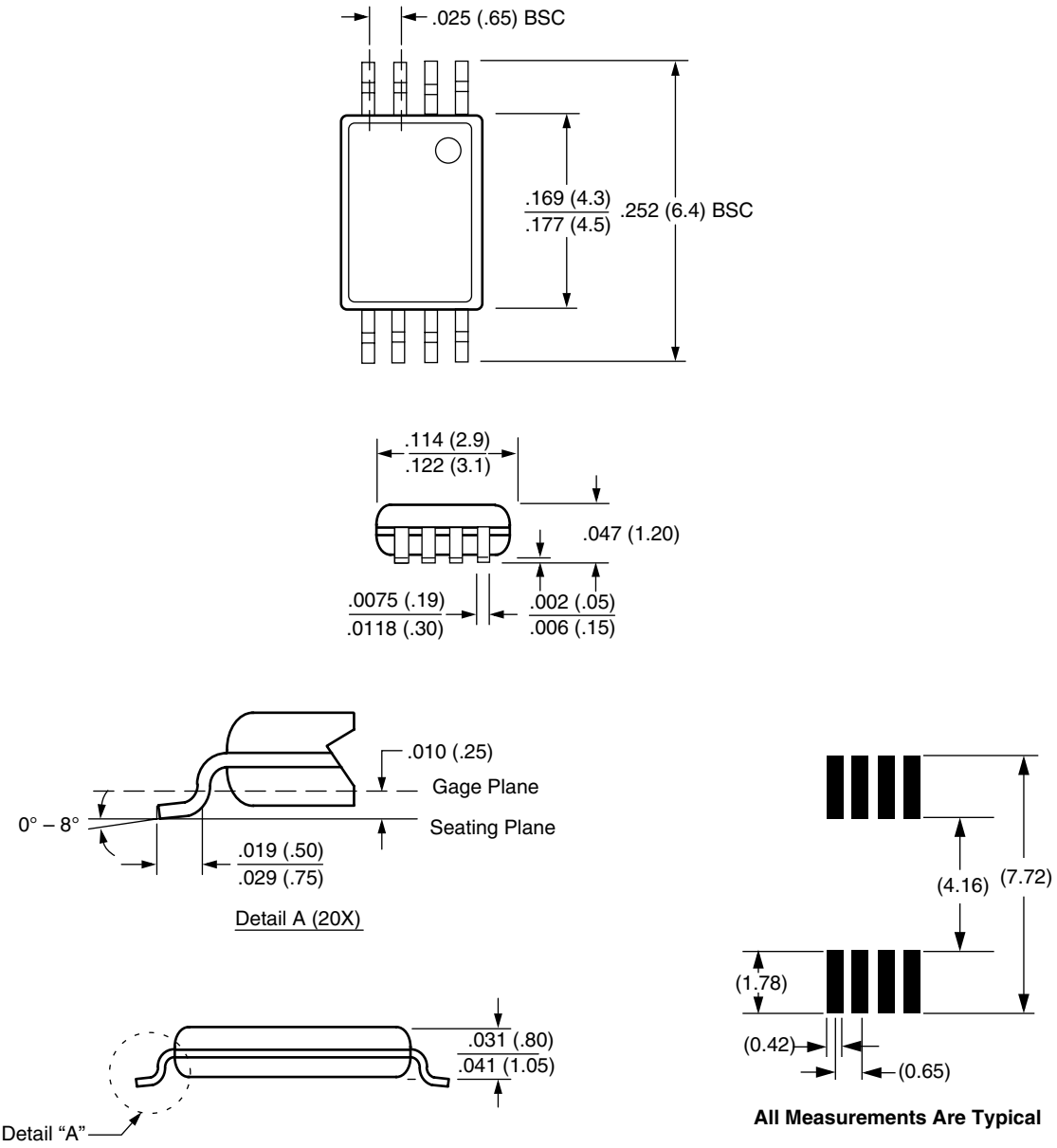
8-Lead Plastic, SOIC, Package Code S8



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

8-Lead Plastic, TSSOP, Package Code V8



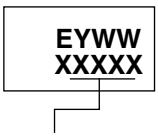
NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

Ordering Information

V_{CC} Range	V_{TRIP}	Package	Operating Temperature Range	Part Number
4.5–5.5V	4.63V ± 3%	8L SOIC	0–70°C	X1202S8-4.5A
			-40–85°C	X1202S8I-4.5A
4.5–5.5V	4.63V ± 3%	8L TSSOP	0–70°C	X1202V8-4.5A
			-40–85°C	X1202V8I-4.5A
4.5–5.5V	4.38V ± 3%	8L SOIC	0–70°C	X1202S8
			-40–85°C	X1202S8I
4.5–5.5V	4.38V ± 3%	8L TSSOP	0–70°C	X1202V8
			-40–85°C	X1202V8I
2.7–3.6V	2.85V ± 3%	8L SOIC	0–70°C	X1202S8-2.7A
			-40–85°C	X1202S8I-2.7A
2.7–3.6V	2.85V ± 3%	8L TSSOP	0–70°C	X1202V8-2.7A
			-40–85°C	X1202V8I-2.7A
2.7–3.6V	2.65V ± 3%	8L SOIC	0–70°C	X1202S8-2.7
			-40–85°C	X1202S8I-2.7
2.7–3.6V	2.65V ± 3%	8L TSSOP	0–70°C	X1202V8-2.7
			-40–85°C	X1202V8I-2.7

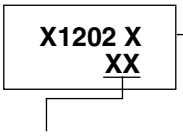
Part Mark Information

8-Lead TSSOP



1202AL = 4.5 to 5.5V, 0 to +70°C, V_{TRIP} = 4.63V ± 3%
1202AM = 4.5 to 5.5V, -40 to +85°C, V_{TRIP} = 4.63V ± 3%
1202 = 4.5 to 5.5V, 0 to +70°C, V_{TRIP} = 4.38V ± 3%
1202I = 4.5 to 5.5V, -40 to +85°C, V_{TRIP} = 4.38V ± 3%
1202AN = 2.7 to 3.6V, 0 to +70°C, V_{TRIP} = 2.85V ± 3%
1202AP = 2.7 to 3.6V, -40 to +85°C, V_{TRIP} = 2.85V ± 3%
1202F = 2.7 to 3.6V, 0 to +70°C, V_{TRIP} = 2.65V ± 3%
1202G = 2.7 to 3.6V, -40 to +85°C, V_{TRIP} = 2.65V ± 3%

8-Lead SOIC



AL = 4.5 to 5.5V, 0 to +70°C, V_{TRIP} = 4.63V ± 3%
AM = 4.5 to 5.5V, -40 to +85°C, V_{TRIP} = 4.63V ± 3%
Blank = 4.5 to 5.5V, 0 to +70°C, V_{TRIP} = 4.38V ± 3%
I = 4.5 to 5.5V, -40 to +85°C, V_{TRIP} = 4.38V ± 3%
AN = 2.7 to 3.6V, 0 to +70°C, V_{TRIP} = 2.85V ± 3%
AP = 2.7 to 3.6V, -40 to +85°C, V_{TRIP} = 2.85V ± 3%
F = 2.7 to 3.6V, 0 to +70°C, V_{TRIP} = 2.65V ± 3%
G = 2.7 to 3.6V, -40 to +85°C, V_{TRIP} = 2.65V ± 3%