R96XFER-B/R144XFER-B eXtended FAXENGINE™ Device Set

INTRODUCTION

The Rockwell R96XFER-B/R144XFER-B eXtended FAXENGINE™ Device Set hardware, Core Code, Application Code, and FAXENGINE Development System (FEES-X and MC24 FERE) comprise a working facsimile machine controller—needing only a power supply, scanner, printer, and paper path components to complete the machine.

FAXENGINE DEVICE SET HARDWARE

The R96XFER-B/R144XFER-B FAXENGINE Device Set hardware (abbreviated XFER-B) consists of the Rockwell eXtended FAXENGINE Facsimile Controller with Reduced Drive (XFCR-B) device (11662-12) and a Rockwell MONOFAX® Modem device (R96DFXL or R144EFXL).

FAXENGINE Integrated Facsimile Controller

The XFCR-B provides design flexibility by virtue of its built-in peripheral functions (e.g., scanner, printer, operator interface) and programmable hardware registers.

The XFCR-B performs the primary facsimile machine control and monitoring functions interfacing with major fax machine components. The MC24™ embedded processor provides a 24-bit internal address bus; and 2 Mbyte direct external memory accessing capability.

Scanner, printer, and keyboard interfaces, as well as motor control and the modem interface, are included. These programmable functions and interfaces support a wide range of peripherals. An integrated flash ADC, combined with Rockwell's Proprietary Image Corrections System (RPICS™), delivers state-of-the-art image processing with both text and half-tone images.

MONOFAX Modems

Two different MONOFAX modems are available with selection depending upon the desired applications.

The R144EFXL and R96DFXL modems are 14400 bps and 9600 bps half-duplex MONOFAX facsimile modems which support Group 3, HDLC framing, tone generation and detection, and DTMF reception.

The modems operate over the public switched telephone network (PSTN) through line terminations provided by a data access arrangement (DAA). The modem satisfies the requirements of CCITT recommendations V.17 (R144EFXL only), V.29, V.27 ter, V.21 Channel 2, and T.4, and meets the binary signaling requirements of T.30.

FAXENGINE Device Set Firmware

The FAXENGINE includes a complete software package for the development of a customized facsimile machine. The following features are supported by the firmware:

- A real-time multitasking environment
- Modular software design
- T.30 protocol and call progress support for multiple countries
- T.4 MH compression and decompression
- B4 to A4 reduction
- Fax copy, transmit and receive capabilities

Application Code. The Application Code “builds” an example fax machine using the XFCR-B in the FEES-X environment. This machine is based on the provided Core Code. The Application Code is provided in source code form and serves as basis for the developer’s application.

Core Code. The Core Code provides the functions with close (functional) proximity to the XFCR-B hardware. The Core Code is provided in object code form ready for linking to developer-provided application program object code. The Core Code is highly structured for maximum application flexibility with minimum overhead.

FAXENGINE DEVELOPMENT SYSTEM

The Rockwell FAXENGINE Development System (FEES-X) provides demonstration, prototype development, and evaluation capabilities to facsimile machine developers using the XFER-B FAXENGINE Device Set. The FEES-X provides flexibility for visibility and access supplying the R96/144MEB Modem Evaluation Board, sockets for programmable parts, and connectors for an emulator and all fax machine peripherals. Also supported is the Rockwell FAXENGINE and ROM Emulator (MC24 FERE), a PC-based code development aid with breakpoint and trace capability for debugging customer-created firmware.

FEATURES

- **Supports R144EFXL and R96DFXL MONOFAX Modems**
- **FAXENGINE Development System** (FEES-X, and MC24 FERE)
  - Provides demonstration, prototype development, and evaluation capabilities to facsimile machine developers using the FAXENGINE Device Set.
  - Connects to a FAXENGINE and ROM emulator (MC24 FERE)
- **Microprocessor and Bus Interface**
  - Enhanced MC24 central processing unit (CPU)
    - 10 MHz clock speed
    - Memory efficient input/output bit manipulation
    - 24-bit internal address bus
  - External Bus
    - Address, data, control, status, interrupt, and decoded chip select signals support connection to external ROM, external RAM, and optional peripheral devices
    - Dedicated internal DMA logic is included for scanner and printer access of internal and/or external memory
  - Twenty bit external address bus
  - External RAM up to 1 Mbyte
  - External ROM up to 1 Mbyte
  - Interrupt controller
  - Three internal DMA channels
  - Chip selects
    - ROMCSn, CS0n for SRAM
    - CS1n for external peripheral
    - MCSn for modem
    - Optional general purpose: CS2n, CS3n, CS4n
- Motor Control for Scanner, and Printer
  - Independent scan and print line times
  - Four outputs to external current drivers for the scanner motor and four for the printer motor
  - The printer or scanner motor outputs can be programmed as general purpose outputs (GPO) for application with a single motor
- **Scanner and Video Control**
  - CCD and CIS scanners supported
  - Six programmable control signals:
    - Four programmable scanner control signals
    - Two video control output signals support external signal pre-processing
  - B4/A4 scanner support
  - 5 ms line time
  - Scanner flash A/D Interface
    - Internal 6-bit flash A/D converter
    - A/D reference inputs available for control by external circuits
  - Video Processing
    - Per single pixel and per eight pixel shading correction
    - Edge enhancement and dynamic background and contrast control
    - Up to 8x8 programmable dither table
    - Image data processing port allows access to scan data prior to video processing
  - Resolution conversion features:
    - Vertical line “OR”ing
    - Scanner output bit order reversal
- **Thermal Printer Interface**
  - 1 to 4 programmable strobe signals
  - Traditional printers and latchless “split mode” printers
  - Line lengths up to 4096 pixels
  - Line times from 5 to 40 ms
  - A/D converter monitors printer head temperature
- **Programmable Tone Generator**
- **Operator Interface**
  - The XFCR-B can directly drive a 20-key keypad
  - A 5x15 keyboard array is supportable with external circuitry
  - Up to five LEDs are driven directly
  - A 2-line LCD display module, with 20 characters per line, is supported
- **Synchronous Asynchronous Receiver Transmitter (SART) Interface**
  - Programmable baud rate generator support to 9600 bps
  - Async mode: 1 start bit, 7/8 data bits, 1 stop bit, no parity
  - Sync mode: 8 data bits
  - Firmware controllable TXD and SCLK
- **General Purpose Inputs and/or Outputs**
  - Provides up to 16 GPIO and 8 GPOs
- **Real Time Clock**
  - Battery backup
  - 32 years range with leap year compensation
- **Watchdog Timer**

HARDWARE DESCRIPTION

The XFER-B system-level functional interface is shown in Figure 1. (Note: The suffix n indicates an active low signal.)

Integrated Facsimile Controller (XFCR-B)

The XFCR-B contains an internal 8-bit microprocessor with a 2-Mbyte external address space and dedicated circuitry optimized for facsimile image processing and for facsimile machine control and monitoring.

Microprocessor

The microprocessor is an enhanced MC24 central processing unit (CPU). This CPU provides fast instruction execution (10 MHz clock speed) and memory efficient input/output bit manipulation. The CPU connects to other internal XFCR-B functions over an 8-bit data and 24-bit internal/20-bit external address bus and dedicated control lines.

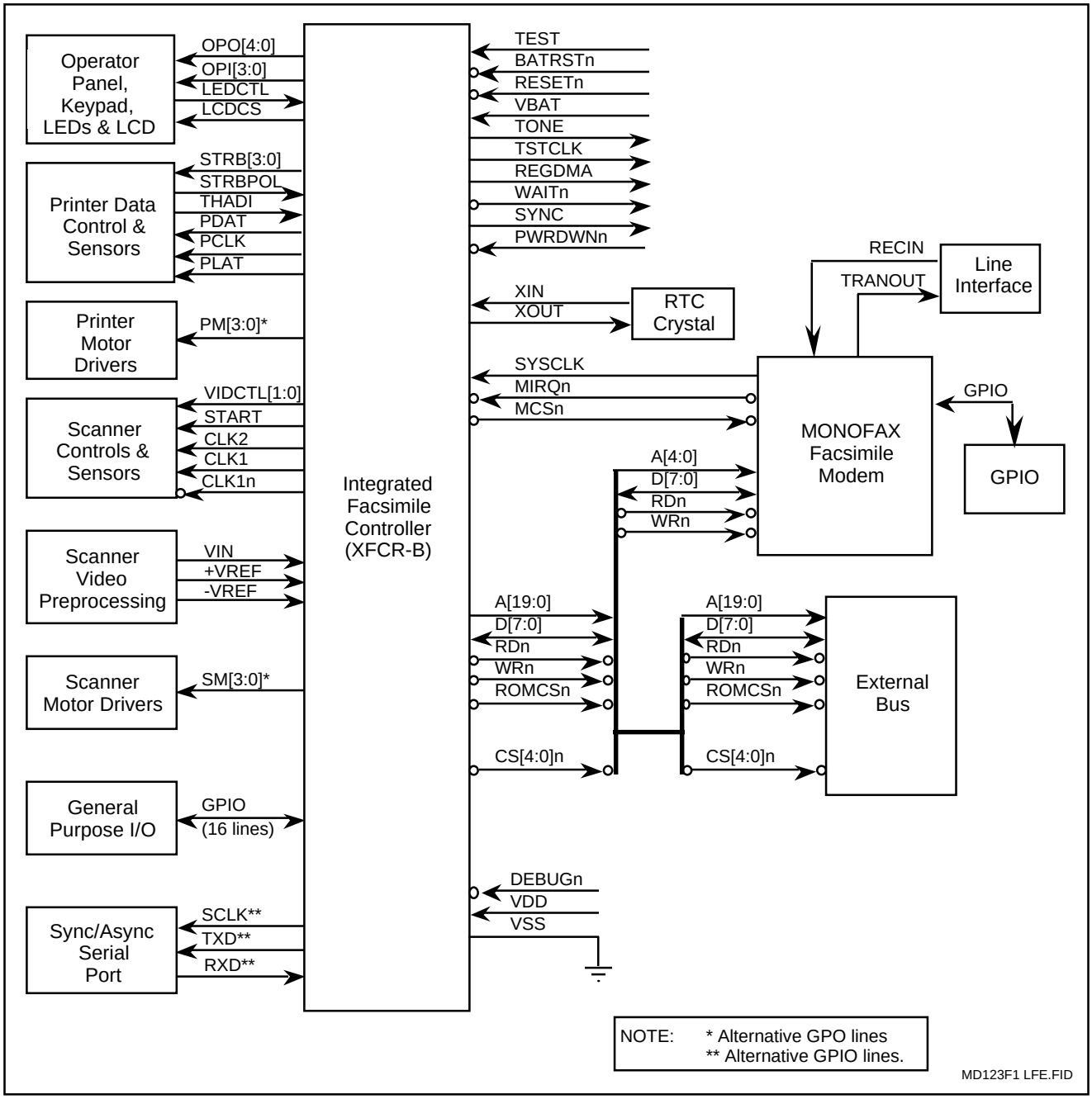


Figure 1. R144XFER-B Functional Interconnect Diagram

External Bus Control

Address, data, control, status, interrupt, and decoded chip select signals support connection to external ROM, external RAM, and to optional peripheral devices. Dedicated internal DMA logic is included for scanner and printer access of internal and/or external RAM.

External RAM and ROM. Up to 1 Mbyte RAM and up to 1Mbyte ROM can be connected to the XFCR-B as well as external peripherals. ROM stores all the FAXENGINE program object code and RAM is used by the FAXENGINE CPU, shading RAM and line buffer RAM. Three internal DMA channels support scanner and printer access of the external shading RAM and line buffer RAM. (RAM wait states: 0-3; sizes: 8K, 32K, 64K, and 1 Mbyte.)

Chip Selects

Various chip selects (CS) are provided by the XFCR-B such as ROMCSn, CS0n for SRAM, CS1n for external peripheral, MCSn for modem, and optional general purpose chip selects CS2n, CS3n, CS4n.

Interrupt Signals

Two external interrupts are provided. IRQ8 is an active high level sensitive interrupt and IRQ5 is an active low level sensitive interrupt. A third interrupt, MIRQn, is dedicated to the modem.

Scanner and Printer Motor Control

Eight outputs are provided to external current drivers: four for the scanner motor and four for the printer motor. The printer and scanner motor outputs can be programmed as general purpose outputs (GPO) for applications using a single motor. Independent scan and print line times are supported in supplied Application Code Firmware.

The thermal printer interface consists of programmable data, latch, clock, and up to four strobe signals. Programmable timing supports traditional thermal printers, as well as latchless and two-clock split mode printers, and line lengths up to 4096 pixels.

From one to four strobes are generated, with the length of the strobe cycle (line time) and strobe pulse width programmable. Line times from 5 to 40 ms are supported. A strap input to the XFCR-B sets the strobe polarity.

Three signals (PDAT, PCLK, and PLAT) control the transfer of data to the printer.

The XFCR-B includes a 6-bit A/D converter (conversion rate < 80 ms) to monitor the head temperature of the thermal printer. Two external terminating resistors are determined by the specific printhead selected.

Scanner and Video Control

Six programmable control and timing signals support common CCD and CIS scanners. The video control function provides signals for controlling the scanner and for processing its video output. Four programmable control signals (START, CLK1, CLK1n, and CLK2) provide timing related to line and pixel timing. These are programmable with regard to start time, relative delay and pulse width.

Two video control output signals (VIDCTL[1:0]) provide digital control for external signal pre-processing circuitry. These signals provide a per pixel period, or per line period, timing with programmable positive-going and negative-going transitions for each signal.

Scanner Flash A/D Interface

An internal 6-bit flash A/D converter (FADC) and ADC clock are provided. The A/D reference inputs (Vref+ and Vref–) are available for control by external circuits. A programmable ADC sample position is provided and external video circuits can be tailored by the developer.

Video Processing

The XFCR-B supports two modes of correction for scanner data non-uniformities arising from uneven sensor output or uneven illumination. Correction may be provided to an 8-pixel group at a time or, may be applied separately to each pixel. Less than 1k byte of RAM is required to support shading correction. Edge enhancement and dynamic background and contrast control (auto background control, contrast control, MTF) are also performed. The XFCR-B includes an 8x8 dither table, which is programmable and stored in internal RAM (8 bits per table entry). The table is arranged in a matrix of up to 8 rows by up to 8 columns.

The XFCR-B also includes an optional external image data processing port (multiplexed with GPIO–see below) to allow the OEM developer to access scan data prior to video processing in order to perform proprietary processing.

VID0 - VID7 = parallel output port for multi-level FADC data or shading corrected data (or reduced shading corrected data)

VIDC0 - VIDC1 = control for synchronization with video port data

VIDC2 = bi-level data input for externally processed image data

Operator Interface

Operator interface functions are supported by the operator output bus (OPO[4:0]), the operator input bus (OPI[3:0]), and two control outputs (LEDCTL and LCDCS).

The XFCR-B can directly drive a 20-key keypad. External blocking diodes are required to isolate the keyboard strobe lines from the LEDs, as the LEDs and keyboard strobe signals use the same lines. A 5 by 15 keyboard array is supportable with external circuitry.

Up to five LEDs can be driven directly by the XFCR-B. The keyboard strobes are shared with the LED drivers. An LED control signal is provided to disable the LEDs during keyboard strobing. The XFCR-B slightly offsets LED turn on/off times thereby preventing power supply overload when all indicators must be activated simultaneously. The LEDCTL signal can supply 12 mA.

Typical LCD display modules are driven by the XFCR-B. The XFCR-B drives the 4-bit bus (OPO[3:0]) and two separate control lines (OPO4 and LCDCS). (For example, the FAXENGINE Development System FEES-X uses a 2-line, 20 character per line, display.)

Synchronous Asynchronous Receiver Transmitter (SART)

The SART performs serial-to-parallel (S/P) conversion for data received from a peripheral device, and a parallel-to-serial (P/S) conversion of data for transmission to a peripheral device. The interface consists of three lines: TXD, RXD and clock (SCLK). The SART includes a programmable baud rate generator and produces an 8X clock for driving internal logic. Receive data is double-buffered to ease received timing restrictions.

SART status can be read at any time by the CPU. Status includes: IRQ source (TXD or RXD) and operation mode (sync or async). The CPU can also control and monitor TXD and SCLK: RXD can be monitored at any time.

Real Time Clock (RTC)

The XFCR-B includes a battery backed-up real time clock. The RTC life is 32 years. The RTC includes leap year compensation. A 32.768 kHz watch crystal is required by the RTC.

General Purpose Inputs and/or Outputs

The XFCR-B provides up to 16 GPIO and 8 GPO lines.

Programmable Tone Generator

A programmable tone generator provides single tone digital output, variable in frequency from 20 to 4000 Hz.

System Timing

The XFCR-B can derive its timing from the modem clock or from an external oscillator. Two internal timer interrupts are provided:

- A 1 ms timer derived from the RTC oscillator timebase
- A programmable Mechanical System Interrupt (MSINT)

Reset and Power Control

The BATRSTn input initializes the XFCR-B at power-on. An externally generated power-down input, PWRDWNn, controls switching between primary and battery power. The open drain RESETn I/O pin provides a reset output to external circuits, or can accept an externally generated reset. External reset will not reset the RTC.

FACSIMILE MODEM

Complete modem documentation is provided in the references cited in Table 1.

ENVIRONMENTAL AND POWER REQUIREMENTS

Environmental requirements are given in Table 2 and power requirements are given in Table 3.

XFCR-B INTERFACE SIGNALS

XFCR-B pin assignments are shown in Figure 2 and listed in Table 4. Signals are described in Tables 5 - 7.

FACSIMILE MODEM INTERFACE SIGNALS

R96DFXL and R144EFXL pin assignments are shown in Figure 3 and described in Table 6. R96DFXL and R144EFXL hardware interface signals are listed by functional group in Table 7. The modem digital interface characteristics are listed in Table 8, and the analog interface characteristics are in Table 9.

REFERENCE DOCUMENTATION

Table 1. Reference Documentation

Document	Order No.
R96DFXL MONOFAX Modem Data Sheet	MD92
R144EFXL MONOFAX Modem Data Sheet	MD90
MC24 Megacell CPU Programmer's Guide	415
9600 bps MONOFAX Modem Designer's Guide	820
9600 bps MONOFAX Modem Designer's Guide–Addendum for R96DFXL	820A
R144EFXL MONOFAX Modem Designer's Guide	895
eXtended Facsimile Controller (XFC-B) Hardware Description	1039
eXtended Facsimile Controller (XFC-B) Evaluation System (FEES-X) User's Manual	1040
eXtended FAXENGINE (XFE-B) Firmware Description	1041
MC24 FAXENGINE ROM Emulator System (MC24 FERE) User's Manual	1016
MC24 CPU Megacell Programming Manual	415

Table 2. Environmental Specifications

Parameter	Specification
Temperature:	
Operating	0°C to 70°C (32°F to 158°F)
Storage	-40°C to 80°C (-40°F to 176°F)
Relative Humidity	Up to 90% non-condensing, or a wet bulb temperature up to 35°C, whichever is less.

Table 3. Power Requirements

Device	Voltage[1]	Typical Current @25°C	Maximum Current @ 0°C
XFC with Primary Power			
	+5 VDC +5%/-10%	60 mA	
XFC with Battery Power and RTC[2]			
	+5 VDC	20µA	
	+3 VDC	5 µA	
MONOFAX Modems			
R96DFXL	+5 VDC ±5%	50 mA	55 mA
R144EFXL	+5 VDC ±5%	54 mA	60 mA

Notes:
1. Input voltage ripple •0.1 volts peak-to-peak. The amplitude of any frequency between 20 and 150 kHz must be less than 500 microvolts peak.
2. Battery power measurements made with a 32.768 kHz crystal oscillator.

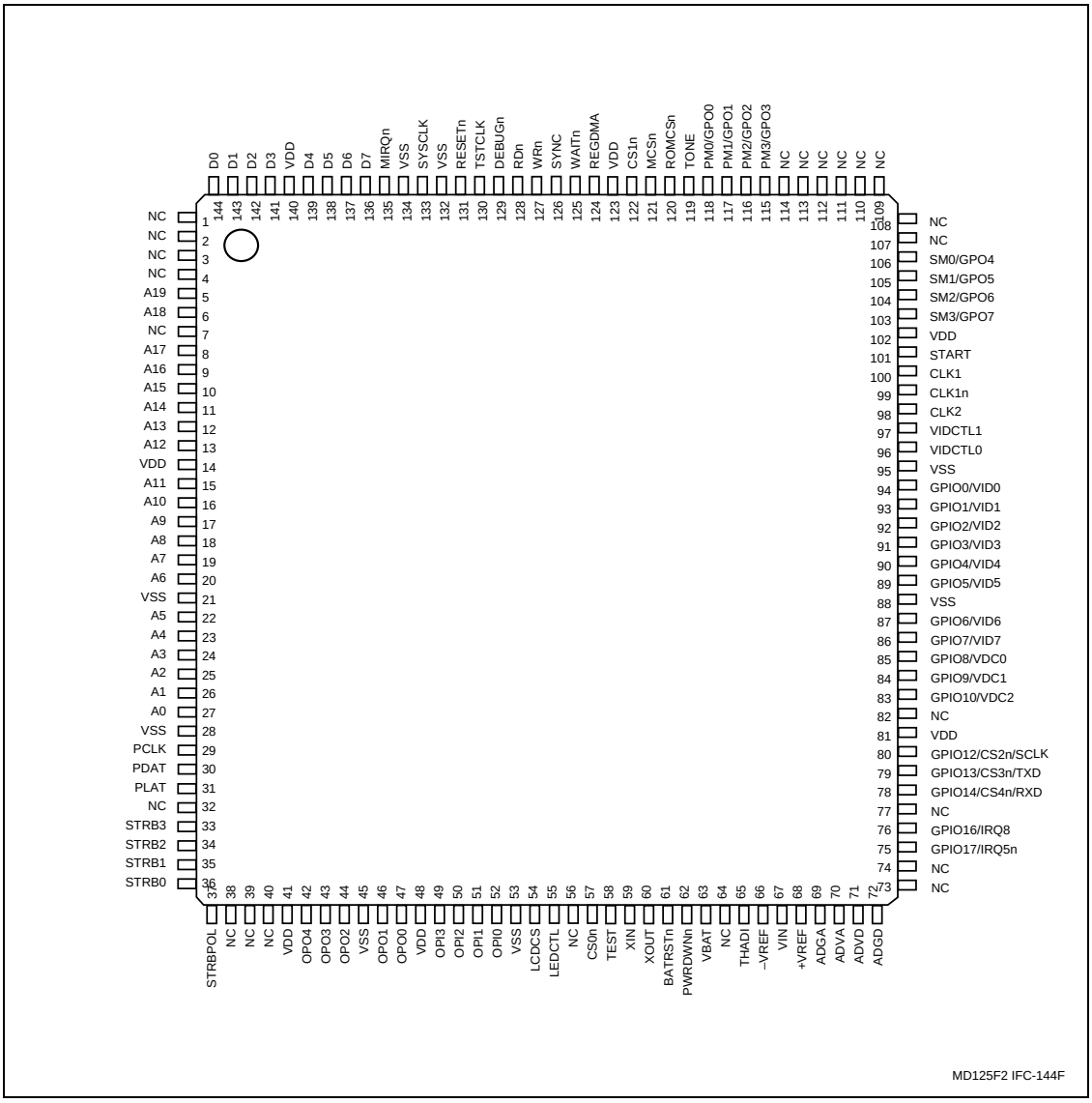


Figure 2. XFCR-B Pin Signals - 144-Pin PQFP

Table 4. XFCR-B Pin Assignments

Pin Name	Pin No.	I/O	Input Type	Output Type	Pin Description (Note: Active low signals have an "n" pin name ending.)
CPU Control Interface					
MIRQn	135	I	HU	--	Modem interrupt. (Hysteresis In, Internal Pullup.)
SYSCLK	133	I	H	--	System clock. (Hysteresis In.)
TSTCLK	130	O	--	1XC	Test clock.
Bus Control Interface					
A[19:0]	[5:6][8:13] [15:20][22:27]	O	T	1XT	Address bus (20-bit).
D[7:0]	[136:139] [141:144]	I/O	T	1XT	Data bus (8-bit).
RDn	128	O	--	1XTT	Read strobe.
WRn	127	O	--	1XTT	Write strobe.
ROMCSn	120	O	--	1XT	ROM chip select.
CS1n	122	O	--	1XT	I/O chip select.
CS0n	57	O	--	1XTT	SRAM chip select. (Battery powered.)
MCSn	121	O	--	1XC	Modem chip select.
SYNC	126	O	--	1XC	Indicates CPU op code fetch cycle (active high).
REGDMA	124	O	--	1XC	Indicates REGSEL cycle and DMA cycle.
WAITn	125	O	--	1XC	Indicates current TSTCLK cycle is a wait state or a halt state.
Prime Power Reset Logic and Test					
DEBUGn	129	I	HU	--	External non-maskable input (NMI).
RESETn	131	I/O	HU	2XO	XFCR-B Reset.
TEST	58	I	C	--	Sets Test mode (battery powered).
Battery Power Control and Reset Logic					
XIN	59	I	OSC	--	Crystal oscillator input pin.
XOUT	60	O	--	OSC	Crystal oscillator output pin.
PWRDWNn	62	I	H	--	Indicates loss of prime power (results in NMI).
BATRSTn	61	I	H	--	Battery power reset input
Scanner Interface					
START	101	O	--	2XS	Scanner shift gate control.
CLK1	100	O	--	2XS	Scanner clock.
CLK1n	99	O	--	2XS	Scanner clock-inverted.
CLK2	98	O	--	2XS	Scanner reset gate control (or clock for CIS scanner).
VIDCTL[1:0]	[97:96]	O	--	2XC	Control for video preprocessing circuits.
Printer Interface					
PCLK	29	O	--	3XC	Thermal Print Head (TPH) clock.
PDAT	30	O	--	2XP	Serial printing data (to TPH).
PLAT	31	O	--	3XP	TPH data latch.
STRB[3:0]	[33:36]	O	--	1XP	Strobe signals for the TPH.
STRBPOL	37	I	C	--	Sets strobe polarity, active high/low.
Operator Panel Interface					
OPO[4:0]		O	--	2XL	Keyboard / LED strobe [4:0].
OPI[3:0]	[49:52]	I	HU	--	Keyboard return [3:0]. (Pullup, Hysteresis In.)
LEDCTL	55	O	--	4XC	Indicates outputs OPO[4:0] are for LEDs.
LCDCS	54	O	--	1XC	LCD chip select.

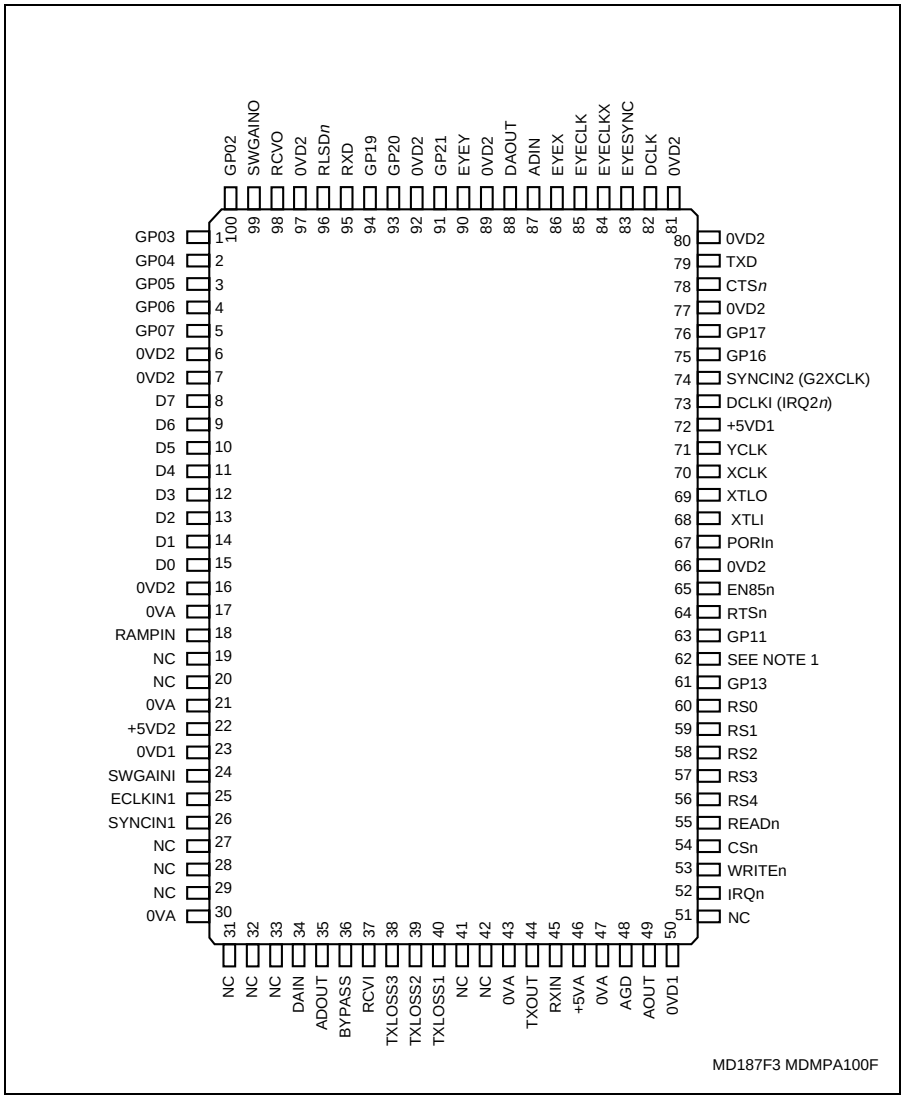
continued

Table 4. XFCR-B Pin Assignments (Continued)

Pin Name	Pin No.	I/O	Input Type	Output Type	Pin Description
General Purpose I/O					
GPIO[7:0]/ VID[7:0]	[86:87][89:94]	I/O	H	2XC	Programmable: GPIO (8 lines) or video data bus.
GPIO[10:8]/ VDC[2:0]	[83:85]	I/O	H	2XC	Programmable: GPIO (3 lines) or video data control signals.
GPIO12/CS2n/ SCLK	80	I/O	H	2XC	Programmable: GPIO line, I/O chip select or SCLK (SART).
GPIO13/CS3n/TXD	79	I/O	H	2XC	Programmable: GPIO line, I/O chip select or TXD (SART).
GPIO14/CS4n/RXD	78	I/O	H	2XC	Programmable: GPIO line, I/O chip select or RXD (SART).
GPIO16/IRQ8	76	I/O	H	1XC	Programmable: GPIO line or active high interrupt.
GPIO17/IRQ5n	75	I/O	H	1XC	Programmable: GPIO line or active low interrupt.
Miscellaneous					
SM[3:0]/GPO[7:4]	[103:106]	O	--	1XC	Programmable: scan motor control pins or GPO pins.
PM[3:0]/GPO[3:0]	[115:118]	O	--	1XC	Programmable: print motor control pins or GPO pins
TONE	119	O	--	1XC	Tone output signal.
Power, Reference Voltages and Ground					
-Vref	66	I	–VR	--	Negative Reference Voltage for Video A/D.
+Vref	68	I	+VR	--	Positive Reference Voltage for Video A/D.
ADGA	69		VADG		A/D Analog Ground.
ADVA	70		VADV		A/D Analog Power.
ADGD	72		VADG		A/D Digital Ground.
ADVD	71		VADV		A/D Digital Power.
VIN	67	I	VA	--	Analog Video A/D input.
THADI	65	I	TA	--	Analog Thermal A/D input.
VSS(8)	134, 132, 95, 88, 53, 45, 28, 21				Digital Ground.
VDD (7)	140, 123, 102, 81, 48, 41, 14				Digital Power.
VBAT	63				Battery Power.
No Connection					
NC	1, 2, 3, 4, 7, 32, 38, 39, 40, 56, 64, 73, 74, 77, 82, 107, 108, 109, 110, 111, 112, 113, 114				No connection.

Table 5. XFCR-B Input and Output Signal Characteristics

Input Signal Characteristics						
Input Type	**Description**	**VIL (V max)**	**VIH (V min)**	**Hysteresis (V min)**	**Pullup Resistance kOhm**	
C	CMOS Input	0.3*VDD	0.7*VDD	--	--	
H	Hysteresis	0.3*VDD	0.6*VDD	1.0	--	
HU	Hysteresis/Pullup	0.3*VDD	0.6*VDD	1.0	35–150	
T	TTL Input	0.8	2.0	--	--	
TU	TTL/Pullup	0.8	2.0	--	35-150	
OSC	CMOS Input	0.3*VDD	0.7*VDD	--	--	
Absolute Input Range = 0.5 to VDD+0.5						
Input Type	**Description**	**Operating (V min)**	**Operating (V max)**	**Abs. Max. (V min)**	**Abs. Max. (V max)**	
TA	Thermal Head Analog Input	0.2*VDD	0.8*VDD	–0.5	VDD+0.5	
VA	Video Analog In	-VR	+VR	-0.5	VADV + 0.5	
+VR	Video A/D +Vref	0.8	3.3	-0.5	VADV + 0.5	
-VR	Video A/D -Vref	-0.2	2.0	-0.5	VADV + 0.5	
VADV	Video A/D Power	VDD-0.1	VDD + 0.1	-0.5	7.0	
VADG	Video A/D GND	-0.1	0.1	-0.5	0.5	
VDD	Digital Power	4.5	5.25	–0.5	7.0	
GND	Digital Ground	0	0	0	0	
VBAT	Battery Power	2.25	5.25	–0.5	7.0	
Output Signal Characteristics						
Output Type	**Description**	**VOL (V max)**	**IOL (mA max)**	**VOH (V min)**	**IOH (mA max)**	**CL (pF max)**
1XC	CMOS Output (1X)	0.4	1.6	VDD–1.5	1.6	50
1XP, 2XP	High Capacitance Driver	0.4	1.6	VDD–1.5	1.6	200
2XC	CMOS Output (2X)	0.4	3.5	VDD–1.5	3.5	50
2XT	TTL Output (2X)	0.4	4	2.4	4	50
2XS	CMOS Output (2X)	0.4	3.5	VDD–1.5 1.5	3.5 15	50 50
2XL	LED Driver	0.7	10	VDD–1.5	3.5	100
2XO	CMOS Output, Open Drain	0.4	3.5	N/A	N/A	50
3XC	CMOS Output (3X)	0.4	6	VDD–1.5	6	50
3XP	High Capacitance Driver (3X)	0.4	6	VDD–1.5	6	700
3XT	TTL Output (3X)	0.4	6	2.4	6	50
4XC	CMOS Output (4X)	0.4	12	VDD–1.0	12	50
2XTT	2X Tristate TTL Output	0.4	4	2.4	4	50
3XTT	3X Tristate TTL Output	0.4	6	2.4	6	50



Note 1.	For R96DFXL, connect pin 62 to +5VD1 or leave open (nc); For R144EFXL, connect pin 62 to +5VD1.

Figure 3. R96DFXL, R144EFXL Facsimile Modem Pin Assignments.

Table 6. R96DFXL and R144EFXL Modem Pin Assignments

Pin No.	Signal Name	I/O Type	Pin No.	Signal Name	I/O Type
1	GP03	IA/OB	51	NC	
2	GP04	IA/OB	52	IRQn, IRQ1n	OC (Note 4)
3	GP05	IA/OB	53	WRITEn, R/Wn	IA
4	GP06	IA/OB	54	CSn	IA
5	GP07	IA/OB	55	READn-ϕ2	IA
6	0VD2	GND	56	RS4	IA
7	0VD2	GND	57	RS3	IA
8	D7	IA/OB	58	RS2	IA
9	D6	IA/OB	59	RS1	IA
10	D5	IA/OB	60	RS0	IA
11	D4	IA/OB	61	GP13	IA/OB
12	D3	IA/OB	62	NC (+5VD1)	(Note 4)
13	D2	IA/OB	63	GP11	IA/OB
14	D1	IA/OB	64	RTSn	IA
15	D0	IA/OB	65	EN85n	R
16	0VD2	GND	66	0VD2	GND
17	0VA	GND	67	PORIn	ID
18	RAMPIN	R	68	XTLI	R
19	NC		69	XTLO	R
20	NC		70	XCLK	OD
21	0VA	GND	71	YCLK	OD
22	+5VD2	PWR	72	+5VD1	PWR
23	0VD1	GND	73	DCLKI /IRQ2n/DCLK1	R
24	SWGAINI	R	74	SYNCIN2 (G2xCLK)	R (Note 4)
25	ECLKIN1	R	75	GP16	IA/OB
26	SYNCIN1	R	76	GP17	IA/OB
27	NC		77	0VD2	GND
28	NC		78	CTSn	OA
29	NC		79	TXD	IA
30	0VA	GND	80	0VD2	GND
31	NC		81	0VD2	GND
32	NC		82	DCLK	OA
33	NC		83	EYESYNC	OA
34	DAIN	R	84	EYECLKX	OA
35	ADOUT	R	85	EYECLK	OA
36	BYPASS	IC	86	EYEX	OA
37	RCVI	R	87	ADIN	R
38	TXLOSS3	IC	88	DAOUT	R
39	TXLOSS2	IC	89	0VD2	GND
40	TXLOSS1	IC	90	EYEY	OA
41	NC		91	GP21	IA/OB
42	NC		92	0VD2	GND
43	0VA	GND	93	GP20	IA/OB
44	TXOUT	AA	94	GP19	IA/OB
45	RXIN	AB	95	RXD	OA
46	+5VA	PWR	96	RLSDn	OA
47	0VA	GND	97	0VD2	GND
48	AGD	R	98	RCVO	R
49	AOUT	R	99	SWGAINO	R
50	0VD1	GND	100	GP02	IA/OB

Notes:
1. NC = No connection; leave pin open.
2. I/O Type (See Tables 8, 9.)
3. R = Required modem interconnection; no connection to host equipment.
4. The name in parentheses applies to the R144EFXL only.

Table 7. R96DFXL and R144EFXL Hardware Interface Signals

Name	Type[1]	Description
Overhead Signals		
XTLI	R	Connect to Crystal/Oscillator
XTLO	R	Connect to Crystal/Oscillator
PORIn	ID	Power-On-Reset Input
+5VD1	PWR	Connect to +5V power.
+5VD2	PWR	Connect to +5V power.
+5VA	PWR	Connect to Analog +5V Power
0VD1	GND	Connect to digital ground.
0VD2	GND	Connect to digital ground.
0VA	GND	Connect to Analog 0V Gnd
AGD	R	+2.5 V Analog Ground
Microprocessor Bus Interface		
D[7:0]	IA/OB	Data Bus lines 7-0.
RS[4:0]	IA	Register Select lines 4-0.
CSn	IA	Chip Select
READn--ϕ2	IA	Read Enable (808X), ϕ2 Clock (65XX)
WRITEn -R/Wn	IA	Write Enable (808X), R/Wn (65XX)
IRQn, IRQ1n, IRQ2n	OC	Interrupt Request
V.24 Serial Interface		
TXD	IA	Transmit Data
RXD	OA	Received Data
RTSn	IA	Request to Send
CTSn	OA	Clear to Send
RLSDn	OA	Received Line Sig. Detect
DCLK	OA	Transmit, Receive Data Clock
G2XCLK	IA	Group 2 External Transmit and Receive Data Clock
Analog Signals		
TXOUT	AA	Connect to Smoothing Filter Input
RXIN	AB	Connect to Anti-aliasing Filter Output
Auxiliary Signals		
BYPASS	IC	Receiver Highpass Filter Bypass Enable
TXLOSS1	IC	2 dB of Analog Transmit Level Attenuation
TXLOSS2	IC	4 dB of Analog Transmit Level Attenuation
TXLOSS3	IC	8 dB of Analog Transmit Level Attenuation
XCLK	OD	12 MHz/19 MHz Output
YCLK	OD	6 MHz/9.5 MHz Output
EN85n	IA	Enable 8085 Bus
GPx	IA/OB	General Purpose I/O
Eye Diagnostic Interface		
EYEX	OA	Serial Eye Pattern X Output
EYEY	OA	Serial Eye Pattern Y Output
EYECLK	OA	Serial Eye Pattern Clock (576 kHz)
EYESYNC	OA	Serial Eye Pattern Strobe (9600 Hz)
Modem Interconnect		
DCLKI	R	Connect to DCLK
ECLKIN1	R	Connect to EYECLK
SYNCIN1	R	Connect to EYESYNC
SYNCIN2	R	Connect to EYESYNC
RCVI	R	Connect to RCVO
RCVO	R	Mode Select Output
ADIN	R	Connect to ADOUT
ADOUT	R	ADC Output
DAIN	R	Connect to DAOUT
DAOUT	R	DAC/AGC Output
SWGAINI	R	Connect to SWGAINO
SWGAINO	R	Connect to SWGAINI
RAMPIN	R	Receiver Amplifier Input
AOUT	R	Smoothing Filter Output

Notes: 1. Digital signals are described in Table 8. Analog signals are described in Table 9.
2. R = Required overhead connection; no connection to host equipment.

Table 8. R96DFXL and R144EFXL Digital Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input High Voltage	V_{IH}				VDC	
Type IA and IB		2.0	–	V_{CC}		
Type IC and ID		0.8 V_{CC}	–	V_{CC}		
Input High Current	II_H				µA	VCC = 5.25 V, V_{IN}= 5.25 V
Type IB		–	–	40		
Type IC		–	–	2.5		
Input Low Voltage	V_{IL}				VDC	
Type IA, IB, ID		–0.3	–	0.8		
Type IC		–0.3	–	0.2 (V_{CC})		
Input Low Current	I_{IL}				µA	V_{CC} = 5.25 V
Type IB and IC		–	–	–400		
Input Leakage Current	I_{IN}	–	–	±2.5	µADC	V_{IN} = 0 to +5V, VCC =5.25V
Types IA and ID						
Output High Voltage	V_{OH}		–	–	VDC	
Type OA and OB		3.5	–	V_{CC}		I_{LOAD} = – 100 µA
Type OD		2.4				I_{LOAD} = – 40 µA
Output Low Voltage	V_{OL}				VDC	
Type OA and OC		–	–	0.4		I_{LOAD} = 1.6 mA
Type OB		–	–	0.4		I_{LOAD} = 0.8 mA
Type OD		–	–	0.4		I_{LOAD} = 0.4 mA
Output Leakage Current	I_{LO}			±10	µADC	V_{IN} = 0.4 to VCC-1
Types OA and OB						
Capacitive Load	C_L				pF	
Types IA and ID			–	5		
Type IB			–	20		
Capacitive Drive	C_D				pF	
Types OA, OB, OC			–	100		
Type OD				50		
Circuit Type						
Type IA						TTL
Type IB						TTL with pull-up
Type IC						CMOS with pull-up
Type ID						POR
Types OA and OB						TTL with 3-state
Type OC						Open drain
Type OD						Clock driver

Table 9. R96DFXL and R144EFXL Analog Electrical Characteristics

Name	Type	Characteristic	Value
RXIN	AB	Input Impedance	Greater than 1MΩ
		Maximum AC Input Voltage	2.0 V_{p-p}
		Reference Voltage	+2.5 VDC
TXOUT	AB	Output	TXOUT can supply a maximum of 2.5 ± 1.015 volts into a minimum of 10k ohms. A 600 • line impedance can be matched using an external smoothing filter with a 604 • series resistor in its output.

SOFTWARE INTERFACE

MEMORY MAP AND CHIP SELECT

Memory Map

Although the MC24 processor can directly access 16M bytes, the XFCR-B can access only 2M bytes of this memory by means of the 20-bit external address bus (A0-A19), and the chip selects. Figure 4 shows the XFER-B FAXENGINE memory map.

External Memory Space

The external memory space (up to 2048k bytes) consists of ROM, VRAM (support includes programmable refresh rates and duration), SRAM, modem and variable use spaces with assigned chip selects. Most external chip selects have programmable wait states, and read and write strobe timing. The SRAM chip select has programmable size, and can be battery backed up.

External memory spaces are summarized in the table opposite. Note that ROMCSn and CS0n occupy the same (20 bit) physical address range, but are selected by different (24 bit) logical addresses via the appropriate chip selects.

Item (see notes below)	CPU (Logical) Address Range	External (Physical) Address Range
ROMCSn	F00000 - FFFFFF	00000 - FFFFF
CS0n, SRAM or general (Note 3)	000000 - 0FFFFF	00000 - FFFFF
MCSn, Modem	00FF00 - 00FFFF	0FF00 - 0FFFF
CS1	00FC00 - 00FCFF	0FC00 - 0FCFF
CS2n - CS4n, optional, general	00FD00 - 00FDFF	0FD00 - 0FDFF

ROMCSn is a read/write, fixed location and size, chip select. CS0n is intended primarily for external SRAM, but may be used for other purposes, and can be programmed to one of four sizes (from 8k bytes to 1M byte). MCS is the modem chip select, and CS1n selects a variable use 256 byte memory space. Optional chip selects CS2n through CS4n are multiplexed with GPIO12-GPIO14. CS3n is generated only on write accesses; CS4n is generated only on read accesses.

Portions of the CS0n memory space are displaced by other chip selects (e.g., internal memory, modem, and CS1n - CS4n).

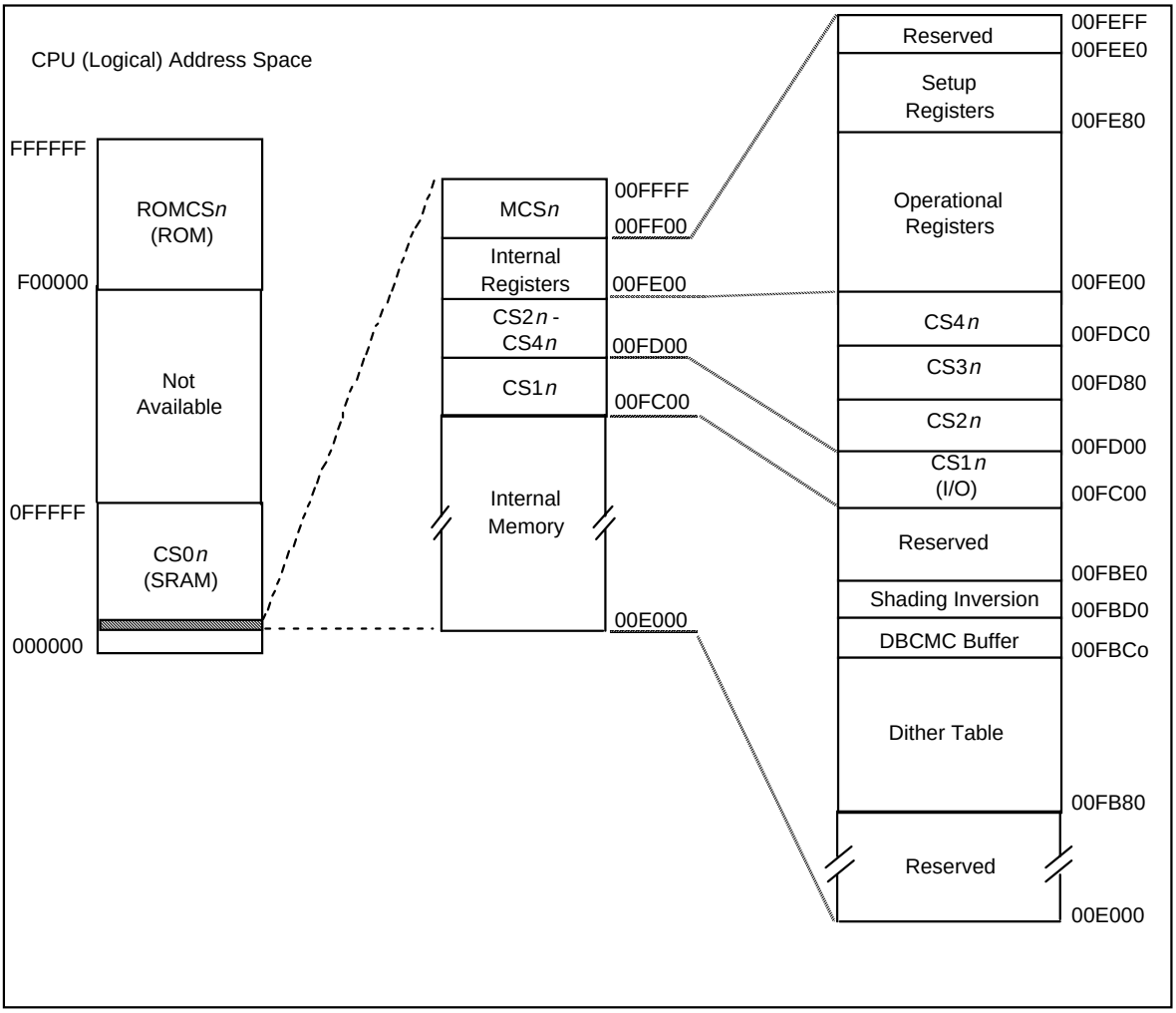


Figure 4. XFER-B Memory Map

Internal Memory Space

The XFCR-B internal memory occupies ~7k bytes of the address range from 00E000 - 00FEFF and displaces this portion of the CS0n chip select if CS0n is programmed to extend into this area. Internal memory space includes the following:

Internal registers	00FE00	- 00FEFF
Operational Registers	00FE00	- 00FE7F
Setup Registers	00FE80	- 00FEDF
Reserved register space	00FEE0	- 00FEFF
Internal RAM space	00E000	- 00FBFF
Reserved area	00E000	- 00FB7F
Dither Table	00FB80	- 00FBBF
DBCMC Buffer	00FBC0	- 00FBCF
Shading Inversion Table	00FBD0	- 00FBDF
Reserved area	00FBE0	- 00FBFF

Operational registers are those that are modified during normal operation, but which do not require firmware initialization after reset. Setup registers are those that are generally written only once for system initialization after reset.

The internal RAM space is used by the internal image processing logic for Dynamic background, contrast, and MTF correction (DBCC buffer), shading correction, and dithering.

The CPU (logical) address space from 100000 - EFFFFF is not available.

SUPPLIED FIRMWARE

FAXENGINE firmware supplied with the XFER-B consists of Core Code and Application Code. The Application Code, in conjunction with Core Code and XFER-B when connected to scanner and printer peripherals, provides a complete working facsimile machine.

The Core Code (subdivided as Macro and Primitive functions) is supplied as object code, whereas the Application Code (to complete a fax machine) is supplied as assembly-level source code.

Core Code

The Core Code includes proprietary primitives and macros in object code form located in ROM at the top of the FAXENGINE processor address space (see Figure 3). These Core Code primitives and macros provide the following functions:

- Low level subroutines for accessing various modem functions (R96DFXL, R144EFXL)
- T.30 framing and control
- T.4 MH compression and decompression. Line times of 5 ms per line are supported.
- Send and receive a page
- Real-time multitasking executive for scheduling high priority (interrupt-driven) tasks and servicing low priority (background) tasks

The Core Code subroutines are organized with a modular layered structure which allows for the replacement of any of these subroutines by original equipment manufacturer-written custom subroutines.

Core Code routines are organized in a library and the Core Code linkage routine optimizes ROM space code by preventing code duplication when Core Code routines are unused or replaced by Developer routines.

Application Code

The Application Code provides the Developer with the source assembly code for a complete facsimile machine application. The Application Code links to the Core Code functions to control the FAXENGINE peripheral functions. The Application Code performs all the functions that can be customized to give enough flexibility to the Developer, such as:

- Scanner and printer control
- Operator panel control (Keypad, LED, LCD, Beeper)
- Scan document handling (e.g., pull-in and eject)
- Printer paper handling (e.g., eject and cut)
- Copy page
- Setup controls for the facsimile machine (e.g., date and time, header, transmit level, etc.)
- Call progress controls with parameter tables to allow modification for PTT requirements in different countries
- T.30 control by generating frame content and sequence used during a T.30 negotiation
- Fax/Voice discrimination with external answering machine interface

Other functions which are supported, but which are included in the final object code only when the appropriate conditional assembly switches are enabled.

- Error Correction Mode (ECM) with the appropriate amount of block buffer
- Page Memory support that includes broadcast / delayed capabilities and receiving to memory
- B4/A4 reduction

OPERATOR PANEL AND USER INTERFACE

The FEES-X operator panel consists of a control keypad, a 20 key dialing keypad, a 20-column by 2-line liquid crystal display, five indicator LEDs, a beeper, and a speaker.

INITIALIZATION

When the FEES-X power is applied, or the RESET switch is pressed, all the LEDs turn on for 3 seconds, the beeper sounds, and a sign-on message is displayed on the LCD. When initialization is complete, the FEES-X will enter idle mode and display the clock on the second line of the LCD.

PROGRAM OPERATION

Several operational parameters can be set by the user. These parameters are separated into the Fax Menu, Phone Menu, System Menu, and Service Menu.

FAX Menu

The Fax menu includes the following items:

Enabling Receive-By-Polling

Programming a Delayed Broadcast

Programming Delayed Receive-By-Polling

Storing a Transmit-By-Polling Document

Printing And Deleting Documents From Page Memory

Setting the Local ID

Setting the Text Header

Setting the Fax/Voice Silence Time

Setting the Fax/Voice Timeout

Phone Menu

The Phone menu includes:

Setting Speed Dial Numbers

Setting the Number of Rings to Answer On

Setting the Dial Mode

Enabling Blind Dialing

System Menu

The System menu includes:

Setting the Clock

Setting the Speaker Control

Setting the Darkness Level

Printing User Settings

Resetting To Factory Defaults

Service Menu

The Service Menu includes:

Setting FAX Options

The fax options parameter specifies several options in the T.30 and modem operation. These options are bit-mapped, and may be set or reset independently. Included options:

- Ignore page memory capabilities when receiving
- Ignore ECM capabilities
- Transmit echo protector disable tone in V.29 mode
- Ignore echo of FCF frames
- International mode (1100 Hz CED, 2 retries of transmitter commands)

Setting The Starting Speed

Setting the Transmitter Attenuation

Setting the Fax Equalizer

Reference Voltage Test

FAX OPERATION

The Operation menu includes the following items:

Setting Auto-Answer

Setting Image Resolution and Halftone

Copying a Document

Transmitting a Document Using Manual Dialing

Transmitting a Document Using Automatic Dialing

Transmitting a Document by Polling

Receiving a Document Manually

Receiving a Document Automatically

Receiving a Document to Page Memory

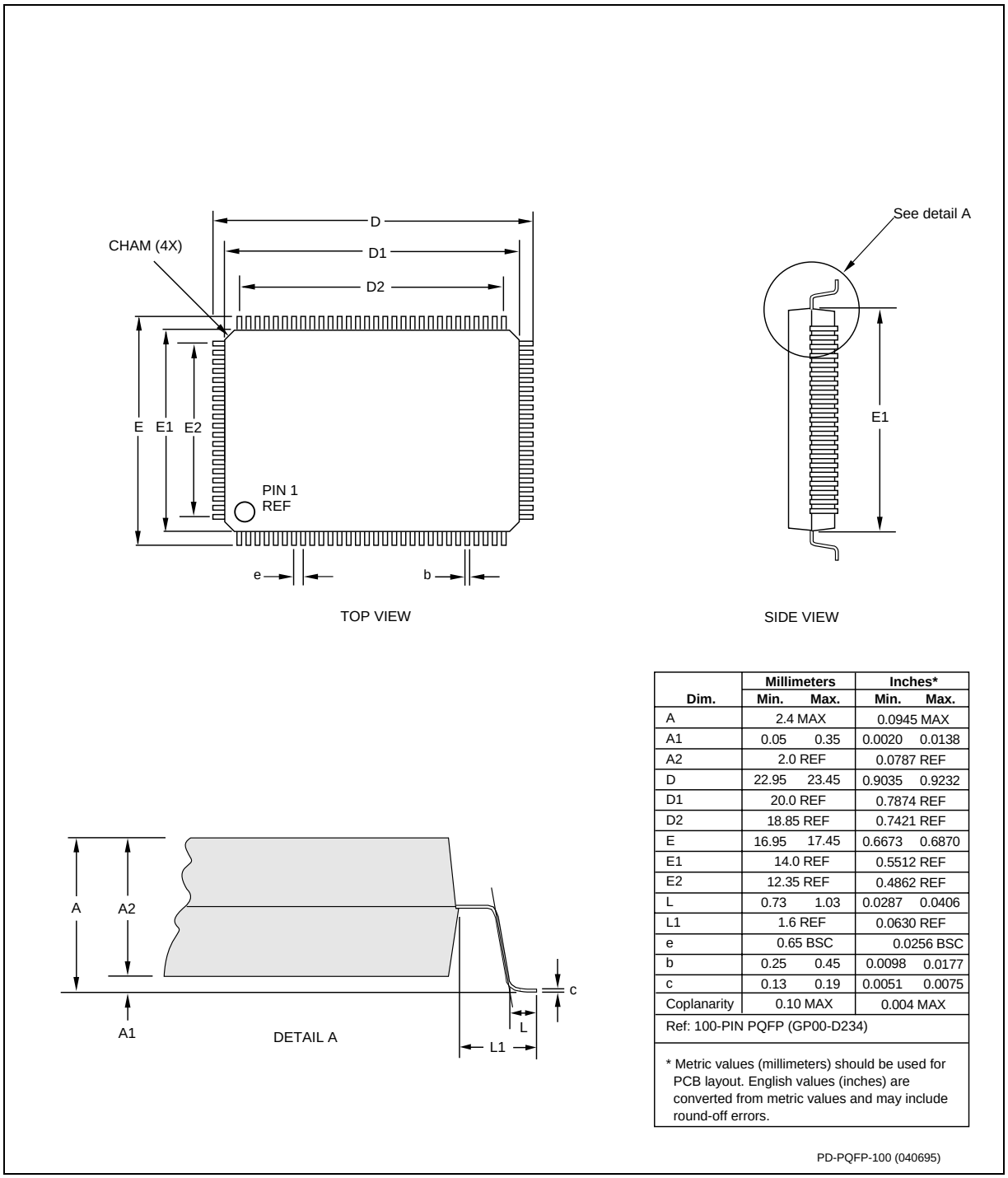
Receiving by Polling

Initiating a Voice Request

Responding to a Voice Request

PACKAGE DIMENSIONS

Figures 5 and 6 are package outline drawings for the 100-pin and 144-pin packages, respectively.



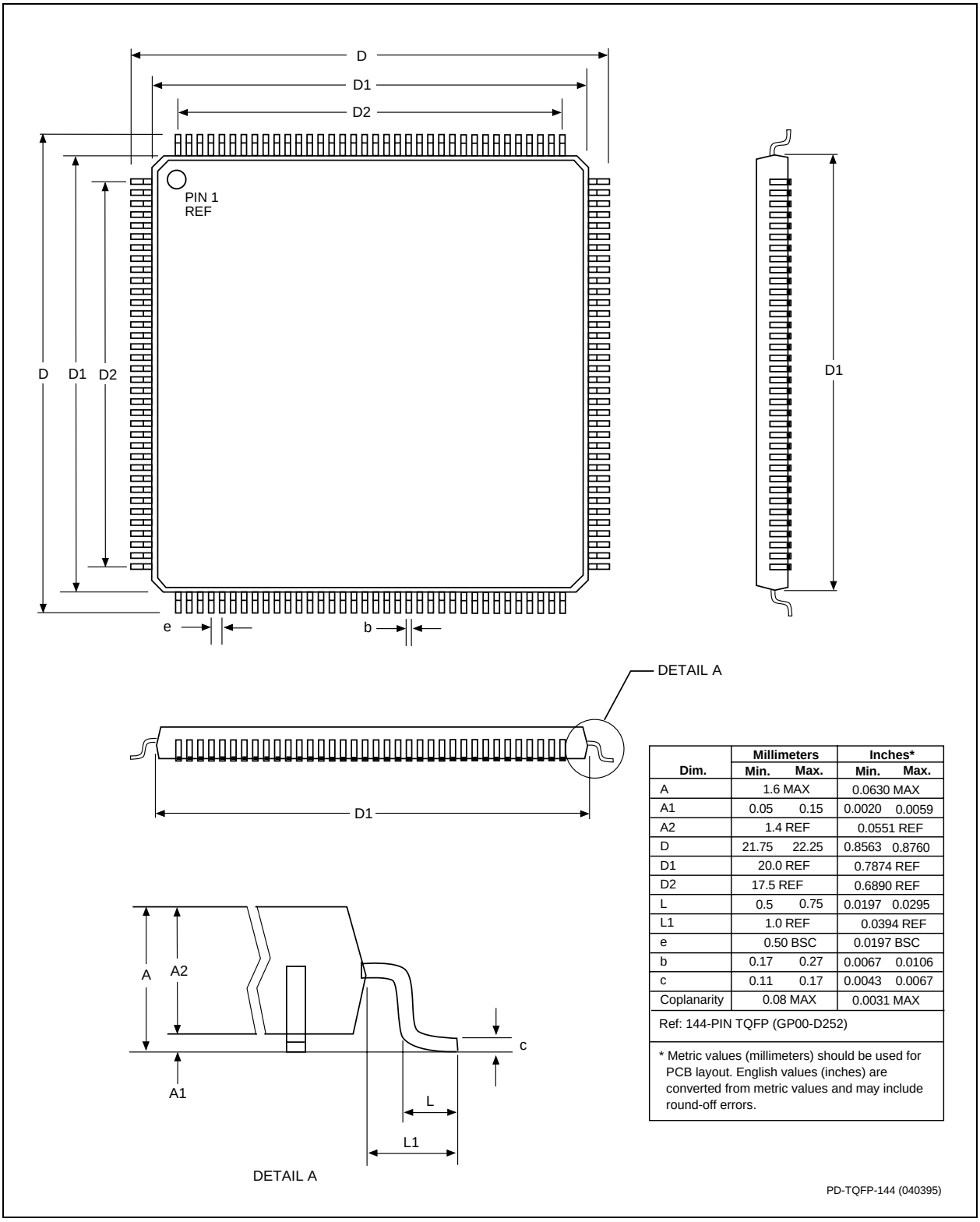
Dim.	Millimeters Min.	Millimeters Max.	Inches* Min.	Inches* Max.
A		2.4 MAX		0.0945 MAX
A1	0.05	0.35	0.0020	0.0138
A2		2.0 REF		0.0787 REF
D	22.95	23.45	0.9035	0.9232
D1		20.0 REF		0.7874 REF
D2		18.85 REF		0.7421 REF
E	16.95	17.45	0.6673	0.6870
E1		14.0 REF		0.5512 REF
E2		12.35 REF		0.4862 REF
L	0.73	1.03	0.0287	0.0406
L1		1.6 REF		0.0630 REF
e		0.65 BSC		0.0256 BSC
b	0.25	0.45	0.0098	0.0177
c	0.13	0.19	0.0051	0.0075
Coplanarity		0.10 MAX		0.004 MAX

Ref: 100-PIN PQFP (GP00-D234)

* Metric values (millimeters) should be used for PCB layout. English values (inches) are converted from metric values and may include round-off errors.

PD-PQFP-100 (040695)

Figure 5. 100-Pin PQFP Dimensions



Dim.	Millimeters Min.	Millimeters Max.	Inches* Min.	Inches* Max.
A	1.6 MAX		0.0630 MAX	
A1	0.05	0.15	0.0020	0.0059
A2	1.4 REF		0.0551 REF	
D	21.75	22.25	0.8563	0.8760
D1	20.0 REF		0.7874 REF	
D2	17.5 REF		0.6890 REF	
L	0.5	0.75	0.0197	0.0295
L1	1.0 REF		0.0394 REF	
e	0.50 BSC		0.0197 BSC	
b	0.17	0.27	0.0067	0.0106
c	0.11	0.17	0.0043	0.0067
Coplanarity	0.08 MAX		0.0031 MAX	

Ref: 144-PIN TQFP (GP00-D252)

* Metric values (millimeters) should be used for PCB layout. English values (inches) are converted from metric values and may include round-off errors.

Figure 6. 144-Pin PQFP Dimensions

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