GENERAL DESCRIPTION

The XRT72L13 is a fully integrated, low power, Multiplexer/Framer IC which performs Multiplexing/Demutiplexing of 28 DS1or 21 E1 signals into/from a DS3 signal with either M13 or C-bit parity frame format, performs Clear Channel DS3 Framing, and supports High speed HDLC/LAPD data linking.

The XRT72L13 also contains M12 and M23 bit-interleaving multiplexing/demultiplexing functions with necessary stuffing and destuffing control. Seven internal DS2/G.747 framers are included to support Mux/Demux purposes.

The XRT72L13 contains an integral DS3 Framer which provides Clear Channel DS3 Framing and Error Accumulation in accordance with ANSI/ITU-T specifications.

The XRT72L13 provides the intelligent functions of DS3/DS2 mode control, signaling control, error and alarm reporting and handles the HDLC/LAPD data link through internal registers accessible via an 8-bit parallel, memory mapped, µProcessor interface.

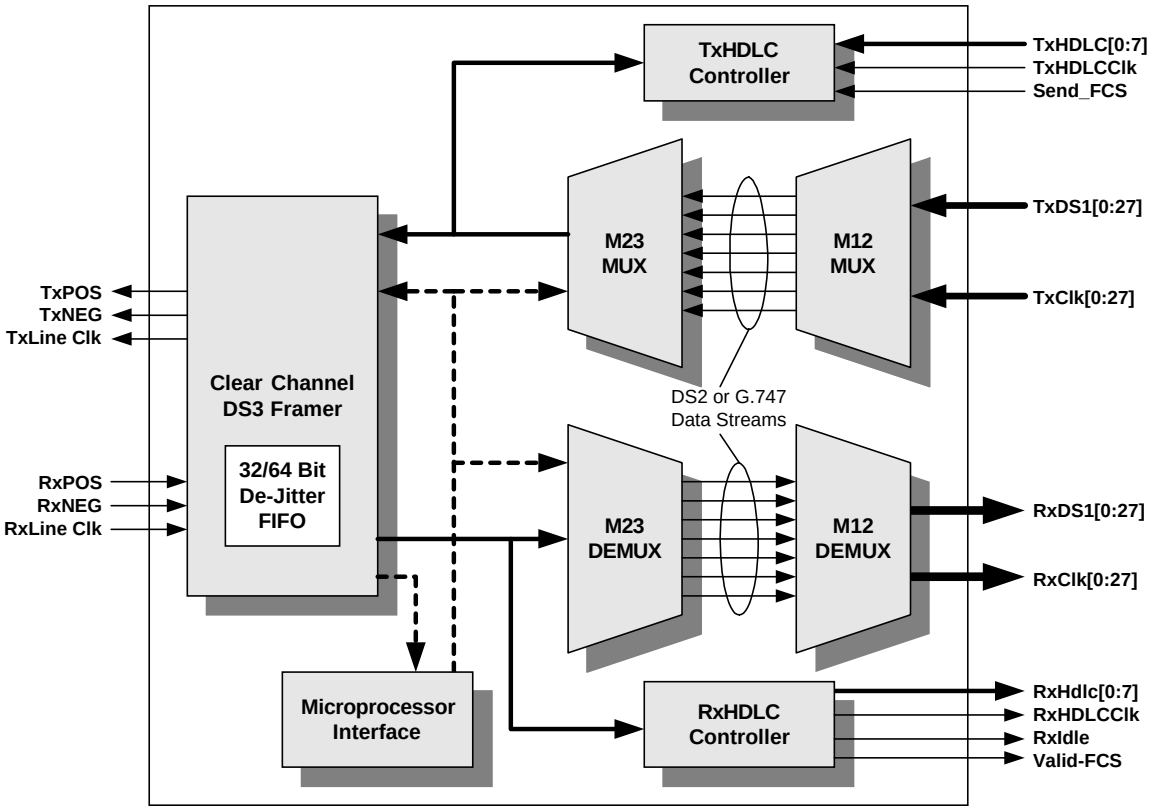
FEATURES

- A fully integrated device that supports:
  - Multiplexing/Demultiplexing Mode
  - Clear Channel DS3 Framer Mode
  - High Speed HDLC Controller Mode
- Supports Multiple Loop-back modes
- Smooths gapped clock signals
- Supports Intel or Motorola PIO µP interfaces
- Available in a 208 pin PQFP package
- Single 3.3V Power Supply
- 5V Tolerant I/O
- Operates over the Industrial Temperature Range

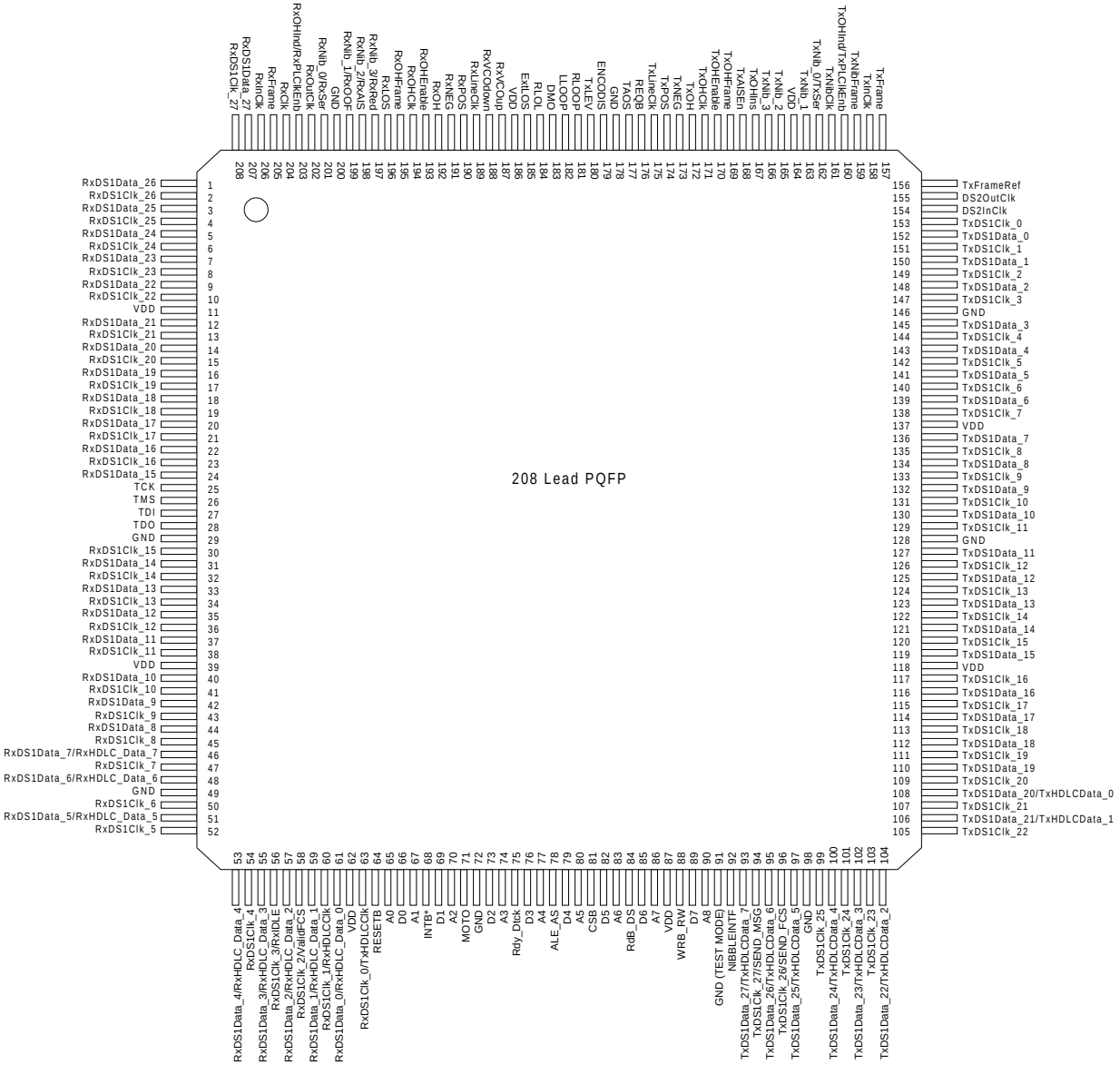
APPLICATIONS

- M13 Multiplexer/Demuliplexer Applications.
- Frame Relay Systems
- Digital Access and Cross Connect Systems
- Local Digital Switch
- Add/Drop Multiplexers
- DS3 Data/Channel Service Units.
- Test Equipment

FIGURE 1. BLOCK DIAGRAM OF THE XRT72L13 MULTIPLEXER/FRAMER



PIN OUT OF THE 72L13 FRAMER IC



ORDERING INFORMATION

PART #	PACKAGE	OPERATING TEMPERATURE
XRT72L13IQ	208 pin PQFP	-40°C to +85°C

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PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
1	RxDS1Data_26	O	**Receive DS1/E1 Data Output - Channel 26:** This pin outputs either a DS1 or E1 signal from the M12 multiplexer. Each bit, within the DS1 or E1 data stream is output upon the rising edge of RxDS1Clk_26.
2	RxDS1Clk_26	O	**Receive DS1/E1 Clock Output - Channel 26:** This pin outputs either a DS1 (1.544MHz) or an E1 (2.048MHz) clock signal to the Terminal Equipment. The XRT72L13 will update the data on the "RxDS1Data_26" line, upon the rising edge of this signal.
3	RxDS1Data_25	O	**Receive DS1/E1 Data Output - Channel 25:** This pin outputs either a DS1 or E1 signal from the M12 multiplexer. Each bit, within the DS1 or E1 data stream is output upon the rising edge of RxDS1Clk_25.
4	RxDS1Clk_25	O	**Receive DS1/E1 Clock Output - Channel 25:** This pin outputs either a DS1 (1.544MHz) or an E1 (2.048MHz) clock signal to the Terminal Equipment. The XRT72L13 will update the data on the "RxDS1Data_25" line, upon the rising edge of this signal.
5	RxDS1Data_24	O	**Receive DS1/E1 Data Output - Channel 24:** This pin outputs either a DS1 or E1 signal from the M12 multiplexer. Each bit, within the DS1 or E1 data stream is output upon the rising edge of RxDS1Clk_24.
6	RxDS1Clk_24	O	**Receive DS1/E1 Clock Output - Channel 24:** This pin outputs either a DS1 (1.544MHz) or an E1 (2.048MHz) clock signal to the Terminal Equipment. The XRT72L13 will update the data on the "RxDS1Data_24" line, upon the rising edge of this signal.
7	RxDS1Data_23	O	**Receive DS1 Data Output - Channel 23:** This pin outputs a DS1 signal from the M12 multiplexer. Each bit, within the DS1 data stream is output upon the rising edge of RxDS1Clk_23. ***NOTES:*** 1. *This output pin is inactive if the corresponding M12 DEMUX is de-multiplexing an ITU-T G.747 data stream.* 2. *This pin will output the contents of DS2 channel # 6, if M12 MUX # 6 is bypassed.*
8	RxDS1Clk_23	O	**Receive DS1/E1 Clock Output - Channel 23:** This pin outputs a DS1 (1.544MHz) clock signal to the Terminal Equipment. The XRT72L13 will update the data on the "RxDS1Data_23" line, upon the rising edge of this signal. ***NOTES:*** 1. *This output pin is inactive if the corresponding M12 DEMUX is de-multiplexing an ITU-T G.747 data stream.* 2. *This pin will output a DS2 rate clock signal (6.312MHz) if M12 # 6 is bypassed.*
9	RxDS1Data_22	O	**Receive DS1/E1 Data Output - Channel 22:** This pin outputs either a DS1 or E1 signal from the M12 multiplexer. Each bit, within the DS1 or E1 data stream is output upon the rising edge of RxDS1Clk_22.

PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
10	RxDS1Clk_22	O	**Receive DS1/E1 Clock Output - Channel 22:** This pin outputs either a DS1 (1.544MHz) or an E1 (2.048MHz) clock signal to the Terminal Equipment. The XRT72L13 will update the data on the "RxDS1Data_22" line, upon the rising edge of this signal.
11	VDD	****	**Power Supply Pin**
12	RxDS1Data_21	O	**Receive DS1/E1 Data Output - Channel 21** This pin outputs either a DS1 or E1 signal from the M12 multiplexer. Each bit, within the DS1 or E1 data stream is output upon the rising edge of RxDS1Clk_21.
13	RxDS1Clk_21	O	**Receive DS1/E1 Clock Output - Channel 21:** This pin outputs either a DS1 (1.544MHz) or an E1 (2.048MHz) clock signal to the Terminal Equipment. The XRT72L13 will update the data on the "RxDS1Data_21" line, upon the rising edge of this signal.
14	RxDS1Data_20	O	**Receive DS1/E1 Data Output - Channel 20:** This pin outputs either a DS1 or E1 signal from the M12 multiplexer. Each bit, within the DS1 or E1 data stream is output upon the rising edge of RxDS1Clk_20.
15	RxDS1Clk_20	O	**Receive DS1/E1 Clock Output - Channel 20:** This pin outputs either a DS1 (1.544MHz) or an E1 (2.048MHz) clock signal to the Terminal Equipment. The XRT72L13 will update the data on the "RxDS1Data_20" line, upon the rising edge of this signal.
16	RxDS1Data_19	O	**Receive DS1 Data Output - Channel 19:** This pin outputs a DS1 signal from the M12 multiplexer. Each bit, within the DS1 data stream is output upon the rising edge of RxDS1Clk_19. ***NOTES:*** 1. *This output pin is inactive if the corresponding M12 DEMUX is de-multiplexing an ITU-T G.747 data stream.* 2. *This pin will output the contents of DS2 channel # 5, if M12 MUX # 5 is bypassed.*
17	RxDS1Clk_19	O	**Receive DS1 Clock Output - Channel 19:** This pin outputs a DS1 (1.544MHz) clock signal to the Terminal Equipment. The XRT72L13 will update the data on the "RxDS1Data_19" line, upon the rising edge of this signal. This output pin is inactive if the corresponding M12 DEMUX is de-multiplexing an ITU-T G.747 data stream. ***NOTES:*** 1. *This output pin is inactive if the corresponding M12 DEMUX is de-multiplexing an ITU-T G.747 data stream.* 2. *This pin will output a DS2 rate clock signal (6.312MHz) if M12 # 5 is bypassed.*
18	RxDS1Data_18	O	**Receive DS1/E1 Data Output - Channel 18** This pin outputs either a DS1 or E1 signal from the M12 multiplexer. Each bit, within the DS1 or E1 data stream is output upon the rising edge of RxDS1Clk_18.

PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
19	RxDS1Clk_18	O	**Receive DS1/E1 Clock Output - Channel 18:** This pin outputs either a DS1 (1.544MHz) or an E1 (2.048MHz) clock signal to the Terminal Equipment. The XRT72L13 will update the data on the "RxDS1Data_18" line, upon the rising edge of this signal.
20	RxDS1Data_17	O	**Receive DS1/E1 Data Output - Channel 17:** This pin outputs either a DS1 or E1 signal from the M12 multiplexer. Each bit, within the DS1 or E1 data stream is output upon the rising edge of RxDS1Clk_17.
21	RxDS1Clk_17	O	**Receive DS1/E1 Clock Output - Channel 17:** This pin outputs either a DS1 (1.544MHz) or an E1 (2.048MHz) clock signal to the Terminal Equipment. The XRT72L13 will update the data on the "RxDS1Data_17" line, upon the rising edge of this signal.
22	RxDS1Data_16	O	**Receive DS1/E1 Data Output - Channel 16:** This pin outputs either a DS1 or E1 signal from the M12 multiplexer. Each bit, within the DS1 or E1 data stream is output upon the rising edge of RxDS1Clk_16.
23	RxDS1Clk_16	O	**Receive DS1/E1 Clock Output - Channel 16:** This pin outputs either a DS1 (1.544MHz) or an E1 (2.048MHz) clock signal to the Terminal Equipment. The XRT72L13 will update the data on the "RxDS1Data_16" line, upon the rising edge of this signal.
24	RxDS1Data_15	O	**Receive DS1 Data Output - Channel 15:** This pin outputs a DS1 signal from the M12 multiplexer. Each bit, within the DS1 data stream is output upon the rising edge of RxDS1Clk_15. ***NOTES:*** 1. *This output pin is inactive if the corresponding M12 DEMUX is de-multiplexing an ITU-T G.747 data stream.* 2. *This pin will output the contents of DS2 channel # 4, if M12 MUX # 4 is bypassed.*
25	TCK		**Boundary Scan Pin**
26	TMS		**Boundary Scan Pin**
27	TDI		**Boundary Scan Pin**
28	TDO		**Boundary Scan Pin**
29	GND	****	**Ground Pin**
30	RxDS1Clk_15	O	**Receive DS1 Clock Output - Channel 15:** This pin outputs a DS1 (1.544MHz) clock signal to the Terminal Equipment. The XRT72L13 will update the data on the "RxDS1Data_15" line, upon the rising edge of this signal. ***NOTES:*** 1. *This output pin is inactive if the corresponding M12 DEMUX is de-multiplexing an ITU-T G.747 data stream.* 2. *This pin will output a DS2 rate clock signal (6.312MHz) if M12 # 4 is bypassed.*

PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
31	RxDS1Data_14	O	**Receive DS1/E1 Data Output - Channel 14:** This pin outputs either a DS1 or E1 signal from the M12 multiplexer. Each bit, within the DS1 or E1 data stream is output upon the rising edge of RxDS1Clk_14.
32	RxDS1Clk_14	O	**Receive DS1/E1 Clock Output - Channel 14:** This pin outputs either a DS1 (1.544MHz) or an E1 (2.048MHz) clock signal to the Terminal Equipment. The XRT72L13 will update the data on the "RxDS1Data_14" line, upon the rising edge of this signal.
33	RxDS1Data_13	O	**Receive DS1/E1 Data Output - Channel 13:** This pin outputs either a DS1 or E1 signal from the M12 multiplexer. Each bit, within the DS1 or E1 data stream is output upon the rising edge of RxDS1Clk_13.
34	RxDS1Clk_13	O	**Receive DS1/E1 Clock Output - Channel 13:** This pin outputs either a DS1 (1.544MHz) or an E1 (2.048MHz) clock signal to the Terminal Equipment. The XRT72L13 will update the data on the "RxDS1Data_13" line, upon the rising edge of this signal.
35	RxDS1Data_12	O	**Receive DS1/E1 Data Output - Channel 12:** This pin outputs either a DS1 or E1 signal from the M12 multiplexer. Each bit, within the DS1 or E1 data stream is output upon the rising edge of RxDS1Clk_12.
36	RxDS1Clk_12	O	**Receive DS1/E1 Clock Output - Channel 12:** This pin outputs either a DS1 (1.544MHz) or an E1 (2.048MHz) clock signal to the Terminal Equipment. The XRT72L13 will update the data on the "RxDS1Data_12" line, upon the rising edge of this signal.
37	RxDS1Data_11	O	**Receive DS1 Data Output - Channel 11:** This pin outputs a DS1 signal from the M12 multiplexer. Each bit, within the DS1 data stream is output upon the rising edge of RxDS1Clk_11. This output pin is inactive if the corresponding M12 DEMUX is de-multiplexing an ITU-T G.747 data stream. This pin will output the contents of DS2 channel # 3, if M12 MUX # 3 is bypassed.
38	RxDS1Clk_11	O	**Receive DS1 Clock Output - Channel 11:** This pin outputs a DS1 (1.544MHz) clock signal to the Terminal Equipment. The XRT72L13 will update the data on the "RxDS1Data_11" line, upon the rising edge of this signal. ***NOTES:*** 1. *This output pin is inactive if the corresponding M12 DEMUX is de-multiplexing an ITU-T G.747 data stream.* 2. *This pin will output a DS2 rate clock signal (6.312MHz) if M12 # 3 is bypassed.*
39	VDD	****	**Power Supply Pin**
40	RxDS1Data_10	O	**Receive DS1/E1 Data Output - Channel 10:** This pin outputs either a DS1 or E1 signal from the M12 multiplexer. Each bit, within the DS1 or E1 data stream is output upon the rising edge of RxDS1Clk_10.

PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
41	RxDS1Clk_10	O	**Receive DS1/E1 Clock Output - Channel 10:** This pin outputs either a DS1 (1.544MHz) or an E1 (2.048MHz) clock signal to the Terminal Equipment. The XRT72L13 will update the data on the "RxDS1Data_10" line, upon the rising edge of this signal.
42	RxDS1Data_9	O	**Receive DS1/E1 Data Output - Channel 9:** This pin outputs either a DS1 or E1 signal from the M12 multiplexer. Each bit, within the DS1 or E1 data stream is output upon the rising edge of RxDS1Clk_9.
43	RxDS1Clk_9	O	**Receive DS1/E1 Clock Output - Channel 9:** This pin outputs either a DS1 (1.544MHz) or an E1 (2.048MHz) clock signal to the Terminal Equipment. The XRT72L13 will update the data on the "RxDS1Data_9" line, upon the rising edge of this signal.
44	RxDS1Data_8	O	**Receive DS1/E1 Data Output - Channel 8:** This pin outputs either a DS1 or E1 signal from the M12 multiplexer. Each bit, within the DS1 or E1 data stream is output upon the rising edge of RxDS1Clk_8.
45	RxDS1Clk_8	O	**Receive DS1/E1 Clock Output - Channel 8:** This pin outputs either a DS1 (1.544MHz) or an E1 (2.048MHz) clock signal to the Terminal Equipment. The XRT72L13 will update the data on the "RxDS1Data_8" line, upon the rising edge of this signal.
46	RxDS1Data_7 RxHDLC_Data_7	O	**Receive DS1 Data Output - Channel 7/Receive HDLC Controller Block Output - Bit 7:** The funtion of this output pin depends upon whether the XRT72L13 is operating in the "Multiplexer/De-Multiplexer" Mode or in the "High Speed HDLC Controller" Mode. **Receive DS1 Data Output - Channel 7: (Multiplexer/De-Multiplexer Mode):** This pin outputs a DS1 signal from the M12 multiplexer. Each bit, within the DS1 data stream is output upon the rising edge of RxDS1Clk_7. ***NOTES:*** 1. *This output pin is inactive if the corresponding M12 DEMUX is de-multiplexing an ITU-T G.747 data stream.* 2. *This pin will output the contents of DS2 channel # 2, if M12 MUX # 2 is bypassed.* **Receive HDLC Controller Block Output - Bit 7 (High Speed HDLC Controller Mode)** This output pin along with RxHDLC_Data[0:6] output the contents of all HDLC frames that have been received (via the DS3 payload) from the remote terminal equipment. The data on this output pin is updated upon the rising edge of "RxHDLCClk". ***NOTE:*** *This pin is inactive while the Receive HDLC Controller is receiving the "Flag Sequence" octet.*

PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
47	RxDS1Clk_7	O	**Receive DS1 Clock Output - Channel 7:** This pin outputs a DS1 (1.544MHz) clock signal to the Terminal Equipment. The XRT72L13 will update the data on the "RxDS1Data_7" line, upon the rising edge of this signal. ***NOTES:*** 1. *This output pin is inactive if the corresponding M12 DEMUX is de-multiplexing an ITU-T G.747 data stream.* 2. *This pin will output a DS2 rate clock signal (6.312MHz) if M12 # 2 is bypassed.*
48	RxDS1Data_6 RxHDLC_Data_6	O	**Receive DS1/E1 Data Output - Channel 6/Receive HDLC Controller Block Output - Bit 6:** The funtion of this output pin depends upon whether the XRT72L13 is operating in the "Multiplexer/De-Multiplexer" Mode or in the "High Speed HDLC Controller" Mode. **Receive DS1/E1 Data Output - Channel 6: (Multiplexer/De-Multiplexer Mode):** This pin outputs either a DS1 or E1 signal from the M12 multiplexer. Each bit, within the DS1 or E1 data stream is output upon the rising edge of RxDS1Clk_6. **Receive HDLC Controller Block Output - Bit 6: (High Speed HDLC Controller Mode)** This output pin along with RxHDLC_Data[0:5] and RxHDLC_Data_7 output the contents of all HDLC frames that have been received (via the DS3 payload) from the remote terminal equipment. The data on this output pin is updated upon the rising edge of "RxHDLCClk". ***NOTE:*** *This pin is inactive while the Receive HDLC Controller is receiving the "Flag Sequence" octet.*
49	GND	****	**Ground Pin**
50	RxDS1Clk_6	O	**Receive DS1/E1 Clock Output - Channel 6:** This pin outputs either a DS1 (1.544MHz) or an E1 (2.048MHz) clock signal to the Terminal Equipment. The XRT72L13 will update the data on the "RxDS1Data_6" line, upon the rising edge of this signal.

PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
51	RxDS1Data_5 RxHDLC_Data_5	O	**Receive DS1/E1 Data Output - Channel 5/Receive HDLC Controller Block Output - Bit 5:** The funtion of this output pin depends upon whether the XRT72L13 is operating in the "Multiplexer/De-Multiplexer" Mode or in the "High Speed HDLC Controller" Mode. **Receive DS1/E1 Data Output - Channel 5: (Multiplexer/De-Multiplexer Mode):** This pin outputs either a DS1 or E1 signal from the M12 multiplexer. Each bit, within the DS1 or E1 data stream is output upon the rising edge of RxDS1Clk_5. **Receive HDLC Controller Block Output - Bit 5: (High Speed HDLC Controller Mode)** This output pin along with RxHDLC_Data[0:4] and RxHDLC_Data[6:7] output the contents of all HDLC frames that have been received (via the DS3 payload) from the remote terminal equipment. The data on this output pin is updated upon the rising edge of "RxHDLCClk". ***NOTE:*** *This pin is inactive while the Receive HDLC Controller is receiving the "Flag Sequence" octet.*
52	RxDS1Clk_5	O	**Receive DS1/E1 Clock Output - Channel 5:** This pin outputs either a DS1 (1.544MHz) or an E1 (2.048MHz) clock signal to the Terminal Equipment. The XRT72L13 will update the data on the "RxDS1Data_5" line, upon the rising edge of this signal.
53	RxDS1Data_4/ RxHDLC_Data_4	O	**Receive DS1/E1 Data Output - Channel 4/Receive HDLC Controller Block Output - Bit 4:** The funtion of this output pin depends upon whether the XRT72L13 is operating in the "Multiplexer/De-Multiplexer" Mode or in the "High Speed HDLC Controller" Mode. **Receive DS1/E1 Data Output - Channel 4: (Multiplexer/De-Multiplexer Mode):** This pin outputs either a DS1 or E1 signal from the M12 multiplexer. Each bit, within the DS1 or E1 data stream is output upon the rising edge of RxDS1Clk_4. **Receive HDLC Controller Block Output - Bit 4: (High Speed HDLC Controller Mode)** This output pin along with RxHDLC_Data[0:3] and RxHDLC_Data[5:7] output the contents of all HDLC frames that have been received (via the DS3 payload) from the remote terminal equipment. The data on this output pin is updated upon the rising edge of "RxHDLCClk". ***NOTE:*** *This pin is inactive while the Receive HDLC Controller is receiving the "Flag Sequence" octet.*
54	RxDS1Clk_4	O	**Receive DS1/E1 Clock Output - Channel 4:** This pin outputs either a DS1 (1.544MHz) or an E1 (2.048MHz) clock signal to the Terminal Equipment. The XRT72L13 will update the data on the "RxDS1Data_4" line, upon the rising edge of this signal.

PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
55	RxDS1Data_3/ RxHDLC_Data_3	O	**Receive DS1 Data Output - Channel 3/Receive HDLC Controller Block Output - Bit 3** The funtion of this output pin depends upon whether the XRT72L13 is operating in the "Multiplexer/De-Multiplexer" Mode or in the "High Speed HDLC Controller" Mode. **Receive DS1 Data Output - Channe1 3 (Multiplexer/De-Multiplexer Mode)** This pin outputs a DS1 signal from the M12 de-multiplexer. Each bit, within the DS1 data stream is output upon the rising edge of RxDS1Clk_3. ***NOTES:*** 1. *This output pin is inactive if the corresponding M12 DEMUX is de-multiplexing an ITU-T G.747 data stream.* 2. *This pin will output the contents of DS2 channel # 1, if M12 MUX # 1 is bypassed.* **Receive HDLC Controller Block Output - Bit 3 (High Speed HDLC Controller Mode)** This output pin along with RxHDLC_Data[0:2] and RxHDLC_Data[4:7] output the contents of all HDLC frames that have been received (via the DS3 payload) from the remote terminal equipment. The data on this output pin is updated upon the rising edge of "RxHDLCClk". ***NOTE:*** *This pin is inactive while the Receive HDLC Controller is receiving the "Flag Sequence" octet.*
56	RxDS1Clk_3/ RxIDLE	O	**Receive DS1 Clock Output - Channel 3/Receive Idle (Flag Sequence) Indicator Output:** The funtion of this output pin depends upon whether the XRT72L13 is operating in the "Multiplexer/De-Multiplexer" Mode or in the "High Speed HDLC Controller" Mode. **Receive DS1 Clock Output - Channel 3 (Multiplexer/De-Multiplexer Mode):** This pin outputs a DS1 (1.544MHz) clock signal to the Terminal Equipment. The XRT72L13 will update the data on the "RxDS1Data_3" line, upon the rising edge of this signal. ***NOTES:*** 1. *This output pin is inactive if the corresponding M12 DEMUX is de-multiplexing an ITU-T G.747 data stream.* 2. *This pin will output a DS2 rate clock signal (6.312MHz) if M12 # 1 is bypassed.* **RxIDLE - Receive Idle (Flag Sequence) Indicator Output (High Speed HDLC Controller Mode):** The Receive HDLC Controller block will drive this output pin "high" any time it is receiving a continuous stream of the "Flag Sequence" octet (0x7E) via the DS3 payload.

PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
57	RxDS1Data_2/ RxHDLC_Data_2	O	**Receive DS1/E1 Data Output - Channel 2/Receive HDLC Controller Block Output - Bit 2** The funtion of this output pin depends upon whether the XRT72L13 is operating in the "Multiplexer/De-Multiplexer" Mode or in the "High Speed HDLC Controller" Mode. **Receive DS1 Data Output - Channel 2 (Multiplexer/De-Multiplexer Mode)** This pin outputs either a DS1 or E1 signal from the M12 multiplexer. Each bit, within the DS1 or E1 data stream is output upon the rising edge of RxDS1Clk_2. **Receive HDLC Controller Block Output - Bit 2 (High Speed HDLC Controller Mode)** This output pin along with RxHDLC_Data[0:1] and RxHDLC_Data[3:7] output the contents of all HDLC frames that have been received (via the DS3 payload) from the remote terminal equipment. The data on this output pin is updated upon the rising edge of "RxHDLCClk". ***NOTE:*** *This pin is inactive while the Receive HDLC Controller is receiving the "Flag Sequence" octet.*
58	RxDS1Clk_2/ ValidFCS	O	**Receive DS1/E1 Clock Output - Channel 2/Valid FCS Indicator Output :** The funtion of this output pin depends upon whether the XRT72L13 is operating in the "Multiplexer/De-Multiplexer" Mode or in the "High Speed HDLC Controller" Mode. **Receive DS1 Clock Output - Channel 2 (Multiplexer/De-Multiplexer Mode)** This pin outputs either a DS1 (1.544MHz) or an E1 (2.048MHz) clock signal to the Terminal Equipment. The XRT72L13 will update the data on the "RxDS1Data_2" line, upon the rising edge of this signal. **Valid FCS Indicator Output - (High Speed HDLC Controller Mode)** This output pin is driven "high" anytime the Receive HDLC Controller block has received an HDLC frame with a valid FCS value.
59	RxDS1Data_1/ RxHDLC_Data_1	O	**Receive DS1/E1 Data Output - Channel 1/Receive HDLC Controller Block Output - Bit 1:** The funtion of this output pin depends upon whether the XRT72L13 is operating in the "Multiplexer/De-Multiplexer" Mode or in the "High Speed HDLC Controller" Mode. **Receive DS1 Data Output - Channel 1: (Multiplxer/De-Multiplexer Mode):** This pin outputs either a DS1 or E1 signal from the M12 multiplexer. Each bit, within the DS1 or E1 data stream is output upon the rising edge of RxDS1Clk_1. **Receive HDLC Controller Block Output - Bit 1 (High Speed HDLC Controller Mode)** This output pin along with RxHDLC_Data_0 and RxHDLC_Data[2:7] output the contents of all HDLC frames that have been received (via the DS3 payload) from the remote terminal equipment. The data on this output pin is updated upon the rising edge of "RxHDLCClk". ***NOTE:*** *This pin is inactive while the Receive HDLC Controller is receiving the "Flag Sequence" octet.*

PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
60	RxDS1Clk_1/ RxHDLCClk	O	**Receive DS1/E1 Clock Output - Channel 0/Receive HDLC Controller Clock Output:** The funtion of this output pin depends upon whether the XRT72L13 is operating in the "Multiplexer/De-Multiplexer" Mode or in the "High Speed HDLC Controller" Mode. **Receive DS1/E1 Clock Output - Channel 1 (Multiplexer/De-Multiplexer Mode):** This pin outputs either a DS1 (1.544MHz) or an E1 (2.048MHz) clock signal to the Terminal Equipment. The XRT72L13 will update the data on the "RxDS1Data_0" line, upon the rising edge of this signal. **Receive HDLC Clock Output pin (High Speed HDLC Controller Mode)** The contents of the "received" HDLC frames are output via the RxHDLC_Data[7:0] bus, upon the rising edge of this input pin.
61	RxDS1Data_0/ RxHDLC_Data_0	O	**Receive DS1/E1 Data Output - Channel 0/Receive HDLC Controller Block Output - Bit 0:** The funtion of this output pin depends upon whether the XRT72L13 is operating in the "Multiplexer/De-Multiplexer" Mode or in the "High Speed HDLC Controller" Mode. **Receive DS1/E1 Data Output - Channel 0 (Multiplexer/De-Multiplexer Mode)** This pin outputs either a DS1 or E1 signal from the M12 multiplexer. Each bit, within the DS1 or E1 data stream is output upon the rising edge of RxDS1Clk_0. **Receive HDLC Controller Block Output - Bit 0: (High Speed HDLC Controller Mode)** This output pin along with RxHDLC_Data[1:7] output the contents of all HDLC frames that have been received (via the DS3 payload) from the remote terminal equipment. The data on this output pin is updated upon the rising edge of "RxHDLCClk". ***NOTE:*** *This pin is inactive while the Receive HDLC Controller is receiving the "Flag Sequence" octet.*
62	VDD	****	**Power Supply Pin**
63	RxDS1Clk_0/ TxHDLCClk	O	**Receive DS1/E1 Clock Output - Channel 0/Transmit HDLC Controller Clock Output:** The funtion of this output pin depends upon whether the XRT72L13 is operating in the "Multiplexer/De-Multiplexer" Mode or in the "High Speed HDLC Controller" Mode. **Receive DS1/E1 Clock Output - Channel 0 (Multiplexer/De-Multiplexer Mode):** This pin outputs either a DS1 (1.544MHz) or an E1 (2.048MHz) clock signal to the Terminal Equipment. The XRT72L13 will update the data on the "RxDS1Data_0" line, upon the rising edge of this signal. **Transmit HDLC Controller Clock Output (High Speed HDLC Controller Mode):** The data on the "TxHDLC_Data[7:0] bus, are latched into the "Transmit HDLC Controller" block upon the rising edge of this clock signal.
64	$\overline{\text{RESET}}$	I	**Reset Input:** When this "active-low" signal is asserted, the Framer will be asynchronously reset. Additionally, all outputs will be "tri-stated", and all on-chip registers will be reset to their default values.

PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
65	A0	I	**Address Bus Input (Microprocessor Interface) - LSB (Least Significant Bit)** (Please see description for A8)
66	D0	I/O	**Bi-directional Data Bus (Microprocessor Interface Section):** Please see description for D7
67	A1	I	**Address Bus Input (Microprocessor Interface) - LSB (Least Significant Bit)** (Please see description for A8)
68	$\overline{INT}$	O	**Interrupt Request Output:** This open-drain, active-low output signal will be asserted when the Framer is requesting interrupt service from the local microprocessor. This output pin should typically be connected to the "Interrupt Request" input of the local microprocessor.
69	D1	I/O	**Bi-directional Data Bus (Microprocessor Interface Section):** Please see description for D7
70	A2	I	Address Bus Input (Microprocessor Interface) - LSB (Least Significant Bit) (Please see description for A8)
71	MOTO	I	**Motorola/Intel Processor Interface Select Mode:** This input pin allows the user to configure the Microprocessor Interface to interface with either a "Motorola-type" or "Intel-type" microprocessor/microcontroller. Tying this input pin to VCC, configures the microprocessor interface to operate in the Motorola mode (e.g., the Framer can be readily interfaced to a "Motorola type" local microprocessor). Tying this input pin to GND configures the Microprocessor Interface to operate in the Intel Mode (e.g., the Framer can be readily interfaced to a Intel type" local microprocessor).
72	GND	****	**Ground Pin**
73	D2	I/O	**Bi-directional Data Bus (Microprocessor Interface Section):** Please see description for D7
74	A3	I	**Address Bus Input (Microprocessor Interface) - LSB (Least Significant Bit)** (Please see description for A8)

PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
75	Rdy_Dtck	O	**READY or DTACK:** This "active-low" output pin will function as the READY output, when the microprocessor interface is running in the "Intel" Mode; and will function as the DTACK output, when the microprocessor interface is running in the "Motorola" Mode. **"Intel" Mode - READY Output** When the Framer negates this output pin (e.g., toggles it "low"), it indicates (to the mP) that the current READ or WRITE cycle is to be extended until this signal is asserted (e.g., toggled "high"). **"Motorola" Mode: - DTACK (Data Transfer Acknowledge) Output** The Framer will assert this pin in order to inform the local microprocessor that the present READ or WRITE cycle is nearly complete. If the Framer requires that the current READ or WRITE cycle be extended, then the Framer will delay its assertion of this signal. The 68000 family of mPs requires this signal from its peripheral devices, in order to quickly and properly complete a READ or WRITE cycle.
76	D3	I/O	**Bi-directional Data Bus (Microprocessor Interface Section):** Please see description for D7
77	A4	I	**Address Bus Input (Microprocessor Interface) - LSB (Least Significant Bit)** (Please see description for A8)
78	ALE_AS	I	**Address Latch Enable/Address Strobe:** This input is used to latch the address (present at the Microprobessor Interface Address Bus, A[8:0]) into the Framer Microprocessor Interface circuitry and to indicate the start of a READ/WRITE cycle. This input is active-high in the Intel Mode (MOTO = "low") and active-low in the Motorola Mode (MOTO = "high").
79	D4	I/O	**Bi-directional Data Bus (Microprocessor Interface Section):** Please see description for D7
80	A5	I	**Address Bus Input (Microprocessor Interface) - LSB (Least Significant Bit):** (Please see description for A8)
81	$\overline{CS}$	I	**Chip Select Input:** This active-low input signal selects the Microprocessor Interface Section of the Framer and enables Read/Write operations between the "local" microprocessor and the Framer on-chip registers and RAM locations.
82	D5	I/O	**Bi-directional Data Bus (Microprocessor Interface Section):** Please see description for D7
83	A6	I	**Address Bus Input (Microprocessor Interface) - LSB (Least Significant Bit):** (Please see description for A8)

PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
84	$\overline{Rd}$_DS	I	**Read Data Strobe (Intel Mode):** If the microprocessor interface is operating in the Intel Mode, then this input will function as the RD* (READ STROBE) input signal from the local mP. Once this active-low signal is asserted, then the Framer will place the contents of the addressed registers (within the Framer) on the Microprocessor Data Bus (D[7:0]). When this signal is negated, the Data Bus will be tri-stated. **Data Strobe (Motorola Mode):** If the microprocessor interface is operating in the Motorola mode, then this pin will function as the active-low Data Strobe signal.
85	D6	I/O	**Bi-directional Data Bus (Microprocessor Interface Section):** Please see description for D7
86	A7	I	**Address Bus Input (Microprocessor Interface):** (Please see description for A8)
87	VDD	****	**Power Supply Pin**
88	$\overline{WR}$_RW	I	**Write Data Strobe (Intel Mode)** If the microprocessor interface is operating in the Intel Mode, then this active-low input pin functions as the WR* (Write Strobe) input signal from the mP. Once this active-low signal is asserted, then the Framer will latch the contents of the mP Data Bus, into the addressed register (or RAM location) within the Framer IC. **R/W Input Pin (Motorola Mode)** When the Microprocessor Interface Section is operating in the "Motorola Mode", then this pin is functionally equivalent to the "R/W*" pin. In the Motorola Mode, a "READ" operation occurs if this pin is at a logic "1". Similarly, a WRITE operation occurs if this pin is at a logic "0".
89	D7	I/O	**MSB of Bi-Directional Data Bus (Microprocessor Interface Section):** This pin, along with pins D0 - D6, function as the Microprocessor Interface bi-directional data bus, and is intended to be interfaced to the "local" microprocessor.
90	A8	I	**Address Bus Input (Microprocessor Interface) - MSB (Most Significant Bit):** This input pin, along with inputs A0 - A7 are used to select the on-chip Framer register and RAM space for READ/WRITE operations with the "local" microprocessor.
91	GND (TEST MODE)	****	**Ground Pin**

PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
92	NIBBLEINTF	I	**Nibble Interface Select Input Pin** This input pin allows the user to configure the Transmit Payload Data Input Interface and the Receive Payload Data Output Interface to operate in either the "Serial-Mode" or the "Nibble/Parallel-Mode". Setting this input pin "high" configures the Transmit and Receive Terminal Interfaces to operate in the "Nibble/Parallel-Mode". In this mode, the “Transmit Payload Data Input Interface” block will accept the “outbound” payload data (from the Terminal Equipment) in a “nibble-parallel” manner via the “TxNib[3:0]” input pins. Further, the “Receive Payload Data Output Interface” block will output the “inbound” payload data (to the Terminal Equipment) in a “nibble-parallel” manner via the “RxNib[3:0]” output pin. Setting this input pin "low" configures the Transmit and Receive Terminal Interfaces to operate in the "Serial" Mode. In this mode, the “Transmit Payload Data Input Interface” block will accept the “outbound” payload data (from the Terminal Equipment) in a “serial” manner via the “TxSer” input pin. Further, the “Receive Payload Data Output Interface” block will output the “inbound” payload data (to the Terminal Equipment) in a “serial” manner via the “RxSer” output pin.
93	TxDS1Data_27/ TxHDLCData_7	I	**Transmit DS1 Data Input - Channel 27:** This input pin accepts a DS1 signal from the Terminal Equipment. This input pin is sampled upon the "falling edge" of the TxDS1Clk_27 signal. ***NOTES:*** 1. *This input pin is inactive if the corresponding M12 MUX is multiplexing 3 E1's into an ITU-T G.747 data stream.* 2. *This input pin accepts DS2 data if M12 MUX # 7 is bypassed.*
94	TxDS1Clk_27/ SEND_MSGI	I	**Transmit DS1 Clock Input - Channel 27/SEND_MSG Request Input:** The function of this output pin depends upon whether the XRT72L13 is operating in the "Multiplexer/De-Multiplexer" Mode or in the "High Speed HDLC Controller" Mode. **Transmit DS1 Clock Input - Channel 27 (Multiplexer/De-Multiplexer Mode):** This input pin accepts a DS1 (1.544MHz) clock signal from the Terminal Equipment. The falling edge of this signal is used to sample the data at the "TxDS1Data_27" input pin. ***NOTES:*** 1. *This input pin is inactive if the corresponding M12 MUX is multiplexing 3 E1's into an ITU-T G.747 data stream.* 2. *This input pin accepts a DS2 rate clock signal (6.312MHz) if M12 MUX # 7 is bypassed.* **SEND_MSG Request Input: (High Speed HDLC Controller Mode):** Setting this input pin "HIGH" indicates that the byte, currently on the TxHDLC_Data[7:0] bus is the last byte to be included in the HDLC frame (not counting the CRC-16 or CRC-32 value).

PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
95	TxDS1Data_26/ TxHDLCData_6	I	**Transmit DS1/E1 Data Input - Channel 26/Transmit HDLC Controller Block Input - Bit 6:** The function of this output pin depends upon whether the XRT72L13 is operating in the "Multiplexer/De-Multiplexer" Mode or in the "High Speed HDLC Controller" Mode. **Transmit DS1/E1 Data Input - Channel 26 (Multiplexer/De-Multiplexer Mode):** This input pin accepts either a DS1 or E1 signal from the Terminal Equipment. This input pin is sampled upon the "falling edge" of the TxDS1Clk_26 signal. **Transmit HDLC Controller Block Input - Bit 6: (High Speed HDLC Controller Mode)** This input pin, along with TxHDLC_Data[0:5] and TxHDLC_Data_7 function as the "Transmit HDLC Controller Byte input interface. Data that resides on this bus, during the rising edge of "TxHDLCClk" is latched into the "Transmit HDLC Controller Block" and will be encapsulated into a HDLC frame and transmitted to the remote terminal equipment.
96	TxDS1Clk_26/ SEND_FCS	I	**Transmit DS1/E1 Clock Input - Channel 26/SEND_FCS Request Input pin:** The function of this output pin depends upon whether the XRT72L13 is operating in the "Multiplexer/De-Multiplexer" Mode or in the "High Speed HDLC Controller" Mode. **Transmit DS1/E1 Clock Input - Channel 26 (Multiplexer/De-Multiplexer Mode):** This input pin accepts either a DS1 (1.544MHz) or an E1 (2.048MHz) clock signal from the Terminal Equipment. The falling edge of this signal is used to sample the data at the "TxDS1Data_26" input pin. **SendFCS Request Input (High Speed HDLC Controller Mode)** Setting this input pin "HIGH, at the end of enter data to be transported over the DS3 transport medium via an out-bound HDLC frame, commands the Transmit HDLC Controller to compute FCS value (e.g., either a CRC-16 or CRC-32 value) and append it to the outbound HDLC frame.
97	TxDS1Data_25/ TxHDLCData_5	I	**Transmit DS1/E1 Data Input - Channel 25/Transmit HDLC Controller Block Input - Bit 5:** The funtion of this output pin depends upon whether the XRT72L13 is operating in the "Multiplexer/De-Multiplexer" Mode or in the "High Speed HDLC Controller" Mode. **Transmit DS1/E1 Data Input - Channel 25 (Multiplexer/De-Multiplexer Mode):** This input pin accepts either a DS1 or E1 signal from the Terminal Equipment. This input pin is sampled upon the "falling edge" of the TxDS1Clk_25 signal. **Transmit HDLC Controller Block Input - Bit 5: (High Speed HDLC Controller Mode)** This input pin, along with TxHDLC_Data[0:4] and TxHDLC_Data[6:7] function as the "Transmit HDLC Controller Byte input interface. Data that resides on this bus, during the rising edge of "TxHDLCClk" is latched into the "Transmit HDLC Controller Block" and will be encapsulated into a HDLC frame and transmitted to the remote terminal equipment.
98	GND	****	**Ground Pin**

PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
99	TxDS1Clk_25	I	**Transmit DS1/E1 Clock Input - Channel 25:** This input pin accepts either a DS1 (1.544MHz) or an E1 (2.048MHz) clock signal from the Terminal Equipment. The falling edge of this signal is used to sample the data at the "TxDS1Data_25" input pin.
100	TxDS1Data_24/ TxHDLCData_4	I	**Transmit DS1/E1 Data Input - Channel 24/Transmit HDLC Controller Block Input - Bit 4:** The funtion of this output pin depends upon whether the XRT72L13 is operating in the "Multiplexer/De-Multiplexer" Mode or in the "High Speed HDLC Controller" Mode. **Transmit DS1/E1 Data Input - Channel 24 (Multiplexer/De-Multiplexer Mode):** This input pin accepts either a DS1 or E1 signal from the Terminal Equipment. This input pin is sampled upon the "falling edge" of the TxDS1Clk_24 signal. **Transmit HDLC Controller Block Input - Bit 4: (High Speed HDLC Controller Mode)** This input pin, along with TxHDLC_Data[0:3] and TxHDLC_Data[5:7] function as the "Transmit HDLC Controller Byte input interface. Data that resides on this bus, during the rising edge of "TxHDLCClk" is latched into the "Transmit HDLC Controller Block" and will be encapsulated into a HDLC frame and transmitted to the remote terminal equipment.
101	TxDS1Clk_24	I	**Transmit DS1/E1 Clock Input - Channel 24:** This input pin accepts either a DS1 (1.544MHz) or an E1 (2.048MHz) clock signal from the Terminal Equipment. The falling edge of this signal is used to sample the data at the "TxDS1Data_24" input pin.
102	TxDS1Data_23/ TxHDLCData_3	I	**Transmit DS1 Data Input - Channel 23/Transmit HDLC Controller Block Input - Bit 3:** The funtion of this output pin depends upon whether the XRT72L13 is operating in the "Multiplexer/De-Multiplexer" Mode or in the "High Speed HDLC Controller" Mode. **Transmit DS1 Data Input - Channel 23 (Multiplexer/De-Multiplexer Mode):** This input pin accepts a DS1 signal from the Terminal Equipment. This input pin is sampled upon the "falling edge" of the TxDS1Clk_1 signal. ***NOTES:*** 1. *This input pin is inactive if the corresponding M12 MUX is multiplexing 3 E1's into an ITU-T G.747 data stream.* 2. *This input pin accepts DS2 data if M12 MUX # 6 is bypassed.* **Transmit HDLC Controller Block Input - Bit 3: (High Speed HDLC Controller Mode)** This input pin, along with TxHDLC_Data[0:2] and TxHDLC_Data[4:7] function as the "Transmit HDLC Controller Byte input interface. Data that resides on this bus, during the rising edge of "TxHDLCClk" is latched into the "Transmit HDLC Controller Block" and will be encapsulated into a HDLC frame and transmitted to the remote terminal equipment.

PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
103	TxDS1Clk_23	I	**Transmit DS1 Clock Input - Channel 23:** This input pin accepts a DS1 (1.544MHz) clock signal from the Terminal Equipment. The falling edge of this signal is used to sample the data at the "TxDS1Data_23" input pin. ***NOTES:*** 1. *This input pin is inactive if the corresponding M12 MUX is multiplexing 3 E1's into an ITU-T G.747 data stream.* 2. *This input pin accepts a DS2 rate clock signal (6.312MHz) if M12 MUX # 6 is bypassed.*
104	TxDS1Data_22/ TxHDLCData_2	I	**Transmit DS1/E1 Data Input - Channel 22/Transmit HDLC Controller Block Input - Bit 2:** The funtion of this output pin depends upon whether the XRT72L13 is operating in the "Multiplexer/De-Multiplexer" Mode or in the "High Speed HDLC Controller" Mode. **Transmit DS1/E1 Data Input - Channel 22 (Multiplexer/De-Multiplexer Mode)** This input pin accepts either a DS1 or E1 signal from the Terminal Equipment. This input pin is sampled upon the "falling edge" of the TxDS1Clk_22 signal. **Transmit HDLC Controller Block Input - Bit 2: (High Speed HDLC Controller Mode)** This input pin, along with TxHDLC_Data[0:1 and TxHDLC_Data[3:7] function as the "Transmit HDLC Controller Byte input interface. Data that resides on this bus, during the rising edge of "TxHDLCClk" is latched into the "Transmit HDLC Controller Block" and will be encapsulated into a HDLC frame and transmitted to the remote terminal equipment.
105	TxDS1Clk_22	I	**Transmit DS1/E1 Clock Input - Channel 22:** This input pin accepts either a DS1 (1.544MHz) or an E1 (2.048MHz) clock signal from the Terminal Equipment. The falling edge of this signal is used to sample the data at the "TxDS1Data_22" input pin.
106	TxDS1Data_21/ TxHDLCData_1	I	**Transmit DS1/E1 Data Input - Channel 21/Transmit HDLC Controller Block Input - Bit 1:** The funtion of this output pin depends upon whether the XRT72L13 is operating in the "Multiplexer/De-Multiplexer" Mode or in the "High Speed HDLC Controller" Mode. **Transmit DS1/E1 Data Input - Channel 21 (Multiplexer/De-Multiplexer Mode):** This input pin accepts either a DS1 or E1 signal from the Terminal Equipment. This input pin is sampled upon the "falling edge" of the TxDS1Clk_21 signal. **Transmit HDLC Controller Block Input - Bit 1: (High Speed HDLC Controller Mode)** This input pin, along with TxHDLC_Data_0 and TxHDLC_Data[2:7] function as the "Transmit HDLC Controller Byte input interface. Data that resides on this bus, during the rising edge of "TxHDLCClk" is latched into the "Transmit HDLC Controller Block" and will be encapsulated into a HDLC frame and transmitted to the remote terminal equipment.

PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
107	TxDS1Clk_21		**Transmit DS1/E1 Clock Input - Channel 21:** This input pin accepts either a DS1 (1.544MHz) or an E1 (2.048MHz) clock signal from the Terminal Equipment. The falling edge of this signal is used to sample the data at the "TxDS1Data_21" input pin.
108	TxDS1Data_20/ TxHDLCData_0	I	**Transmit DS1/E1 Data Input - Channel 20/Transmit HDLC Controller Block Input - Bit 0:** The funtion of this output pin depends upon whether the XRT72L13 is operating in the "Multiplexer/De-Multiplexer" Mode or in the "High Speed HDLC Controller" Mode. **Transmit DS1/E1 Data Input - Channel 20 (Multiplexer/De-Multiplexer Mode)** This input pin accepts either a DS1 or E1 signal from the Terminal Equipment. This input pin is sampled upon the "falling edge" of the TxDS1Clk_20 signal. **Transmit HDLC Controller Block Input - Bit 0: (High Speed HDLC Controller Mode)** This input pin, along with TxHDLC_Data[1:7] function as the "Transmit HDLC Controller Byte input interface. Data that resides on this bus, during the rising edge of "TxHDLCClk" is latched into the "Transmit HDLC Controller Block" and will be encapsulated into a HDLC frame and transmitted to the remote terminal equipment.
109	TxDS1Clk_20	I	**Transmit DS1 Clock Input - Channel 20:** This input pin accepts either a DS1 (1.544MHz) or an E1 (2.048MHz) clock signal from the Terminal Equipment. The falling edge of this signal is used to sample the data at the "TxDS1Data_20" input pin.
110	TxDS1Data_19	I	**Transmit DS1 Data Input - Channel 19:** This input pin accepts a DS1 signal from the Terminal Equipment. This input pin is sampled upon the "falling edge" of the TxDS1Clk_19 signal. ***NOTES:*** 1. *This input pin is inactive if the corresponding M12 MUX is multiplexing 3 E1's into an ITU-T G.747 data stream.* 2. *This input pin accepts DS2 data if M12 MUX # 5 is bypassed.*
111	TxDS1Clk_19	I	**Transmit DS1 Clock Input - Channel 19:** This input pin accepts a DS1 (1.544MHz) clock signal from the Terminal Equipment. The falling edge of this signal is used to sample the data at the "TxDS1Data_19" input pin. ***NOTES:*** 1. *This input pin is inactive if the corresponding M12 MUX is multiplexing 3 E1's into an ITU-T G.747 data stream.* 2. *This input pin accepts a DS2 rate clock signal (6.312MHz) if M12 MUX # 5 is bypassed.*
112	TxDS1Data_18	I	**Transmit DS1/E1 Data Input - Channel 18:** This input pin accepts either a DS1 or E1 signal from the Terminal Equipment. This input pin is sampled upon the "falling edge" of the TxDS1Clk_18 signal.
113	TxDS1Clk_18	I	**Transmit DS1/E1 Clock Input - Channel 18:** This input pin accepts either a DS1 (1.544MHz) or an E1 (2.048MHz) clock signal from the Terminal Equipment. The falling edge of this signal is used to sample the data at the "TxDS1Data_18" input pin.

PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
114	TxDS1Data_17	I	**Transmit DS1/E1 Data Input - Channel 17:** This input pin accepts either a DS1 or E1 signal from the Terminal Equipment. This input pin is sampled upon the "falling edge" of the TxDS1Clk_17 signal.
115	TxDS1Clk_17	I	**Transmit DS1/E1 Clock Input - Channel 17:** This input pin accepts either a DS1 (1.544MHz) or an E1 (2.048MHz) clock signal from the Terminal Equipment. The falling edge of this signal is used to sample the data at the "TxDS1Data_17" input pin.
116	TxDS1Data_16	I	**Transmit DS1/E1 Data Input - Channel 16:** This input pin accepts either a DS1 or E1 signal from the Terminal Equipment. This input pin is sampled upon the "falling edge" of the TxDS1Clk_16 signal.
117	TxDS1Clk_16	I	**Transmit DS1/E1 Clock Input - Channel 16:** This input pin accepts either a DS1 (1.544MHz) or an E1 (2.048MHz) clock signal from the Terminal Equipment. The falling edge of this signal is used to sample the data at the "TxDS1Data_1" input pin.
118	VDD	****	**Power Supply Pin**
119	TxDS1Data_15	I	**Transmit DS1 Data Input - Channel 15:** This input pin accepts a DS1 signal from the Terminal Equipment. This input pin is sampled upon the "falling edge" of the TxDS1Clk_15 signal. ***NOTES:*** 1. *This input pin is inactive if the corresponding M12 MUX is multiplexing 3 E1's into an ITU-T G.747 data stream.* 2. *This input pin accepts DS2 data if M12 MUX # 4 is bypassed.*
120	TxDS1Clk_15	I	**Transmit DS1 Clock Input - Channel 15:** This input pin accepts a DS1 (1.544MHz) clock signal from the Terminal Equipment. The falling edge of this signal is used to sample the data at the "TxDS1Data_15" input pin. ***NOTES:*** 1. *This input pin is inactive if the corresponding M12 MUX is multiplexing 3 E1's into an ITU-T G.747 data stream.* 2. *This input pin accepts a DS2 rate clock signal (6.312MHz) if M12 MUX # 4 is bypassed.*
121	TxDS1Data_14	I	**Transmit DS1/E1 Data Input - Channel 14:** This input pin accepts either a DS1 or E1 signal from the Terminal Equipment. This input pin is sampled upon the "falling edge" of the TxDS1Clk_14 signal.
122	TxDS1Clk_14	I	**Transmit DS1/E1 Clock Input - Channel 14:** This input pin accepts either a DS1 (1.544MHz) or an E1 (2.048MHz) clock signal from the Terminal Equipment. The falling edge of this signal is used to sample the data at the "TxDS1Data_14" input pin.
123	TxDS1Data_13	I	**Transmit DS1/E1 Data Input - Channel 13:** This input pin accepts either a DS1 or E1 signal from the Terminal Equipment. This input pin is sampled upon the "falling edge" of the TxDS1Clk_13 signal.

PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
124	TxDS1Clk_13	I	**Transmit DS1/E1 Clock Input - Channel 13:** This input pin accepts either a DS1 (1.544MHz) or an E1 (2.048MHz) clock signal from the Terminal Equipment. The falling edge of this signal is used to sample the data at the "TxDS1Data_13" input pin.
125	TxDS1Data_12	I	**Transmit DS1/E1 Data Input - Channel 12:** This input pin accepts either a DS1 or E1 signal from the Terminal Equipment. This input pin is sampled upon the "falling edge" of the TxDS1Clk_12 signal.
126	TxDS1Clk_12	I	**Transmit DS1/E1 Clock Input - Channel 12:** This input pin accepts either a DS1 (1.544MHz) or an E1 (2.048MHz) clock signal from the Terminal Equipment. The falling edge of this signal is used to sample the data at the "TxDS1Data_12" input pin.
127	TxDS1Data_11	I	**Transmit DS1 Data Input - Channel 11:** This input pin accepts a DS1 signal from the Terminal Equipment. This input pin is sampled upon the "falling edge" of the TxDS1Clk_11 signal. ***NOTES:*** *1. This input pin is inactive if the corresponding M12 MUX is multiplexing 3 E1's into an ITU-T G.747 data stream.* *2. This input pin accepts DS2 data if M12 MUX # 3 is bypassed.*
128	GND	****	**Ground Pin**
129	TxDS1Clk_11	I	**Transmit DS1 Clock Input - Channel 11:** This input pin accepts a DS1 (1.544MHz) clock signal from the Terminal Equipment. The falling edge of this signal is used to sample the data at the "TxDS1Data_11" input pin. ***NOTES:*** **1.** This input pin is inactive if the corresponding M12 MUX is multiplexing 3 E1's into an ITU-T G.747 data stream. **2.** This input pin accepts a DS2 rate clock signal (6.312MHz) if M12 MUX # 3 is bypassed.
130	TxDS1Data_10	I	**Transmit DS1/E1 Data Input - Channel 10:** This input pin accepts either a DS1 or E1 signal from the Terminal Equipment. This input pin is sampled upon the "falling edge" of the TxDS1Clk_10 signal.
131	TxDS1Clk_10	I	**Transmit DS1/E1 Clock Input - Channel 10:** This input pin accepts either a DS1 (1.544MHz) or an E1 (2.048MHz) clock signal from the Terminal Equipment. The falling edge of this signal is used to sample the data at the "TxDS1Data_10" input pin.
132	TxDS1Data_9	I	**Transmit DS1/E1 Data Input - Channel 9:** This input pin accepts either a DS1 or E1 signal from the Terminal Equipment. This input pin is sampled upon the "falling edge" of the TxDS1Clk_9 signal.
133	TxDS1Clk_9	I	**Transmit DS1/E1 Clock Input - Channel 9:** This input pin accepts either a DS1 (1.544MHz) or an E1 (2.048MHz) clock signal from the Terminal Equipment. The falling edge of this signal is used to sample the data at the "TxDS1Data_9" input pin.

PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
134	TxDS1Data_8	I	**Transmit DS1/E1 Data Input - Channel 8:** This input pin accepts either a DS1 or E1 signal from the Terminal Equipment. This input pin is sampled upon the "falling edge" of the “TxDS1Clk_8” signal.
135	TxDS1Clk_8	I	**Transmit DS1/E1 Clock Input - Channel 8:** This input pin accepts either a DS1 (1.544MHz) or an E1 (2.048MHz) clock signal from the Terminal Equipment. The falling edge of this signal is used to sample the data at the "TxDS1Data_8" input pin.
136	TxDS1Data_7	I	**Transmit DS1 Data Input - Channel 7:** This input pin accepts a DS1 signal from the Terminal Equipment. This input pin is sampled upon the "falling edge" of the TxDS1Clk_7 signal. ***NOTES:*** 1. *This input pin is inactive if the corresponding M12 MUX is multiplexing 3 E1's into an ITU-T G.747 data stream.* 2. *This input pin accepts DS2 data if M12 MUX # 2 is bypassed.*
137	VDD	****	**Power Supply Pin**
138	TxDS1Clk_7	I	**Transmit DS1 Clock Input - Channel 7:** This input pin accepts a DS1 (1.544MHz) clock signal from the Terminal Equipment. The falling edge of this signal is used to sample the data at the "TxDS1Data_7" input pin. ***NOTES:*** 1. *This input pin is inactive if the corresponding M12 MUX is multiplexing 3 E1's into an ITU-T G.747 data stream.* 2. *This input pin accepts a DS2 rate clock signal (6.312MHz) if M12 MUX # 2 is bypassed.*
139	TxDS1Data_6	I	**Transmit DS1/E1 Data Input - Channel 6:** This input pin accepts either a DS1 or E1 signal from the Terminal Equipment. This input pin is sampled upon the "falling edge" of the TxDS1Clk_6 signal.
140	TxDS1Clk_6	I	**Transmit DS1/E1 Clock Input - Channel 6:** This input pin accepts either a DS1 (1.544MHz) or an E1 (2.048MHz) clock signal from the Terminal Equipment. The falling edge of this signal is used to sample the data at the "TxDS1Data_6" input pin.
141	TxDS1Data_5	I	**Transmit DS1/E1 Data Input - Channel 5:** This input pin accepts either a DS1 or E1 signal from the Terminal Equipment. This input pin is sampled upon the "falling edge" of the TxDS1Clk_5 signal.
142	TxDS1Clk_5	I	**Transmit DS1/E1 Clock Input - Channel 5:** This input pin accepts either a DS1 (1.544MHz) or an E1 (2.048MHz) clock signal from the Terminal Equipment. The falling edge of this signal is used to sample the data at the "TxDS1Data_5" input pin.
143	TxDS1Data_4	I	**Transmit DS1/E1 Data Input - Channel 4:** This input pin accepts either a DS1 or E1 signal from the Terminal Equipment. This input pin is sampled upon the "falling edge" of the TxDS1Clk_4 signal.

PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
144	TxDS1Clk_4	I	**Transmit DS1/E1 Clock Input - Channel 4:** This input pin accepts either a DS1 (1.544MHz) or an E1 (2.048MHz) clock signal from the Terminal Equipment. The falling edge of this signal is used to sample the data at the "TxDS1Data_4" input pin.
145	TxDS1Data_3	I	**Transmit DS1 Data Input - Channel 3:** This input pin accepts a DS1 signal from the Terminal Equipment. This input pin is sampled upon the "falling edge" of the TxDS1Clk_3 signal. ***NOTES:*** 1. *This input pin is inactive if the corresponding M12 MUX is multiplexing 3 E1's into an ITU-T G.747 data stream.* 2. *This input pin accepts DS2 data if M12 MUX # 1 is bypassed.*
146	GND	****	**Ground Pin**
147	TxDS1Clk_3	I	**Transmit DS1 Clock Input - Channel 3:** This input pin accepts a DS1 (1.544MHz) clock signal from the Terminal Equipment. The falling edge of this signal is used to sample the data at the "TxDS1Data_3" input pin. ***NOTES:*** 1. *This input pin is inactive if the corresponding M12 MUX is multiplexing 3 E1's into an ITU-T G.747 data stream.* 2. *This input pin accepts a DS2 rate clock signal (6.312MHz) if M12 MUX # 1 is bypassed.*
148	TxDS1Data_2	I	**Transmit DS1/E1 Data Input - Channel 2:** This input pin accepts either a DS1 or E1 signal from the Terminal Equipment. This input pin is sampled upon the "falling edge" of the TxDS1Clk_2 signal.
149	TxDS1Clk_2	I	**Transmit DS1/E1 Clock Input - Channel 2:** This input pin accepts either a DS1 (1.544MHz) or an E1 (2.048MHz) clock signal from the Terminal Equipment. The falling edge of this signal is used to sample the data at the "TxDS1Data_2" input pin.
150	TxDS1Data_1	I	**Transmit DS1/E1 Data Input - Channel 1:** This input pin accepts either a DS1 or E1 signal from the Terminal Equipment. This input pin is sampled upon the "falling edge" of the TxDS1Clk_1 signal.
151	TxDS1Clk_1	I	**Transmit DS1/E1 Clock Input - Channel 1:** This input pin accepts either a DS1 (1.544MHz) or an E1 (2.048MHz) clock signal from the Terminal Equipment. The falling edge of this signal is used to sample the data at the "TxDS1Data_1" input pin.
152	TxDS1Data_0	I	**Transmit DS1/E1 Data Input - Channel 1:** This input pin accepts either a DS1 or E1 signal from the Terminal Equipment. This input pin is sampled upon the "falling edge" of the TxDS1Clk_0 signal.
153	TxDS1Clk_0	I	**Transmit DS1/E1 Clock Input - Channel 1:** This input pin accepts either a DS1 (1.544MHz) or an E1 (2.048MHz) clock signal from the Terminal Equipment. The falling edge of this signal is used to sample the data at the "TxDS1Data_0" input pin.
154	DS2InClk	I	**Transmit DS2 Clock Input**

PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
155	DS2OutClk	O	**Transmit DS2 Clock Output**
156	TxFrameRef	I	**Transmit Framer Reference Input:** This input pin functions as the "Transmit Frame Generation" reference signal, if the XRT72L13 has been configured to operate in the "Local-Time/Frame Slave" Mode. If the XRT72L13 has been configured to operate in the "Local-Time/Frame-Slave" Mode, then the user's terminal equipment is expected to apply a pulse (to this input pin) once every 106.4 microseconds. In the "Local-Time/Frame-Slave" Mode, the Transmit Section of the XRT72L13 M13 Multiplexer/Framer IC will initiate its generation of a new "outbound" DS3 frame, upon the rising edge of this signal. ***NOTE:*** *The user can configure the XRT72L13 M13 Multiplexer/Framer IC to operate in the "Local Time/Frame Slave" Mode by writing "xxxx xx01" into the "Operating Mode" Register (Address = 0x00).*
157	TxFrame	O	**Transmit End of DS3 Frame Indicator:** .The Transmit Section of the XRT72L13 will pulse this output pin "high" (for one bit-period), when the Transmit Payload Data Input Interface is processing the last bit of a given DS3 frame. The purpose of this output pin is to alert the Terminal Equipment that it needs to begin transmission of a new DS3 frame to the XRT72L13 (e.g., to permit the XRT72L13 to maintain Transmit DS3 framing alignment control over the Terminal Equipment).
158	TxInClk	I	**Transmit Framer Reference Clock Input.** This input pin functions as the "Timing Reference" for the Transmit Section of the "Clear Channel DS3 Framer" block within XRT72L13 M13 Multiplexer/Framer IC; if the device has been configured to operate in the "Local-Time" Mode. Further, if the XRT72L13 M13 Multiplexer/Framer IC has been configured to operate in the "Local-Time" Mode, the "Transmit Payload Data Input Interface will sample the data at the TxSer input pin, upon the rising edge of "TxInClk". ***NOTES:*** 1. *The user should apply a 44.736MHz clock signal to this input pin.* 2. *The user can configure the XRT72L13 M13 Multiplexer/ Framer IC to operate in the "Local-Time" mode by writing "xxxx xx01" or "xxxx xx1x" into the "Operating Mode" register (Address = 0x00).*
159	TxNibFrame	O	**Transmit Frame Boundary Indicator - Nibble/Parallel Interface** This output pin pulses "high" when the last nibble of a given DS3 frame is expected at the TxNib[3:0] input pins. The purpose of this output pin is to alert the Terminal Equipment that it needs to begin transmission of a new DS3 frame to the XRT72L13. ***NOTE:*** *This pin is only used for "Clear-Channel Framer" applications.*

PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
160	TxOHInd/ TxPLClkEnb	O	**Transmit Overhead Data Indicator/Transmit Payload Data Clock Enable Output..** The funtion of this output pin depends upon whether the XRT72L13 is operating in the “Clear-Channel” or the “High-Speed HDLC Controller” Mode. **Clear Channel Framer Mode.** This output pin will pulse "high" one-bit period prior to the time that the Transmit Section of the XRT72L13 will be processing an Overhead bit. The purpose of this output pin is to warn the Terminal Equipment that, during the very next bit-period, the XRT72L13 is going to be processing an "Overhead" bit and will be ignoring any data that is applied to the "TxSer" input pin. ***NOTE:*** *This output pin is only active if the XRT72L13 is operating in the "Serial" Mode. This output pin will be pulled "low" if the device is operating in the "Nibble-Parallel" Mode.* **High Speed HDLC Controller Mode.**
161	TxNibClk	O	**Transmit Nibble Clock Signal** If the user opts to operate the XRT72L13 in the “Nibble-Parallel” mode, then the XRT72L13 will derive this clock signal from either the “TxInClk” or the “RxLineClk” signal (depending upon which signal is selected as the timing reference). The user is advised to configure the Terminal Equipment to output the “outbound” payload data (to the XRT72L13 Framer IC) onto the “TxNib[3:0]” input pins, upon the rising edge of this clock signal. ***NOTES:*** 1. *The XRT72L13 M13/Framer IC will output 1176 clock edges (to the Terminal Equipment) for each “outbound” DS3 frame.* 2. *This pin is only active for “Clear-Channel Framer” applications.*

PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
162	TxNib_0/ TxSer	I	**Transmit Nibble-Parallel Payload Data Input -0/Transmit Serial Payload Data Input pin:** The exact function of this pin depends upon whether the XRT72L13 is operating in the "Serial" or "Nibble-Parallel" interface Mode. TxNib_0 - (Nibble Parallel Interface Mode): The Terminal Equipment is expected to input data, that is intended to be transmitted to the remote terminal, over a DS3 transport medium. The Framer IC will take data, applied to this pin (along with TxNib1, TxNib2, and TxNib3), and insert it into an outbound "DS3" frame. The XRT72L13 will sample the data that is at these input pins, upon the rising edge of the "TxNibClk" signal. Transmit Serial Payload Data Input Pin - (Serial Interface Mode): The Terminal Equipment is expected to input data, that is intended to be transmitted to the remote terminal, over a DS3 transport medium. The Framer IC will take data, applied to this pin, and insert it into an outbound "DS3" frame. If the XRT72L13 M13 Multiplexer/Framer IC has been configured to operate in the "Local Time" Mode, then it will sample the data (on this pin) upon the rising edge of "TxInClk". If the XRT72L13 M13 Multi-plexer/Framer IC has been configured to operate in the "Loop-Time" Mode, then it will sample the data (on this pin) upon the rising edge of "RxOutClk". ***NOTE:*** *This input pin is active only if the Serial Mode has been selected.*
163	TxNib_1	I	**Transmit Nibble-Paralle Payload Data Input -1:** The Terminal Equipment is expected to input data, that is intended to be transmitted to the remote terminal, over a DS3 transport medium. The Framer IC will take data, applied to this pin, and insert it into an outbound "DS3" frame. The XRT72L13 will sample the data that is at these input pins, upon the rising edge of the "TxNibClk" signal. ***NOTE:*** *This input pin is active only if the Nibble/Parallel Mode has been selected.*
164	VDD	****	**Power Supply Pin**
165	TxNib_2	I	**Transmit Nibble-Parallel Payload Data Input -2:** The Terminal Equipment is expected to input data, that is intended to be transmitted to the remote terminal, over a DS3 transport medium. The Framer IC will take data, applied to this pin, and insert it into an outbound " DS3" frame. The XRT72L13 will sample the data that is at these input pins, upon the rising edge of the "TxNibClk" signal. ***NOTE:*** *This input pin is active only if the Nibble/Parallel Mode has been selected.*
166	TxNib_3	I	**Transmit Nibble-Parallel Payload Data Input -3:** The Terminal Equipment is expected to input data, that is intended to be transmitted to the remote terminal, over an DS3 transport medium. The Framer IC will take data, applied to this pin (along with TxNib1, TxNib2, and TxNib3), and insert it into an outbound DS3" frame. The XRT72L13 will sample the data that is at these input pins, upon the rising edge of the "TxNibClk" signal. Note: This input pin is active only if the Nibble/Parallel Mode has been selected.

PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
167	TxOHIns	I	**Transmit Overhead Data Insert Input.** Asserting this input signal (e.g., setting it "high") enables the Transmit Overhead Data Input Interface to accept "overhead" data from the Terminal Equipment. In other words, while this input pin is "high", the Transmit Overhead Data Input Interface will sample the data at the "TxOH" input pin, on the falling edge of the "TxOHClk" output signal. Conversely, setting this pin "low" configures the "Transmit Overhead Data Input Interface" to NOT sample (e.g., ignore) the data at the "TxOH" input pin, on the falling edge of the "TxOHClk" output signal. ***NOTES:*** 1. *If the Terminal Equipment attempts to insert an overhead bit that cannot be accepted by the "Transmit Overhead Data Input Interface" (e.g., if the Terminal Equipment asserts the "TxOHIns" signal, at a time when one of these "non-insertable" overhead bits are being processed); that particular insertion effort will be ignored.* 2. *This pin is only used in "Clear-Channel Framer" applications.*
168	TxAISEn	I	**Transmit AIS Command Input:** Setting this input pin "high" configures the XRT72L13 to transmit an AIS (Alarm Indication Signal) pattern to the remote terminal. Setting this input pin "low" configures the Transmit Section to generate DS3 traffic in a normal manner.
169	TxOHFrame	O	**Transmit Overhead Frame:** This output pin pulses "high" when the Transmit Overhead Data Input Interface block is expecting the first Overhead bit, within a DS3 frame to be applied to the TxOH input pin. This pin is "high" for one clock period of TxOHClk.
170	TxOHEnable	O	**Transmit Overhead Frame Enable:** The XRT72L13 will assert this signal, for one "TxInClk" period, just prior to the instant that the "Transmit Overhead Data Input Interface" will be sampling and processing an overhead bit. If the Terminal Equipment intends to insert its own value for an overhead bit, into the outbound DS3 frame, it is expected to sample the state of this signal, upon the falling edge of "TxInClk". Upon sampling the "TxOHEnable" high, the Terminal Equipment should (1) place the desired value of the overhead bit, onto the "TxOH" input pin and (2) assert the "TxOHIns" input pin. The Transmit Overhead Data Input Interface" block will sample and latch the data on the "TxOH" signal, upon the rising edge of the very next "TxInClk" input signal.

PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
171	TxOHClk	O	**Transmit Overhead Clock** This output signal serves two purposes: 1. The Transmit Overhead Data Input Interface block will provide a rising clock edge on this signal, one bit-period prior to the start to the instant that the “Transmit Overhead Data Input Interface” block is processing an overhead bit. 2. The Transmit Overhead Data Input Interface will sample the data at the “TxOH” input pin, on the falling edge of this clock signal (provided that the “TxOHIns” input pin is “HIGH”). ***NOTE:*** *The Transmit Overhead Data Input Interface block will supply a clock edge for all overhead bits within the DS3 frame (via the “TxOHClk” output signal). This includes those overhead bits that the “Transmit Overhead Data Input Interface” will not accept from the Terminal Equipment.*
172	TxOH	O	**Transmit Overhead Input Pin** The Transmit Overhead Data Input Interface accepts the overhead data via this input pin, and inserts into the "overhead" bit position within the very next "outbound" DS3 frame. If the "TxOHIns" pin is pulled "high", the Transmit Overhead Data Input Interface will sample the data at this input pin (TxOH), on the falling edge of the "TxOHClk" output pin. Conversely, if the "TxOHIns" pin is pulled "low", then the Transmit Overhead Data Input Interface will NOT sample the data at this input pin (TxOH). Consequently, this data will be ignored
173	TxNEG	O	**Transmit Negative Polarity Pulse:** The exact role of this output pin depends upon whether the Framer is operating in the Unipolar or Bipolar Mode. **Unipolar Mode:** This output signal pulses "high" for one bit period, at the end of each "outbound" DS3 frame. This output signal is at a logic "low" for all of the remaining bit-periods of the "outbound" DS3 frames **Bipolar Mode:** This output pin functions as one of the two dual-rail output signals that commands the sequence of pulses to be driven on the line. TxPOS is the other output pin. This input is typically connected to the TNData input of the external DS3/E3 Line Interface Unit IC. When this output is asserted, it will command the LIU to generate a negative polarity pulse on the line.
174	TxPOS	O	**Transmit Positive Polarity Pulse:** The exact role of this output pin depends upon whether the Framer is operating in the Unipolar or Bipolar Mode. **Unipolar Mode:** This output pin functions as the "Single-Rail" output signal for the "outbound" DS3 data stream. The signal, at this output pin, will be updated on the "user-selected" edge of the TxLineClk signal. **Bipolar Mode:** This output pin functions as one of the two dual rail output signals that commands the sequence of pulses to be driven on the line. TxNEG is the other output pin. This input is typically connected to the TPData input of the external DS3 or E3 Line Interface Unit IC. When this output is asserted, it will command the LIU to generate a positive polarity pulse on the line.

PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
175	TxLineClk	O	**Transmit Line Interface Clock:** This clock signal is output to the Line Interface Unit, along with the TxPOS and TxNEG signals. The purpose of this output clock signal is to provide the LIU with timing information that it can use to generate the AMI pulses and deliver them over the transmission medium to the Far-End Receiver. The user can configure the source of this clock to be either the RxLineClk (from the Receiver portion of the Framer) or the TxInClk input. The nominal frequency of this clock signal is 34.368 MHz.
176	$\overline{\text{REQ}}$	O	**Receive Equalization Enable/Disable Select output pin - (to be connected to the XRT7300 DS3/E3 Line Interface Unit IC).** This output pin is intended to be connected to the REQB input pin of the XRT7300 DS3/E3 Line Interface Unit IC. The user can control the state of this output pin by writing a '0' or '1' to Bit 5 (REQB) within the Line Interface Driver Register (Address = 0x80). If the user commands this signal to toggle "high" then the internal Receive Equalizer (within the XRT7300) will be disabled. Conversely, if the user commands this output signal to toggle "low", then the internal Receive Equalizer (within the XRT7300) will be enabled. For information on the criteria that should be used when deciding whether to bypass the equalization circuitry or not, please consult the "XRT7300 DS3/E3 Line Interface Unit" data sheet. Writing a "1" to Bit 5 of the Line Interface Drive Register (Address = 0x80) will cause this output pin to toggle "high". Writing a "0" to this bit-field will cause this output pin to toggle "low". Note: If the customer is not using the XRT7300 DS3/E3 Line Interface Unit IC, then he/she can use this output pin for a variety of other purposes.
177	TAOS	O	**"Transmit All Ones Signal" (TAOS) Command (for the XRT7300 Line Interface Unit IC).** This output pin is intended to be connected to the TAOS input pin of the XR-T7300 DS3/E3 Line Interface Unit IC. The user can control the state of this output pin by writing a '0' or '1' to Bit 4 (TAOS) of the Line Interface Drive Register (Address = 0x80). If the user commands this signal to toggle "high" then it will force the XRT7300 Line Interface Unit IC to transmit an "All Ones" pattern onto the line. Conversely, if the user commands this output signal to toggle "low" then the XR-T7300 DS3/E3 Line Interface Unit IC will proceed to transmit data based upon the pattern that it receives via the TxPOS and TxNEG output pins. Writing a "1" to Bit 4 of the Line Interface Drive Register (Address = 0x80) will cause this output pin to toggle "high". Writing a "0" to this bit-field will cause this output pin to toggle "low". ***NOTE:*** *This output pin can be used for a variety of other purposes if the XRT7300 DS3/E3 LIU is not used.*
178	GND	****	**Ground Pin**

PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
179	ENCODIS	O	**Encoder (HDB3) Disable Output pin (intended to be connected to the XRT7300 DS3/E3 Line Interface Unit IC).** This output pin is intended to be connected to the Encodis input pin of the XRT7300 DS3/E3 Line Interface Unit IC. The user can control the state of this output pin by writing a "0" or "1" to Bit 3 (Encodis) within the Line Interface Driver Register (Address = 0x80). If the user commands this signal to toggle "high" then it will disable the B3ZS encoder circuitry within the XRT7300 IC. Conversely, if the user commands this output signal to toggle "low", then the B3ZS Encoder circuitry, within the XRT7300 IC will be enabled. Writing a "1" to Bit 3 of the Line Interface Driver Register (Address = 0x80) will cause this output pin to toggle "high". Writing a "0" to this bit-field will cause this output pin to toggle "low". ***NOTES:*** 1. *The user is advised to disable the B3ZS encoder (within the XRT7300 IC) if the XRT72L13 M13 Multiplexer/Framer IC has been configured to operate in the B3ZS/HDB3 line code.* 2. *If the customer is not using the XRT7300 DS3/E3 Line Interface Unit IC, then this output pin can be used for a variety of other purposes.*
180	TxLEV	O	**Transmit Line Build-Out Enable/Disable Select Output (to be connected to the XRT7300 DS3/E3 Line Interface Unit IC).** This output pin is intended to be connected to the TxLev input pin of the XRT7300 DS3/E3 Line Interface Unit IC. The user can control the state of this output pin by writing a "0" or a "1" to Bit 2 (TxLev) within the Line Interface Driver Register (Address = 0x80). Writing a "1" to Bit 2 of the Line Interface Drive Register (Address = 0x80) will cause this output pin to toggle "high". Writing a "0" to this bit-field will cause this output pin to toggle "low". If the user commands this signal to toggle "high" then the "Transmit Line Build-Out" circuit (within the XRT7300) will be disabled. In this mode, the XRT7300 will output unshaped (e.g., square) pulses onto the line (via the TTIP and TRING output pins). Conversely, if the user commands this signal to toggle "low" then the "Transmit Line Build-Out" circuit (within the XRT7300) will be disabled. In this mode, the XRT7300 will output shaped (e.g., more rounded) pulses onto the line (via the TTIP and TRING output pins). In order to comply with the "DSX-3 Isolated Pulse Template Requirement" (per Bellcore GR-499-CORE), the user is advised to command this output pin to be "high" if the cable length (between the transmit output of the XRT7300 and the DSX-3 Cross Connect System) is greater than 225 feet. Conversely, the user is advised to command this output pin to be "low" if the cable length (between the transmit output of the XRT7300 and the DSX-3 Cross Connect System) is less than 225 feet. ***NOTE:*** *This output pin can be used for a variety of other purposes if the XRT7300 DS3/E3 LIU is not used.*

PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
181	RLOOP	O	**Remote Loopback Output Pin (to the XRT7300 DS3/E3 Line Interface Unit IC).** This output pin is intended to be connected to the RLOOP input pin of the XRT7300 DS3/E3 Line Interface Unit IC. The user can command this signal to toggle "high" and, in turn, force the XRT7300 DS3/E3 Line Interface Unit IC into the "Remote Loopback" mode. Conversely, the user can command this signal to toggle "low" and allow the XRT7300 to operate in the normal mode. (For a detailed description of the XR-T7300 DS3/E3 Line Interface Unit IC's operation during Remote Loopback, please see the XR-T7300 DS3/STS-1/ E3 Line Interface Unit IC's Data Sheet). Writing a "1" to bit 1 of the "Line Interface Drive Register (Address = 0x80) will cause this output pin to toggle "high". Writing a "0" to this bit-field will cause the RLOOP output to toggle "low". ***NOTE:*** *This output pin can be used for a variety of other purposes if the XRT7300 DS3/E3 LIU is not used.*
182	LLOOP	O	**Local Loopback Output Pin (to the XRT7300 DS3/E3 Line Interface Unit IC).** This output pin is intended to be connected to the LLOOP input pin of the XRT7300 LIU IC. The user can command this signal to toggle "high" and, in turn, force the LIU into the "Local Loopback" mode. (For a detailed description of the XRT7300 DS3/E3 Line Interface Unit IC's operation during Local Loopback, please see the XRT7300 DS3/STS-1/E3 Line Interface Unit IC's Data Sheet). Writing a "1" to bit 1 of the "Line Interface Drive Register (Address = 0x80) will cause this output pin to toggle "high". Writing a "0" to this bit-field will cause the RLOOP output to toggle "low". ***NOTE:*** *This output pin can be used for a variety of other purposes if the XRT7300 DS3/E3 LIU is not used.*
183	DMO	O	**"Drive Monitor Output" Input (from the XRT7300 DS3 Line Interface Unit IC).** This input pin is intended to be tied to the DMO output pin of the XRT7300 DS3 Line Interface Unit IC. The user can determine the state of this input pin by reading Bit 2 (DMO) within the Line Interface Scan Register (Address = 0x81). If this input signal is "high", then it means that the drive monitor circuitry (within the XRT7300 DS3 Line Interface Unit IC) has not detected any bipolar signals at the MTIP and MRING inputs within the last 128 ± 32 bit-periods. If this input signal is "low", then it means that bipolar signals are being detected at the MTIP and MRING input pins of the XRT7300. ***NOTE:*** *This output pin can be used for a variety of other purposes if the XRT7300 DS3/E3 LIU is not used.*

PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
184	RLOL	I	**Receive Loss of Lock Indicator - from the XRT7300 DS3/E3 Line Interface Unit IC.** This input pin is intended to be connected to the RLOL (Receive Loss of Lock) output pin of the XRT7300 Line Interface Unit IC. The user can monitor the state of this pin by reading the state of Bit 1 (RLOL) within the Line Interface Scan Register (Address = 0x81). If this input pin is "low", then it means that the "clock recovery phase-locked-loop" circuitry, within the XRT7300 is properly locked onto the incoming DS3 data-stream; and is properly recovering clock and data from this DS3 data-stream. However, if this input pin is "high", then it means that the phase-locked-loop circuitry, within the XRT7300 has lost lock with the incoming DS3 data-stream, and is not properly recovering clock and data. For more information on the operation of the XRT7300 DS3/E3 Line Interface Unit IC, please consult the "XRT7300 DS3/E3 Line Interface Unit" data sheet. ***NOTE:*** *This output pin can be used for a variety of other purposes if the XRT7300 DS3/E3 LIU is not used.*
185	ExtLOS	I	**Receive LOS (Loss of Signal) Indicator Input (from XRT7300 LIU IC).** This input pin is intended to be connected to the RLOS (Receive Loss of Signal) output pin of the XRT7300 Line Interface Unit IC. The user can monitor the state of this pin by reading the state of Bit 0 (RLOS) within the Line Interface Scan Register (Address = 0x81). If this input pin is "low", then it means that the XRT7300 is currently NOT declaring an "LOS (Loss of Signal) condition. However, if this input pin is "high", then it means that the XRT7300 is currently declaring an LOS (Loss of Signal) condition. For more information on the operation of the XR-T7300 DS3/E3 Line Receiver IC, please consult the "XRT7300 DS3/STS-1/E3 Line Interface Unit IC" data sheet. ***NOTE:*** *Asserting the RLOS input pin will cause the XRT72L13 M13 Multiplexer/Framer to declare an "LOS (Loss of Signal) condition. Therefore, this input pin should not be used as a general purpose input.*
186	VDD	****	**Power Supply Pin**
187	RxVCOup	O	**Receive VCO Frequency Increase:**
188	RxVCOdown	O	**Receive VCO Frequency Decrease:**
189	RxLineClk	I	**Receiver LIU (Recovered) Clock:** This input signal serves three purposes: The Receive Framer uses it to sample and "latch" the signals at the RxPOS and RxNEG input pins (into the Receive Framer circuitry). This input signal functions as the timing reference for the Receive Framer block. The Transmit Framer block can be configured to use this input signal as its timing reference. ***NOTE:*** *This signal is the recovered clock from the external DS3 LIU (Line Interface Unit) IC, which is derived from the incoming DS3 data.*

PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
190	RxPOS	I	**Receive Positive Data Input:** The exact role of this input pin depends upon whether the Framer is operating in the Unipolar or Bipolar Mode. Unipolar Mode: This input pin functions as the "Single-Rail" input for the "incoming" DS3 data stream. The signal at this input pin will be sampled and latched (into the Receive Framer block) on the "user-selected" edge of the RxLineClk signal. Bipolar Mode: This input functions as one of the dual rail inputs for the incoming AMI/B3ZS encoded DS3 data that has been received from an external Line Interface Unit (LIU) IC. RxNEG functions as the other dual rail input for the Framer. When this input pin is asserted, it means that the LIU has received a "positive polarity" pulse from the line.
191	RxNEG	I	**Receive Negative Data Input:** The exact role of this input pin depends upon whether the Framer is operating in the Unipolar or Bipolar Mode. Unipolar Mode: This input pin is inactive, and should be pulled ("low" or "high") when the Framer is operating in the Unipolar Mode. Bipolar Mode: This input pin functions as one of the dual rail inputs for the incoming AMI/B3ZS encoded DS3 data that has been received from an external Line Interface Unit (LIU) IC. RxPOS functions as the other dual rail input for the Framer. When this input pin is asserted, it means that the LIU has received a "negative polarity" pulse from the line.
192	RxOH	O	**Receive Overhead Output Port:** All overhead bits, which are received via the "Receive Section" of the Framer IC; will be output via this output pin, upon the rising edge of RxOHClk.
193	RxOHEnable	O	**Receive Overhead Enable Indicator:** The XRT72L13 will assert this output signal for one “RxOutClk” period when it is safe for the Terminal Equipment to sample the data on the “RxOH” output pin.
194	RxOHClk	O	**Receive Overhead Clock:** The XRT72L13 will output the Overhead bits (within the incoming DS3 frames), via the "RxOH" output pin, upon the falling edge of this clock signal. As a consequence, the "user's data link equipment" should use the rising edge of this clock signal to sample the data on both the "RxOH" and "RxOHFrame" output pins. ***NOTE:*** *This clock signal is always active.*
195	RxOHFrame	O	**Receive Overhead Frame Boundary Indicator:** This output pin pulses "high" whenever the Receive Overhead Data Output Interface outputs the first overhead bit (or nibble) of a new DS3 frame.
196	RxLOS	O	**Receive Section - Loss of Signal Output Indicator:** This pin is asserted when the Receive Section encounters a string of 180 consecutive 0's via the RxPOS and RxNEG pins. This pin will be negated once the Receive Section has detected at least 60 pulses within 180 bit-periods.

PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
197	RxNib_3/ RxRed	O	**Receive Nibble Output - Bit 3/Receive Red Alarm Indicator:** The funtion of this output pin depends upon whether the XRT72L13 is operating in the “Clear-Channel Framing/Nibble-Parallel” Mode or not.. **Clear Channel Framer Applications - Receive Nibble Output - Bit 3** The Framer IC will output "Received data (from the Remote Terminal) to the local Terminal Equipment via this pin along with RxNib0, RxNib1 and RxNib2. The data at this pin is updated on the rising edge of the RxClk output signal. ***NOTE:*** *This output pin is active only if the Nibble-Parallel Mode has been selected.* **All other Modes - Receiver Red Alarm Indicator:** The Framer asserts this output pin to denote that one of the following events has been detected by the Receive Framer: • LOS - Loss of Signal Condition • OOF - Out of Frame Condition • AIS - Alarm Indication Signal Detection
198	RxNib_2/RxAIS	O	**Receive Nibble Output - Bit 2/Receive AIS Condition Indicator:** The funtion of this output pin depends upon whether the XRT72L13 is operating in the “Clear-Channel-Framing/Nibble-Parallel” Modes or not. **Clear-Channel Framing/Nibble-Parallel Modes - Receive Nibble Output - Bit 2** The Framer IC will output "Received data (from the Remote Terminal) to the local Terminal Equipment via this pin along with RxNib0, RxNib1 and RxNib2. The data at this pin is updated on the rising edge of the RxClk output signal. **All other Modes - Receive "Alarm Indication Signal" Output pin:** The Framer will assert this pin to indicate that the Alarm Indication Signal (AIS) has been identified in the Receive DS3 data stream. An "AIS" is detected if the payload consists of the recurring pattern of 1010... and this pattern persists for 63 M-frames. An additional requirement for AIS indication is that the C-bits are set to 0, and the X-bits are set to 1. This pin will be negated when a sufficient number of frames, not exhibiting the "1010..." pattern in the payload has been detected.

PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
199	RxNib_1/RxOOF	O	**Receive Nibble Output - Bit 1/Receive "Out-Of-Frame" Indicator:** The funtion of this output pin depends upon whether the XRT72L13 is operating in the "Clear-Channel-Framing/Nibble-Parallel" Mode or not. **Clear-Channel Framing/Nibble-Parallel Mode - Receive Nibble Output - Bit 1:** The Framer IC will output "Received data (from the Remote Terminal) to the local Terminal Equipment via this pin along with RxNib0, RxNib2 and RxNib3. The data at this pin is updated on the rising edge of the RxClk output signal. **All other Modes - Receiver "Out of Frame" Indicator:** The Receive Section of the XRT72L13 M13 Multiplexer/Framer IC will assert this output signal whenever it has declared an "Out of Frame" (OOF) condition with the incoming DS3 frames. This signal is negated when the framer correctly locates the framing alignment bits or bytes and correctly aligns itself with the incoming DS3 frames.
200	GND	****	**Ground Pin**
201	RxNib_0/RxSer	O	**Receive Nibble Output -Bit 0/Receive Serial Output:** The funtion of this output pin depends upon whether the XRT72L13 is operating in the "Clear-Channel-Framing/Nibble-Parallel" Mode or in the "Clear-Channel-Framing/Serial" Modes **Clear-Channel Framing/Nibble-Parallel Mode - Receive Nibble Output - Bit 0:** The Framer IC will output "Received data (from the Remote Terminal) to the local Terminal Equipment via this pin along with RxNib1, RxNib2 and RxNib3. The data at this pin is updated on the rising edge of the RxClk output signal. ***NOTE:*** *In this case, the RxClk output signal is approximately 11.184MHz* **Clear-Channel Framing/Serial Mode Receive Serial Output;** The Framer IC will output "Received data (from the Remote Terminal) to the local Terminal Equipment via this pin. The data at this pin is updated on the "selected" edge of the RxClk output pin. ***NOTES:*** 1. *For "Serial-Mode" applications, the "RxClk" output signal is 44.736MHz.* 2. *If the XRT72L13 is operating in the "Channelized" or "High-Speed HDLC Controller" modes, then this output pin is in-active.*
202	RxOutClk	O	**Receive Out Clock - Transmit Terminal Interface Clock for Loop-Timing:** This clock signal functions as the "Terminal Interface" clock source, if the XRT72L13 M13 Multiplexer/Framer IC is operating in the "loop-timing" mode. In this mode, the Transmitting Terminal Equipment is expected to input data to the Framer IC, via the TxSer input pin, upon the rising edge of this clock signal. The XRT72L13 will use the rising edge of this clock signal to sample the data at the TxSer input. This clock signal is a buffered version of the RxLineClk signal.

PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
203	RxOHInd/ RxPLClkEnb	O	**Receive Overhead Bit Indicator:** This output pin pulses "high" whenever an "overhead" bit is being output via the "RxSer" output pin, by the "Receive Payload Data Output Interface" block. The purpose of this output pin is to alert the "Receive Terminal Equipment" that an overhead bit is being output via the "RxSer" output pin, and that this data should be ignored.
204	RxClk	O	**Receive Clock Output Signal for Serial and Nibble/Parallel Data Interface:** The exact behavior of this signal depends upon whether the XRT72L13 is operating in the “Clear-Channel-Framing/Serial” or “Clear-Channel-Framing/Nibble-Parallel” Modes. **Clear-Channel Framing - Serial Mode Operation:** In the "serial" mode, this signal is a 44.736MHz clock output signal. The Receive Payload Data Output Interface will update the data via the RxSer output pin, upon the rising edge of this clock signal. The user is advised to design (or configure) the Terminal Equipment to sample the data on the "RxSer" pin, upon the falling edge of this clock signal. **Clear-Channel Framing - Nibble-Parallel Mode Operation** In this Nibble-Parallel Mode, the XRT72L13 will derive this clock signal, from the RxLineClk signal. The XRT72L13 will pulse this clock signal 1176 times for each "inbound" DS3 frame. The Receive Payload Data Output Interface will update the data, on the "RxNib[3:0]" output pins upon the falling edge of this clock signal. The user is advised to design (or configure) the Terminal Equipment to sample the data on the "RxNib[3:0] output pins, upon the rising edge of this clock signal
205	RxFrame	O	**Receive Boundary of DS3 Frame Output Indicator:** The funtion of this output pin depends upon whether the XRT72L13 Framer IC is operating in the “Clear-Channel-Framing/Serial” or “Clear-Channel-Framing/Nibble-Parallel” Modes. **Clear-Channel Framing - Serial Mode Operation** The Receive Section of the XRT72L13 will pulse this output pin “high” (for one bit-period) when the “Receive Payload Data Output Interface” block is driving the very first bit of a given given DS3 frame, onto the “RxSer” output pin. **Clear-Channel Framing -Nibble-Parallel Operation** The Receive Section of the XRT72L13 will pulse this output pin “high” (for one nibble-period), when the “Receive Payload Data Output Interface” block is driving the very first nibble of a given DS3 frame, onto the “RxNib[3:0] output pins.
206	RxInClk	I	**Receive Input Clock:**
207	RxDS1Data_27	O	**Receive DS1 Data Output - Channel 27:** This pin outputs a DS1 signal from the M12 multiplexer. Each bit, within the DS1 data stream is output upon the rising edge of RxDS1Clk_27. ***NOTES:*** 1. *This output pin is inactive if the corresponding M12 DEMUX is de-multiplexing an ITU-T G.747 data stream.* 2. *This pin will output the contents of DS2 channel # 7, if M12 MUX # 7 is bypassed.*

PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
208	RxDS1Clk_27	O	**Receive DS1 Clock Output - Channel 27:** This pin outputs either a DS1 (1.544MHz) clock signal to the Terminal Equipment. The XRT72L13 will update the data on the "RxDS1Data_27" line, upon the rising edge of this signal. ***NOTES:*** 1. *This output pin is inactive if the corresponding M12 DEMUX is de-multiplexing an ITU-T G.747 data stream.* 2. *This pin will output a DS2 rate clock signal (6.312MHz) if M12 # 7 is bypassed.*

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUMS

ABSOLUTE MAXIMUM RATINGS:

Power Supply..... -0.5V to +3.465V	Power Dissipation PQFP Package..... ???W
Storage Temperature .....-65°C to 150°C	Input Voltage (Any Pin) .....-0.5V to VDD + 0.5V
Voltage at Any Pin ..... -0.5V to VDD + 0.5V	Input Current (Any Pin) ..... ± 100mA

DC ELECTRICAL CHARACTERISTICS

Test Conditions: TA = 25(C, VCC = 3.3V ± 5% unless otherwise specified

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
I_{CC}	Power Supply Current		180		mA	
I_{LL}	Data Bus Tri-State Bus Leakage Current		TBD		µA	
V_{IL}	Input Low voltage			0.8	V	
V_{IH}	Input High Voltage	2.0		VCC	V	
V_{OL}	Output Low Voltage	0.0		0.4	V	
V_{OH}	Output High Voltage	2.4		VCC	V	
I_{OC}	Open Drain Output Leakage Current		TBD		µA	
I_{IH}	Input High Voltage Current		TBD		µA	V_{IH} = VCC
I_{IL}	Input Low Voltage Current		TBD		µA	V_{IL} = GND

AC ELECTRICAL CHARACTERISTICS

Test Conditions: TA = 25(C, VCC = 3.3V ± 5% unless otherwise specified

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Transmit Payload Data Input Interface - Loop-Timed/Serial Mode (See Figure 2)						
t_1	Payload data (TxSer) set-up time to rising edge of RxOutClk	6			ns	
t_2	Payload data (TxSer) hold time, from rising edge of RxOutClk	0			ns	
t_3	RxOutClk to TxFrame output delay			8	ns	
t_4	RxOutClk to TxOHInd output delay			8	ns	
Transmit Payload Data Input Interface - Local Timed/Serial Mode (See Figure 3)						
t_5	Payload data (TxSer) set-up time to rising edge of "TxInClk"	0			ns	
t_6	Payload data (TxSer) hold time, from rising edge of "TxInClk"	2.5			ns	
t_7	"TxFrameRef" set-up time to rising edge of "TxInClk"	0			ns	Framer IC is "Frame Slave"

AC ELECTRICAL CHARACTERISTICS

Test Conditions: TA = 25(C, VCC = 3.3V ± 5% unless otherwise specified						
SYMBOL	**PARAMETER**	**MIN.**	**TYP.**	**MAX.**	**UNITS**	**CONDITIONS**
t_8	"TxFrameRef" hold-time, from rising edge of "TxInClk"	2.3			ns	Frame IC is "Frame Slave"
t_9	"TxInClk" to "TxOHInd" output delay			14	ns	
t_{10}	"TxInClk" to "TxFrame" output delay			14	ns	
Transmit Payload Data Input Interface - Looped-Timed/Nibble Mode (See Figure 4)						
t_{11}	Payload data set-up time to "latching edge" of RxOutClk	6			ns	
Transmit Payload Data Input Interface - Looped-Timed/Nibble Mode (See Figure 4)						
t_{12}	Payload data hold time, from "latching edge" of RxOutClk	0				
t_{13}	TxNibClk to TxNibFrame output delay			8	ns	
Transmit Payload Data Input Interface - Local-Timed/Nibble Mode (See Figure 5)						
t_{14}	Payload Nibble set-up time, to "latching edge" of "TxInClk"	0			ns	
t_{15}	Payload Nibble hold time, from "latching edge" of "TxInClk"	15			ns	
t_{16}	TxFrameRef set-up time, to "latching edge" of "TxInClk"	0			ns	Frame IC is "Frame Slave"
t_{17}	TxFrameRef hold time, from "latching edge" of "TxInClk"	15			ns	Frame IC is "Frame Slave"
t_{18}	"TxNibClk" to "TxNibFrame" output delay time	21			ns	

AC ELECTRICAL CHARACTERISTICS (CONT.)

Test Conditions: TA = 25(C, VCC = 3.3V ± 5% unless otherwise specified						
SYMBOL	**PARAMETER**	**MIN.**	**TYP.**	**MAX.**	**UNITS**	**CONDITIONS**
Transmit Overhead Input Interface Timing - Method 1 (see Figure 6)						
t_{21}	"TxOHClk" to "TxOHFrame" output delay			0	ns	
t_{22}	"TxOHIns" set-up time, to falling edge of "TxOHClk"	0			ns	
t_{23}	"TxOHIns" hold time, from falling edge of "TxOHClk"	0			ns	
t_{24}	"TxOH" data set-up time, to falling edge of "TxOHClk"	0			ns	
t_{25}	"TxOH" data hold time, from falling edge of "TxOHClk"	0			ns	
Transmit Overhead Data Input Interface - Method 2 (see Figure 7)						
t_{26}	“TXOHIns” to “TxInClk” (rising edge) set-up Time	0			ns	
t_{27}	TxInClk clock rising edge to “TxOHIns” hold-time	0			ns	

AC ELECTRICAL CHARACTERISTICS (CONT.)

Test Conditions: TA = 25(C, VCC = 3.3V ± 5% unless otherwise specified

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_{28}	"TXOH" to "TxInClk" rising edge set-up Time	0			ns	
t_{29A}	TxInClk to "TxOHEnable"			8	ns	
Transmit LIU Interface Timing (see Figure 8 and Figure 9)						
t_{30}	Rising edge of "TxLineClk" to rising edge of "TxPOS" or "TxNEG" output signal. (Framer is configured to output data on "TxPOS" and "TxNEG" on rising edge of "TxLineClk"			0.6	ns	
t_{31}	Falling edge of "TxLineClk" to rising edge of "TxPOS" or "TxNEG" (Framer is configured to output data via "TxPOS" and "TxNEG" on falling edge of "TxLineClk")			0.6	ns	
$f_{TxLineClk}$	Period of TxLineClk clock signal		44.736		MHz	
t_{32}	Period of TxLineClk		22.36		ns	
Receive LIU Interface Timing (see Figure 10 and Figure 11)						
t_{38}	"RxPOS" or "RxNEG" set-up time to rising edge of "RxLineClk". (Framer is configured to sample data on "RxPOS" and "RxNEG" input pins, on the rising edge of "RxLineClk")	0			ns	
t_{39}	"RxPOS" or "RxNEG" hold time, from rising edge of "RxLineClk" (Framer is configured to sample data on "RxPOS" and "RxNEG" input pins, on the rising edge of "RxLineClk")	2.4			ns	
t_{40}	"RxPOS" or "RxNEG" set-up time to falling edge of "RxLineClk". (Framer is configured to sample data on "RxPOS" and "RxNEG" input pins, on the falling edge of "RxLineClk")	0			ns	
t_{41}	"RxPOS" or "RxNEG" hold time, from falling edge of "RxLineClk" (Framer is configured to sample data on "RxPOS" and "RxNEG" input pins, on the falling edge of "RxLineClk")	2.4			ns	
Receive Payload Data Output Inteface Timing - Serial Mode Operation (See Figure 12)						
t_{50}	Falling edge of RxClk to "Payload Data" (RxSer) output delay			0	ns	
t_{51}	Falling edge of "RxClk" to "RxFrame" output delay			1.3	ns	
t_{52}	Falling edge of "RxClk" to "RxOHInd" output delay.			2.6	ns	
Receive Payload Data Output Interface Timing - Nibble Mode Operation (see Figure 13)						
t_{53}	Falling edge of "RxClk" to rising edge of "RxFrame" output delay			22	ns	

AC ELECTRICAL CHARACTERISTICS (CONT.)

Test Conditions: TA = 25(C, VCC = 3.3V ± 5% unless otherwise specified						
SYMBOL	**PARAMETER**	**MIN.**	**TYP.**	**MAX.**	**UNITS**	**CONDITIONS**
t_{54}	Falling edge of “RxClk” to rising edge of “RxNib[3:0]” output delay			22	ns	
Receive Overhead Data Output Interface Timing - Method 1 - Using RxOHEnable (see)Figure 14						
t_{59A}	Falling edge of “RxOHClk” to “RxFrame” output			0	ns	
t_{59B}	Falling edge of “RxOHClk” to “RxOH” output delay			21.3	ns	
Receive Overhead Data Output Interface Timing - Method 2 - Using RxOHEnable (see Figure 15)						
t_{60}	Rising edge of "RxOutClk" to rising edge of "RxOHEnable" delay.			5.5	ns	
t_{60A}	Falling edge of "RxOHFrame" to rising edge of "RxOHEnable" delay			0	ns	
t_{60B}	“RxOH” Data Valid to rising edge of "RxOHEnable" delay				ns	
Microprocessor Interface - Intel (See Figure 16)						
t_{64}	A8 - A0 Setup Time to ALE_AS Low	1			ns	
t_{65}	A8 - A0 Hold Time from ALE_AS Low.	2			ns	
Intel Type Read Operations (See Figure 16)						
t_{66}	RDS_$\overline{DS}$, WRB_$\overline{RW}$ Pulse Width	80			ns	
t_{67}	Data Valid from RDS_$\overline{DS}$ Low.	20			ns	
t_{68}	Data Bus Floating from RDS_$\overline{DS}$ High			1.0	ns	
t_{69}	ALE to $\overline{RD}$ Time	20			ns	
t_{701}	$\overline{RD}$ Time to "NOT READY" (e.g., Rdy_Dtck toggling "Low")	12			ns	
t_{70}	$\overline{RD}$ to READY Time (e.g., Rdy_Dtck toggling "high")	65			ns	
Intel Type Read Burst Operations (see Figure 18)						
t_{76}	Minimum Time between Read Burst Access (e.g., the rising edge of $\overline{RD}$ to falling edge of $\overline{RD}$)	60			ns	
Intel Type Write Operations (see Figure 17 and Figure 19)						
t_{71}	Data Setup Time to $\overline{WR}$_$\overline{RW}$ High	70			ns	
t_{72}	Data Hold Time from $\overline{WR}$_$\overline{RW}$ High	10			ns	
t_{73}	High Time between Reads and/or Writes	60			ns	
t_{74}	ALE to $\overline{WR}$ Time	20			ns	
t_{77}	Min Time between Write Burst Access (e.g., the rising edge of $\overline{WR}$ to the falling edge of $\overline{WR}$)	60			ns	
t_{770}	$\underline{CS}$ Assertion to falling edge of WR_RW	40			ns	
Microprocessor Interface - Motorola Read Operations (See Figure 20)						

AC ELECTRICAL CHARACTERISTICS (CONT.)

Test Conditions: TA = 25(C, VCC = 3.3V ± 5% unless otherwise specified

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_{78}	A8 - A0 Setup Time to falling edge of ALE_AS	5			ns	
t_{79}	A8 - A0 risinfg edge of $\overline{RD}$_DS to rising edge of RDY_DTCK delay	0			ns	
t_{80}	Rising edge of RDY_DTCK to tri-state of D[7:0]	0			ns	
Microprocessor Interface - Motorola Write Operations (See Figure 21)						
t_{78}	A8 -A0 Set-up time to falling edge of ALE_AS	5				
t_{81}	D[7:0] Set-up time to falling edge of $\overline{RD}$_DS	10			ns	
t_{82}	Rising edge of $\overline{RD}$_DS to rising edge of RDY_DTCK	0			ns	
Reset Pulse Width - Both Motorola and Intel Operations (See Figure 24)						
t_{90}	$\overline{Reset}$ pulse width	200			ns	

FIGURE 2. TIMING DIAGRAM FOR TRANSMIT PAYLOAD INPUT INTERFACE, WHEN THE XRT72L13 IS OPERATING IN BOTH THE DS3 AND LOOP-TIMING MODES

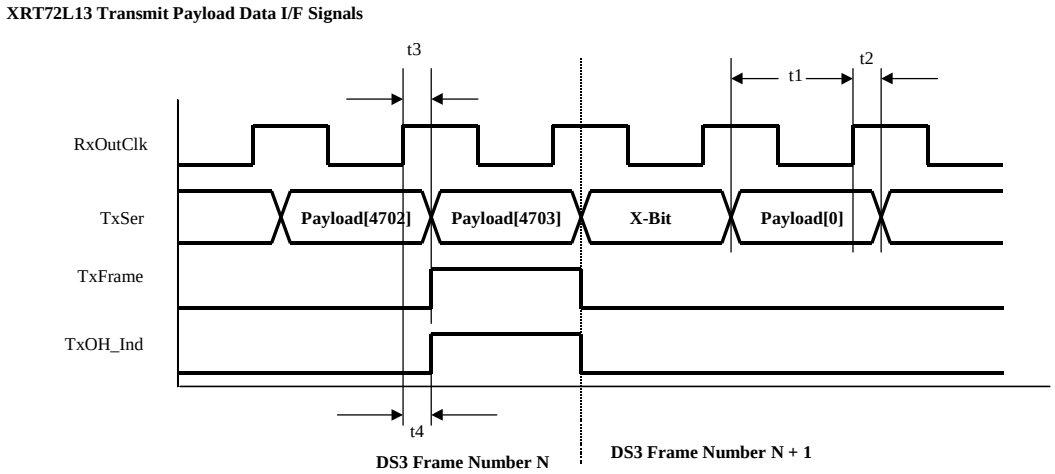

FIGURE 3. TIMING DIAGRAM FOR THE TRANSMIT PAYLOAD INPUT INTERFACE, WHEN THE XRT72L13 IS OPERATING IN BOTH THE DS3/SERIAL AND LOCAL-TIMING MODES

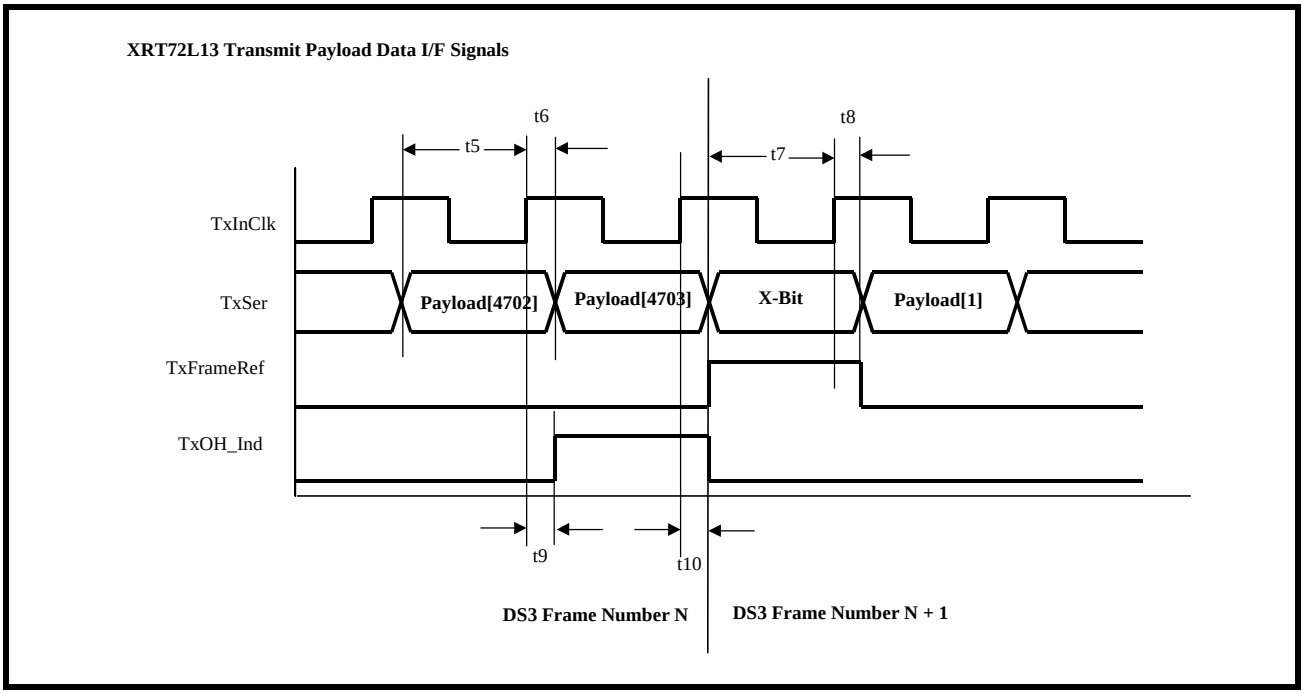

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FIGURE 4. TIMING DIAGRAM FOR THE TRANSMIT PAYLOAD DATA INPUT INTERFACE, WHEN THE XRT72L13 IS OPERATING IN BOTH THE DS3/NIBBLE AND LOOPED-TIMING MODES

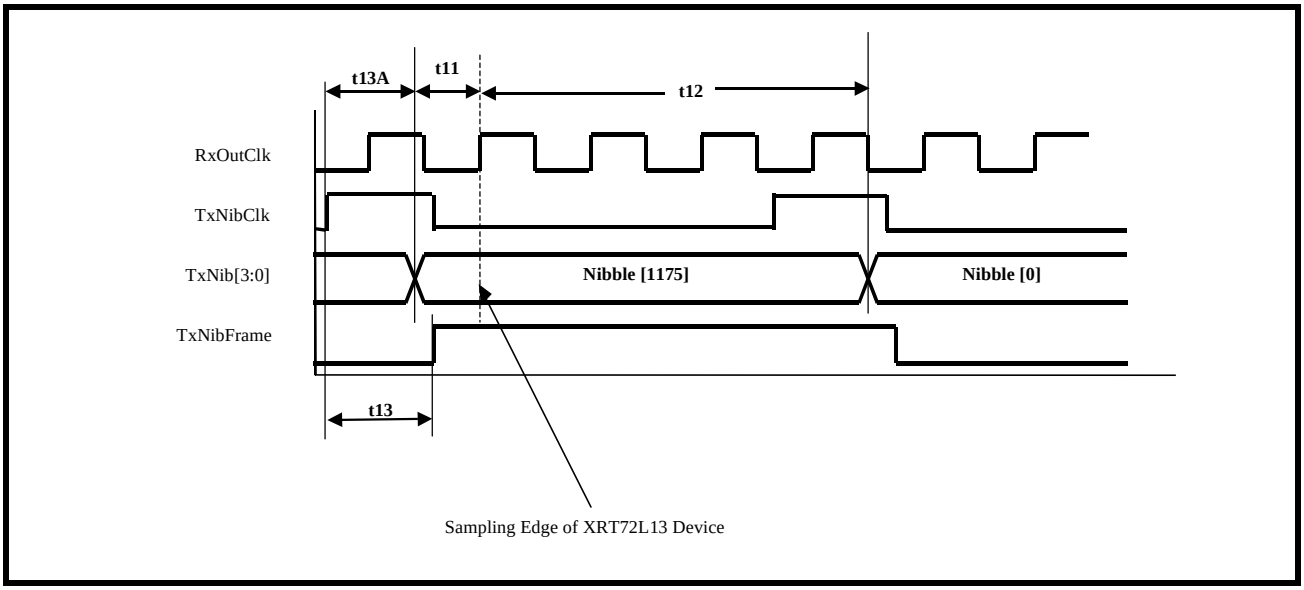


FIGURE 5. TIMING DIAGRAM FOR THE TRANSMIT PAYLOAD DATA INPUT INTERFACE, WHEN THE XRT72L13 IS OPERATING IN THE DS3/NIBBLE AND LOCAL-TIMING MODES

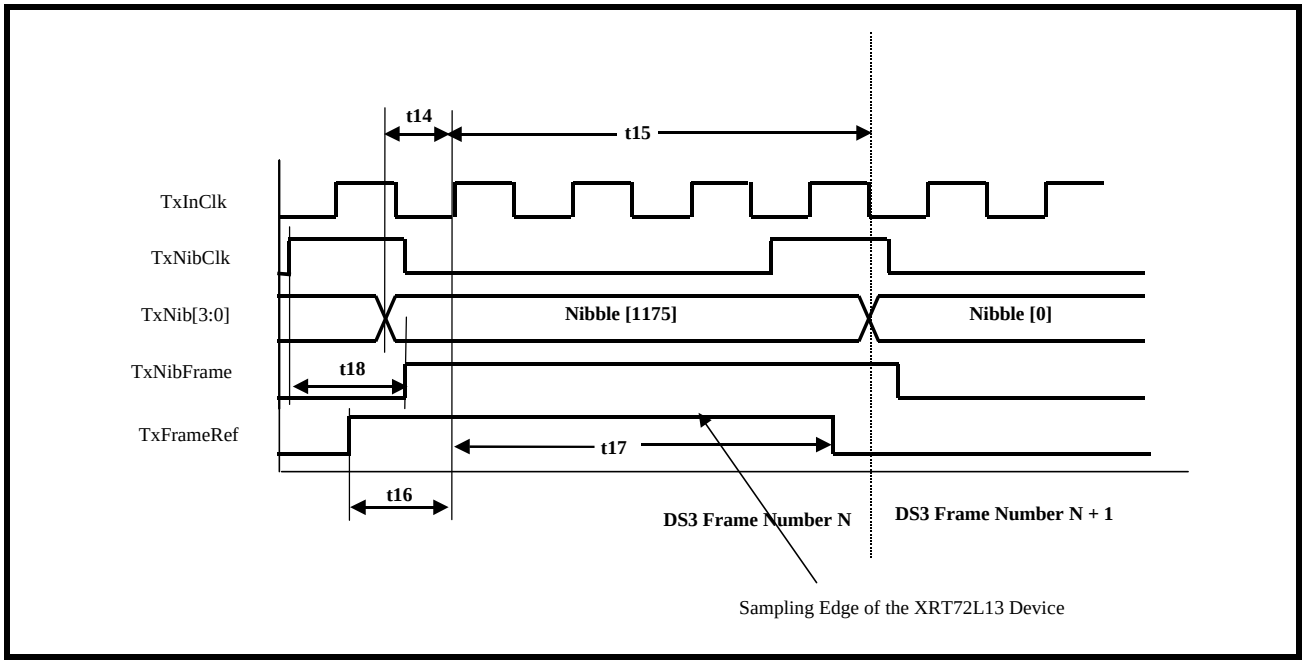


FIGURE 6. TIMING DIAGRAM FOR THE TRANSMIT OVERHEAD DATA INPUT INTERFACE (METHOD 1 ACCESS)

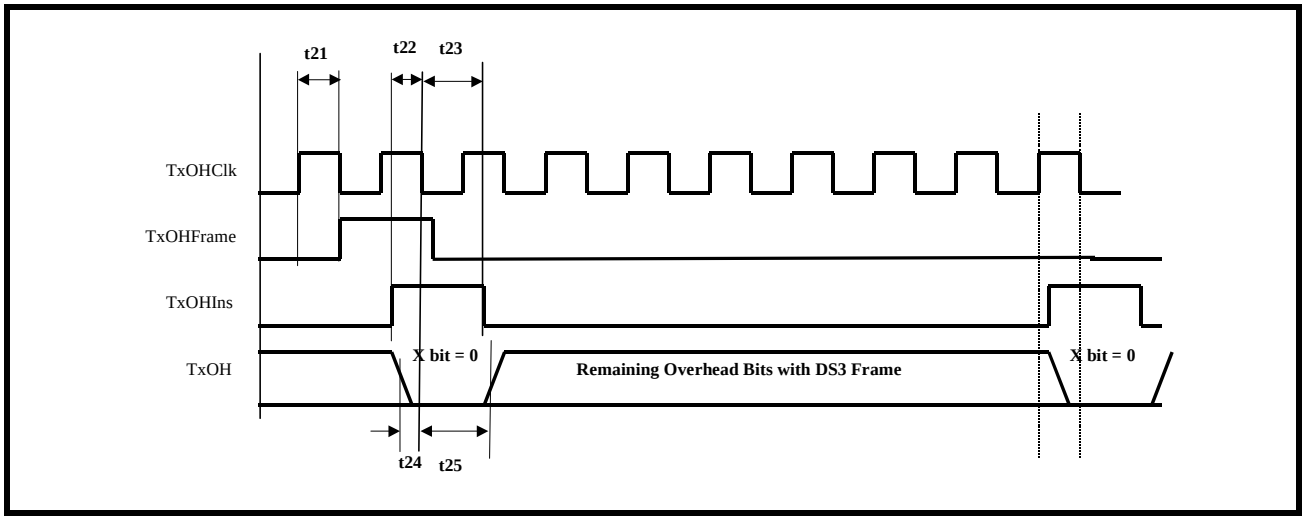


FIGURE 7. TIMING DIAGRAM FOR THE TRANSMIT OVERHEAD DATA INPUT INTERFACE (METHOD 2 ACCESS)

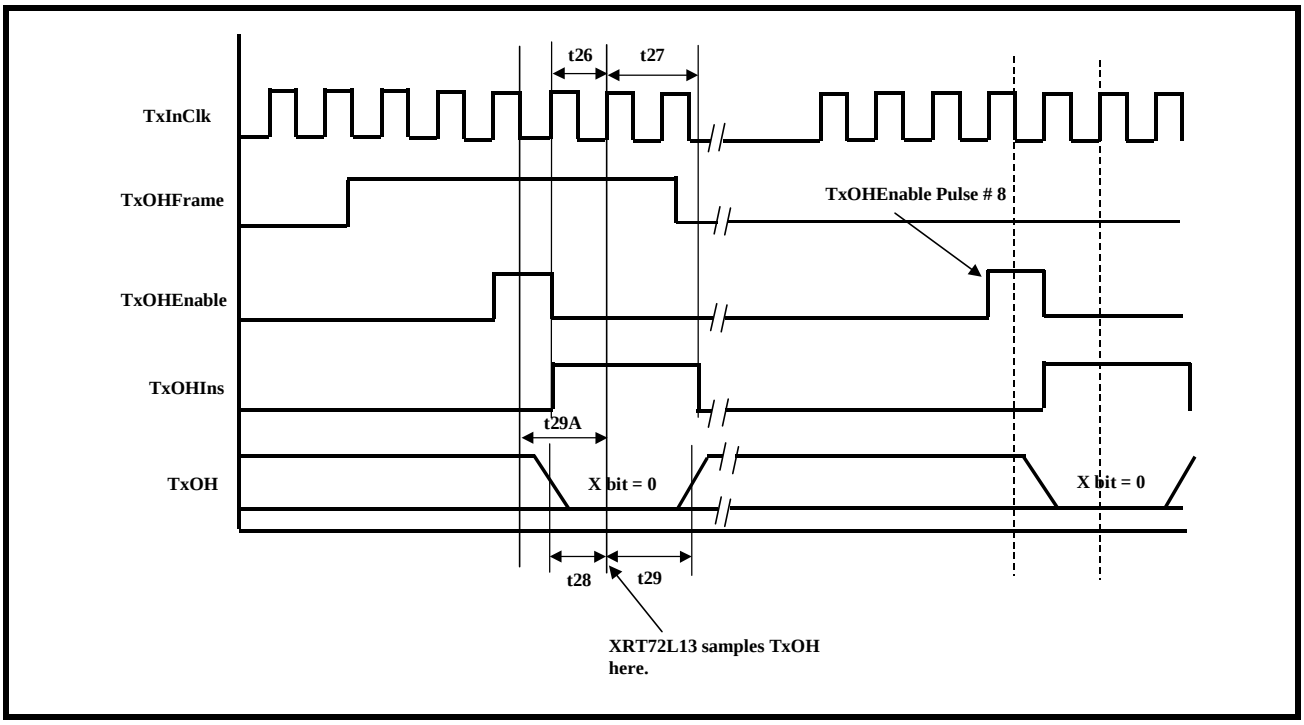


FIGURE 8. TRANSMIT LIU INTERFACE TIMING - FRAMER IS CONFIGURED TO UPDATE "TXPOS" AND "TXNEG" ON THE RISING EDGE OF "TXLINECLK"

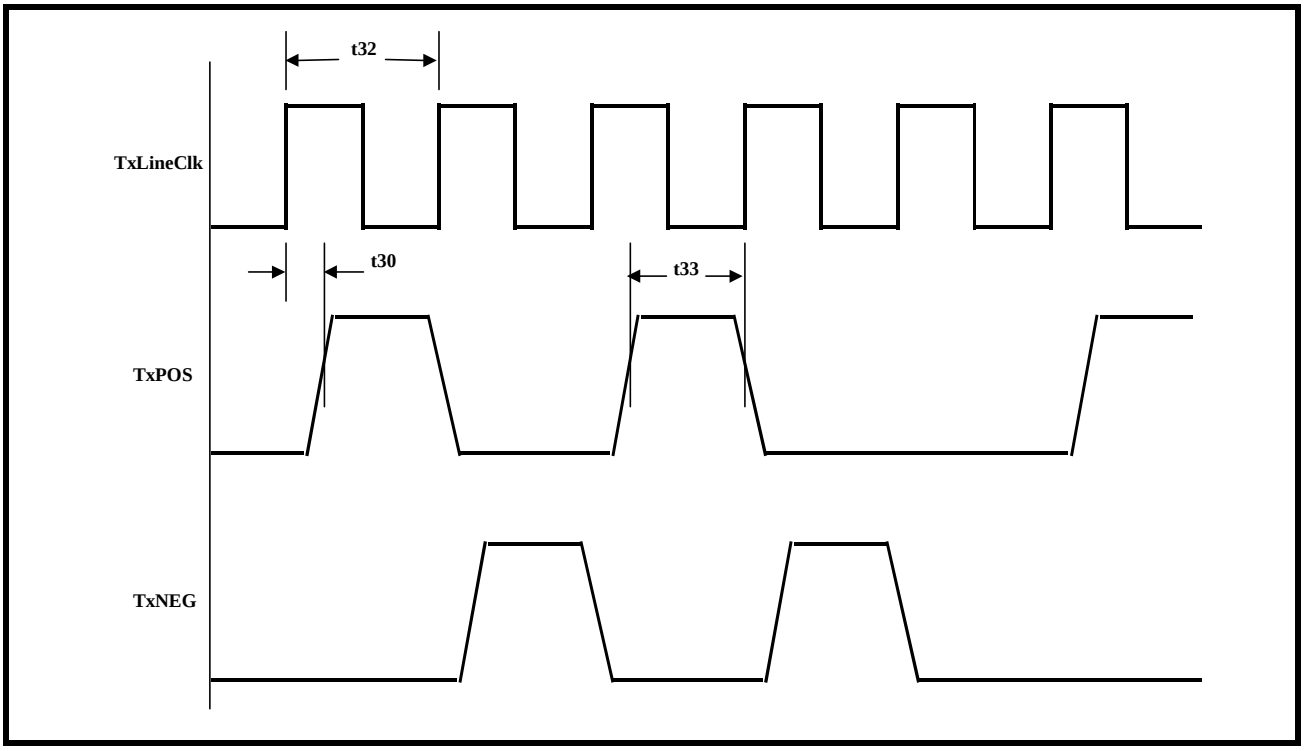


FIGURE 9. TRANSMIT LIU INTERFACE TIMING - FRAMER IS CONFIGURED TO UPDATE "TXPOS" AND "TXNEG" ON THE FALLING EDGE OF "TXLINECLK"

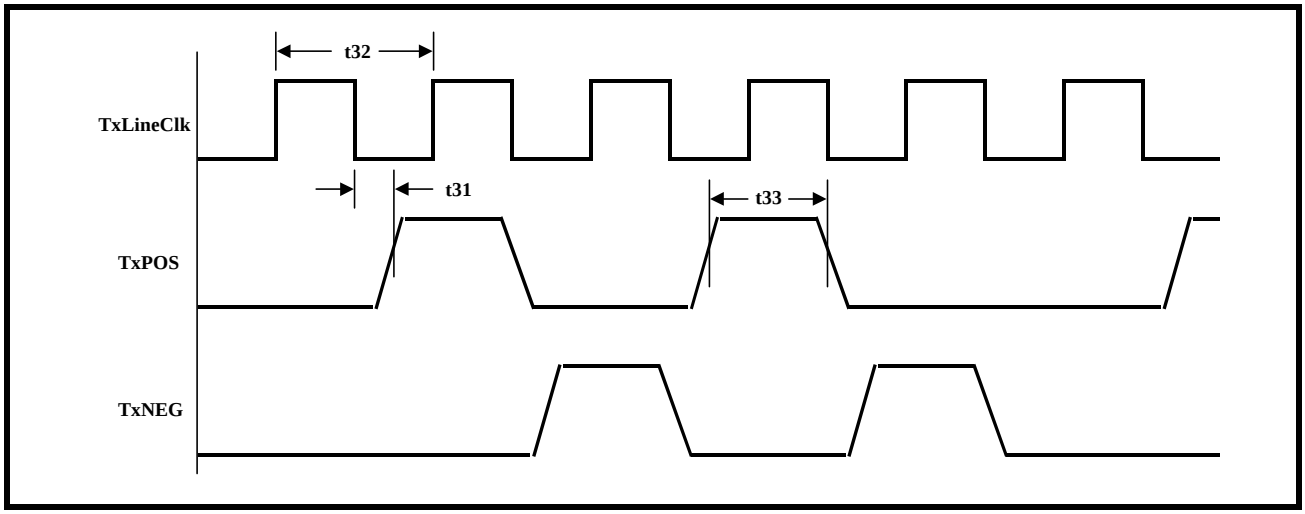


FIGURE 10. RECEIVE LIU INTERFACE TIMING - FRAMER IS CONFIGURED TO SAMPLE "RXPOS" AND "RXNEG" ON THE RISING EDGE OF "RXLINECLK"

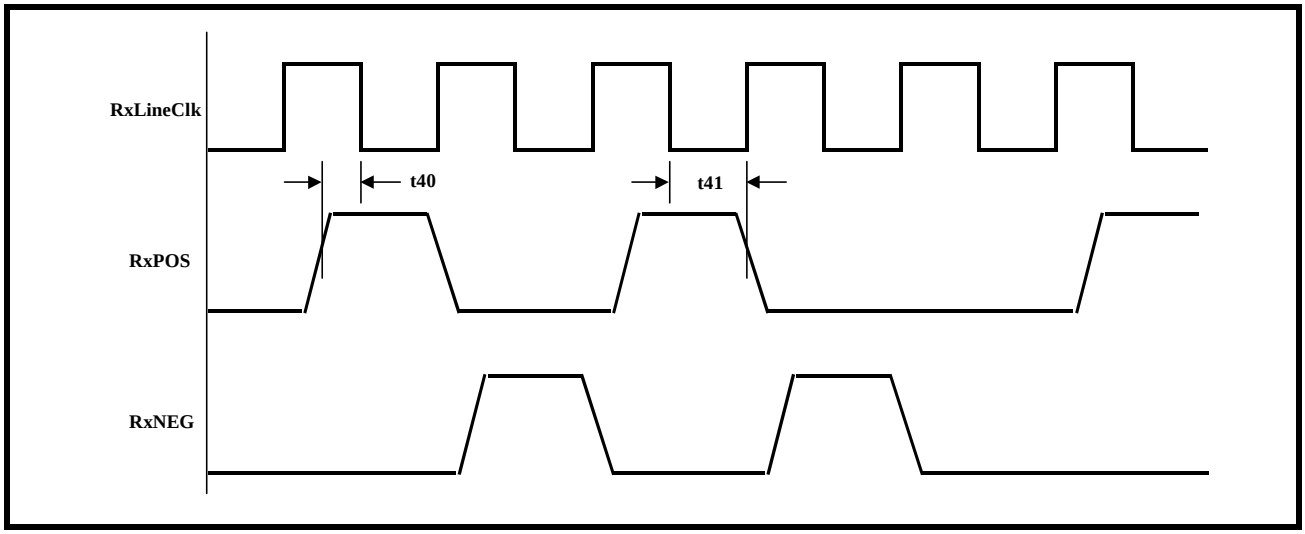


FIGURE 11. RECEIVER LIU INTERFACE TIMING - FRAMER IS CONFIGURED TO SAMPLE "RXPOS" AND "RXNEG" ON THE FALLING EDGE OF "RXLINECLK"

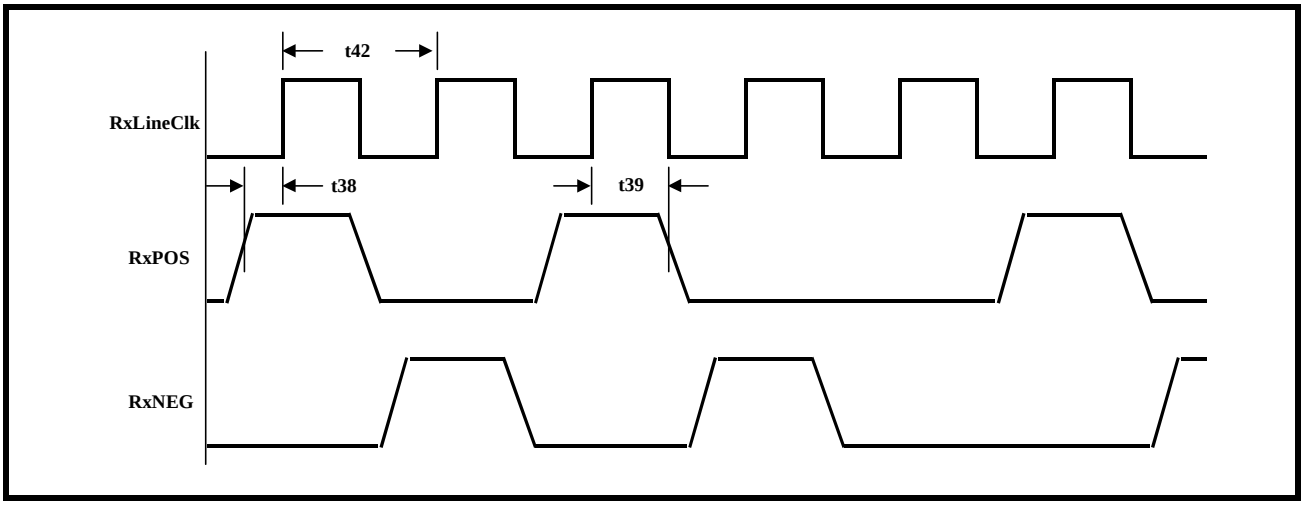


FIGURE 12. RECEIVE PAYLOAD DATA OUTPUT INTERFACE TIMING (SERIAL MODE OPERATION)

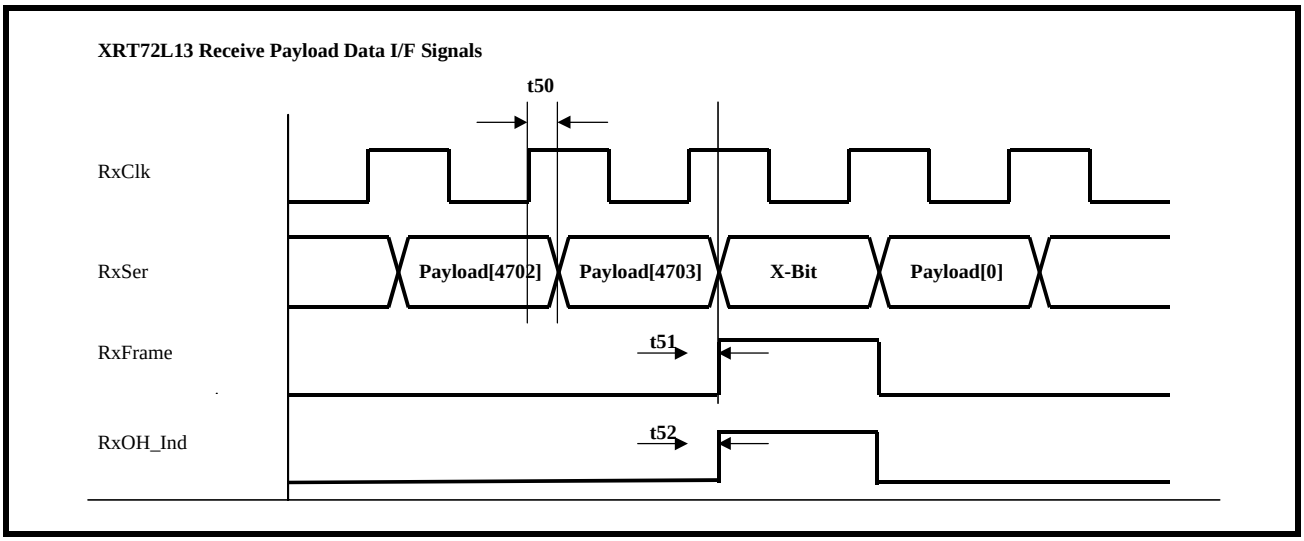


FIGURE 13. RECEIVE PAYLOAD DATA OUTPUT INTERFACE TIMING (NIBBLE MODE OPERATION)

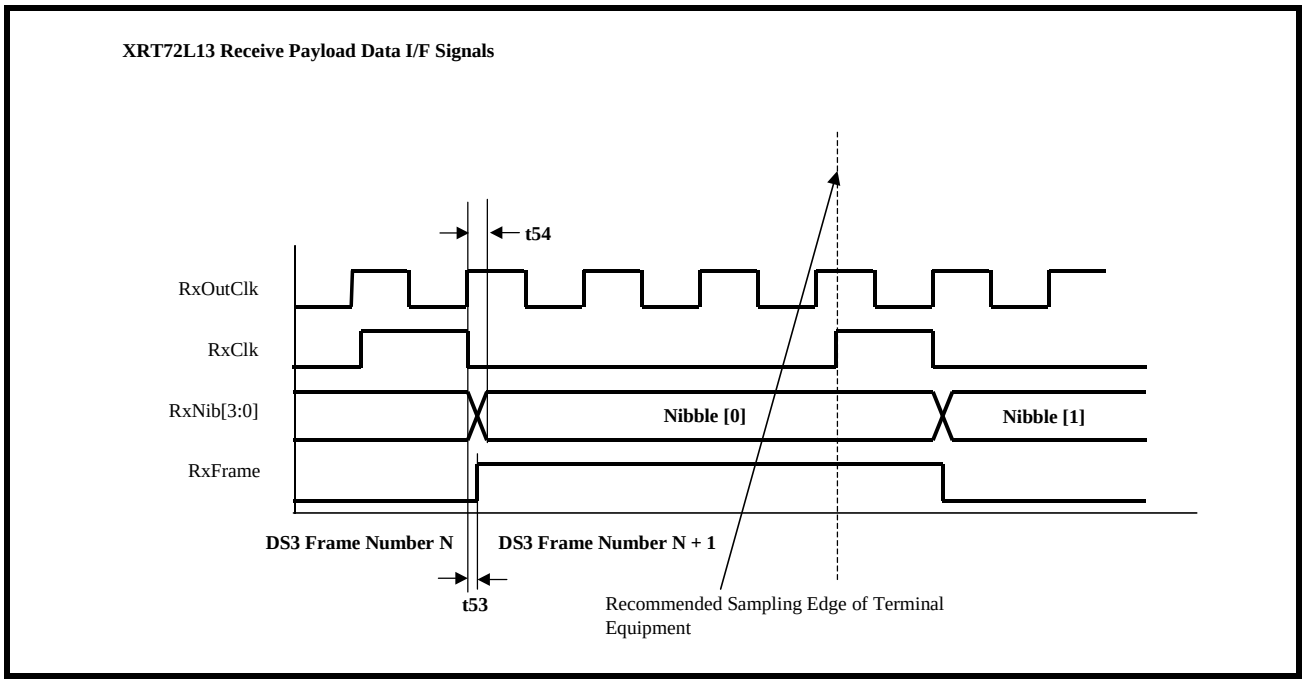


FIGURE 14. RECEIVE OVERHEAD DATA OUTPUT INTERFACE TIMING (METHOD 1 - USING RXOHCLK)

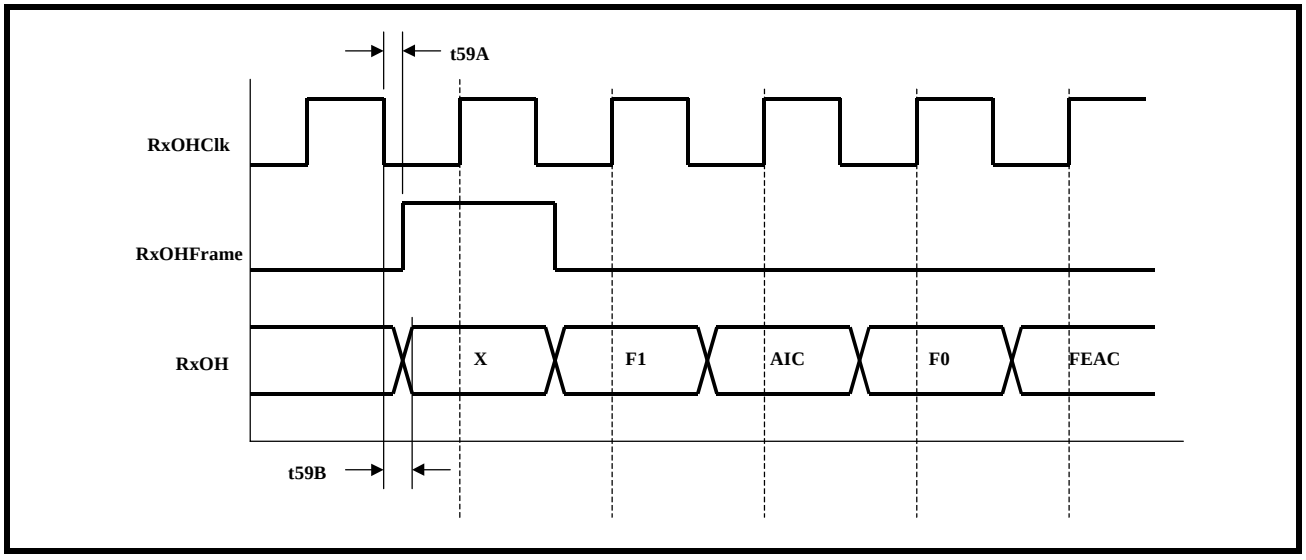


FIGURE 15. RECEIVE OVERHEAD DATA OUTPUT INTERFACE TIMING (METHOD 2 - USING RXOHENABLE)

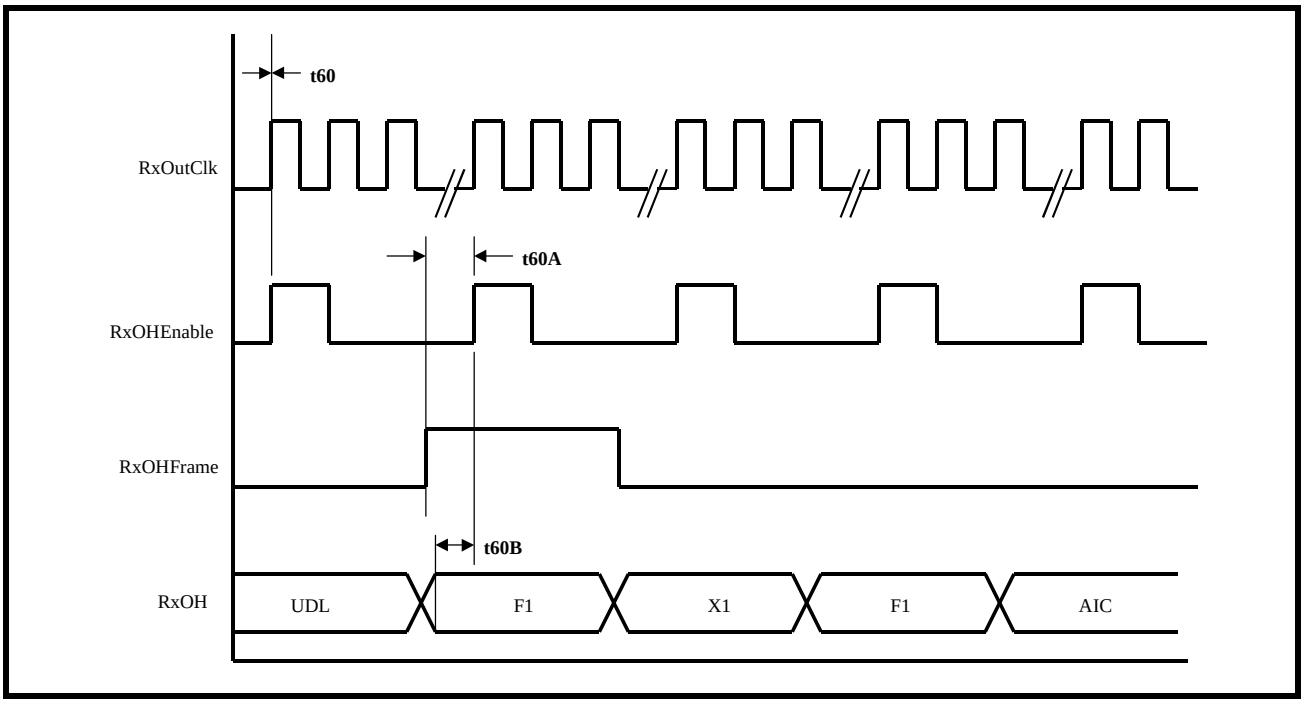


FIGURE 16. MICROPROCESSOR INTERFACE TIMING - INTEL TYPE PROGRAMMED I/O READ OPERATIONS

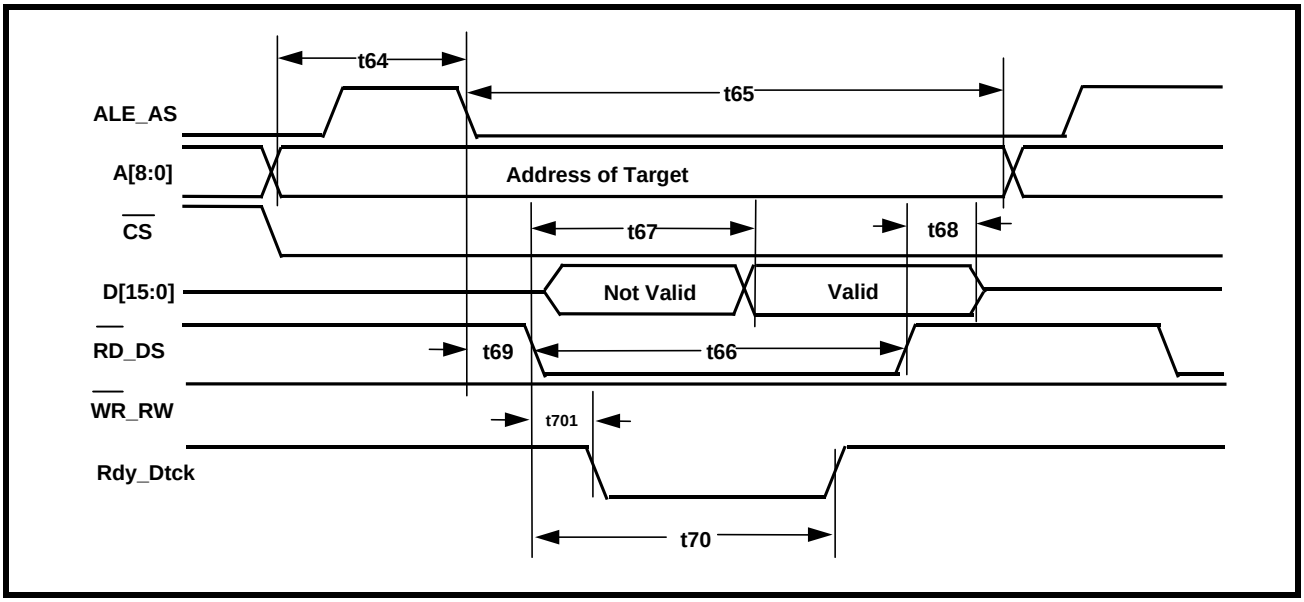


FIGURE 17. MICROPROCESSOR INTERFACE TIMING - INTEL TYPE PROGRAMMED I/O WRITE OPERATIONS

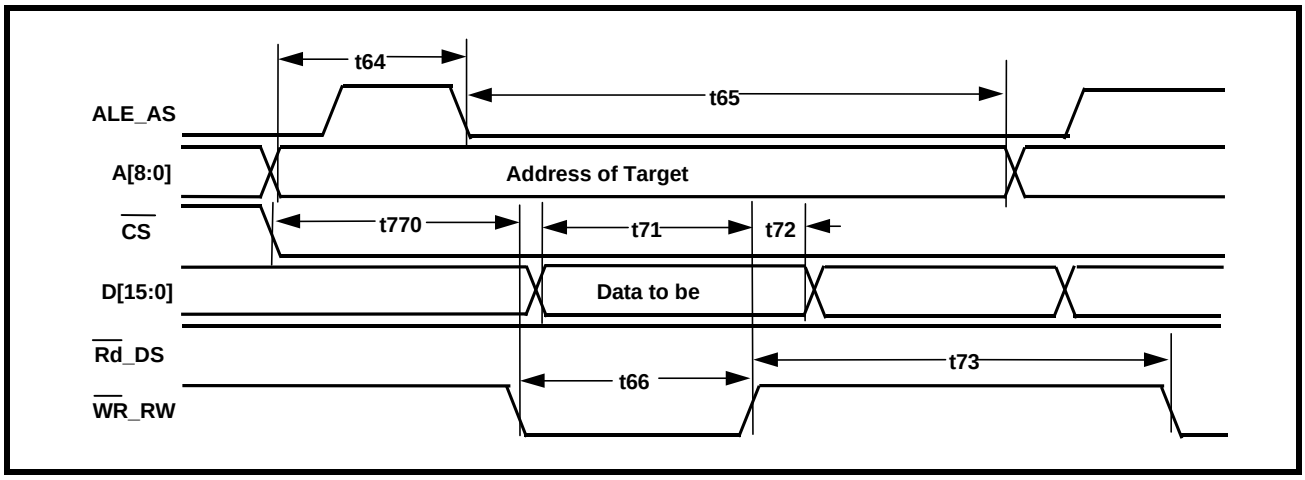


FIGURE 18. MICROPROCESSOR INTERFACE TIMING - INTEL TYPE READ BURST ACCESS OPERATION

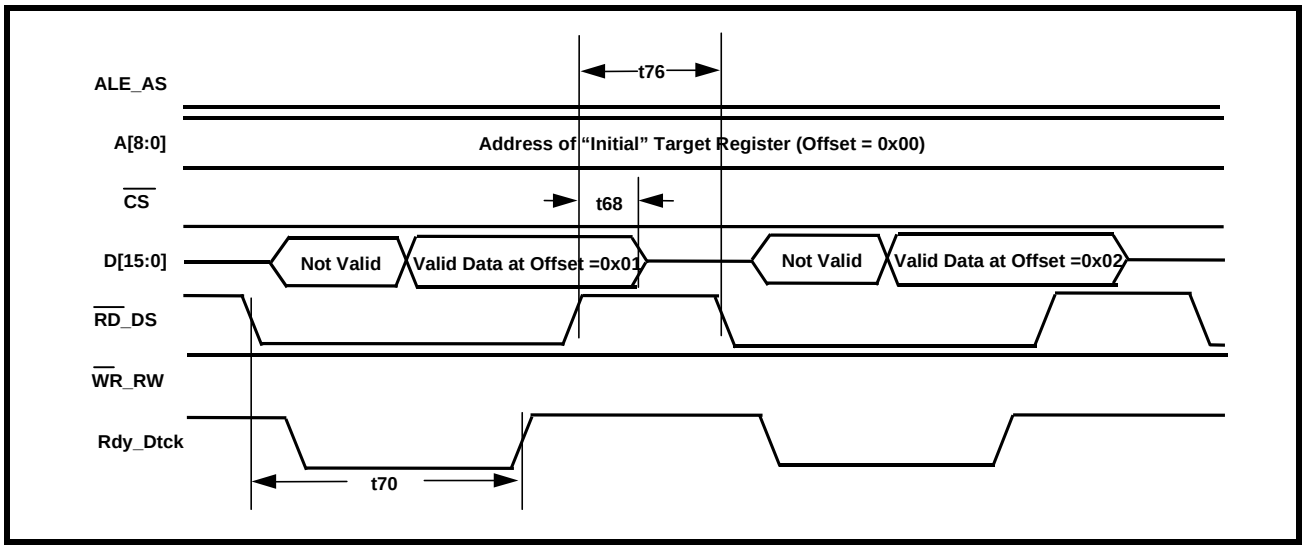


FIGURE 19. MICROPROCESSOR INTERFACE TIMING - INTEL TYPE WRITE BURST ACCESS OPERATION

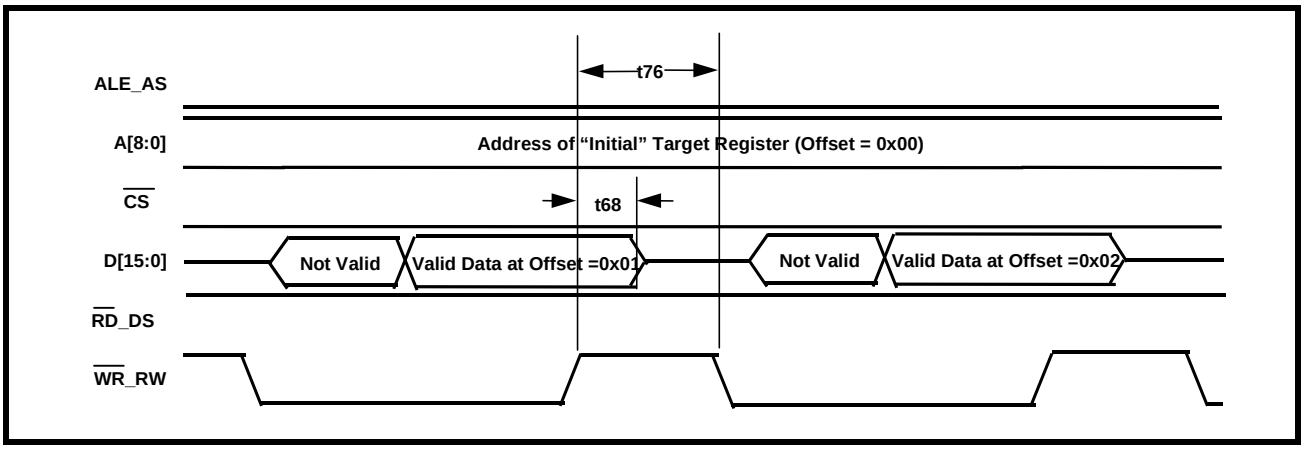


FIGURE 20. MICROPROCESSOR INTERFACE TIMING - MOTOROLA TYPE PROGRAMMED I/O READ OPERATION

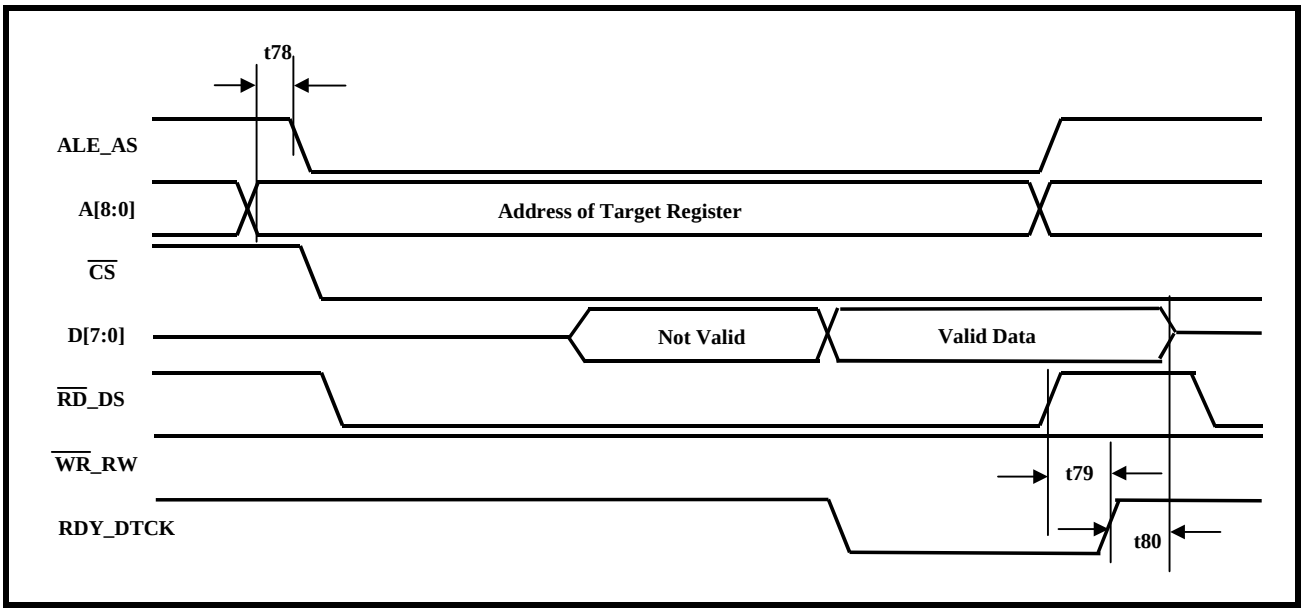


FIGURE 21. MICROPROCESSOR INTERFACE TIMING - MOTOROLA TYPE PROGRAMMED I/O WRITE OPERATION

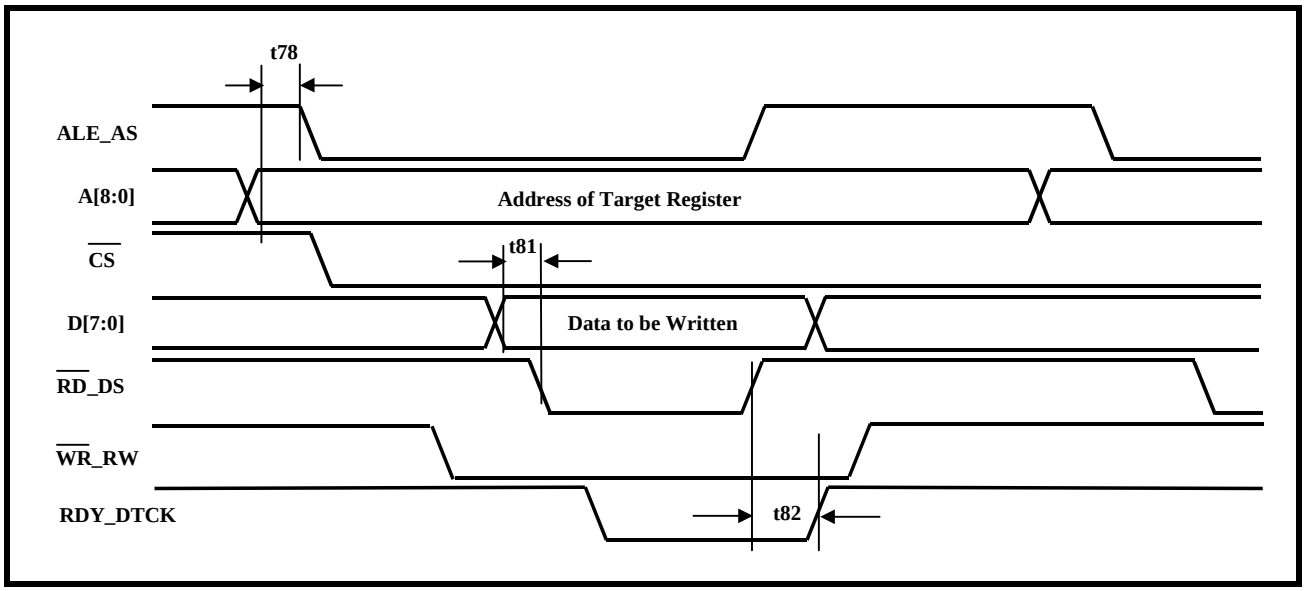
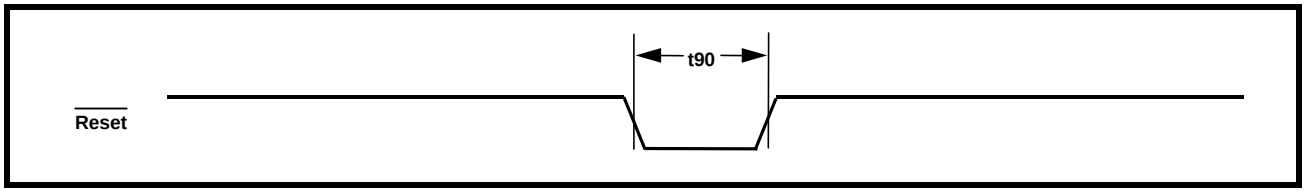


FIGURE 22. MICROPROCESSOR INTERFACE TIMING - MOTOROLA TYPE READ BURST ACCESS OPERATION

FIGURE 23. MICROPROCESSOR INTERFACE TIMING - MOTOROLA TYPE WRITE BURST ACCESS OPERATION

FIGURE 24. MICROPROCESSOR INTERFACE TIMING - RESETB* PULSE WIDTH



1.0 SYSTEM DESCRIPTION

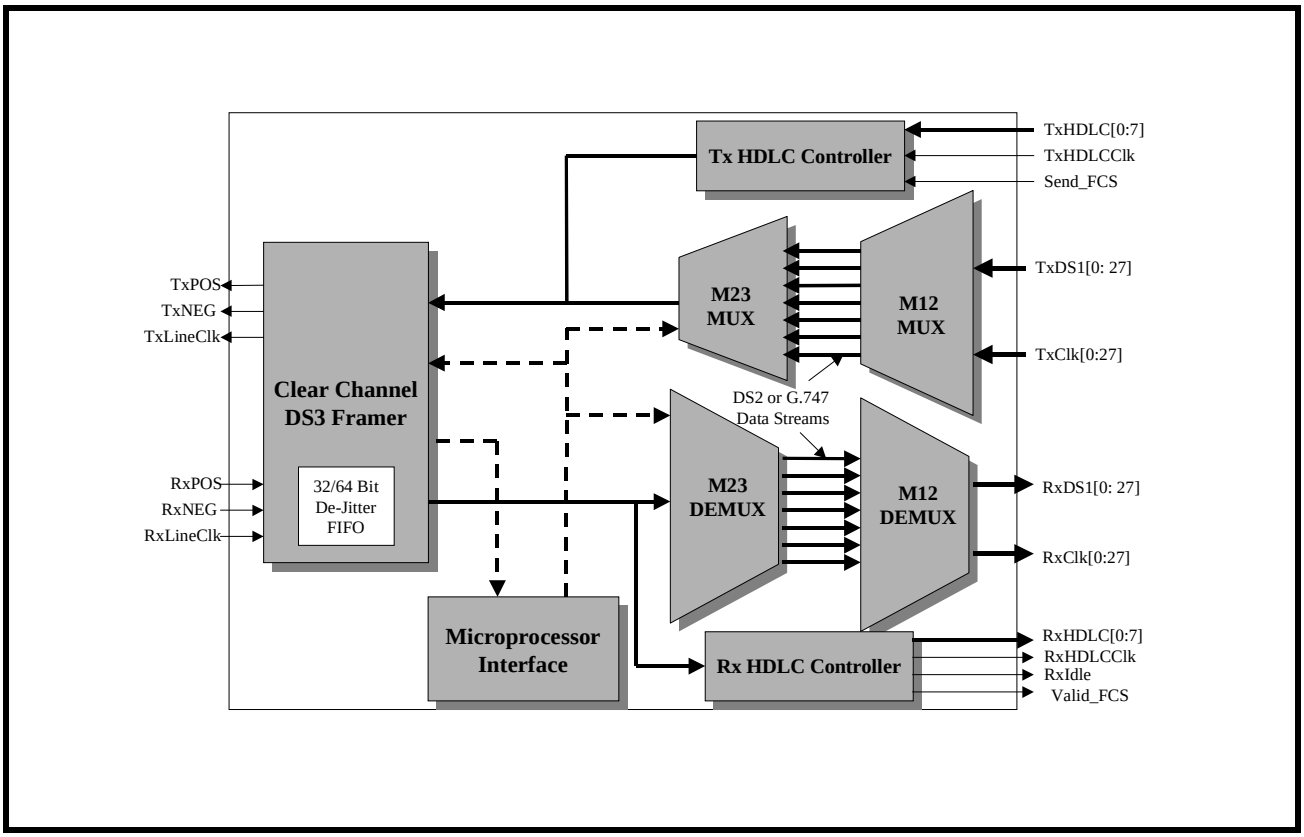
The XRT72L13 M13 Multiplexer/Framer IC can be configured to operate in any of the following modes:

- Multiplexer/De-Multiplexer Mode.
- Clear Channel DS3 Framer Mode.
- High Speed HDLC Controller Mode.

Each of these modes are briefly described below

Figure 25 presents a simple block diagram of the XRT72L13 M13 Multiplexer/Framer IC.

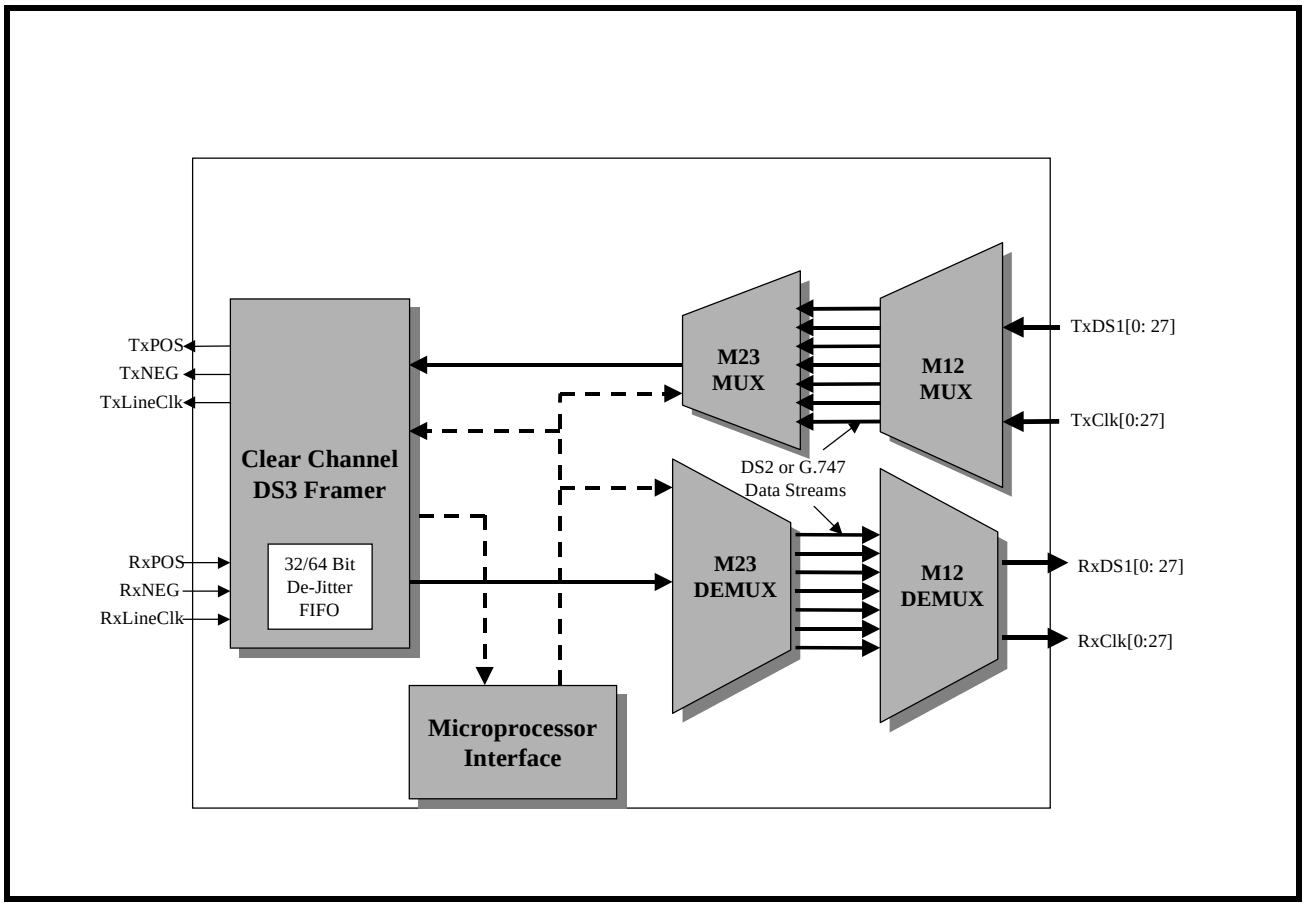
FIGURE 25. BLOCK DIAGRAM OF THE XRT72L13 M13 MULTIPLEXER/FRAMER IC



1.1 XRT72L13 OPERATION WHILE IN THE MULTIPLEXER/DE-MULTIPLEXER MODE

Figure 26, presents a function block diagram of the XRT72L13 when it has been configured to operate in the "Multiplexer/De-Multiplexer Mode.

FIGURE 26. FUNCTIONAL BLOCK DIAGRAM OF THE XRT72L13 M13 MULTIPLEXER/FRAMER IC, WHILE OPERATING IN THE "MULTIPLEXER/DE-MULTIPLEXER MODE



When the XRT72L13 has been configured to operate in the "Multiplexer/De-Multiplexer Mode, then the chip will function as follows.

1.1.1 In the Transmit Direction

When the XRT72L13 is operating the "Multiplexer/De-Multiplexer" Mode, it consist of the following blocks.

- Seven (7) M12 MUXes.
- An M23 MUX.
- The Clear Channel DS3 Framer Block.

1.1.1.1 Operation of the M12 MUX

Each M12 MUX can be configured to accept either 4 DS1 signals, 3 E1 signals or a DS2 signal. Whenever a given M12 MUX is configured to operate in the “DS1” Mode, then it will accept four (4) DS1 signals (via the “TxDS1Data_n” input pins) and it will multiplex these DS1 signals into a DS2 signal.

Whenever a given M12 MUX is configured to operate in the “ITU-T G.747” Mode, then it will accept three (3) E1 signals (via 3 out of 4 of the “TxDS1_n” input pins) and it will multiplex these E1 signals into an “ITU-T G.747” signal.

Finally, whenever a given M12 MUX is configured to operate in the “DS2 Pass-Thru” Mode, then it will accept a DS2 signal (via one of the “TxDS1Data_n” input pins) and will route these signals to the M23 MUX.

Each M12 MUX also consists of a “Transmit DS2” or “ITU-T G.747 Framer” block. As the M12 MUX outputs its DS2 or ITU-T G.747 data stream to the “M23 MUX” then the “Transmit DS2/G.747 Framer” block will do the following.

- Encapsulate the composite data stream (derived from 4 DS1 signals) into an outbound DS2 framing structure.
- Set the “Cxx” bits to the appropriate values in order to indicate whether or not a bit-stuff event occurred when creating this particular DS2 frame.

- Set the “X” bits (within each “outbound” DS2 frame) to the appropriate value in order to reflect the “DS2 FERF” indicator when conditions warrant.

The XRT72L13 will accept up to 28 DS1 lines or up to 21 E1 lines as inputs to the M12 Multiplexer. Associated with each of these DS1 or E1 lines is an input clock signal that the device will use to sample and latch into the device.

In all, the M12 MUX is capable of MUXing 28 DS1 lines into 7 DS2 lines. Additionally, the M12 MUX is also capable of MUXing 21 E1 lines into 7 ITU-T G.747 lines.

1.1.1.2 Operation of the M23 MUX

The M23 MUX, within the XRT72L13 will accept up to 7 DS2 or ITU-T G.747 data streams and will MUX these signals into a DS3 data stream. Afterwards, this DS3 data stream will be routed to the "Clear Channel DS3 Framer" block for further processing.

1.1.1.3 Operation of the "Clear Channel DS3 Framer Block"

Once this data is routed to the "Clear Channel DS3 Framer Block", the DS3 data stream will be encapsulated into a "outbound" DS3 framing structure, and will be transmitted to an off-chip LIU IC. The Clear Channel DS3 Framer Block is also responsible for a variety of other necessary function, such as:

- Transmission of PMDL (Path Maintenance Data Link) Messages
- Transmission of FEAC (Far-End Alarm & Control) Messages
- Transmission of the FERF (Far-End Receive Failure) Indicator
- Transmission of the FEBE (Far-End Block Error) Indicator
- Computation of P and CP-Bits

1.1.2 In the Receive Direction

When the XRT72L13 is operating in the "Multiplexer/De-Multiplexer" Mode, the data (in the "Receive Direction") passes through the following block.

- The Clear Channel DS3 Framer Block
- An M23 DEMUX
- An M12 DEMUX

1.1.2.1 Operation of the Clear Channel DS3 Framer Block

The purpose of the "Clear Channel DS3 Framer Block" is to perform the following functions:

- To verify the P and CP-bits.
- To Terminate the PMDL Messages.
- To Terminate the FEAC Messages
- To Terminate and interpret the FERF Indicator
- To Terminate and interpret the FEBE Indicator.
- To strip off the "Overhead" bytes and route the payload portion of the "inbound" DS3 frame to the M23 DEMUX

1.1.2.2 Operation of the M23 DEMUX

The purpose of the M23 DEMUX, within the XRT72L13 is to accept this DS3 data stream and demultiplex either 7 DS2 or ITU-T G.747 data streams. Afterwards, these data streams will be routed to the M12 DEMUX.

1.1.2.3 Operation of the M12 DEMUX

The purpose of the M12 DEMUX, within the XRT72L13 is to accept either the 7 DS2 or ITU-T G.747 data streams and to de-multiplex up to 28 DS1 signals or up to 21 E1 signals.

1.1.3 Diagnostic Resources available for MUX/DEMUX Mode

In all, the XRT72L13 supports two types of loop-back modes, while it is configured to operate in the "MUX/DEMUX" Mode.

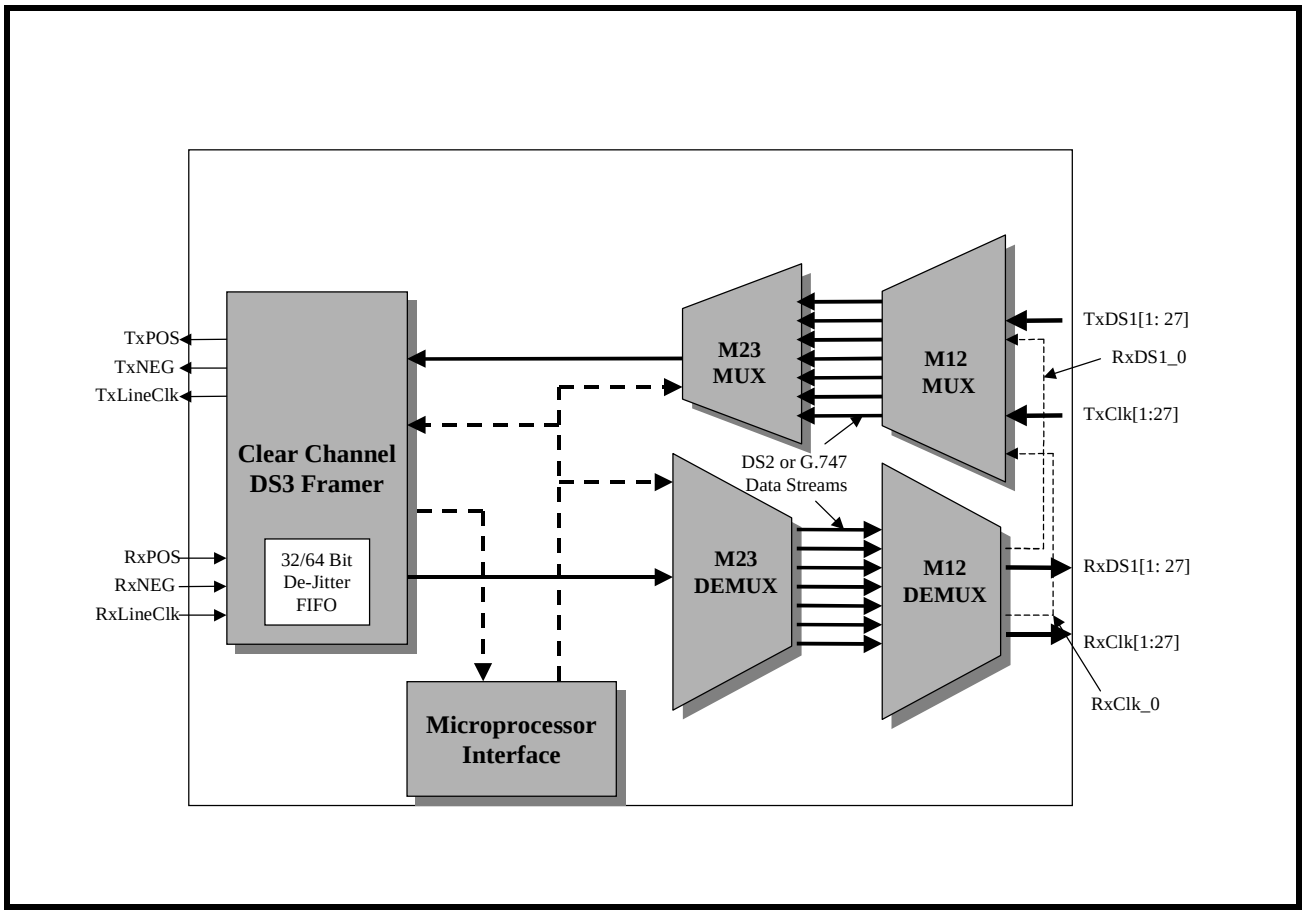
- DS1/E1 Tributary Loop-Back
- DS2/ITU-T G.747 Tributary Loop-Back

Each of these Loop-Back Modes are briefly discussed below.

1.1.3.1 DS1/E1 Tributary Loop-Back

Figure 27 presents an illustration of the XRT72L13 operating in the "DS1/E1 Tributary Loop-Back Mode.

FIGURE 27. ILLUSTRATION OF THE XRT72L13 OPERATING IN THE "DS1/E1 TRIBUTARY LOOP-BACK MODE

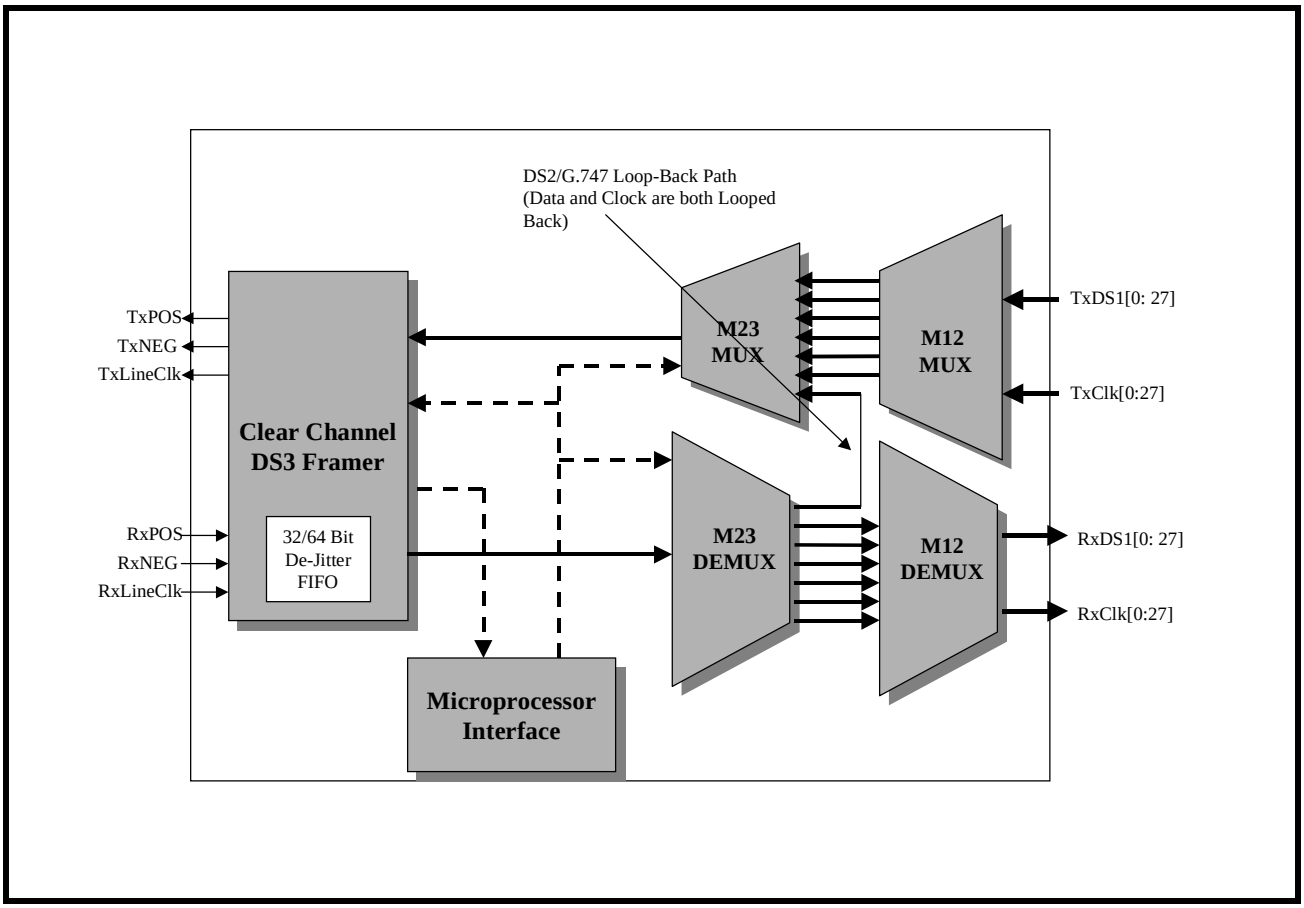


As Figure 27 indicates, a given DS1 line can be commanded into the "DS1/E1 Tributary Loop-Back" Mode. When this happens, then a selected DS1 or E1 line, in the Receive Path, is looped back into the Transmit Path. It is important to note that the corresponding DS1 or E1 clock signal is also looped back.

1.1.3.2 DS2/ITU-T G.747 Tributary Loop-Back Mode

Figure 28 presents an illustration of the XRT72L13 operating in the "DS2/ITU-T G.747 Tributary Loop-Back" Mode.

FIGURE 28. ILLUSTRATION OF THE XRT72L13 OPERATING IN THE "DS2/ITU-T G.747 TRIBUTARY LOOP-BACK MODE

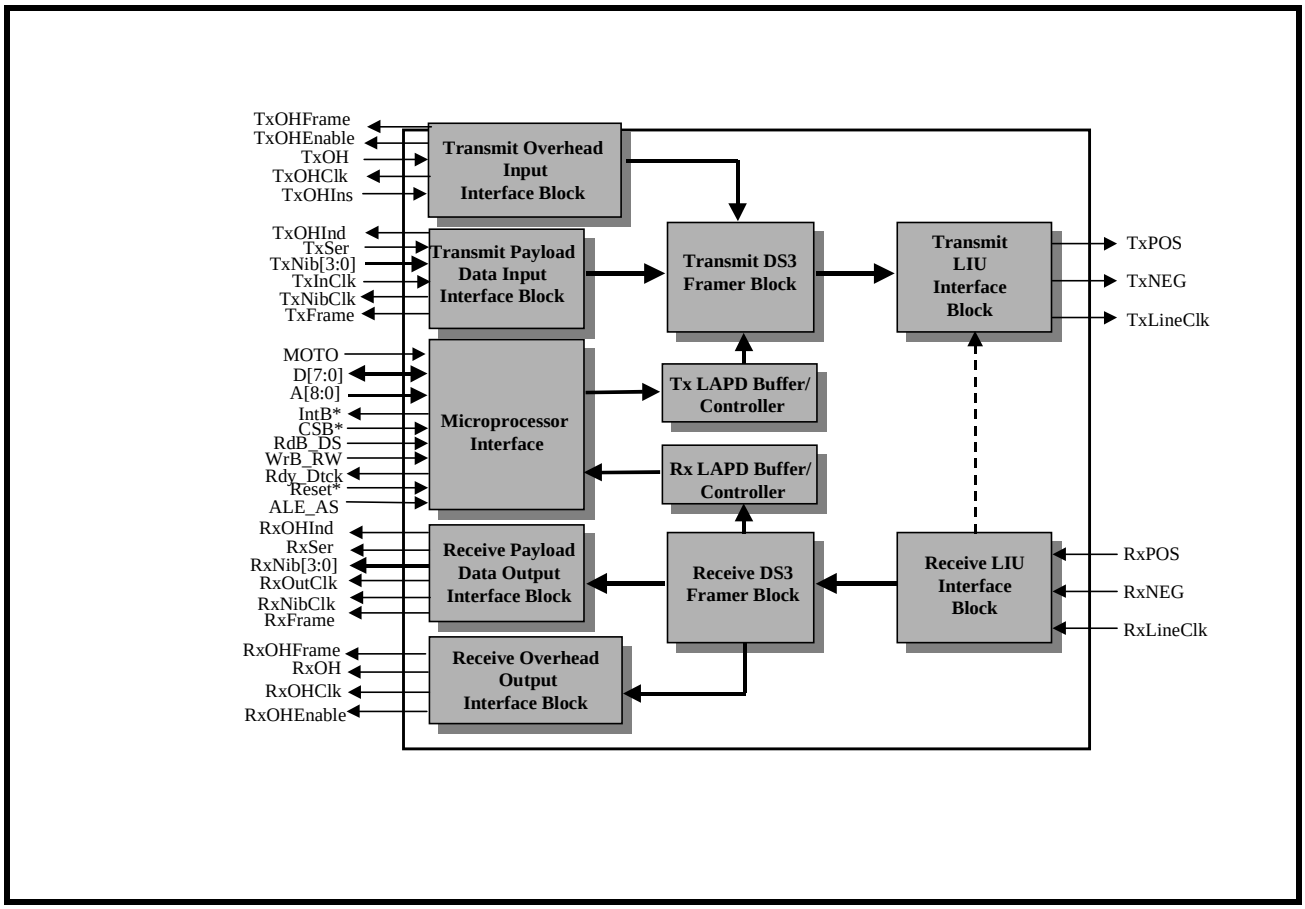


As Figure 28 indicates, a given DS2 or ITU-T G.747 line can be commanded into the "DS2/ITU-T G.747 Tributary Loop-Back" Mode. When this happens, then a selected DS2 or ITU-T G.747 data stream (in the Receive Path) is looped back into the Transmit Path. It is important to note that the corresponding DS2 or ITU-T G.747 clock signal is also looped back into the Transmit Path.

1.2 XRT72L13 OPERATION WHILE IN THE "CLEAR CHANNEL DS3 FRAMER MODE"

Figure 29 presents a functional block diagram of the XRT72L13 when it has been configured to operate in the "Clear Channel DS3 Framer Mode".

FIGURE 29. FUNCTIONAL BLOCK DIAGRAM OF THE XRT72L13 M13 MULTIPLEXER/FRAMER IC, WHILE OPERATING IN THE "CLEAR CHANNEL DS3 FRAMER MODE"



As this mode implies, the "Clear Channel DS3 Framer Mode" permits the user to transmit and receive any type of data over the DS3 Transport Medium.

1.2.1 Operation of the XRT72L13 while in the "Clear Channel DS3 Framer Mode"

To be provided in the next update.

1.2.1.1 Diagnostic Features

When the XRT72L13 is operating in the "Clear Channel DS3 Framer" Mode, then the following diagnostic features are available.

- Local Loop-back Mode
- Remote Loop-back Mode
- PRBS Pattern Generation/Reception

1.2.1.1.1 Local Loop-back Mode

Figure 30 presents an illustration of the XRT72L13 operating in the Local-Loop-back Mode.

FIGURE 30. ILLUSTRATION OF THE XRT72L13 M13 MULTIPLEXER/FRAMER OPERATING IN THE "CLEAR CHANNEL DS3 FRAMER LOCAL LOOP-BACK" MODE

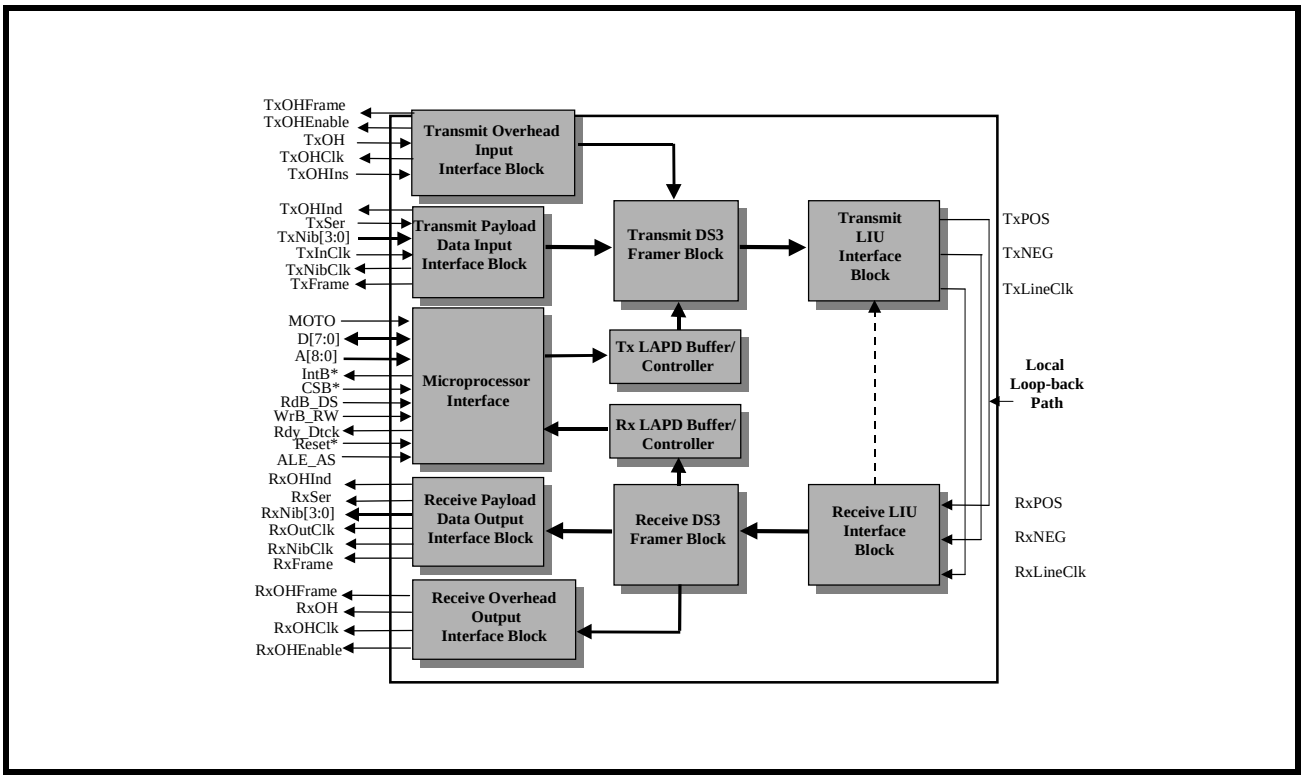


Figure 30 indicates that when the XRT72L13 has been configured to operate in the "Clear Channel DS3 Framer Local Loop-back" Mode, then the following internal connections are made.

- The TxPOS output signal is routed into the RxPOS input pin.
- The TxNEG output signal is routed into the RxNEG input pin
- The TxLineClk output clock signal is routed into the RxLineClk input pin.

1.2.1.1.2 Remote Loop-back Mode

Figure 31 presents an illustration of the XRT72L13 M13 Multiplexer/Framer IC operating in the "Clear Channel DS3 Framer Remote Loop-back" Mode.

FIGURE 31. ILLUSTRATION OF THE XRT72L13 M13 MULTIPLEXER/FRAMER OPERATING IN THE "CLEAR CHANNEL DS3 FRAMER REMOTE LOOP-BACK" MODE

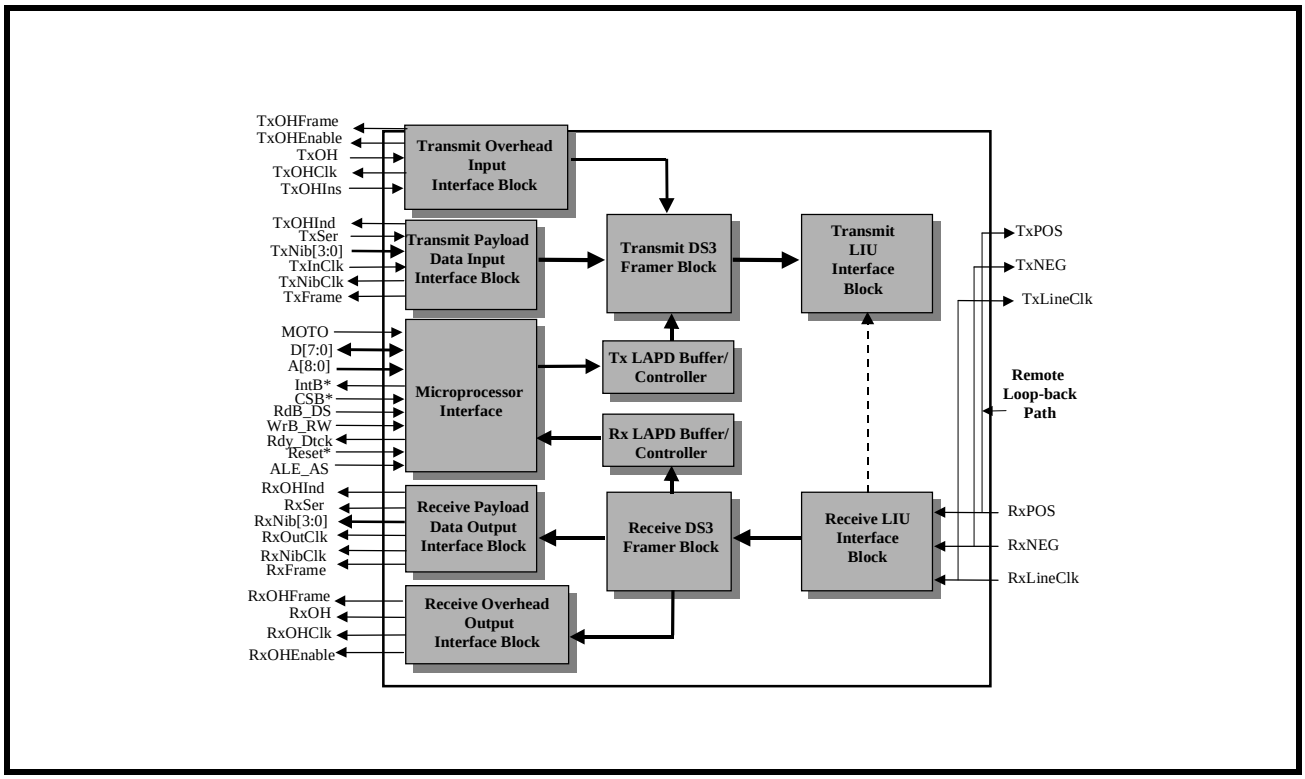


Figure 31 indicates that when the XRT72L13 has been configured to operate in the "Clear Channel DS3 Framer Remote Loop-back" Mode, then the following internal connections are made:

- The RxPOS input signal is routed to the TxPOS output pin.
- The RxNEG input signal is routed to the TxNEG output pin.
- The RxLineClk output clock signal is routed to the TxLineClk input pin.

1.2.1.1.3 PRBS Generator/Receiver

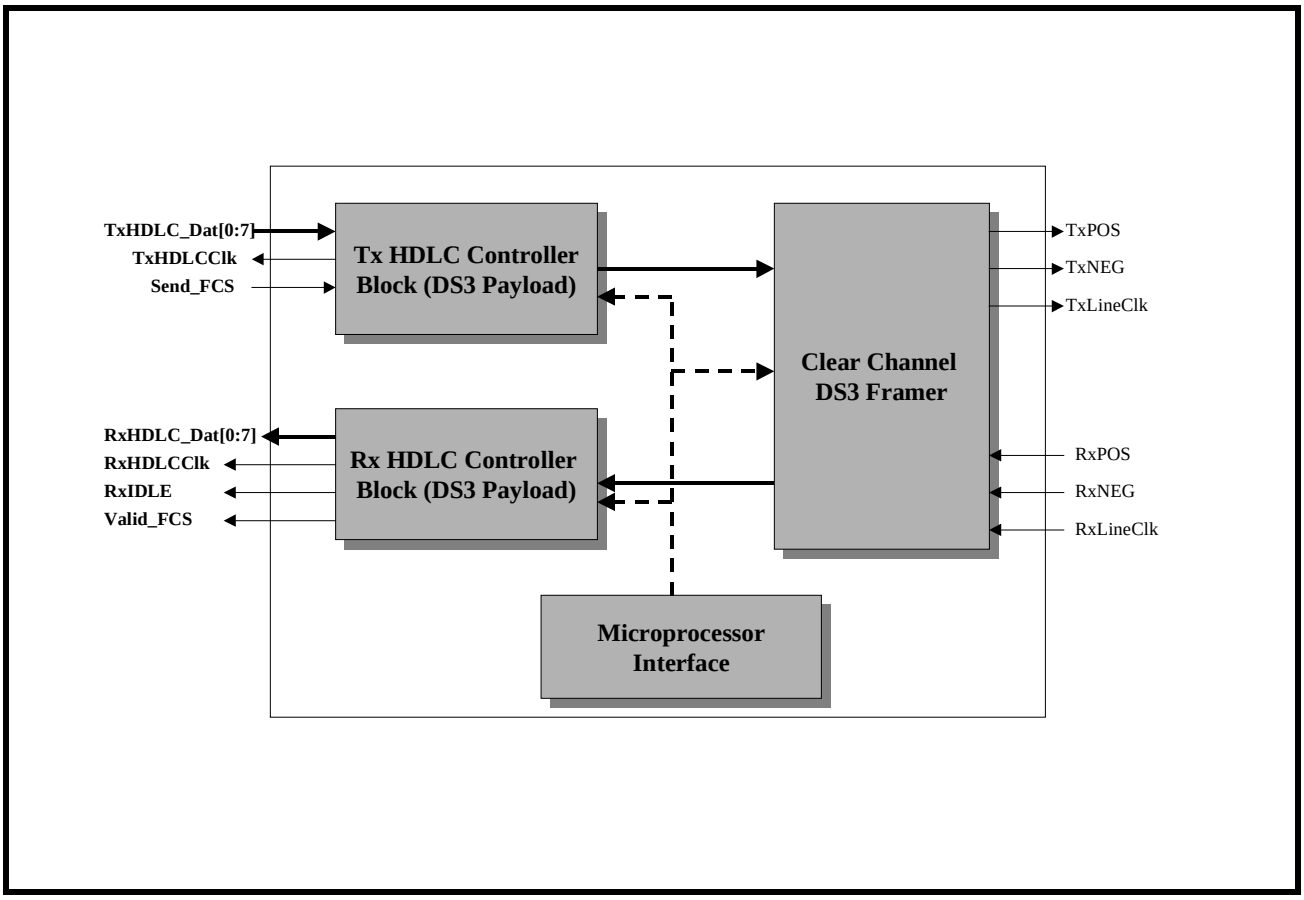
In order to support diagnostic testing of the signal path, the XRT72L13 contains a PRBS Generator and Receiver. This feature can be operated in conjunction with (or not) with the "Clear Channel DS3 Framer Local" or "Remote" Loop-back Modes.

A more detailed description of this feature will be presented in the next revision of the XRT72L13 Data Sheet.

1.3 XRT72L13 OPERATION WHILE IN THE "HIGH SPEED HDLC CONTROLLER" MODE

Figure 32 presents a Functional Block Diagram of the XRT72L13 M13 Multiplexer/Framer IC, when it has been configured to operate in the "High Speed HDLC Controller Mode"

FIGURE 32. ILLUSTRATION OF THE XRT72L13 M13 MULTIPLEXER/FRAMER IC, WHEN IT HAS BEEN CONFIGURED TO OPERATE IN THE "HIGH SPEED HDLC CONTROLLER" MODE



A more detailed description of the "High Speed HDLC Controller" Mode will be presented in the next update of this document.

2.0 THE MICROPROCESSOR INTERFACE BLOCK

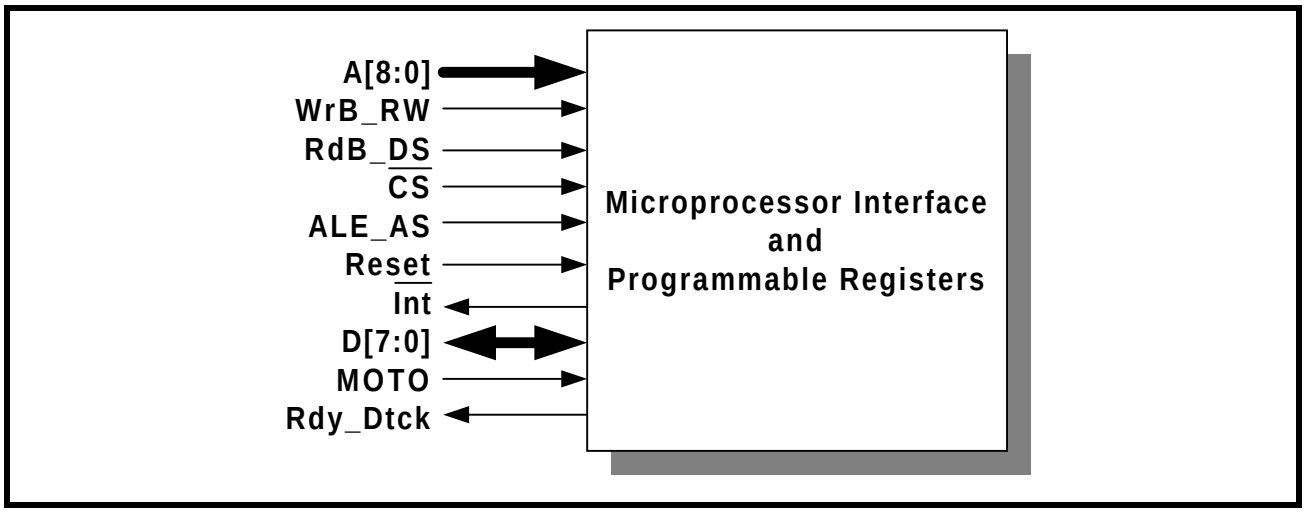
The Microprocessor Interface section supports communication between the "local" microprocessor (µP) and the Framer IC. In particular, the Microprocessor Interface section supports the following operations between the local microprocessor and the Framer.

- The writing of configuration data into the Framer on-chip (addressable) registers.
- The writing of an "outbound" PMDL µPath Maintenance Data Link) message into the "Transmit LAPD Message" buffer (within the Framer IC).
- The Framer IC's generation of an Interrupt Request to the µP.
- The µP's servicing of the interrupt request from the Framer IC.
- The monitoring of the system's "health" by periodically reading the on-chip Performance Monitor registers.
- The reading of an "inbound" PMDL Message from the "Receive LAPD" Message Buffer (within the Framer IC).

Each of these operations (between the local microprocessor and the Framer IC) will be discussed in some detail, throughout this data sheet.

Figure 33 presents a simple block diagram of the Microprosser Interface Block.

FIGURE 33. SIMPLE BLOCK DIAGRAM OF THE MICROPROCESSOR INTERFACE BLOCK, WITHIN THE FRAMER IC



2.1 THE MICROPROCESSOR INTERFACE BLOCK SIGNAL

The Framer IC may be configured into a wide variety of different operating modes and have its performance monitored by software through a standard (local "housekeeping") microprocessor, using data, address and control signals.

The local µP configures the Framer IC (into a desired operating mode) by writing data into specific addressable, on-chip "Read/Write" registers; or on-chip RAM. The microprocessor interface provides the signals which are required for a general purpose microprocessor to read or write data into these registers. The Microprocessor Interface also supports "polled" and interrupt driven environments. These interface signals are described below in Table 1, 2, and 3. The microprocessor interface can be configured to operate in the "Motorola" Mode or in the "Intel" mode. When the Microprocessor Interface is operating in the "Motorola" mode, then some of the control signals function in a manner as required by the Motorola 68000 family of microprocessors. Likewise, when the Microprocessor Interface is operating in the "Intel" Mode, then some of these Control Signals function in a manner as required by the Intel 80xx family of microprocessors.

Table 1 lists and describes those Microprocessor Interface signals whose role is constant across the two modes. Table 2 describes the role of some of these signals when the Microprocessor Interface is operating in the Intel Mode. Likewise, Table 3 describes the role of these signals when the Microprocessor Interface is operating in the Motorola Mode.

TABLE 1: DESCRIPTION OF THE MICROPROCESSOR INTERFACE SIGNALS THAT EXHIBIT CONSTANT ROLES IN BOTH THE "INTEL" AND "MOTOROLA" MODES

PIN NAME	TYPE	DESCRIPTION
MOTO	I	Selection input for Intel/Motorola µP Interface. Setting this pin to a logic "high" configures the Microprocessor Interface to operate in the "Motorola" mode. Likewise, setting this pin to a logic "low" configures the Microprocessor Interface to operate in the "Intel" Mode.
D[7:0]	I/O	Bi-Directional Data Bus for register read or write operations
A[8:0]	I	Nine Bit Address Bus input: This nine bit Address Bus is provided to allow the user to select an on-chip register or on-chip RAM location.
CSB	I	Chip Select input. This "active low" signal selects the Microprocessor Interface of the UNI device and enables read/write operations with the on-chip registers/on-chip RAM.
IntB	O	Interrupt Request Output: This "open-drain/active-low" output signal will inform the local µP that the UNI has an interrupt condition that needs servicing.

TABLE 2: PIN DESCRIPTION OF MICROPROCESSOR INTERFACE SIGNALS - WHILE THE MICROPROCESSOR INTERFACE IS OPERATING IN THE INTEL MODE

PIN NAME	EQUIVALENT PIN IN INTEL ENVIRONMENT	TYPE	DESCRIPTION
ALE_AS	ALE	I	Address-Latch Enable: This "active-high" signal is used to latch the contents on the address bus, A[8:0]. The contents of the Address Bus are latched into the A[8:0] inputs on the falling edge of ALE_AS. Additionally, this signal can be used to indicate the start of a burst cycle.
RdB_DS	RD*	I	Read Signal: This "active-low" input functions as the read signal from the local µP. When this signal goes "low", the UNI Microprocessor Interface will place the contents of the addressed register on the Data Bus pins (D[15:0]). The Data Bus will be "tri-stated" once this input signal returns "high".
WRB_RW	WR*	I	Write Signal: This "active-low" input functions as the write signal from the local µP. The contents of the Data Bus (D[15:0]) will be written into the addressed register (via A[8:0]), on the rising edge of this signal.
Rdy_Dtck	READY*	O	Ready Output: This "active-low" signal is provided by the UNI device, and indicates that the current read or write cycle is to be extended until this signal is asserted. The local µP will typically insert "WAIT" states until this signal is asserted. This output will toggle "low" when the device is ready for the next Read or Write cycle.

TABLE 3: PIN DESCRIPTION OF THE MICROPROCESSOR INTERFACE SIGNALS WHILE THE MICROPROCESSOR INTERFACE IS OPERATING IN THE MOTOROLA MODE

PIN NAME	EQUIVALENT PIN IN MOTOROLA ENVIRONMENT	TYPE	DESCRIPTION
ALE_AS	AS*	I	Address Strobe: This "active-low" signal is used to latch the contents on the address bus input pins: A[8:0] into the Microprocessor Interface circuitry. The contents of the Address Bus are latched into the UNI device on the rising edge of the ALE_AS signal. This signal can also be used to indicate the start of a burst cycle.
RdB_DS	DS*	I	Data Strobe: This signal latches the contents of the bi-directional data bus pins into the Addressed Register (within the UNI) during a Write Cycle.
WRB_RW	R/W*	I	Read/Write* Input: When this pin is "high", it indicates a Read Cycle. When this pin is "low", it indicates a Write cycle.
Rdy_Dtck	DTACK*	O	Data Transfer Acknowledge: The UNI device asserts DTACK* in order to inform the CPU that the present READ or WRITE cycle is nearly complete. The 68000 family of CPUs requires this signal from its peripheral devices, in order to quickly and properly complete a READ or WRITE cycle.

2.2 INTERFACING THE XRT 72L13 DS3 FRAMER TO THE LOCAL µC/µP OVER VIA THE MICROPROCESSOR INTERFACE BLOCK

The Microprocessor Interface block, within the Framer device is very flexible and provides the following options to the user.

- To interface the Framer device to a µC/µP over an 8-bit wide bi-directional data bus.
- To interface the Framer to an Intel-type or Motorola-type µC/µP.
- To transfer data (between the Framer IC and the µC/µP) via the Programmed I/O or Burst Mode

Each of the options are discussed in detail below. Section 2.2.1 will discussed the issues associated with interfacing the Framer to a µC/µP over an 8-bit bi-directional data bus. Afterwards, Section 2.2.2 will discuss Data Access (e.g., Programmed I/O and Burst) Mode when interfaced to both Motorola-type and Intel-type µC/µP.

2.2.1 Interfacing the XRT 72L13 DS3 Framer to the Microprocessor over an 8 bit wide bi-directional Data Bus

The XRT 72L13 DS3 Framer Microprocessor Interface permits the user to interface it to a µC/µP over an 8 wide bi-directional data bus.

2.2.1.1 Interfacing the Framer to the µC/µP over an 8-bit wide bi-directional data bus.

In general, interfacing the Framer to an "8-bit" µC/µP is quite straight-forward. This is because most of the registers, within the Framer, are 8-bits wide. Further, in this mode, the µC/µP can read or write data into both even and odd numbered addresses within the Framer address space.

Reading Performance Monitor (PMON) Registers

The only issue that the user should be wary of (while operating in the "8-bit" mode) occurs whenever the µC/µP needs to read the contents of one of the PMON (Performance Monitor) registers.

The XRT 72L13 DS3 Framer consists of the following PMON Registers.

- PMON LCV Event Count Register
- PMON Framing Error Event Count Register
- PMON Received FEBE Event Count Register
- PMON Parity Error Event Count Register
- PMON Received Single-Bit HEC Error Count Register
- PMON Received Multiple-Bit HEC Error Count Register
- PMON Received Idle Cell Count Register
- PMON Received Valid Cell Count Register
- PMON Discarded Cell Count Register
- PMON Transmitted Idle Cell Count Register
- PMON Transmitted Valid Cell Count Register.

Unlike most of the registers within the Framer, the PMON registers are "16-bit" registers (or 16-bits wide). Table 4 lists each of these PMON registers as consisting of two 8-bit registers. One of these "8-bit" register is labeled "MSB" (or Most Significant Byte")

and the other register is labeled "LSB" (or Least Significant Byte). When an "8-bit" PMON Register is concatenated with its "companion 8-bit" PMON Register, one obtains the "full 16-bit expression" within that PMON Register.

The consequence of having these 16-bit registers is that an "8-bit" µC/µP will have to perform two consecutive read operations in order to read in the full 16-bit expression contained within a given PMON register. To complicate matters, these PMON Registers are "Reset-Upon-Read" registers. More specifically, these PMON Register are "Reset-Upon-Read" in the sense that, the entire "16-bit" contents, within a given PMON Register is reset, as soon as an "8-bit" µC/µP reads in either "byte" of this "two-byte" (e.g., 16 bit) expression.

For example;

Consider that an "8-bit" µC/µP needs to read in the "PMON LCV Event Count" Register. In order to accomplish this task, the 8-bit µC/µP is going to have to read in the contents of "PMON LCV Event Count Register - MSB" (located at Address = 0x40) and the contents of the "PMON LCV Event Count Register - LSB (located at Address = 0x41). These two "eight-bit" registers, when concatenated together, make up the "PMON LCV Event Count" Register.

If the 8-bit µC/µP reads in the "PMON LCV Event Count-LSB" register first; then the entire "PMON LCV Event Count" register will be reset to 0x0000. As a consequence, if the 8-bit µC/µP attempts to read in the "PMON LCV Event Count-MSB" register in the very next read cycle, it will read in the value 0x00.

The PMON Holding Register

In order to "get-around" this "Reset-Upon-Read" problem, the XRT 72L13 DS3 Framer includes a special register, which permits "8-bit" µC/µP to read in the full 16-bit contents of these PMON registers. This special register is called the "PMON Holding" Register; and is located at 0x56 within the Framer Address space.

The way the PMON Holding register works is as follows. Whenever an "8-bit" µC/µP reads in one of the bytes (of the "2-byte" PMON register); the contents of the "unread" (e.g., other) byte will be stored in the PMON Holding Register. Therefore, the "8-bit" µC/µP must then read in the contents of the PMON Holding Register in the very next read operation.

In Summary: Whenever an "8-bit" µC/µP needs to read a PMON Register, it must execute the following steps.

Step 1: Read in the contents of a given "8-bit" PMON Register (it does not matter whether the µC/µP reads in the "-MSB" or the "-LSB" register).

Step 2: Read in the contents of the "PMON Holding" Register (located at Address = 0x56). This register will contain the contents of the "other" byte.

2.2.2 Data Access Modes

As mentioned earlier, the Microprocessor Interface block supports data transfer between the Framer and the µC/µP (e.g., "Read" and "Write" operations) via two modes: the "Programmed I/O" and the "Burst" Modes. Each of these "Data Access" Modes are discussed in detail below.

2.2.2.1 Data Access using Programmed I/O

"Programmed I/O" is the conventional manner in which a microprocessor exchanges data with a peripheral device. However, it is also the slowest method of data exchange between the Framer and the µC/µP; as will be described in this text.

The next two sections present detailed information on Programmed I/O Access, when the XRT 72L13 DS3 Framer is operating in the "Intel Mode" and in the "Motorola Mode".

2.2.2.1.1 Programmed I/O Access in the "Intel" Mode

If the XRT 72L13 DS3 Framer is interfaced to an "Intel-type" µC/µP (e.g., the 80x86 family, etc.), then it should be configured to operate in the "Intel" mode (by tying the "MOTO" pin to ground). Intel-type "Read" and "Write" operations are described below.

2.2.2.1.1.1 The Intel Mode Read Cycle

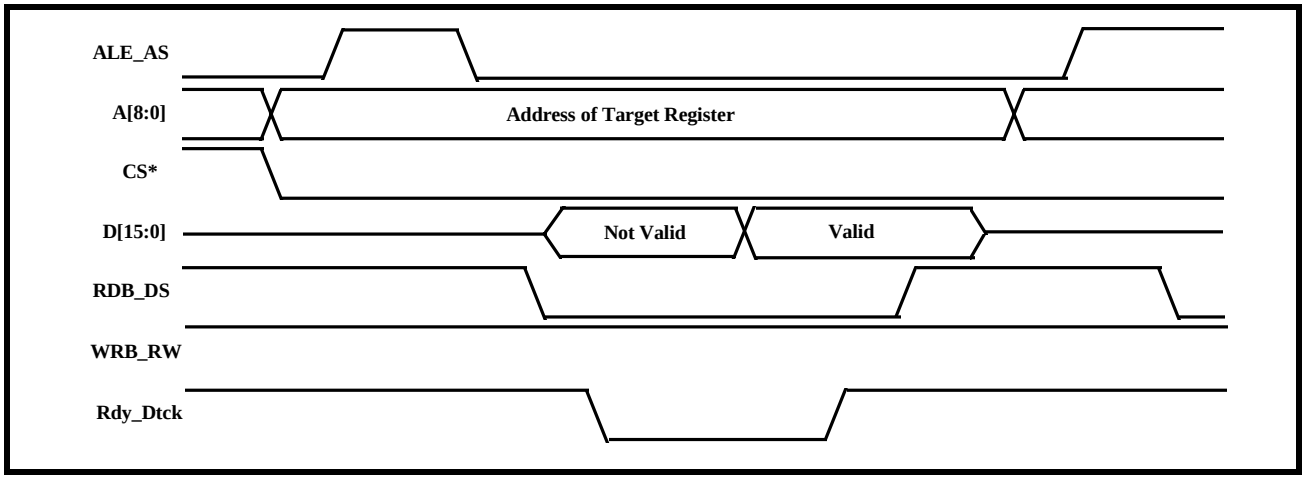
Whenever an Intel-type µC/µP wishes to read the contents of a register or some location within the Receive LAPD Message buffer or the Receive OAM Cell Buffer, (within the Framer device), it should do the following.

1. Place the address of the "target" register or buffer location (within the Framer) on the Address Bus input pins A[8:0].
2. While the µC/µP is placing this address value on the Address Bus, the Address Decoding circuitry (within the user's system) should assert the CS* (Chip Select) pin of the Framer, by toggling it "low". This action enables further communication between the µC/µP and the Framer Microprocessor Interface block.
3. Toggle the ALE_AS (Address Latch Enable) input pin "high". This step enables the "Address Bus" input drivers, within the Microprocessor Interface block of the Framer.

4. After allowing the data on the Address Bus pins to settle (by waiting the appropriate "Address" Data Setup time"), the µC/µP should toggle the ALE_AS pin "low". This step causes the Framer device to "latch" the contents of the "Address Bus" into its internal circuitry. At this point, the address of the register or buffer locations (within the Framer), has now been selected.
5. Next, the µC/µP should indicates that this current bus cycle is a "Read" Operation by toggling the RdB_DS (Read Strobe) input pin "low". This action also enables the bi-directional data bus output drivers of the Framer device. At this point, the "bi-directional" data bus output drivers will proceed to drive the contents of the "latched addressed" register (or buffer location) onto the bi-directional data bus, D[7:0].
6. Immediately after the µC/µP toggles the "Read Strobe" signal "low", the Framer device will toggle the Rdy_Dtck output pin "low". The Framer device does this in order to inform the µC/µP that the data (to be read from the data bus) is "NOT READY" to be "latched" into the µC/µP.
7. After some settling time, the data on the "bi-directional" data bus will stabilize and can be read by the µC/µP. The XRT 72L13 DS3 Framer will indicate that this data can be read by toggling the Rdy_Dtck (READY) signal "high".
8. After the µC/µP detects the Rdy_Dtck signal (from the XRT 72L13 DS3 Framer), it can then terminate the Read Cycle by toggling the RdB_DS (Read Strobe) input pin "high".

Figure 34 presents a timing diagram which illustrates the behavior of the Microprocessor Interface signals, during an "Intel-type" Programmed I/O Read Operation.

FIGURE 34. BEHAVIOR OF MICROPROCESSOR INTERFACE SIGNALS DURING AN "INTEL-TYPE" PROGRAMMED I/O READ OPERATION



2.2.2.1.1.2 The Intel Mode Write Cycle

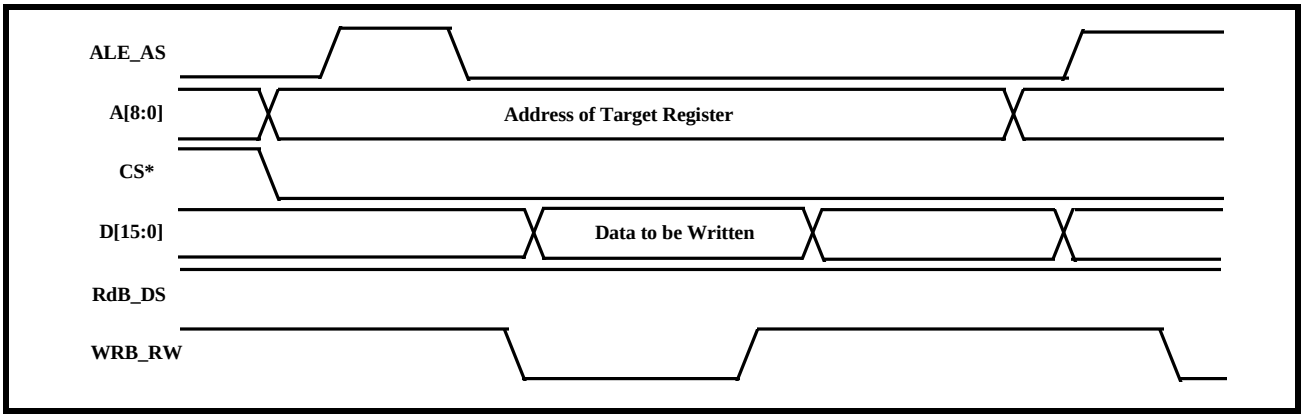
Whenever an Intel-type µC/µP wishes to write a byte or word of data into a register or buffer location, within the Framer, it should do the following.

1. Assert the ALE_AS (Address Latch Enable) input pin by toggling it "high". When the µC/µP asserts the ALE_AS input pin, it enables the "Address Bus Input Drivers" within the Framer chip.
2. Place the address of the "target" register or buffer location (within the Framer), on the Address Bus input pins, A[8:0].
3. While the µC/µP is placing this address value onto the Address Bus, the Address Decoding circuitry (within the user's system) should assert the CS* input pin of the Framer device by toggling it "low". This step enables further communication between the µC/µP and the Framer Microprocessor Interface block.
4. After allowing the data on the Address Bus pins to settle (by waiting the appropriate "Address Setup" time); the µC/µP should toggle the ALE_AS input pin "low". This step causes the Framer device to "latch" the contents of the "Address Bus" into its internal circuitry. At this point, the address of the register or buffer location (within the Framer), has now been selected.
5. Next, the µC/µP should indicate that this current bus cycle is a "Write" Operation; by toggling the WRB_RW (Write Strobe) input pin "low". This action also enables the "bi-directional" data bus input drivers of the Framer device.

6. The µC/µP should then place the byte or word that it intends to write into the "target" register, on the bi-directional data bus, D[7:0].
7. After waiting the appropriate amount of time, for the data (on the bi-directional data bus) to settle; the µC/µP should toggle the WRB_RW (Write Strobe) input pin "high". This action accomplishes two things:
   a. It latches the contents of the bi-directional data bus into the XRT 72L13 DS3 Framer Microprocessor Interface block.
   b. It terminates the write cycle.

Figure 35 presents a timing diagram which illustrates the behavior of the Microprocessor Interface signals, during an "Intel-type" Programmed I/O Write Operation.

FIGURE 35. BEHAVIOR OF THE MICROPROCESSOR INTERFACE SIGNALS, DURING AN "INTEL-TYPE" PROGRAMMED I/O WRITE OPERATION



2.2.2.1.2 Programmed I/O Access in the Motorola Mode

If the XRT 72L13 DS3 Framer is interfaced to a "Motorola-type" µC/µP (e.g., the MC680X0 family, etc.); it should be configured to operate in the "Motorola" mode (by tying the "MOTO" pin to Vcc). Motorola-type Programmed I/O "Read" and "Write" operations are described below.

2.2.2.1.2.1 The Motorola Mode Read Cycle

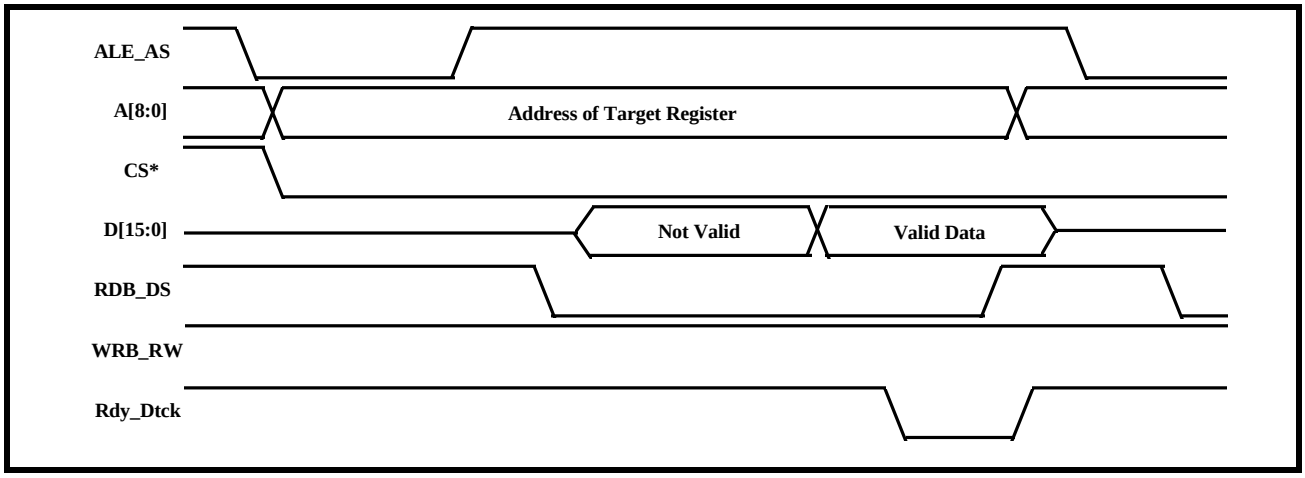
Whenever a "Motorola-type" µC/µP wishes to read the contents of a register or some location within the Receive LAPD Message or Receive OAM Cell Buffer, (within the Framer device) it should do the following.

1. Assert the ALE_AS (Address-Strobe) input pin by toggling it low. This step enables the Address Bus input drivers, within the Microprocessor Interface Block of the Framer IC.
2. Place the address of the "target" register (or buffer location) within the Framer, on the Address Bus input pins, A[8:0].
3. At the same time, the Address Decoding circuitry (within the user's system) should assert the CS* (Chip Select) input pin of the Framer device, by toggling it "low". This action enables further communication between the µC/µP and the Framer Microprocessor Interface block.
4. After allowing the data on the Address Bus pins to settle (by waiting the appropriate "Address Setup" time), the µC/µP should toggle the ALE_AS input pin "high". This step causes the Framer device to latch the contents of the "Address Bus" into its internal circuitry. At this point, the address of the register or buffer location (within the Framer) has now been selected.
5. Further, the µC/µP should indicate that this cycle is a "Read" cycle by setting the WRB_RW (R/W*) input pin "high".
6. Next the µC/µP should initiate the current bus cycle by toggling the RdB_DS (Data Strobe) input pin "low". This step enables the bi-directional data bus output drivers, within the XRT 72L13 DS3 Framer. At this point, the bi-directional data bus output drivers will proceed to driver the contents of the "Address" register onto the bi-directional data bus, D[7:0].
7. After some settling time, the data on the "bi-directional" data bus will stabilize and can be read by the µC/µP. The XRT 72L13 DS3 Framer will indicate that this data can be read by asserting the Rdy_Dtck (DTACK) signal.
8. After the µC/µP detects the Rdy_Dtck signal (from the XRT 72L13 DS3 Framer) it will termi-

nate the Read Cycle by toggling the "RdB_DS" (Data Strobe) input pin "high".

Figure 36 presents a timing diagram which illustrates the behavior of the Microprocessor Interface signals during a "Motorola-type" Programmed I/O Read Operation.

FIGURE 36. ILLUSTRATION OF THE BEHAVIOR OF MICROPROCESSOR INTERFACE SIGNALS, DURING A "MOTOROLA-TYPE" PROGRAMMED I/O READ OPERATION



2.2.2.1.2.2 The Motorola Mode Write Cycle

Whenever a Motorola-type µC/µP wishes to write a byte or word of data into a register or buffer location, within the Framer, it should do the following.

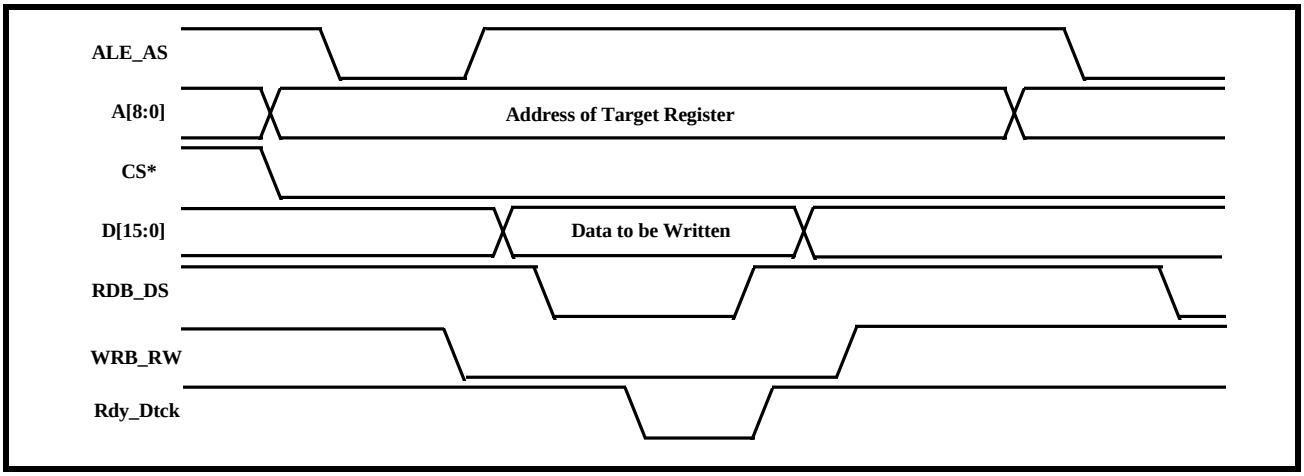
1. Assert the ALE_AS (Address Select) input pin by toggling it "low". This step enables the "Address Bus" input drivers (within the Framer chip).
2. Place the address of the "target" register or buffer location (within the Framer), on the Address Bus input pins, A[8:0].
3. While the µC/µP is placing this address value onto the Address Bus, the Address-Decoding circuitry (within the user's system) should assert the CS* (Chip Select) input pins of the Framer by toggling it "low". This step enables further communication between the µC/µP and the Framer Microprocessor Interface block.
4. After allowing the data on the Address Bus pins to settle (by waiting the appropriate "Address Setup" time), the µC/µP should toggle the ALE_AS input pin "high". This step causes the Framer device to "latch" the contents of the "Address Bus" into its own circuitry. At this point, the Address of the register or buffer location (within the Framer), has now been selected.
5. Further, the µC/µP should indicate that this current bus cycle is a "Write" operation by toggling the WRB_RW (R/W*) input pin "low".
6. The µC/µP should then place the byte or word that it intends to write into the "target" register, on the bi-directional data bus, D[7:0].
7. Next, the µC/µP should initiate the bus cycle by toggling the RdB_DS (Data Strobe) input pin "low". When the XRT 72L13 DS3 Framer senses that the WRB_RW (R/W*) input pin is "high" and that the RdB_DS (Data Strobe) input pin has toggled "low", it will enable the "input drivers" of the bi-directional data bus, D[7:0].
8. After waiting the appropriate time, for this newly placed data to settle on the bi-directional data bus (e.g., the "Data Setup" time) the Framer will assert the Rdy_Dtck output signal.
9. After the µC/µP detects the Rdy_Dtck signal (from the Framer), the µC/µP should toggle the RdB_DS input pin "high". This action accomplishes two things.

a. It latches the contents of the bi-directional data bus into the XRT72L13 Microprocessor Interface block.

b. It terminates the "Write" cycle.

Figure 37 presents a timing diagram which illustrates the behavior of the Microprocessor Interface signals, during a "Motorola-type" Programmed I/O Write Operation.

FIGURE 37. ILLUSTRATION OF THE BEHAVIOR OF THE MICROPROCESSOR INTERFACE SIGNAL, DURING A "MOTOROLA-TYPE" PROGRAMMED I/O WRITE OPERATION



2.2.2.2 Data Access using Burst Mode I/O

Burst Mode I/O access is a much faster way to transfer data between the µC/µP and the Microprocessor Interface (of the XRT 72L13 DS3 Framer), than Programmed I/O. The reason why Burst Mode I/O is so much faster follows.

Data is placed upon the Address Bus input pins A[8:0]; only for the very first access, within a given burst access. The remaining read or write operations (within this burst access) do not require the placement of the Address Data on the Address Data Bus. As a consequence, the user does not have to wait through the "Address Setup" and "Hold" times; for each of these Read/Write operation, within the "Burst" Access.

It is important to note that there are some limitations associated with Burst Mode I/O Operations.

1. All cycles within the Burst Access, must be either "all Read" or "all Write" cycles. No "mixing of "Read" and "Write" cycles is permitted.
2. A Burst Access can only be used when "Read" or "Write" operations are to be employed over a contiguous range of address locations, within the Framer device.
3. The very first "Read" or "Write" cycle, within a burst access, must start at the "lowest" address value, of the range of addresses to be accessed. Subsequent operations will automatically be incremented to the very next higher address value.

Examples of Burst Mode I/O operations are presented below for read and write operations, with both "Intel-type" and "Motorola-type" µC/µP.

2.2.2.2.1 Burst I/O Access in the Intel Mode

If the XRT 72L13 DS3 Framer is interfaced to an "Intel-type" µC/µP (e.g., the 80x86 family, etc.), then it should be configured to operate in the "Intel" mode (by tying the "MOTO" pin to ground). Intel-type "Read" and "Write" Burst I/O Access operations are described below.

2.2.2.2.1.1 The "Intel-Mode" Read Burst Access

Whenever an "Intel-type" µC/µP wishes to read the contents of numerous registers or buffer locations over a "contiguous" range of addresses; then it should do the following.

a. Perform the initial "read" operation of the burst access.

b. Perform the remaining "read" operations of the burst access.

c. Terminate the "burst access" operation.

Each of these "operations" within the burst access are described below.

2.2.2.2.1.1.1 The Initial Read Operation

The initial read operation of an "Intel-type" read burst access is accomplished by executing a "Programmed I/O" Read Cycle as summarized below.

A.0 Execute a Single Ordinary (Programmed I/O) Read Cycle, as described in steps A.1 through A.7 below.

A.1 Place the address of the "initial-target" register or buffer location (within the Framer) on the Address Bus input pins A[8:0].

A.2 While the µC/µP is placing this address value onto the Address Bus, the Address Decoding

circuitry (within the user's system) should assert the CS* input pin of the Framer, by toggling it "low". This step enables further communication between the µC/µP and the Framer Microprocessor Interface block.

A.3 Assert the ALE_AS (Address Latch Enable) pin by toggling it "high". This step enables the "Address Bus" input drivers, within the Microprocessor Interface block of the Framer.

A.4 After allowing the data on the Address Bus pins to settle (by waiting the appropriate "Address" Data Setup time"), the µC/µP should then toggle the ALE_AS pin "low". This step latches the contents, on the Address Bus pins, A[8:0], into the XRT 72L13 DS3 Framer Microprocessor Interface block. At this point, the "initial" address of the burst access has now been selected.

NOTE: *The ALE_AS input pin should remain "low" for the remainder of this "Burst Access" operation.*

A.5 Next, the µC/µP should indicate that this current bus cycle is a "Read" Operation by toggling the RdB_DS (Read Strobe) input pin "low". This action also enables the "bi-directional" data bus output drivers of the Framer device. At this point, the bi-directional data bus output drivers will proceed to drive the contents of the "addressed" register onto the "bi-directional" data bus, D[7:0].

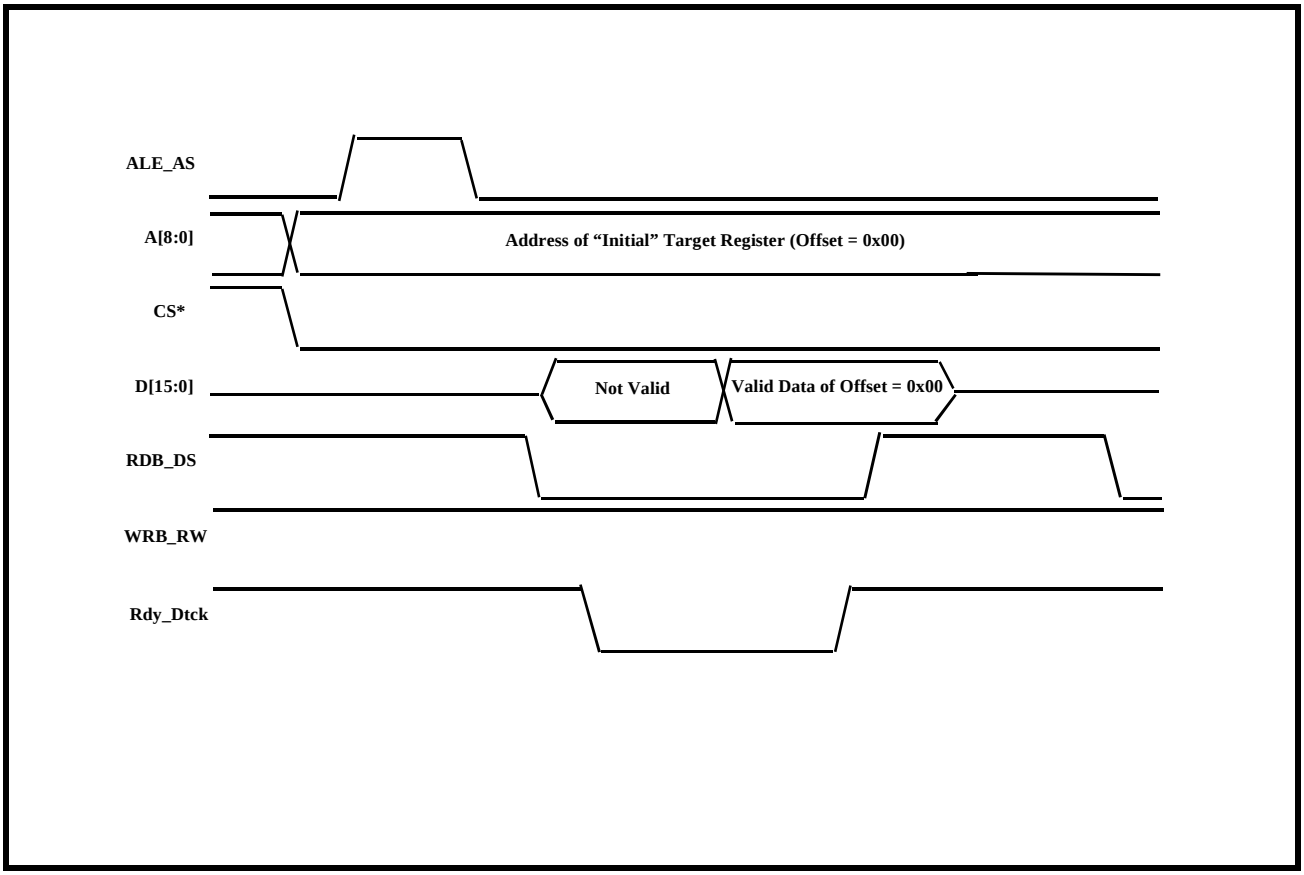
A.6 Immediately after the µC/µP toggles the "Read Strobe" signal "low", the Framer device will toggle the Rdy_Dtck (READY) output pin "low". The Framer device does this in order to inform the µC/µP that the data (to be read from the data bus) is "NOT READY" to be latched into the µC/µP.

A.7 After some settling time, the data on the "bi-directional" data bus will stabilize and can be read by the µC/µP. The XRT 72L13 DS3 Framer will indicate that this data is ready to be read, by toggling the Rdy_Dtck (Ready) signal "high".

A.8 After the µC/µP detects the Rdy_Dtck signal (from the XRT 72L13 DS3 Framer IC), it can then will terminate the "Read" cycle by toggling the RdB_DS (Read Strobe) input pin "high".

Figure 38 presents an illustration of the behavior of the Microprocessor Interface Signals, during the "initial" Read Operation, within a Burst I/O Cycle; for an Intel-type µC/µP.

FIGURE 38. BEHAVIOR OF THE MICROPROCESSOR INTERFACE SIGNALS, DURING THE "INITIAL" READ OPERATION OF A BURST CYCLE (INTEL TYPE PROCESSOR)



At the completion of this initial read cycle, the µC/µP has read in the contents of the first register or buffer location (within the XRT 72L13 DS3 Framer) for this particular burst I/O access operation. In order to illustrate how this "burst access operation" works, the byte (or word) of data, that is being read in Figure 38, has been labeled "Valid Data at Offset = 0x00". This label indicates that the µC/µP is reading the very first register (or buffer location) in this burst access operation.

2.2.2.2.1.1.2 The Subsequent Read Operations

The procedure that the µC/µP must use to perform the remaining read cycles, within this Burst Access operation, is presented below.

B.0 Execute each subsequent Read Cycles, as described in steps 1 through 3 below.

B.1 Without toggling the ALE_AS input pin (e.g., keeping it "low"); toggle the RdB_DS input pin "low". This step accomplishes the following.

a. The Framer will internally increments the "latched address" value (within the Microprocessor Interface circuitry).

b. The output drivers of the "bi-directional" data bus, D[7:0] are enabled. At some time later, the register or buffer location corresponding to the "incremented" latched address value will be driven onto the bi-directional data bus.

B.2 Immediately after the "Read Strobe" pin toggles "low" the Framer IC will toggle the Rdy_Dtck (READY) output pin "low" to indicate its "NOT READY" status.

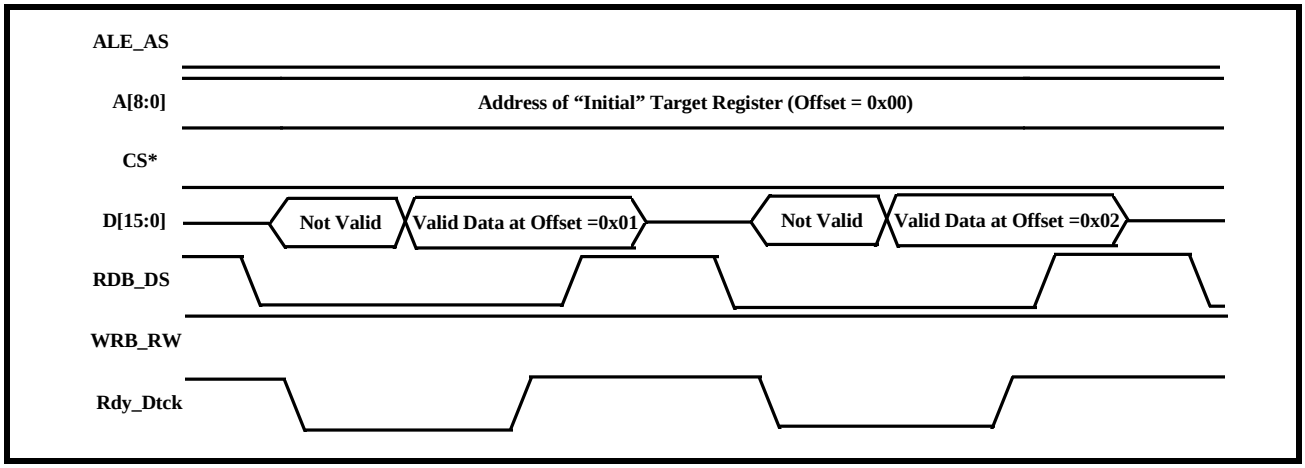
B.3 After some settling time, the data on the bi-directional data bus will stabilize and can be read by the µC/µP. The XRT 72L13 DS3 Framer will indicate that this data is ready to be read by toggling the Rdy_Dtck (READY) signal "high".

B.4 After the µC/µP detects the Rdy_Dtck signal (from the XRT 72L13 DS3 Framer), it can then

terminates the "Read" cycle by toggling the RdB_DS (Read Strobe) input pin "high".

For subsequent read operations, within this burst cycle, the µC/µP simply repeats steps 1 through 3, as illustrated in Figure 39.

FIGURE 39. BEHAVIOR OF THE MICROPROCESSOR INTERFACE SIGNALS, DURING SUBSEQUENT "READ" OPERATIONS WITHIN THE BURST I/O CYCLE



In addition to the behavior of the Microprocessor Interface signals, Figure 39 also illustrates other points regarding the "Burst Access Operation".

a. The Framer internally increments the address value, from the original "latched" value shown in Figure 38. This is illustrated by the data, appearing on the data bus, (for the first read access) being labeled "Valid Data at Offset = 0x01"; and that for the second read access being labeled "Valid Data at Offset = 0x02.".

b. The Framer performs this "address incrementing" process even though there are no changes in the Address Bus Data, A[8:0].

2.2.2.2.1.1.3 Terminating the Burst Access Operation

The Burst Access Operation will be terminated upon the rising edge of the ALE_AS input signal. At this point the Framer will cease to internally increment the "latched" address value. Further, the µC/µP is now free to execute either a "Programmed I/O" access or to start another "Burst Access" Operation with the XRT 72L13 DS3 Framer.

2.2.2.2.1.2 The "Intel-Mode" Write Burst Access

Whenever an "Intel-type" µC/µP wishes to write data into a "contiguous" range of addresses, then it should do the following.

a. Perform the initial "write" operation; of the burst access.

b. Perform the remaining "write" operations, of the burst access.

c. Terminate the burst access operation.

Each of these "operations" within the burst access are described below.

2.2.2.2.1.2.1 The Initial Write Operation

The initial write operation of an "Intel-type" Write Burst Access is accomplished by executing a "Programmed I/O" write cycle as summarized below.

A.0 Execute a Single Ordinary (Programmed I/O) Write cycle, as described in Steps A.1 through A.7 below.

A.1 Place the address of the "initial" target register (or buffer location) within the Framer, on the Address Bus pins, A[8:0].

A.2 A.2 At the same time, the "Address-Decoding" circuitry (within the user's system) should assert the CS* (Chip Select) input pin of the Framer, by toggling it "low". This step enables further communication between the µC/µP and the Framer Microprocessor Interface block.

A.3 Assert the ALE_AS (Address Latch Enable) input pin "high". This step enables the Address Bus input drivers, within the Microprocessor Interface Block of the Framer.

A.4 After allowing the data on the Address Bus pins to settle (by waiting the appropriate "Address Setup" time); the µC/µP should then toggle the ALE_AS input pin "low". This step latches the

contents, on the Address Bus pins, A[8:0], into the XRT 72L13 DS3 Framer Microprocessor Interface block. At this point, the "initial" address of the "burst access" has now been selected.

NOTE: *The ALE_AS input pin should remain "low" for the remainder of this "Burst I/O Access" operation.*

A.5 Next, the µC/µP should indicate that this current bus cycle is a "Write" operation by keeping the RdB_DS pin "high" and toggling the WRB_RW (Write Strobe) pin "low". This action also enables the "bi-directional" data bus input drivers of the Framer device.

A.6 The µC/µP places the byte (or word) that it intends to write into the "target" register on the "bi-directional data" bus, D[7:0].

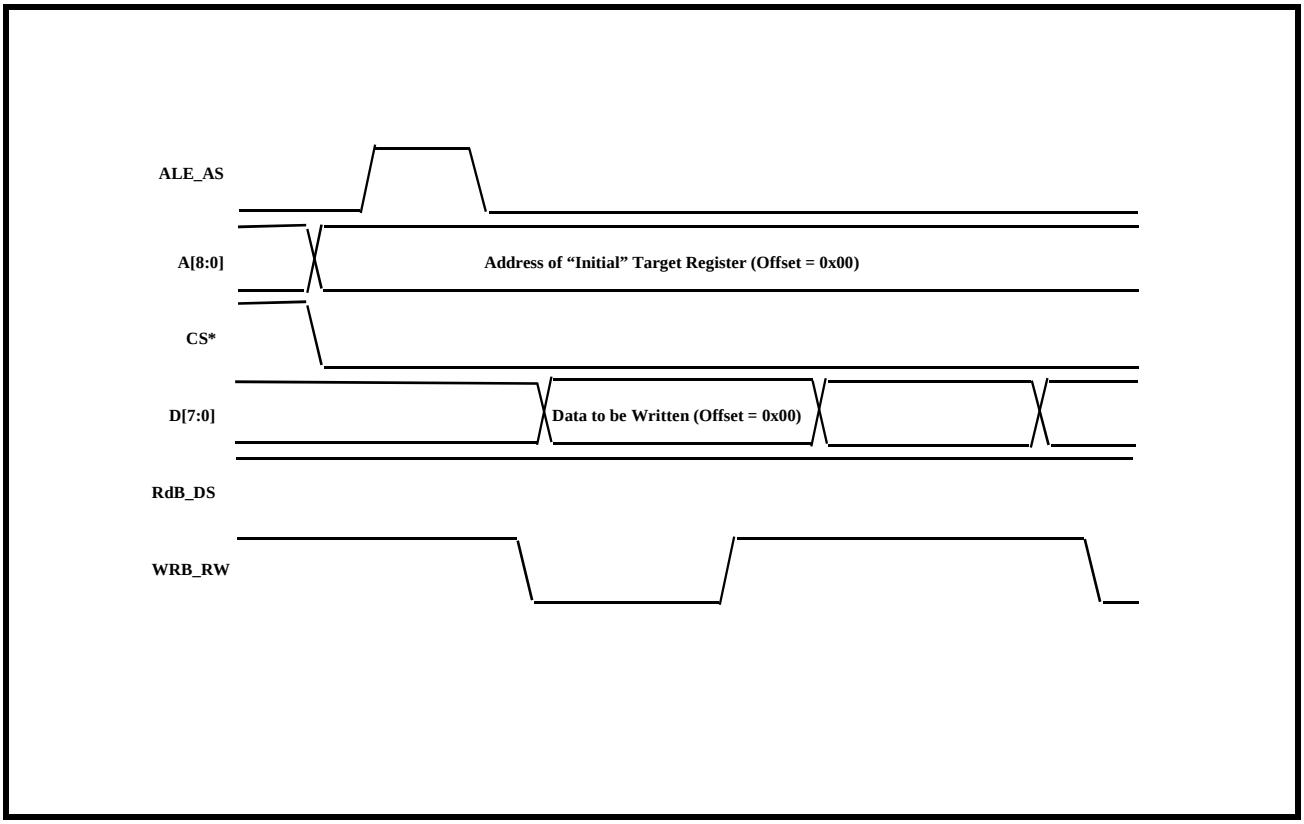
A.7 After waiting the appropriate amount of time, for the data (on the bi-directional data bus) to settle, the µC/µP should toggle the WRB_RW (Write Strobe) input pin "high". This action accomplishes two things.

a. It latches the contents of the bi-directional data bus into the XRT 72L13 DS3 Framer Microprocessor Interface Block.

b. It terminates the write cycle.

Figure 40 presents a timing diagram which illustrates the behavior of the Microprocessor Interface signals, during the "initial" write operation within a Burst Access, for an "Intel-type" µC/µP.

FIGURE 40. BEHAVIOR OF THE MICROPROCESSOR INTERFACE SIGNALS, DURING THE "INITIAL" WRITE OPERATION OF A BURST CYCLE (INTEL-TYPE PROCESSOR)



At the completion of this initial write cycle, the µC/µP has written a byte or word into the first register or buffer location (within the XRT 72L13 DS3 Framer) for this particular burst access operation. In order to illustrate this point, the byte (or word) of data, that is being written in Figure 40 has been labeled "Data to be Written (Offset = 0x00)".

2.2.2.2.1.2.2 The Subsequent Write Operations

The procedure that the µC/µP must use to perform the remaining write cycles, within this burst access operation, is presented below.

B.0 Execute each subsequent write cycle, as described in steps B.1 through B.3.

B.1 Without toggling the ALE_AS input pin (e.g., keeping it "low"); apply the value of the next

byte or word (to be written into the Framer) to the bi-directional data bus pins, D[7:0].

B.2 Toggle the WRB_RW (Write Strobe) input pin "low". This step accomplishes two things.

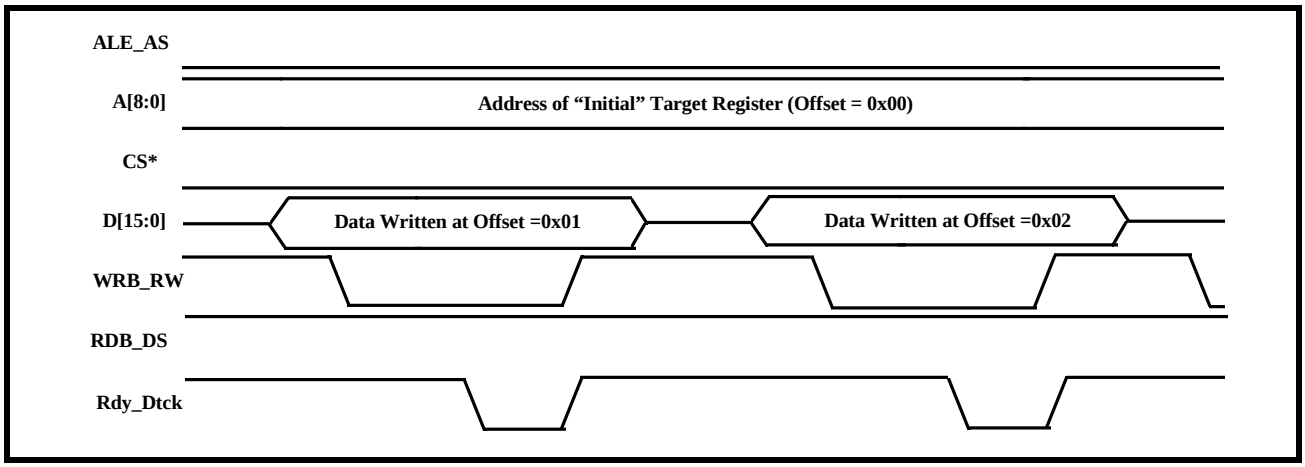
a. It enables the input drivers of the bi-directional data bus.

b. It causes the Framer to internally increment the value of the "latched" address.

B.3 After waiting the appropriate amount of settling time the data, in the internal data bus, will stabilize and is ready to be latched into the Framer Microprocessor Interface block. At this point, the µC/µP should latch the data into the Framer by toggling the WRB_RW input pin "high".

For subsequent write operations, within this burst I/O access, the µC/µP simply repeats steps B.1 through B.3, as illustrated in Figure 41.

FIGURE 41. BEHAVIOR OF THE MICROPROCESSOR INTERFACE SIGNALS, DURING SUBSEQUENT "WRITE" OPERATIONS WITHIN THE BURST I/O CYCLE



2.2.2.2.1.2.3 Terminating the Burst I/O Access

Burst Access Operation will be terminated upon the rising edge of the ALE_AS input signal. At this point the Framer will cease to internally increment the "latched" address value. Further, the µC/µP is now free to execute either a "Programmed I/O" access or to start another "Burst Access Operation" with the XRT 72L13 DS3 Framer.

2.2.2.2.2 Burst I/O Access in the Motorola Mode

If the XRT 72L13 DS3 Framer is interfaced to a "Motorola-type" µC/µP (e.g., the MC680x0 family, etc.), then it should be configured to operate in the "Motorola" mode (by tying the "MOTO" pin to VCC). Motorola-type "Read" and "Write" Burst I/O Access operations are described below.

2.2.2.2.2.1 The "Motorola-Mode" Read Burst I/O Access Operation

Whenever a "Motorola-type" µC/µP wishes to read the contents of numerous registers or buffer locations over a "contiguous" range of addresses, then it should do the following.

a. Perform the initial "Read" operation of the burst access.

b. Perform the remaining "read" operations; in the burst access.

c. Terminate the "burst access" operation.

Each of these operations, within the Burst Access are discussed below.

2.2.2.2.2.1.1 The Initial Read Operation

The initial read operation of a "Motorola-type" read burst access is accomplished by executing a "Programmed I/O Read" cycle, as summarized below.

A.0 Execute a Single Ordinary (Programmed I/O) Read Cycle, as described in steps A.1 through A.8 below.

A.1 Assert the ALE_AS (AS*) input pin by toggling it "low". This step enables the "Address Bus" input drivers (within the XRT 72L13 DS3 Framer) within the Framer Microprocessor Interface Block.

A.2 Place the address of the "initial" target register or buffer location (within the Framer), on the Address Bus input pins, A[8:0].

A.3 At the same time, the Address-Decoding circuitry (within the user's system) should assert the CS* (Chip Select) input pins of the Framer

by toggling it "low". This action enables further communication between the µC/µP and the Framer Microprocessor Interface block.

A.4 After allowing the data on the Address Bus pins to settle (by waiting the appropriate "Address Setup" time), the µC/µP should toggle the ALE_AS input pin "high". This step causes the Framer device to latch the contents of the Address Bus into its internal circuitry. At this point, the "initial" address of the burst access has now been selected.

A.5 Further, the µC/µP should indicate that this cycle is a "Read" cycle by setting the WRB_RW (R/W*) input pin "high".

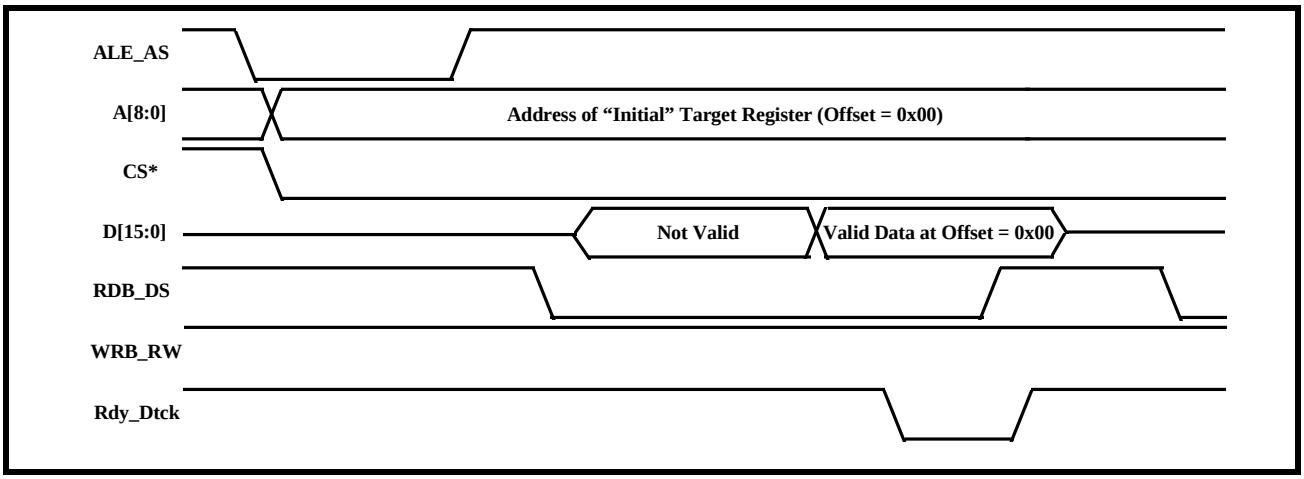
A.6 Next the µC/µP should initiate the current bus cycle by toggling the RdB_DS (Data Strobe) input pin "low". This step will enable the bi-directional data bus output drivers, within the XRT 72L13 DS3 Framer. At this point, the bi-directional data bus output drivers will proceed to driver the contents of the "Address" register onto the bi-directional data bus.

A.7 After some settling time, the data on the bi-directional data bus will stabilize and can be read by the µC/µP. The XRT 72L13 DS3 Framer will indicate that this data can be read by asserting the Rdy_Dtck (DTACK) signal.

A.8 After the µC/µP detects the Rdy_Dtck signal (from the XRT 72L13 DS3 Framer) it will terminate the Read Cycle by toggling the "RdB_DS" (Data Strobe) input pin "high".

Figure 42 presents an illustration of the behavior of the Microprocessor Interface Signals during the "initial" Read Operation, within a Burst I/O Cycle; for a Motorola-type µC/µP.

FIGURE 42. BEHAVIOR OF THE MICROPROCESSOR INTERFACE SIGNALS, DURING THE "INITIAL" READ OPERATION OF A BURST CYCLE (MOTOROLA TYPE PROCESSOR)



At the completion of this initial read cycle, the µC/µP has read in the contents of the first register or buffer location (within the XRT 72L13 DS3 Framer) for this particular burst access operation. In order to illustrate how this "burst I/O cycle" works, the byte (or word) of data, that is being read in Figure 42 has been labeled "Valid Data at Offset = 0x00". This indicates that the µC/µP is reading the very first register (or buffer location) in this burst access.

2.2.2.2.2.1.2 The Subsequent Read Operations

The procedure that the µC/µP must use to perform the remaining read cycles, within this Burst Access operation, is presented below.

B.0 Execute each subsequent Read Cycle, as described in steps B.1 through B.3, below.

B.1 Without toggling the ALE_AS input pin (e.g., keeping it "high"); toggle the RdB_DS (Data Strobe) input pin "low". This step accomplishes the following.

a. The Framer internally increments the "latched address" value (within the Microprocessor Interface circuitry).

b. The output drivers of the "bi-directional" data bus (D[7:0]) are enabled. At some time later, the register or buffer location corresponding to the "incremented" latched address value will be driven onto the bi-directional data bus.

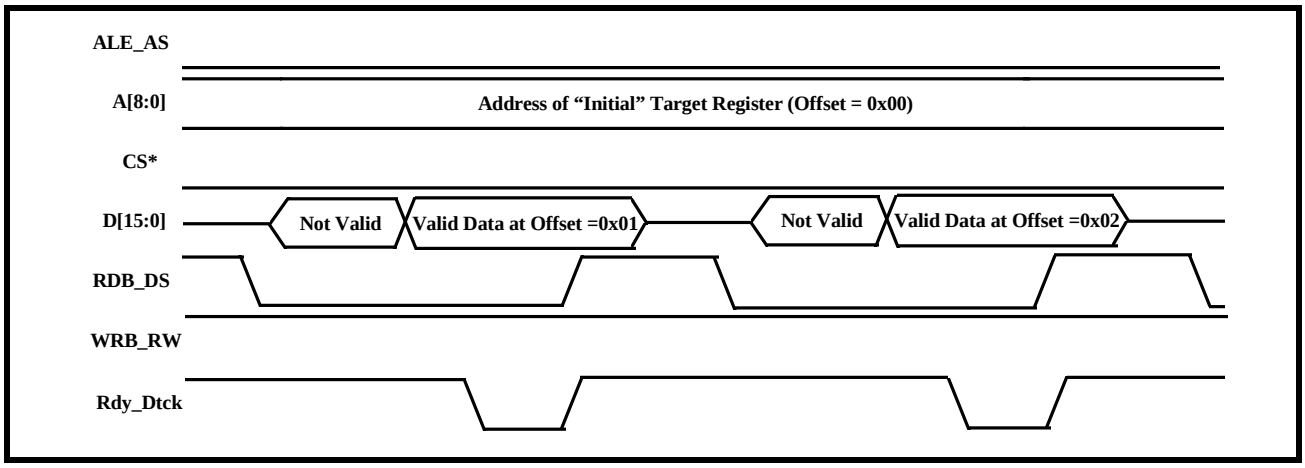
NOTE: *In order to insure that the XRT 72L13 DS3 Framer will interpret this signal as being a "Read" signal, the* µC/µP *should keep the WRB_RW input pin "High".*

B.2 After some settling time, the data on the bi-directional data bus will stabilize and can be read by the µC/µP. The XRT 72L13 DS3 Framer will indicate that this data is ready to be read by asserting the Rdy_Dtck (DTACK*) signal.

B.3 After the µC/µP detects the Rdy_Dtck signal (from the XRT 72L13 DS3 Framer), it terminates the "Read" cycle by toggling the RdB_DS (Data Strobe) input pin "high".

For subsequent read operations, within this burst cycle, the µC/µP simply repeats steps B.1 through B.3, as illustrated in Figure 43.

FIGURE 43. BEHAVIOR THE MICROPROCESSOR INTERFACE SIGNALS, DURING SUBSEQUENT "READ" OPERATIONS WITHIN THE BURST I/O CYCLE (MOTOROLA-TYPE µC/µP)



2.2.2.2.2.1.3 Terminating the Burst Access Operation

The Burst I/O Access will be terminated upon the falling edge of the ALE_AS input signal. At this point the Framer will cease to internally increment the "latched" address value. Further, the µC/µP is now free to execute either a "Programmed I/O" access or to start another "Burst Access" Operation with the XRT 72L13 DS3 Framer.

2.2.2.2.2.2 The "Motorola-Mode" Write Burst Access

Whenever a "Motorola-type" µC/µP wishes to write the contents of numerous registers or buffer locations over a "contiguous" range of addresses, then it should do the following.

a. Perform the initial "write" operation; of the burst access.

b. Perform the remaining "write" operations, of the burst access.

c. Terminate the burst access operation.

Each of these "operations" within the burst access are described below.

2.2.2.2.2.2.1 The Initial Write Operation

The initial write operation of a "Motorola-type" Write Burst Access is accomplished by executing a "Programmed I/O Write Cycle" as summarized below.

A.0 Execute a Single Ordinary (Programmed I/O) Write cycle, as described in Steps A.1 through A.7 below.

A.1 Assert the ALE_AS (Address Strobe) input pin by toggling it "low". This step enables the Address Bus input drivers (within the XRT 72L13 DS3 Framer).

A.2 Place the address of the "initial" target register or buffer location (within the Framer), on the Address Bus input pins, A[8:0].

A.3 At the same time, the Address-Decoding circuitry (within the user's system) should assert the CS* input pin of the Framer by toggling it "low". This step enables further communication between the µC/µP and the Framer Microprocessor Interface block.

A.4 After allowing the data on the Address Bus pins to settle (by waiting the appropriate "Address Setup" time), the µC/µP should toggle the ALE_AS input pin "high". This step causes the Framer device to "latch" the contents of the "Address Bus" into its own circuitry. At this point, the "initial" address of the burst access has now been selected.

A.5 Further, the µC/µP should indicate that this current bus cycle is a "Write" operation by toggling the WRB_RW (R/W*) input pin "low".

A.6 The µC/µP should then place the byte or word that it intends to write into the "target" register, on the bi-directional data bus, D[7:0].

A.7 Next, the µC/µP should initiate the bus cycle by toggling the RdB_DS (Data Strobe) input pin "low". When the XRT 72L13 DS3 Framer senses that the WRB_RW input pin is "low", and that the RdB_DS input pin has toggled "low" it will enable the "input drivers" of the bi-directional data bus, D[7:0].

A.8 After waiting the appropriate amount of time, for this newly placed data to settle on the bi-directional data bus(e.g., the "Data Setup" time) the Framer will assert the Rdy_Dtck (DTACK) output signal.

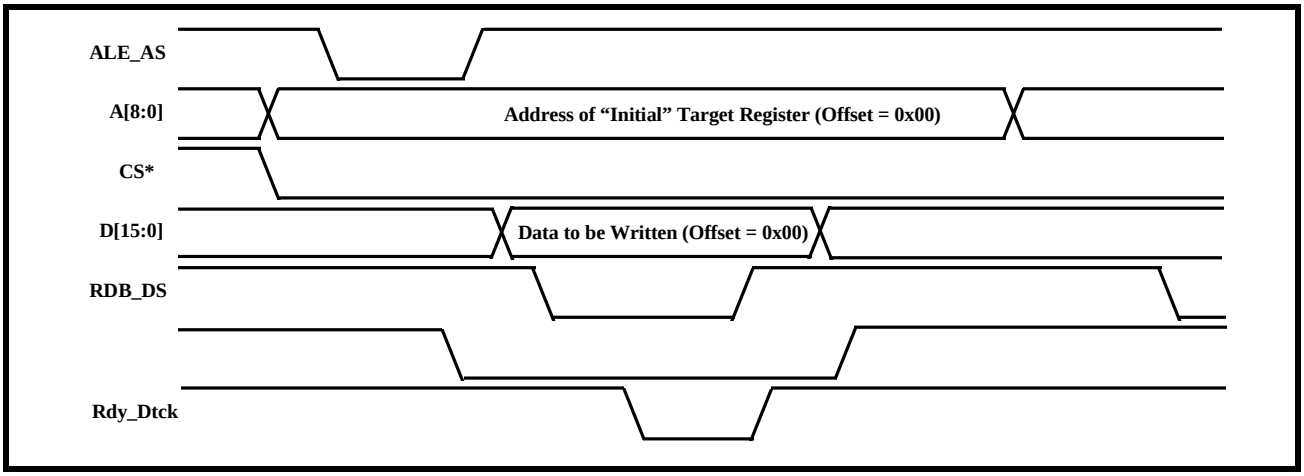
A.9 After the µP/µC detects the Rdy_Dtck signal (from the Framer) it should toggle the RdB_DS input pin "high". This action accomplishes two things:

a. It latches the contents of the bi-directional data bus into the XRT 72L13 DS3 Framer Microprocessor Interface block.

b. It terminates the "Write" cycle.

Figure 44 presents a timing diagram which illustrates the behavior of the Microprocessor Interface signals, during the "Initial" write operation within a Burst Access, for a "Motorola-type" µC/µP.

FIGURE 44. BEHAVIOR OF THE MICROPROCESSOR INTERFACE SIGNALS, DURING THE "INITIAL" WRITE OPERATION OF A BURST CYCLE (MOTOROLA-TYPE PROCESSOR)



At the completion of this initial write cycle, the µC/µP has written a byte or word into the first register or buffer location (within the XRT 72L13 DS3 Framer) for this particular burst I/O access. In order to illustrate how this "burst I/O cycle" works, the byte (or word) of data, that is being written in Figure 44 has been labeled "Data to be Written (Offset = 0x00)."

2.2.2.2.2.2.2 The Subsequent Write Operations

The procedure that the µC/µP must use to perform the remaining write cycles, within this burst access operation, is presented below.

B.0 Execute each subsequent write cycle, as described in Steps B.1 through B.3

B.1 Without toggling the ALE_AS (Address Strobe) input pin (e.g., keeping it "high"); apply the value of the next byte or word (to be written into the Framer) to the bi-directional data bus pins, D[7:0].

B.2 Toggle the RdB_DS (Data Strobe) input pin "low". This step accomplishes the following.

a. The Framer internally increments the "latched address" value (within the Microprocessor Interface).

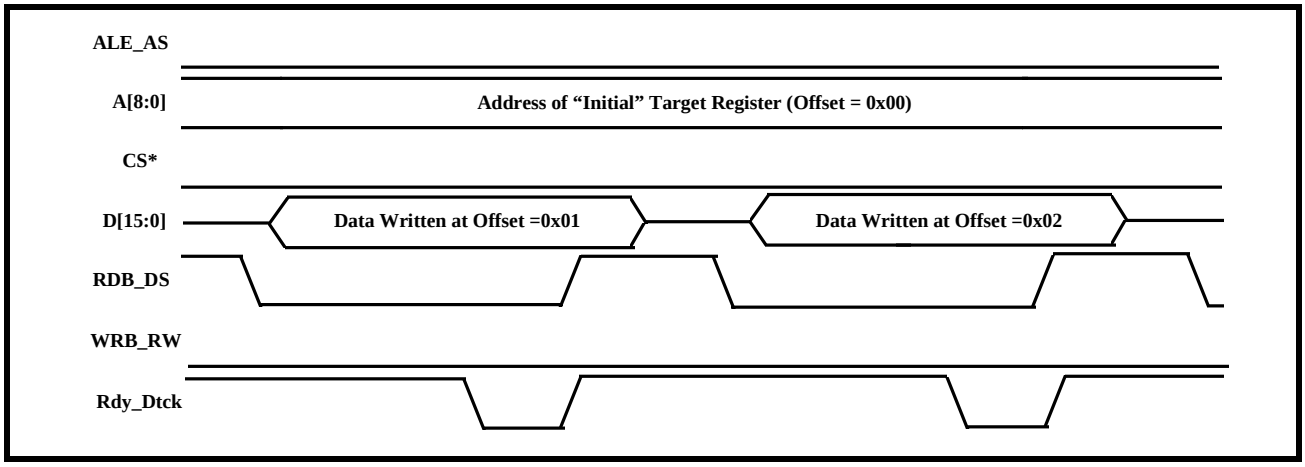
b. The input drivers of the bi-directional data bus are enabled.

NOTE: *In order to insure that the XRT 72L13 DS3 Framer will interpret this signal as being a "Write" signal, the* µC/µP *should keep the WRB_RW input pin "low".*

B.3 After some settling time, the data, in the internal data bus, will stabilize and is ready to be latched into the Framer Microprocessor Interface block. The Microprocessor Interface block will indicate that this data is ready to be latched by asserting the Rdy_Dtck (DTACK) output signal. At this point, the µC/µP should latch the data into the Framer by toggling the RDB_DS input pin "high".

For subsequent write operations, within this burst I/O access, the µC/µP simply repeats steps B.1 through B.3 as illustrated in Figure 45.

FIGURE 45. BEHAVIOR OF THE MICROPROCESSOR INTERFACE SIGNALS, DURING SUBSEQUENT "WRITE" OPERATIONS WITH THE BURST I/O CYCLE (MOTOROLA-TYPE µC/µP)



2.2.2.2.2.3 Terminating the Burst I/O Access

The Burst I/O Access will be terminated upon the falling edge of the ALE_AS input signal. At this point the Framer will cease to internally increment the "latched" address value. Further, the µC/µP is now free to execute either a "Programmed I/O" access or to start another "Burst I/O Access" with the XRT72L13 DS3 Framer.

2.3 ON-CHIP REGISTER ORGANIZATION

The Microprocessor Interface section, within the Framer device allows the user to do the following.

- Configure the Framer into a wide variety of operating modes.
- Employ various features of the Framer device.
- Perform status monitoring
- Enable/Disable and service Interrupt Conditions

All of these things are accomplished by reading from and writing to the many on-chip registers within the Framer device. Table 4 lists each of these registers and their corresponding address locations within the Framer Address space.

2.3.1 Framer Register Addressing

The array of on-chip registers consists of a variety of register types. These registers are denoted in Table 4, as follows.

R/O - Read Only Registers.

R/W - Read/Write Registers

RUR - Reset-upon-Read Registers

Additionally, some of these registers consists of both "R/O" and "R/W" bit-fields. These registers are denoted in Table 4 as "Combination of R/W and R/O".

The bit-format and definitions for each of these registers are presented in Section 2.3.2

2.3.2 M13 Mux/Framer Register Description

This section provides a function description of each bit-field within each of the on-chip Framer Register.

NOTE: *For all on-chip registers, a table containing the bit-format of the register is presented. Additionally, these tables also contain the default values for each of these register bits. Finally, the function description, associated with each register bit-field is presented, along with a reference to a Section Number, within this Data Sheet, that provides a more in-depth discussion of the functions associated with this register bit-field.*

2.3.2.1 Operating Mode Register

TABLE 4: REGISTER ADDRESS MAP

ADDRESS	REGISTER NAME	TYPE	DEFAULT VALUE
0x00	Operating Mode Register	R/W	0x2B
0x01	I/O Control Register	R/W & R/O	0xA0
0x02	Part Number Register	R/O	0x22
0x03	Version Number Register	R/O	0x01
0x04	Block Interrupt Enable Register	R/W	0x00
0x05	Block Interrupt Status Register	RUR	0x00
0x06	RxFIFO Control Register	R/O and R/W	0x00
0x07	M23 Configuration Register	R/W	0x00
0x08	M23 Tx DS2 AIS Register	R/W	0x00
0x09	M23 Request Loop-Back Register	R/W	0x00
0x0A	M23 Loop-Back Activation Register	R/W	0x00
0x0B	M23 Rx DS2 AIS Register	R/W	0x00
0x0C	DS3 Test Register	R/O and R/W	0x00
0x0D - 0x0F	Reserved		
0x10	RxDS3 Configuration & Status Register	R/O and R/W	0x14
0x11	RxDS3 Status Register	R/O	0x00
0x12	RxDS3 Interrupt Enable Register	R/W	0x00
0x13	RxDS3 Interrupt Status Register	RUR	0x00
0x14	RxDS3 Sync Detect Register	R/W	0x00
0x15	Reserved		
0x16	RxDS3 FEAC Register	R/O	0xFF
0x17	RxDS3 FEAC Interrupt Enable and Status Register	R/W & R/O & RUR	0x00
0x18	RxLAPD Control Register	R/W & RUR	0x00
0x19	RxLAPD Status Register	R/O	0x00
0x1A	M12 Configuration Register - 1	R/W	0x08
0x1B	M12 Configuration Register - 2	R/W	0x08
0x1C	M12 Configuration Register - 3	R/W	0x08
0x1D	M12 Configuration Register - 4	R/W	0x08
0x1E	M12 Configuration Register - 5	R/W	0x08
0x1F	M12 Configuration Register - 6	R/W	0x08
0x20	M12 Configuration Register - 7	R/W	0x08
0x21	M12 AIS Register - 1	R/W	0x00
0x22	M12 AIS Register - 2	R/W	0x00
0x23	M12 AIS Register - 3	R/W	0x00
0x24	M12 AIS Register - 4	R/W	0x00
0x25	M12 AIS Register - 5	R/W	0x00
0x26	M12 AIS Register - 6	R/W	0x00
0x27	M12 AIS Register - 7	R/W	0x00
0x28	M12 Loop-back Register - 1	R/W	0x00
0x29	M12 Loop-back Register - 2	R/W	0x00

TABLE 4: REGISTER ADDRESS MAP

ADDRESS	REGISTER NAME	TYPE	DEFAULT VALUE
0x2A	M12 Loop-back Register - 3	R/W	0x00
0x2B	M12 Loop-back Register - 4	R/W	0x00
0x2C	M12 Loop-back Register - 5	R/W	0x00
0x2D	M12 Loop-back Register - 6	R/W	0x00
0x2E	M12 Loop-back Register - 7	R/W	0x00
0x2F	Reserved		
0x30	TxDS3 Configuration Register	R/W	0x07
0x31	TxDS3 FEAC Configuration & Status Register	R/W & R/O & RUR	0x00
0x32	TxDS3 FEAC Register	R/W	0xFF
0x33	Tx LAPD Configuration Register	R/W & R/O	0x08
0x34	TxDS3 LAPD Status and Interrupt Register	R/W & R/O & RUR	0x00
0x35	TxDS3 M-Bit Mask Register	R/W	0x00
0x36	TxDS3 F-Bit Mask Register - 1	R/W	0x00
0x37	TxDS3 F-Bit Mask Register - 2	R/W	0x00
0x38	TxDS3 F-Bit Mask Register - 3	R/W	0x00
0x39	TxDS3 F-Bit Mask Register - 4	R/W	0x00
0x3A	DS2 Framer Configuration Register -1	R/W	0x00
0x3B	DS2 Framer Configuration Register - 2	R/W	0x00
0x3C	DS2 Framer Configuration Register - 3	R/W	0x00
0x3D	DS2 Framer Configuration Register - 4	R/W	0x00
0x3E	DS2 Framer Configuration Register - 5	R/W	0x00
0x3F	DS2 Framer Configuration Register - 6	R/W	0x00
0x40	DS2 Framer Configuration Register - 7	R/W	0x00
0x41 - 0x4F	Reserved		
0x50	PMON LCV Count Register - MSB	RUR	0x00
0x51	PMON LCV Count Register - LSB	RUR	0x00
0x52	PMON Framing Bit Error Count Register - MSB	RUR	0x00
0x53	PMON Framing Bit Error Count Register - LSB	RUR	0x00
0x54	PMON P-Bit Error Count Register - MSB	RUR	0x00
0x55	PMON P-Bit Error Count Register - LSB	RUR	0x00
0x56	PMON FEBE Event Count Register - MSB	RUR	0x00
0x57	PMON FEBE Event Count Register - LSB	RUR	0x00
0x58	PMON CP-Bit Error Count Register - MSB	RUR	0x00
0x59	PMON CP-Bit Error Count Register - LSB	RUR	0x00
0x5A	PMON DS2 Framing Bit Error Count Register - 1	RUR	0x00
0x5B	PMON DS2 Framing Bit Error Count Register - 2	RUR	0x00
0x5C	PMON DS2 Framing Bit Error Count Register - 3	RUR	0x00
0x5D	PMON DS2 Framing Bit Error Count Register - 4	RUR	0x00
0x5E	PMON DS2 Framing Bit Error Count Register - 5	RUR	0x00
0x5F	PMON DS2 Framing Bit Error Count Register - 6	RUR	0x00
0x60	PMON DS2 Framing Bit Error Count Register - 7	RUR	0x00

TABLE 4: REGISTER ADDRESS MAP

ADDRESS	REGISTER NAME	TYPE	DEFAULT VALUE
0x61	PMON G.747 Parity Bit Error Count Register - 1	RUR	0x00
0x62	PMON G.747 Parity Bit Error Count Register - 2	RUR	0x00
0x63	PMON G.747 Parity Bit Error Count Register - 3	RUR	0x00
0x64	PMON G.747 Parity Bit Error Count Register - 4	RUR	0x00
0x65	PMON G.747 Parity Bit Error Count Register - 5	RUR	0x00
0x66	PMON G.747 Parity Bit Error Count Register - 6	RUR	0x00
0x67	PMON G.747 Parity Bit Error Count Register - 7	RUR	0x00
0x68 - 0x6B	Reserved		
0x6C	PMON Holding Register	R/O	0x00
0x6D	One Second Error Status Register	R/O	0x00
0x6E	One Second - LCV Accumulation Register - MSB	R/O	0x00
0x6F	One Second - LCV Accumulation Register - LSB	R/O	0x00
0x70	One Second - P-Bit Error Accumulation Register - MSB	R/O	0x00
0x71	One Second - P- Bit Error Accumulation Register - LSB	R/O	0x00
0x72	One Second - CP-Bit Error Accumulation Register - MSB	R/O	0x00
0x73	One Second - CP-Bit Error Accumulation Register - LSB	R/O	0x00
0x74 - 0x7F	Reserved		
0x80	Line Interface Drive Register	R/W	0x00
0x81	Line Interface Scan Register	R/O	0x00
0x82 - 0x8F	Reserved		
0x90	M23 RxDS2 Loop-back Request Interrupt Enable Register	R/W	0x00
0x91	M23 RxDS2 Loop-Back Request Interrupt Register	RUR	0x00
0x92	M23 RxDS2 Loop-Back Request Status Register	R/O	0x00
0x93	M12 Loop-back Interrupt Status/Enable Register - 1	R/W & RUR	0x00
0x94	M12 Loop-back Status Register - 1	R/O	0x00
0x95	M12 Loop-back Interrupt Status/Enable Register - 2	R/W & RUR	0x00
0x96	M12 Loop-back Status Register - 2	R/O	0x00
0x97	M12 Loop-back Interrupt Status/Enable Register - 3	R/W & RUR	0x00
0x98	M12 Loop-back Status Register - 3	R/O	0x00
0x99	M12 Loop-back Interrupt Status/Enable Register - 4	R/W & RUR	0x00
0x9A	M12 Loop-back Status Register - 4	R/O	0x00
0x9B	M12 Loop-back Interrupt Status/Enable Register - 5	R/W & RUR	0x00
0x9C	M12 Loop-back Status Register - 5	R/O	0x00
0x9D	M12 Loop-back Interrupt Status/Enable Register - 6	R/W & RUR	0x00
0x9E	M12 Loop-back Status Register - 6	R/O	0x00
0x9F	M12 Loop-back Interrupt Status/Enable Register - 7	R/W & RUR	0x00
0xA0	M12 Loop-back Status Register - 7	R/O	0x00
0xA1	DS2 Framer Interrupt Enable Register - 1	R/W	0x00
0xA2	DS2 Framer Interrupt Register - 1	RUR	0x00
0xA3	DS2 Framer Interrupt Status Register - 1	R/O	0x00
0xA4	DS2 Framer Interrupt Enable Register - 2	R/W	0x00

TABLE 4: REGISTER ADDRESS MAP

ADDRESS	REGISTER NAME	TYPE	DEFAULT VALUE
0xA5	DS2 Framer Interrupt Register - 2	RUR	0x00
0xA6	DS2 Framer Interrupt Status Register - 2	R/O	0x00
0xA7	DS2 Framer Interrupt Enable Register - 3	R/W	0x00
0xA8	DS2 Framer Interrupt Register - 3	RUR	0x00
0xA9	DS2 Framer Interrupt Status Register - 3	R/O	0x00
0xAA	DS2 Framer Interrupt Enable Register - 4	R/W	0x00
0xAB	DS2 Framer Interrupt Register - 4	RUR	0x00
0xAC	DS2 Framer Interrupt Status Register - 4	R/O	0x00
0xAD	DS2 Framer Interrupt Enable Register - 5	R/W	0x00
0xAE	DS2 Framer Interrupt Register - 5	RUR	0x00
0xAF	DS2 Framer Interrupt Status Register - 5	R/O	0x00
0xB0	DS2 Framer Interrupt Enable Register - 6	R/W	0x00
0xB1	DS2 Framer Interrupt Register - 6	RUR	0x00
0xB2	DS2 Framer Interrupt Status Register - 6	R/O	0x00
0xB3	DS2 Framer Interrupt Enable Register - 7	R/W	0x00
0xB4	DS2 Framer Interrupt Register - 7	RUR	0x00
0xB5	DS2 Framer Interrupt Status Register - 7	R/O	0x00
0xB6 - 0xFF	Reserved		
0x100 - 0x157	Transmit LAPD Message Buffer (PMDL Messages)	R/W	
0x158	Receive LAPD Message Buffer (PMDL Messages)	R/O	

2.3.2.2 Operating Mode Register

OPERATING MODE REGISTER (ADDRESS = 0X00)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Local Loop-back Mode	Line Loop-back Mode	Internal LOS Enable	RESET	Interrupt Enable RESET	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	1	0	1	0	1	1

Bit 7 - Local Loop-back Mode

This bit-field permits the user to configure the XRT72L13 M13 device to operate in the “Local Loop-back” Mode.

Setting this bit-field to “1” configures the XRT72L13 M13 chip to operate in the “Local Loopback” Mode. Setting this bit-field to “0” configures the XRT72L13 M13 chip to not operate in the “Local Loopback” Mode.

Bit 6 - Line Loopback Mode

This bit-field permits the user to configure the XRT72L13 M13 device to operate in the “Line Loop-back” Mode.

Setting this bit-field to “1” configures the XRT72L13 M13 chip to operate in the “Line Loopback” Mode. Setting this bit-field to “0” configures the XRT72L13 M13 chip to not operate in the “Line Loopback” Mode.

Bit 5 - Internal LOS Enable

This “Read/Write” bit-field permits the user to configure the XRT72L13 M13 chip to either declare an LOS (Loss of Signal) condition, based upon the “Internal Circuit’s” criteria or not.

Setting this bit-field to “0” configures the XRT72L13 M13 chip to NOT declare an LOS condition, based upon its own internal criteria.

Setting this bit-field to “1” configures the XRT72L13 LOS condition, based upon its own internal criteria.

NOTES:

1. *The XRT72L13 M13 chip will declare an “LOS” condition anytime the RLOS input pin is set “high” independent of the setting of this bit-field.*
2. *For more information on the XRT72L13 M13 chip’s “internal criteria” for “Loss of Signal” please see Section _.*

Bit 4 - RESET

This “Read/Write” bit-field permits the user to command the XRT72L13 M13 chip into a software reset state. If the XRT72L13 M13 chip is commanded into the “RESET” state, all of its internal register bits will automatically be set to their default condition.

The user can configure the XRT72L13 to operate in the “RESET” state by inducing a “0” to “1” transition in this bit-field.

Bit 3 - Interrupt Enable RESET

This “Read/Write” bit-field permits the user to configure the XRT72L13 M13 chip to automatically disable all Interrupts that are activated.

Setting this bit-field to “0” configures the XRT72L13 M13 chip to NOT disable the Interrupt Enable Status” of any interrupt following their activation.

Setting this bit-field to “1” configures the XRT72L13 M13 to disable the Interrupt Enable Status” of any interrupt following their activation.

For more information on this feature, please see Section _.

Bit 2 - Frame Format Select

This “Read/Write” bit-field permits the user to select the Framing format that the XRT72L13 M13 device will be operating in.

Setting this bit-field to “0” configures the XRT72L13 M13 device to operate in the C-Bit Parity Framing Format.

Setting this bit-field to “1” configures the XRT72L13 M13 device to operate in the M13 Framing Format.

Bits 1 and 0 - TimRefSel[1:0] - Timing Reference Select

These two “Read/Write” bit-fields permits the user to select both a “Framing Reference” and a “Timing Reference” for the Transmit Section of the XRT72L13. The following table relates the states of the two-fields to the selected “Framing” and “Timing” references.

TIMREFSEL[1:0]	FRAMING REFERENCE	TIMING REFERENCE
00	Asynchronous	RxLineClk Input signal
01	TxFrameRef	RxLineClk Input signal
10	Asynchronous	TxInClk Input signal
11	Asynchronous	TxInClk Input signal

NOTE: *For more information on Framing and Timing References, please see Section _.*

2.3.2.3 I/O Control Register

I/O CONTROL REGISTER (ADDRESS = 0X01)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Disable TxLOC	LOC	Disable RxLOC	AMI/B3ZS* Line Code	Single-Rail/ Dual-Rail*	TxClkInv	RxClkInv	Reframe
R/W	RO	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	0	0	0	0

Bit 7 - Disable TxLOC

To be provided in the next update.

Bit 6 - LOC (Loss of Clock) Indicator

To be provided in the next update.

Bit 5 - Disable RxLOC

To be provided in the next update.

Bit 4 - AMI/B3ZS* Line Code Select

This “Read/Write” bit-field pemits the user to configure the XRT72L13 M13 device to transmit and receive data via the AMI (Alternate Mark Inversion) line code or via the B3ZS (Bipolar 3 Zero Substitution) line code.

Setting this bit-field to “0” configures the XRT72L13 M13 device to transmit and receive data (via the DS3 Framer block) via the B3ZS format. Setting this bit-field to “1” configures the XRT72L13 M13 device to transmit and receive data via the AMI line code.

Bit 3 - Single-Rail/Dual-Rail Select

This “Read/Write” bit-field permits the user to configure the XRT72L13 M13 device to operate in the “Single-Rail” or “Dual-Rail” format.

Setting this bit-field to “0” configures the XRT72L13 to operate in the “Dual-Rail” Mode. In this mode, the “Transmit Section” of the XRT72L13 M13 device will output data to the LIU via the “TxPOS” and “TxNEG” output pins. Additionally, the “Receive Section” of the device will receive data from the LIU via “RxPOS” and “RxNEG” input pins.

Setting this bit-field to “1” configures the XRT72L13 to operate in the “Single-Rail” Mode. In this mode, the “Transmit Section” of the XRT72L13 M13 device will output data to the LIU, in a binary data stream manner via the “TxPOS” output pin. Additionally, the “Receive Section” of the device will receive data from the LIU, in a binary data stream manner, via the RxPOS input pin.

Bit 2 - TxClkInv

This “Read/Write” bit-field permits the user to configure the XRT72L13 M13 device to output data, via the “TxPOS” and “TxNEG” output pins, upon the “rising” or “falling” edge of “TxLineClk”.

Setting this bit-field to “0” configures the XRT72L13 M13 device to output data via the “TxPOS” and “TxNEG” output pins, on the “rising” edge of “TxLineClk”.

Setting this bit-field to “1” configures the XRT72L13 M13 device to output data via the “TxPOS” and “TxNEG” output pins, on the “falling” edge of “TxLineClk”.

Bit 1 - RxClkInv

This “Read/Write” bit-field permits the user to configure the XRT72L13 M13 device to latch data on the “RxPOS” and “RxNEG” input pins input pins, into the XRT72L13 M13 device, on the “rising” or “falling” edge of “RxLineClk”.

Setting this bit-field to “0” configures the XRT72L13 M13 device to latch the data on the “RxPOS” and “RxNEG” input pins, into the device, on the “rising” edge of “RxLineClk”.

Setting this bit-field to “1” configures the XRT72L13 M13 device to latch the data on the “RxPOS” and “RxNEG” input pins, into the device, on the “falling” edge of “RxLineClk”.

Bit 0 - Reframe

This “Read/Write” bit-field permits the user to configure the “Receive Section” of the XRT72L13 M13 device to start a new frame search. A “0” to “1” transition in this bit-field will force the chip to start a new frame search.

2.3.2.4 Part Number Register

PART NUMBER REGISTER (ADDRESS = 0X02)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Part Number Value							
RO	RO	RO	RO	RO	RO	RO	RO
0	0	1	0	0	0	1	0

The Part Number Register (within the XRT72L13 M13 device) contains the fixed value of “0x22”. This part number value permits the user to read out the contents of this register and to uniquely identify this device as the “XRT72L13 M13” device.

2.3.2.5 Version Number Register

The “Version Number” register (within the XRT72L13 M13 device) contains a value which corresponds to the “Revision Number”. The very first Revision of the XRT72L13 (Revision A) will contain the fixed value “0x01”. The contents of the “Version Number” register will be incremented for subsequent version (if needed).

VERSION NUMBER REGISTER (ADDRESS = 0X03)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Version Number Value							
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	1

2.3.2.6 Block Interrupt Enable Register

BLOCK INTERRUPT ENABLE REGISTER (ADDRESS = 0X04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Rx DS3 Interrupt Enable	Not Used	Not Used	M13 Interrupt Enable	Not Used	Not Used	Tx DS3 Interrupt Enable]	One Second Interrupt Enable]
R/W	R/O	R/O	R/W	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

Bit 7 - Rx DS3 Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable all “Receive DS3 Framer” related interrupts (within the XRT72L13) at the “Block Level”.

Setting this bit-field to “0” disables all “Receive DS3 Framer” related interrupts within the XRT72L13 M13 device.

Setting this bit-field to “1” enables all “Receive DS3 Framer” related interrupts (within the XRT72L13 M13 device) at the “Block Level”.

NOTE: *Setting this bit-field to “1” does not enable all “Receive DS3 Framer” related interrupts. Each of these interrupts can still be disabled at the “Source” Level. However, setting this bit-field to “0” does disable all “Receive DS3 Framer” related interrupt.*

Bit 4 - M13 Interrupt Enable

This “Read/Write” bit-field permits the user to enable- or disable all “M13 Multiplexer” related interrupts (within the XRT72L13) at the “Block Level.

Setting this bit-field to “0” disables all “M13 Multiplexer” related interrupts within the XRT72L13 M13 device.

Setting this bit-field to “1” disables all “M13 Multiplexer” related interrupts (within the XRT72L13 M13 device) at the “Block Level”.

Bit 1 - Tx DS3 Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “Transmit DS3 Framer” related interrupts (within the XRT72L13) at the Block Level.

Setting this bit-field to “0” disables all “Transmit DS3 Framer” related interrupts within the XRT72L13 M13 device.

Setting this bit-field to “1” disables all “Transmit DS3 Framer” related interrupts (within the XRT72L13 M13 device) at the “Block Level”.

Bit 0 - One Second Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “One Second” Interrupt, within the XRT72L13. If this interrupt is enabled then the XRT72L13 will generate interrupts to the Microprocessor/Microcontroller at “one-second” intervals.

Setting this bit-field to “0” disables the “One Second” interrupt. Conversely, setting this bit-field to “1” enables the “One Second” interrupt.

2.3.2.7 Block Interrupt Status Register

BLOCK INTERRUPT STATUS REGISTER (ADDRESS = 0X05)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Rx DS3 Interrupt Status	Not Used	Not Used	M13 Interrupt Status	Not Used	Not Used	Tx DS3 Interrupt Status	One Second Interrupt Status
R/O	R/O	R/O	R/O	R/O	R/O	R/O	RUR
0	0	0	0	0	0	0	0

Bit 7 - Rx DS3 Interrupt Status

This “Read-Only” bit-field indicates whether or not a “Receive DS3 Framer” related Interrupt has been requested and is awaiting service.

If this bit-field is set to “0”, then there are no “Receive DS3 Framer” related interrupts awaiting service. Conversely, if this bit-field is set to “1”, then there is at least one “Receive DS3 Framer” related interrupt, awaiting service.

Bit 4 - M13 Multiplexer Interrupt Status

This “Read-Only” bit-field indicates whether or not an “M13 Multiplexer” related interrupt has been requested and is awaiting service.

If this bit-field is set to “0”, then there are no “M13 Multiplexer” related interrupts awaiting service. Conversely, if this bit-field is set to “1”, then there is at least one “M13 Multiplexer” related interrupt, awaiting service.

Bit 1 - Tx DS3 Interrupt Status

This “Read-Only” bit-field indicates whether or not a “Transmit DS3 Framer” related interrupt has been requested and is awaiting service.

If this bit-field is set to “0”, then there are no “Transmit DS3 Framer” related interrupts awaiting service. Conversely, if this bit-field is set to “1”, then there is at least one “Transmit DS3 Framer” related interrupt, awaiting service.

Bit 0 - One Second Interrupt Status

This “Reset-upon-Read” bit-field indicates whether or not a “One Second” interrupt has been requested and is awaiting service.

If this bit-field is set to “0”, then the “One Second” interrupt is not awaiting service. Conversely, if this bit-field is set to “1”, then the “One Second” interrupt is awaiting service.

NOTE: *This bit-field will be cleared immediately after the Microprocessor/Microcontroller has read this register.*

2.3.2.8 RxFIFO Control Register

RXFIFO CONTROL REGISTER (ADDRESS = 0X06)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	RxFIFO32	RxFIFO Enable
R/O	R/O	R/O	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

Bit 1 - RxFIFO32 - 32/64 Operating Depth Select

This “Read/Write” bit-field permits the user to configure the operating depth of the “de-jitter” FIFO to be either 32 or 64 bits.

Setting this bit-field to “0” configures the operating depth of the “De-Jitter” FIFO to be 64 bits.

Setting this bit-field to “1” configures the operating depth of the “De-Jitter” FIFO to be 32 bits.

NOTE: *This bit-field is ignored if the “De-Jitter FIFO” is disabled.*

Bit 0 - RxFIF0 Enable

This “Read/Write” bit-field permits the user to enable or disable the “De-Jitter” FIFO within the XRT72L13.

Setting this bit-field to “0” disables the “De-Jitter” FIFO.

Setting this bit-field to “1” enables the “De-Jitter” FIFO

2.3.2.9 M23 Configuration Register

M23 CONFIGURATION REGISTER (ADDRESS = 0X07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	Payload HDLC Controller Enable	RxDS1Clk Gapped (CRC-32)	M13 Disable	M13 Loopback/ (Remote Loopback)	Tributary Polarity	M23 Loopback Code[1]	M23 Loopback Code[0]
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit 6 - Payload HDLC Controller Enable

This bit-field along with “M13 Disable” (bit 4) pemits the user to specify whether the XRT72L13 M13 device is to operate in either of the following modes.

- The “M13/Channelized” Mode
- The “DS3 Clear Channel Framer” Mode
- The “High Speed HDLC Controller” Mode.

The relationship between these two bit-fields and the resulting operating operating mode of the XRT72L13 M13 device is tabulated below.

PAYLOAD HDLC CONTROLLER ENABLE	M13 DISABLE	RESULTING OPERATING MODE
0	0	M13/ Channelized Mode
0	1	DS3 Clear Channel Framer Mode
1	0	M13/ Channelized Mode
1	1	High Speed HDLC Controller Mode

Bit 5 - RxDS1Clk Gapped (CRC-32) Select

The exact functionality of this bit-field depends upon whether the user is operating the XRT72L13 in the "M13-Channelized" or in the "High Speed HDLC Controller" Mode.

M13-Channelized Mode - RxDS1 Gapped Clock Select

In the "M13-Channelized" Mode, then this bit-field permits the user to either enable or disable the 28 Digital PLL blocks within the XRT72L13 M13 device.

Setting this bit-field to "0" enables all 28 of these Digital PLL blocks. In this mode, all 28 (or 21) of the RxDS1Clk and RxDS1Data output signals will be smoothed by an internal Digital PLL. This permits the user to interface the "Receive DS1/E1" Output interface to an external DS1 or E1 LIU IC.

Setting this bit-field to "1" disables all 28 of these Digital PLL blocks. In this mode, all 28 (or 21) of the RxDS1Clk and RxDS1Data output signals will NOT be smoothed by an internal Digital PLL, and will contain gaps.

HDLC Controller Mode - CRC16/32 Select

In the "High Speed HDLC Controller" Mode, this bit-field permits the user to configure the XRT72L13 to compute and verify a CRC-16 or CRC-32 value within the HDLC frame.

Setting this bit-field to "0" configures the XRT72L13 to compute and verify a CRC-16 value in each HDLC frame.

Setting this bit-field to "1" configures the XRT72L13 to compute and verify a CRC-32 value in each HDLC frame.

Bit 4 - M13 Disable

This bit-field along with "Payload HDLC Controller Enable" (bit 6) pemits the user to specify whether the XRT72L13 M13 device is to operate in either of the following modes.

- The "M13/Channelized" Mode
- The "DS3 Clear Channel Framer" Mode
- The "High Speed HDLC Controller" Mode.

The relationship between these two bit-fields and the resulting operating operating mode of the XRT72L13 M13 device is tabulated below.

PAYLOAD HDLC CONTROLLER ENABLE	M13 DISABLE	RESULTING OPERATING MODE
0	0	M13/ Channelized Mode
0	1	DS3 Clear Channel Framer Mode
1	0	M13/ Channelized Mode
1	1	High Speed HDLC Controller Mode

Bit 3 - M13 Loopback/Remote Loopback

The exact functionality of this bit-field depends upon whether the user is operating the XRT72L13 in the "M13-Channelized" or in the "High Speed HDLC Controller" Mode.

M13-Channelized Mode - M13 Loopback Select

If the XRT72L13 is operating in the "M13 Channelized" Mode, then this bit-field functions as the "M13 Loopback" select bit-field.

Setting this bit-field to "0" disables the "M13 Loopback" Mode. In this mode, the Receive M13 Block will accept data from the Rx DS3 Framer block (Normal Operation).

Setting this bit-field to "1" enables the "M13 Loopback" Mode. In this mode, the Receive M13 Block accepts data from the "Transmit M13 Block" (the Transmit and Receive DS3 Framer blocks are bypassed).

High Speed HDLC Controller Mode - Remote Loopback Select

If the XRT72L13 is operating in the "High Speed HDLC Controller" Mode, then this bit-field functions as the "Remote Loopback" select bit-field.

Setting this bit-field to "0" disables the "Remote Loopback" Mode.

Setting this bit-field to “1” enables the “Remote Loopback” Mode.

Bit 2 - Tributary Polarity

This “Read/Write” bit-field permits the user to select the clock edge at which (a) the XRT72L13 M13 device will sample and latch the “Transmit DS1/E1” and Transmit HDLC data, and (b) the XRT72L13 will output the “Receive DS1/E1” and Receive HDLC data.

Setting this bit-field to “0” configures the XRT72L13 M13 device to (a) sample and latch the “Transmit DS1/E1” and “Transmit HDLC” data on the rising edge of the appropriate clock signal; and (b) to output the “Receive DS1/E1” and “Receive HDLC” data on the rising edge of the appropriate clock signal.

Setting this bit-field to “1” configures the XRT72L13 M13 device to (a) sample and latch the “Transmit DS1/E1” and “Transmit HDLC” data on the falling edge of the appropriate clock signal; and (b) to output the “Receive DS1/E1” and “Receive HDLC” data on the falling edge of the appropriate clock signal.

Bits 1 and 0 - M23LBCode[1, 0]

NOTES:*These two “Read/Write” bits permit the user to define which “C-bit” pattern (in the inbound DS3 data stream) will function as the loopback command. these register bits are only used if the XRT72L13 M13 device is operating in the “M13” Framing Format. These register bits are ignored if the XRT72L13 M13 device is operating in the “C-Bit Parity” Framing Format.*

The following table related the contents of these two bit-fields to the “M23 Loopback” code.

A more detailed description of these loopback codes will be presented in Section _.

TABLE 5:

M23LB CODE[1]	M23 LB CODE[0]	RESULTING “M23” LOOPBACK CODE
0	0	Cj1 = Cj2 = *Cj3
0	1	Cj1 = *Cj2 = Cj3
1	0	*Cj1 = Cj2 = Cj3
1	1	Cj1 = Cj2 = *Cj3

2.3.2.10 M23 DS3 AIS Register

M23 TX DS2 AIS REGISTER (ADDRESS = 0X08)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	TxDS2 AIS Channel 6	TxDS2 AIS Channel 5	TxDS2 AIS Channel 4	TxDS2 AIS Channel 3	TxDS2 AIS Channel 2	TxDS2 AIS Channel 1	TxDS2 AIS Channel 0
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bits 6 thru 0 - TxDS2 AIS Channel[6:0]

These seven (7) “Read/Write” bit-fields permits the user to specify which “outbound” DS2 channel will transmit an AIS (All Ones) pattern.

For example, setting “Bit 5” (within this register) to “1” configures the XRT72L13 M13 device to transmit an AIS pattern via the “outbound” (Transmit) DS2 Channel 5. In this mode, the content of the lower tributary “TxDS1/E1” signals will be over-written by this AIS pattern.

Setting “Bit 5” to “0” configures the “Transmit” DS2 Channel 5 to carry normal traffic (as determined by the lower DS1 or E1 tributaries).

2.3.2.11 M23 Request Loopback Register

M23 REQUEST LOOPBACK REGISTER (ADDRESS = 0X09)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	DS2 Loopback Request Channel 6	DS2 Loopback Request Channel 5	DS2 Loopback Request Channel 4	DS2 Loopback Request Channel 3	DS2 Loopback Request Channel 2	DS2 Loopback Request Channel 1	DS2 Loopback Request Channel 0
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bits 6 thru 0 - DS2 Loopback Request Channel [6:0]

These seven (7) "Read/Write" bit-field permits the user to request that the Remote Terminal Equipment configure one of their DS2 channels to operate in the "Remote Loopback" Mode.

Setting any one of these bit-fields to "1" will cause the XRT72L13 M13 device to insert a "DS2 Remote Loopback Command Request" (for the corresponding DS2 channel) to be inserted into the "outbound" DS3 data stream. The "Remote Terminal Equipment" should respond by executing the appropriate loopback command.

For example, setting Bit 5 (within this register) will cause the XRT72L13 M13 device to insert the "Channel 5 DS2 Remote Loopback Command Register" into the "outbound" DS3 data stream. The Remote Terminal Equipment will be expected to respond by configuring DS2 Channel 5, into the "Remote Loopback" Mode.

NOTE: *This registert is only active if the XRT72L13 M13 device has been configured to operate in the "M13/Channelized" Mode.*

2.3.2.12 M23 Loopback Activation Register

M23 LOOPBACK ACTIVATION REGISTER (ADDRESS = 0X0A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	DS2 Loopback Activation Channel 6	DS2 Loopback Activation Channel 5	DS2 Loopback Activation Channel 4	DS2 Loopback Activation Channel 3	DS2 Loopback Activation Channel 2	DS2 Loopback Activation Channel 1	DS2 Loopback Activation Channel 0
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bits 6 thru 0 - DS2 Loopback Activation Channel [6:0]

These seven (7) "Read/Write" bit-fields permit the user to configure any of the seven DS2 channels into the "Remote Loopback" Mode.

Setting any one of these bit-fields to "1" will cause the corresponding DS2 channel to operate in the "Remote Loopback" Mode.

Setting any one of these bit-fields to "0" will cause the corresponding DS2 channel to terminate "Remote Loopback Mode" operation.

2.3.2.13 M23 RxAIS Register

M23 RX DS2 AIS REGISTER (ADDRESS = 0X0B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	RxDS2 AIS Channel 6	RxDS2 AIS Channel 5	RxDS2 AIS Channel 4	RxDS2 AIS Channel 3	RxDS2 AIS Channel 2	RxDS2 AIS Channel 1	RxDS2 AIS Channel 0
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bits 6 thru 0 - RxDS2 AIS Channel [6:0]

These seven (7) "Read/Write" bit-fields permits the user to specify which "inbound" DS2 channel (which is demultiplexed from the inbound DS3 channel) will carry an AIS (All Ones) pattern.

For example, setting "Bit 5" (within this register) to "1" configures the XRT72L13 M13 device to overwrite the contents of the de-multiplexed DS2 channel (corresponding to channel 5) with the AIS (All Ones) pattern.

Setting "Bit 5" to "0" configures the "Receive" DS2 Channel 5 to carry normal traffic (as de-multiplexed from the inbound DS3 data stream).

2.3.2.14 DS3 Test Register

DS3 TEST REGISTER (ADDRESS = 0X0C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	Rx Payload Clock Enable	Tx Payload Clock Enable	Rx PRBS Lock Indicator	Rx PRBS Enable	Tx PRBS Enable	Rx DS3 Bypass	Tx DS3 Bypass
R/O	R/W	R/W	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit 6 - Rx Payload Clock Enable

This "Read/Write" bit-field permits the user to configure the "Receive Payload Data Output Interface" (of the XRT72L13 M13 device) to generate either (a) a gapped-serial clock signal or (b) an ungapped-serial clock, along with an "RxOHInd" output signal.

Setting this bit-field to "0" configures the XRT72L13 to generate an ungapped (44.736MHz) clock sjgnal via the "RxClk" output pin, and to pulse the "RxOHInd" output pin, coincident with an Overhead bit being output via the "RxSer" output pin.

Setting this bit-field to "1" configures the XRT72L13 to generate a gapped clock signal (e.g., a clock edge for each payload bit) via the "RxOHInd" output pin.

NOTE: *This feature is only applicable if the XRT72L13 has been configured to operate in the "DS3 Clear Channel Framer" Mode.*

Bit 5 - Tx Payload Clock Enable

This "Read/Write" bit-field permits the user to configure the "Transmit Payload Data Input Interface" (or the XRT72L13 M13 device) to generate either (a) a gapped-serial clock signal or (b) an ungapped-serial clock, along with the "TxOHInd" output signal.

Setting this bit-field to "0" configurese the XRT72L13 to accept an ungapped clock (44.736MHz) signal via the "TxInClk" input pin (or to output an ungapped clock signal via the "RxOutClk" output pin). Further, in this mode, the XRT72L13 will pulse the "TxOHInd" output pin one bit period prior to the processing of an overhead bit.

Setting this bit-field to "1" configures the XRT72L13 to generate a gapped clock signal (e.g., a clock edge for each payload bit) via the "TxOHInd" output pin.

NOTE: *This feature is only applicable if the XRT72L13 has been configured to operate in the "DS3 Clear Channel Framer" Mode.*

Bit 4 - Rx PRBS Lock Indicator

This "Read-Only" bit-field indicates whether or not the "PRBS Checker/Receiver has acquired "PRBS Lock" with the payload portion of the "inbound" DS3 data stream.

If this bit-field is set to "0" then the "PRBS Checker/Receiver" has not acquired "PRBS Lock" with the payload portion of the "inbound" DS3 data stream.

Conversely, if this bit-field is set to "1", then the "PRBS Checker/Receiver" has acquired "PRBS Lock" (or Pattern Sync) with the payload portion of the "inbound" DS3 data stream.

NOTE: *The contents of this bit-field are valid only if the "PRBS Checker/Receiver" is enabled.*

Bit 3 - Rx PRBS Enable

This "Read/Write" bit-field permits the user to enable the "PRBS Checker/Receiver" block within the XRT72L13 M13 device.

Setting this bit-field to "0" disables the "PRBS Checker/Receiver" block.

Setting this bit-field to "1" enables the "PRBS Checker/Receiver" block.

Bit 2 - Tx PRBS Enable

This "Read/Write" bit-field permits the user to enable or disable the "PRBS Generator/Transmitter" block within the XRT72L13 M13 device.

Setting this bit-field to "0" disables the "PRBS Generator/Transmitter" block.

Setting this bit-field to "1" enables the "PRBS Generator/Transmitter" block.

Bit 1 - RxDS3 Bypass

To be defined in the next revision

Bit 0 - TxDS3 Bypass

To be defined in the next revision

2.3.2.15 Rx DS3 Configuration and Status Register

RX DS3 CONFIGURATION AND STATUS REGISTER (ADDRESS = 0X10)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Rx AIS	Rx LOS	Rx Idle	Rx OOF	Reserved	Framing On Parity	FSync Algo	MSync Algo
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit 7 - Rx AIS (Receive AIS Pattern) Indicator

This “Read-Only” bit-field indicates whether or not the “Receive DS3 Framer” block (within the XRT72L13 M13 device) is currently receiving an AIS pattern or not.

The XRT72L13 will set this bit-field to “0” if it is not currently detecting an AIS pattern in the incoming data stream. Conversely, the XRT72L13 will set this bit-field to “1” if it is currently receiving an AIS pattern in the incoming data stream.

NOTE: *For a detailed discussion on the AIS pattern please see Section _.*

Bit 6 - Rx LOS (Receive LOS Condition) Indicator

This “Read-Only” bit-field indicates whether or not the “Receive DS3 Framer” block (within the XRT72L13 M13 device) is currently declaring an LOS (Loss of Signal) condition of the incoming DS3 data stream.

If this bit-field is set to “0”, then the “Receive DS3 Framer” block (within the chip) is currently not declaring an LOS condition.

If this bit-field is set to “1”, then the “Receive DS3 Framer” block (within the chip) is currently declaring an LOS condition.

NOTE: *For more information on the “LOS Declaration” criteria, please see Section _.*

Bit 5 - Rx Idle (Receive Idle Pattern) Indicator

This “Read-Only” bit-field indicates whether or not the “Receive DS3 Framer” block (within the XRT72L13 M13 device) is currently detecting the “Idle Pattern” in the “incoming” DS3 data stream.

If this bit-field is set to “0”, then the Receive DS3 Framer block (within the chip) is currently not detecting the Idle pattern.

If this bit-field is set to “1”, then the Receive DS3 Framer block (within the chip) is currently detecting the Idle pattern.

NOTE: *For more information about the “Idle Pattern”, please see Section _.*

Bit 4 - Rx OOF (Receive Out-of-Frame) Indicator

This “Read-Only” bit-field indicates whether or not the “Receive DS3 Framer” block (within the XRT72L13 M13 device) is currently declaring an “OOF” (Out of Frame) condition.

If this bit-field is set to “0”, then the “Receive DS3 Framer” block (of the chip) is currently not declaring the “OOF” condition.

If this bit-field is set to “1”, then the “Receive DS3 Framer block is currently declaring the “OOF” condition.

NOTE: *For more information on the “OOF” and “In-Frame” Declaration Criteria (for DS3) please see Section _.*

Bit 2 - Framing On Parity ON/OFF Select

This “Read/Write” bit-field permits the user to require that the “Receive DS3 Framer” block include P-Bit Verification as a condition for declaring itself “In-Frame”, during “Frame Acquisition”.

This feature also imposes an additional “Frame Maintenance” requirement on the “Receive DS3 Framer” block. In particular, if this additional requirement is implemented, the “Receive DS3 Framer” block will perform a frame search if it detects P-bit errors in at least 2 out of 5 DS3 frames.

Setting this bit-field to “1” imposes this additional requirement.

Conversely, setting this bit-field to “0” configures the “Receive DS3 Framer” block to waive this requirement.

NOTE: *For more information on “Framing with Parity”, please see Section _.*

Bit 1 - FSync Algo(rithm) Select

This “Read/Write” bit-field, in conjunction with Bits 0 and 2 of this register, allows the user to completely define the “Frame Maintenance” criteria of the “Receive DS3 Framer” block (within the chip). This par-

ticular bit-field permits the user to define the “Frame Maintenance” criteria, as it applies to F-bits.

Setting this bit-field to “0” configures the “Receive DS3 Framer” block to declare an “OOF” (Out of Frame” condition) if it determines that 6 out of the last 16 F-bits are in error.

Setting this bit-field to “1” configures the “Receive DS3 Framer” block to declare an “OOF” (Out of Frame” condition) if it determines that 3 out of the last 16 F-bits are in error.

Bit 0 - MSync Algo(rithm) Select

This “Read/Write” bit-field, in conjunction with Bits 1 and 2 of this register, allows the user to completely define the “Frame Maintenance” criteria of the “Receive DS3 Framer” block (within the chip). This particular bit-field permits the user to define the “Frame Maintenance” criteria, as it applies to M-bits.

Setting this bit-field to “0” configures the “Receive DS3 Framer” block to ignore the occurrence of M-bit errors.

Setting this bit-field to “1” configures the “Receive DS3 Framer” block to declare an “OOF” condition if it determines that 3 out of 4 M-bits are in error.

2.3.2.16 RxDS3 Status Register

RX DS3 STATUS REGISTER (ADDRESS = 0X11)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	Not Used	Not Used	RxFERF	RxAIC	RxFEBE[2]	RxFEBE[1]	RxFEBE[0]
R/O	R/W	R/W	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

Bit 4 - RxFERF (Far-End Receive Failure) Indicator

This “Read-Only” bit-field indicates whether or not the “Receive DS3 Framer” block (within the XRT72L13 M13 device) is declaring a FERF (Far-End Receive Failure) condition.

If this bit-field is set to “0”, then the “Receive DS3 Framer” block (of the chip) is currently not declaring a FERF condition.

Conversely, if this bit-field is set to “1”, then the “Receive DS3 Framer” block is currently declaring a FERF condition.

NOTE: *For more information how the “Receive DS3 Framer” block declares a “FERF” condition, please see Section _.*

Bit 3 - RxAIC (Application Identification Channel) indicator

This “Read-Only” bit-field reflects the value of the AIC bit-field, within the most recently received DS3 frames, as detected by the “Receive DS3 Framer” block.

This bit-field is set to “1” if the incoming DS3 data stream is determined to be in the “C-bit Parity” format (AIC bit = 1) for at least 63 consecutive frames.

This bit-field is set to “0” if the incoming DS3 data stream is determined to be in the “M13” format (AIC bit = 0).

Bits 2 thru 0 - RxFEBE[2:0]

These “Read-Only” bit-fields reflect the “FEBE” (Far-End Block Error) value, within the most recently received DS3 frame.

If these bit-fields are set to “111”, then it indicates that the “Remote” Receiving Terminal is receiving DS3 frames in an un-erred manner.

Conversely, if these bit-fields are set to any value other than “111”, then it indicates that the “Remote” Receiving Terminal has detected Framing or Parity bit errors in the DS3 frames that it is receiving.

NOTE: *For more information on FEBE (Far-End-Block Error), please see Section _.*

2.3.2.17 RxDS3 Interrupt Enable Register

RX DS3 INTERRUPT ENABLE REGISTER (ADDRESS = 0X12)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Detection of CP-Bit Error Interrupt Enable	Change in LOS Condition Interrupt Enable	Change in AIS Condition Interrupt Enable	Change in Idle Pattern Interrupt Enable	Change in FERF Condition Interrupt Enable	Change in AIC State Interrupt Enable	Change in OOF Condition Interrupt Enable	Detection of P-Bit Error Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit 7 - Detection of CP-Bit Error Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “Detection of CP-Bit Error” interrupt.

Setting this bit-field to “0” disables the “Detection of CP-Bit Error” Interrupt.

Setting this bit-field to “1” enables the “Detection of CP-Bit Error” Interrupt.

Bit 6 - Change in LOS Condition Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “Change in LOS Condition” Interrupt.

Setting this bit-field to “0” disables the “Change in LOS Condition” Interrupt.

Setting this bit-field to “1” enables the “Change in LOS Condition” Interrupt.

Bit 5 - Change in AIS Condition Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “Change in AIS Condition” Interrupt.

Setting this bit-field to “0” disables the “Change in AIS Condition” interrupt.

Setting this bit-field to “1” enables the “Change in AIS Condition” Interrupt.

Bit 4 - Change in Idle Pattern Condition Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “Change in Idle Pattern Condition” interrupt.

Setting this bit-field to “0” disables the “Change in Idle Pattern Condition” interrupt.

Setting this bit-field to “1” enables the “Change in Idle Pattern Condition” interrupt.

Bit 3 - Change in FERF Condition Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “Change in FERF Condition” Interrupt.

Setting this bit-field to “0” disables the “Change in FERF Condition” Interrupt.

Setting this bit-field to “1” enables the “Change in FERF Condition” Interrupt.

Bit 2 - Change in AIC State Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “Change in AIC State” Interrupt.

Setting this bit-field to “0” disables the “Change in AIC State” Interrupt.

Setting this bit-field to “1” enables the “Change in AIC State” Interrupt.

Bit 1 - Change in OOF Condition Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “Change in OOF Condition” Interrupt.

Setting this bit-field to “0” disables the “Change in OOF Condition” Interrupt.

Setting this bit-field to “1” enables the “Change in OOF Condition” Interrupt.

Bit 0 - Detection of P-Bit Error Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “Detection of P-Bit Error” Interrupt.

Setting this bit-field to “0” disables the “Detection of P-Bit Error” Interrupt.

Setting this bit-field to “1” enables the “Detection of P-Bit Error” Interrupt.

2.3.2.18 RxDS3 Interrupt Status Register

RX DS3 INTERRUPT STATUS REGISTER (ADDRESS = 0X13)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Detection of CP-Bit Error Interrupt Status	Change in LOS Condition Interrupt Status	Change in AIS Condition Interrupt Status	Change in Idle Pattern Condition Interrupt Status	Change in FERF Condition Interrupt Status	Change in AIC State Interrupt Status	Change in OOF Condition Interrupt Status	Detection of P-Bit Error Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

Bit 7 - Detection of CP-Bit Error Interrupt Status

This “Reset-upon-Read” bit-field indicates whether or not the “Receive DS3 Framer” block has detected a “CP-Bit Error” in the “inbound” DS3 data stream, since the last time this register was read.

This bit-field will be “0” if the “Detection of CP-Bit Error” interrupt has not occured since the last read of this register.

This bit-field will be “1” if the interrupt has occurred since the last read of this register.

Bit 6 - Change in LOS (Loss of Signal) Condition Interrupt Status

This “Reset-upon-Read” bit-field will be set to “1” if the “Receive DS3 Framer” block has detected a “Change in LOS” condition, since the last time this register was read. If the “Change in LOS Condition” interrupt is enabled, then this bit-field will be asserted under either of the following conditions.

a. When the Receive DS3 Framer block detects the occurrence of an LOS condition (e.g., the occurrence of 180 consecutive “spaces” in the incoming DS3 data stream), and

b. When the Receive DS3 Framer block detects the end of an LOS condition (e.g., when the “Receive DS3 Framer” block detects at least 60 mark pulses in the last 180 bit periods).

The Microprocessor/Microcontroller can determine the state of the LOS condition by reading bit 6, within the “Rx DS3 Configuration and Status” register (Address location = 0x10).

NOTE: *For more information about the “LOS Condition” please see Section _.*

Bit 5 - Change in AIS (Alarm Indication Signal) Condition Interrupt Status

This “Reset-upon-Read” bit-field will be set to “1” if the “Receive DS3 Framer” block has detected a “Change in AIS” condition, since the last time this register was read. If the “Change in AIS Condition” interrupt is enabled, then this bit-field will be asserted under either of the following conditions.

a. When the Receive DS3 Framer block first detects an AIS condition in the inbound DS3 data stream.

b. When the Receive DS3 Framer block has detected the end of an “AIS Condition”.

The Microprocessor/Microcontroller can determine the state of the AIS condition by reading bit 7, within the “Rx DS3 Configuration and Status” Register (Address location = 0x10).

NOTE: *For more information about the “AIS Condition” please see Section _.*

Bit 4 - Change in Idle Pattern Condition Interrupt Status

This “Reset-upon-Read” bit-field is set to “1” when the Receive DS3 Framer block detects a “Change in Idle Condition” in the incoming DS3 data stream. Specifically, the Receive DS3 Framer block will assert this bit-field under either of the following two conditions.

a. When the Receive DS3 Framer block initially detects the “Idle Pattern” in the “inbound” DS3 data stream.

b. When the Receive DS3 Framer block ceases to detect the “Idle Pattern” in the “inbound” DS3 data stream.

The Microprocessor/Microcontroller can determine the state of the “Idle Pattern Condition” by reading bit 5, within the “Rx DS3 Configuration and Status” register (Address location = 0x10).

NOTE: *For more information about the “Idle Pattern” please see Section _.*

Bit 3 - Change in FERF Condition Interrupt Status

This “Reset-upon-Read” bit-field is set to “1” if the “Receive DS3 Framer” block (within the XRT72L13 M13 device) has detected a “Change in the FERF” Condition, since the last time this register was read.

This bit-field will be asserted under either of the following conditions.

a. When the Receive DS3 Framer block first detects the occurrence of a “FERF” condition in the “inbound” DS3 data stream (e.g., all X-bits are set to “0”).

b. When the Receive DS3 Framer block no longer detects the “FERF” condition in the “inbound” DS3 data stream (e.g., all X-bits are set to “1”).

The Microprocessor/Microcontroller can determine the state of the of the “FERF” condition by reading bit 4 within the “Rx DS3 Status” register (Address location = 0x11).

NOTE: *For more information about the “FERF” condition, please see Section _.*

Bit 2 - Change in AIC State Interrupt Status

This “Reset-upon-Read” bit-field is set to “1” if the AIC bit-field, within the incoming DS3 data stream, has changed state since the last read of this register.

The Microprocessor/Microcontroller can determine the state of the “AIC” bit-field by reading bit 3, within the “Rx DS3 Status” Register (Address location = 0x11).

NOTE: *For more information on this interrupt condition, please see Section _.*

Bit 1 - Change in OOF Condition Interrupt Status

The “Reset-upon-Read” bit-field is set to “1” if the “Receive DS3 Framer” block (within the XRT72L13) has detected a “Change in the Out-of-Frame” (OOF) condition, since the last time this register was read.

This bit-field will be asserted under either of the following conditions.

a. When the “Receive DS3 Framer” block has detected the appropriate condition to declare an “OOF” condition.

b. When the “Receive DS3 Framer” block has transitioned from the “OOF” condition (Frame Acquisition Mode).

The Microprocessor/Microcontroller can detemine the state of the “OOF” condition by reading bit 4 within the “Rx DS3 Configuration and Status” Register (Address location = 0x10).

NOTE: *For more information about the “OOF” condition, please see Section _.*

Bit 0 - Detection of P-Bit Error Interrupt Status

This “Reset-upon-Read” bit-field indicates whether or not the “Detection of P-Bit Error” interrupt has occurred since the last read of this register.

This bit-field will be “0” if the “Receive DS3 Framer” block (within the XRT72L13 M13 device) has not detected a P-bit error since the last read of this register.

Conversely, this bit-field will be “1” if the “Receive DS3 Framer” block (within the XRT72L13 M13 device) has detected a P-Bit error since the last read of this register.

2.3.2.19 RxDS3 Sync Detect Register

RX DS3 SYNC DETECT REGISTER (ADDRESS = 0X14)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	Not Used	Not Used	Reserved	Reserved	Reserved	F Algorithm	One and Only One
R/O	R/O	R/O	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

Bit 1 - F Algorithm

To be provided in the next revision.

Bit 0 - One and Only One

To be provided in the next revision.

2.3.2.20 RxDS3 FEAC Register

RXDS3 FEAC REGISTER (ADDRESS = 0X16)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	RxFEAC[5:0]						Not Used
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	1	1	1	1	1	1	0

This "Read/Write" register contains the latest 6-bit FEAC code that has been "validated" by the Receive FEAC Processor. The contents of this register will be cleared if the previously "validated" code has been "removed" by the FEAC Processor.

2.3.2.21 RxDS3 FEAC Interrupt Enable/Status Register

RXDS3 FEAC INTERRUPT ENABLE/STATUS REGISTER (ADDRESS = 0X17)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			FEAC Valid	RxFEAC Remove Interrupt Enable	RxFEAC Remove Interrupt Status	RxFEAC Valid Interrupt Enable	RxFEAC Valid Interrupt Status
R/O	R/O	R/O	R/O	R/W	RUR	R/W	RUR
0	0	0	0	0	0	0	0

Bit 4 - FEAC Valid

This "Read Only" bit is set to "1" when an incoming FEAC Message Code has been validated by the Receive DS3 Framer. This bit is cleared to "0" when the FEAC code is removed.

NOTE: *For more information on the role of this bit-field and the Receive FEAC Processor, please see Section _.*

Bit 3 - RxFEAC Remove Interrupt Enable

This "Read/Write" bit-field allows the user to enable/disable the "RxFEAC Removal" interrupt. Writing a "1" to this bit enables this interrupt. Likewise, writing a "0" to this bit-field disables this interrupt.

NOTE: *For more information on the role of this bit-field and the Receive FEAC Processor, please see Section _.*

Bit 2 - RxFEAC Remove Interrupt Status

A "1" in this "Read Only" bit-field indicates that the last "validated" FEAC Message has now been removed by the Receive FEAC Processor. The Receive FEAC Processor will remove a validated FEAC message if 3 out of the last 10 received FEAC messages differ from the latest valid FEAC Message.

NOTE: *For more information on this bit-field and the Receive FEAC Processor, please see Section _.*

Bit 1 - RxFEAC Valid Interrupt Enable

This "Read/Write" bit-field allows the user to enable/disable the "Rx FEAC Valid" interrupt. Writing a "1" to this bit-field enables this interrupt. Whereas, writing a "0" disables this interrupt. The value of this bit-field is "0" following power up or reset.

NOTE: *For more information on this bit-field and the Receive FEAC Processor, please see Section _.*

Bit 0 - RxFEAC Valid Interrupt Status

A "1" in this "Read Only" bit-field indicates that a newly received FEAC Message has been validated by the Receive FEAC Processor.

NOTE: *For more information on this bit-field and the Receive FEAC Processor, please see Section _.*

2.3.2.22 RxDS3 LAPD Control Register

RXDS3 LAPD CONTROL REGISTER (ADDRESS = 0X18)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used				RxLAPD Any	RxLAPD Enable	RxLAPD Interrupt Enable	RxLAPD Interrupt Status
RO	RO	RO	RO	RO	R/W	R/W	RUR
0	0	0	0	0	0	0	0

Bit 3 RxLAPD Any

To be provided in the next revision.

Bit 2 RxLAPD Enable

This "Read/Write" bit-field allows the user to enable or disable the LAPD Receiver. The LAPD Receiver MUST be enabled before it can begin to receive and process any LAPD Message frames from the incoming DS3 data stream.

Writing a "0" to this bit-field disables the LAPD Receiver (the default condition). Writing a "1" to this bit-field enables the LAPD Receiver.

Bit 1 RxLAPD (Message Frame Reception Complete) Interrupt Enable

This "Read/Write" bit-field allows the user to enable or disable the "LAPD Message Frame Reception Complete" interrupt. If this interrupt is enabled, then the UNI will generate this interrupt to the local µP, once the last bit of a LAPD Message frame has been

received and the PMDL message has been extracted and written into the "Receive LAPD Message" buffer.

Writing a "0" to this bit-field disables this interrupt (the default condition). Writing a "1" to this bit-field enables this interrupt.

Bit 0 RxLAPD (Message Reception Complete) Interrupt Status

This "Read-Only" bit field indicates whether or not the "LAPD Message Reception Complete" interrupt has occurred since the last read of this register. The "LAPD Message Reception Complete" interrupt will occur once the LAPD Receiver has received the last bit of a complete LAPD Message frame, extracted the PMDL message from this LAPD Message frame and has written this (PMDL) message frame into the "Receive LAPD Message" buffer. The purpose of this interrupt is to notify the local µP that the "Receive LAPD Message" buffer contains a new PMDL message, that needs to be read and/or processed.

A "0" in this bit-field indicates that the "LAPD Message Reception Complete" interrupt has NOT occurred since the last read of this register. A "1" in this bit-field indicates that the "LAPD Message Reception Complete" interrupt has occurred since the last read of this register.

NOTE: *For more information on the LAPD Receiver, please see Section _.*

2.3.2.23 RxDS3 LAPD Status Register

RXDS3 LAPD STATUS REGISTER (ADDRESS = 0X19)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	RxAbort	RxLAPDType[1:0}		RxCR Type	RxFCS Error	End of Message	Flag Present
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

Bit 6 - RxAbort (Receive Abort Sequence)

This "Read-Only" bit-field indicates whether or not the LAPD Receiver has detected the occurrence of an "Abort Sequence" (e.g., a string of seven or more consecutive "1s") from the "far-end" LAPD Transmitter. A "0" in this bit-field indicates that no "Abort-Sequence" has been detected. A "1" in this bit-field indicates that the "Abort-Sequence" has been detected.

NOTE: *For more information on the LAPD Receiver, please see Section _.*

Bits, 5 and 4 - RxLAPDType[1, 0]

These two "Read Only" bit-fields combine to indicate the "type" of LAPD Message frame that has been received by the LAPD Receiver. The relationship between these two bit-fields and the LAPD Message Type follows:

BIT 5	BIT 4	MESSAGE TYPE	MESSAGE LENGTH
		Test Signal Identification	76 Bytes
0	1	Idle Signal Identification	76 Bytes
		CL Path Identification	76 Bytes
		ITU-T Path Identification	82 Bytes

Bit 3 - RxCR (Command/Response) Type

This "Read Only" bit field indicates the value of the C/R (Command/Response) bit-field of the latest received LAPD Message.

Bit 2 - Rx FCS (Frame Check Sequence) Error

This "Read-Only" bit-field indicates whether or not the LAPD Receiver has detected a "Frame Check Sequence" (FCS) error in the newly received LAPD Message Frame. A "0" in this bit-field indicates that the FCS for the latest received LAPD Message Frame is correct. A "1" in this bit-field indicates that the FCS for the latest received LAPD Message Frame is incorrect.

NOTE: *For more information on the LAPD Receiver, please see Section _.*

Bit 1 - End Of Message

This "Read-Only" bit-field indicates whether or not the LAPD Receiver has completed its reception of the latest incoming LAPD Message frame. The local µP can poll the progress of the LAPD Receiver by periodically reading this bit-field.

A "0" in this bit-field indicates that the LAPD Receiver is still receiving the latest message from the "far end" LAPD Transmitter. A "1" in this bit-field indicates that the LAPD Receiver has finished receiving the complete LAPD Message Frame.

Bit 0 - Flag Present

This "Read-Only" bit-field indicates whether or not the LAPD Receiver has detected the occurrence of the Flag Sequence byte (0x7E). A "0" in this bit-field indicates that the LAPD Receiver does not detect the occurrence of the Flag Sequence byte. A "1" in this bit-field indicates that the LAPD Receiver does detect the occurrence of the Flag Sequence byte.

NOTE: *For more information on the LAPD Receiver, please see Section _.*

2.3.2.24 M12 DS2 # 1 Configuration Register)

M12 DS2 # 1 CONFIGURATION REGISTER (ADDRESS = 0X1A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved 7	Reserved 6	M12 Bypass	M12 G.747	M12 G.747 Res	M12 FERF	M12LBCode[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	1	1	1

Bit 7 - Reserved

This bit-field must be set to “0”, in order for the XRT72L13 M13 device to function properly.

Bit 6 - Reserved

This bit-field must be set to “0” in order for the XRT72L13 M13 device to function properly.

Bit 5 - M12 Bypass

This “Read/Write” bit field permits the user to bypass M12 Multiplexer/De-Multiplexer # 1. By doing this the following will happen.

In the Transmit Direction

- The XRT72L13 M13 device will accept a DS2 clock signal (6.312MHz) via the TxDS1Clk3 input pin.
- The XRT72L13 M13 device will accept a DS2 signal via the TxDS1Data_3 input pin

In the Receive Direction

- The XRT72L13 M13 device will output a DS2 clock signal (6.312MHz) via the RxDS1Clk3 output pin.
- XRT72L13 M13 device will output the contents of DS2 Channel # 1 via the RxDS1Data3 output pin.

Setting this bit-field to “1” configures M12 MUX # 1 and M12 DEMUX # 1 to be bypassed.

Setting this bit-field to “0” enables M12 MUX # 1 and M12 DEMUX # 1.

Bit 4 - M12 G.747

This “Read/Write” bit-field permits the user to configure M12 MUX # 1 and DEMUX # 1 to support either a DS2 signal or an ITU-T G.747 signal.

Setting this bit-field to “0” configures M12 # 1 to support DS2. In this mode, the M12 MUX will accept four DS1 signals (via TxDS1Data0 thru TXDS1Data3) and will muitiplex these signals into a DS2 signal. Likewise, the M12 DEMUX will accept an incoming DS2 signal (from the M23 DEMUX) and will de-multiplex this signal into 4 DS1 signals. These four DS1 signals will be output via the “RxDS1Data0” thru “RxDS1Data3” output pins.

Setting this bit-field to “1” configures M12 # 1 to support ITU-T G.747. In this mode, the M12 MUX will accept 3 E1 signals (via TxDS1Data0 thru TxDS1Data2) and will multiplex these signals into an ITU-T G.747 signal. Likewise, the M12 DEMUX will accept an incoming ITU-T G.747 signal (from the M23 DEMUX) and will de-multiplexe this signal into 3 E1 signals. These three E1 signals will output via the “RxDS1Data0” thru “RxDS1Data2” output pins.

Bit 3 - M12G.747 Reserved

Bit 2 - M12 FERF

This “Read/Write” bit-field permits the user to force M12 MUX # 1 to transmit a “FERF” (Far-End-Receive Failure) indicator to the M23 MUX (and in turn to the remote terminal equipment).

Setting this bit-field to “1” configures the M12 MUX to set the “X-bits” (within the “outbound” DS2 data stream) to “0”. This signaling will be interpreted (by the remote terminal equipment) as a FERF indicator.

Settiing this bit-field to “0” configures the M12 MUX to set the “X-bits” (within the “outbound” DS2 data stream) to “1”. This signaling will be interpreted (by the remote terminal equipment) as an indication of no FERF.

Bits 1 and 0 M12 LB Code[1:0]

2.3.2.25 M12 DS2 # 2 Configuration Register)

M12 DS2 # 2 CONFIGURATION REGISTER (ADDRESS = 0X1B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved 7	Reserved 6	M12 Bypass	M12 G.747	M12 G.747 Res	M12 FERF	M12LBCode[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	1	1	1

Bit 7 - Reserved

This bit-field must be set to “0”, in order for the XRT72L13 M13 device to function properly.

Bit 6 - Reserved

This bit-field must be set to “0” in order for the XRT72L13 M13 device to function properly.

Bit 5 - M12 Bypass

This “Read/Write” bit field permits the user to bypass M12 Multiplexer/De-Multiplexer # 1. By doing this the following will happen.

In the Transmit Direction

- The XRT72L13 M13 device will accept a DS2 clock signal (6.312MHz) via the TxDS1Clk7 input pin.
- The XRT72L13 M13 device will accept a DS2 signal via the TxDS1Data_7 input pin

In the Receive Direction

- The XRT72L13 M13 device will output a DS2 clock signal (6.312MHz) via the RxDS1Clk7 output pin.
- XRT72L13 M13 device will output the contents of DS2 Channel # 2 via the RxDS1Data7 output pin.

Setting this bit-field to “1” configures M12 MUX # 1 and M12 DEMUX # 2 to be bypassed.

Setting this bit-field to “0” enables M12 MUX # 1 and M12 DEMUX # 2.

Bit 4 - M12 G.747

This “Read/Write” bit-field permits the user to configure M12 MUX # 2 and DEMUX # 2 to support either a DS2 signal or an ITU-T G.747 signal.

Setting this bit-field to “0” configures M12 # 1 to support DS2. In this mode, the M12 MUX will accept four DS1 signals (via TxDS1Data0 thru TXDS1Data3) and will muitiplex these signals into a DS2 signal. Likewise, the M12 DEMUX will accept an incoming DS2 signal (from the M23 DEMUX) and will de-multiplex this signal into 4 DS1 signals. These four DS1 signals will be output via the “RxDS1Data0” thru “RxDS1Data3” output pins.

Setting this bit-field to “1” configures M12 # 2 to

support ITU-T G.747. In this mode, the M12 MUX will accept 3 E1 signals (via TxDS1Data4 thru TxDS1Data6) and will multiplex these signals into an ITU-T G.747 signal. Likewise, the M12 DEMUX will accept an incoming ITU-T G.747 signal (from the M23 DEMUX) and will de-multiplexe this signal into 3 E1 signals. These three E1 signals will output via the “RxDS1Data4” thru “RxDS1Data6” output pins.

Bit 3 - M12G.747 Reserved

Bit 2 - M12 FERF

This “Read/Write” bit-field permits the user to force M12 MUX # 2 to transmit a “FERF” (Far-End-Receive Failure) indicator to the M23 MUX (and in turn to the remote terminal equipment).

Setting this bit-field to “1” configures the M12 MUX to set the “X-bits” (within the “outbound” DS2 data stream) to “0”. This signaling will be interpreted (by the remote terminal equipment) as a FERF indicator.

Settiing this bit-field to “0” configures the M12 MUX to set the “X-bits” (within the “outbound” DS2 data stream) to “1”. This signaling will be interpreted (by the remote terminal equipment) as an indication of no FERF.

Bits 1 and 0 M12 LB Code[1:0]

2.3.2.26 M12 DS2 # 3 Configuration Register)

M12 DS2 # 3 CONFIGURATION REGISTER (ADDRESS = 0X1C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved 7	Reserved 6	M12 Bypass	M12 G.747	M12 G.747 Res	M12 FERF	M12LBCode[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	1	1	1

Bit 7 - Reserved

This bit-field must be set to “0”, in order for the XRT72L13 M13 device to function properly.

Bit 6 - Reserved

This bit-field must be set to “0” in order for the XRT72L13 M13 device to function properly.

Bit 5 - M12 Bypass

This “Read/Write” bit field permits the user to bypass M12 Multiplexer/De-Multiplexer # 3. By doing this the following will happen.

In the Transmit Direction

- The XRT72L13 M13 device will accept a DS2 clock signal (6.312MHz) via the TxDS1Clk11 input pin.
- The XRT72L13 M13 device will accept a DS2 signal via the TxDS1Data_11 input pin

In the Receive Direction

- The XRT72L13 M13 device will output a DS2 clock signal (6.312MHz) via the RxDS1Clk11 output pin.
- XRT72L13 M13 device will output the contents of DS2 Channel # 2 via the RxDS1Data11 output pin.

Setting this bit-field to “1” configures M12 MUX # 3 and M12 DEMUX # 3 to be bypassed.

Setting this bit-field to “0” enables M12 MUX # 3 and M12 DEMUX # 3.

Bit 4 - M12 G.747

This “Read/Write” bit-field permits the user to configure M12 MUX # 3 and DEMUX # 3 to support either a DS2 signal or an ITU-T G.747 signal.

Setting this bit-field to “0” configures M12 # 3 to support DS2. In this mode, the M12 MUX will accept four DS1 signals (via TxDS1Data8 thru TXDS1Data11) and will muitiplex these signals into a DS2 signal. Likewise, the M12 DEMUX will accept an incoming DS2 signal (from the M23 DEMUX) and will de-multiplex this signal into 4 DS1 signals. These four DS1 signals will be output via the “RxDS1Data8” thru “RxDS1Data11” output pins.

Setting this bit-field to “1” configures M12 # 3 to support ITU-T G.747. In this mode, the M12 MUX will accept 3 E1 signals (via TxDS1Data8 thru TxDS1Data10) and will multiplex these signals into an ITU-T G.747 signal. Likewise, the M12 DEMUX will accept an incoming ITU-T G.747 signal (from the M23 DEMUX) and will de-multiplexe this signal into 3 E1 signals. These three E1 signals will output via the “RxDS1Data8” thru “RxDS1Data10” output pins.

Bit 3 - M12G.747 Reserved

Bit 2 - M12 FERF

This “Read/Write” bit-field permits the user to force M12 MUX # 3 to transmit a “FERF” (Far-End-Receive Failure) indicator to the M23 MUX (and in turn to the remote terminal equipment).

Setting this bit-field to “1” configures the M12 MUX to set the “X-bits” (within the “outbound” DS2 data stream) to “0”. This signaling will be interpreted (by the remote terminal equipment) as a FERF indicator.

Settiing this bit-field to “0” configures the M12 MUX to set the “X-bits” (within the “outbound” DS2 data stream) to “1”. This signaling will be interpreted (by the remote terminal equipment) as an indication of no FERF.

Bits 1 and 0 M12 LB Code[1:0]

2.3.2.27 M12 DS2 # 4 Configuration Register)

M12 DS2 # 4 CONFIGURATION REGISTER (ADDRESS = 0X1D)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved 7	Reserved 6	M12 Bypass	M12 G.747	M12 G.747 Res	M12 FERF	M12LBCode[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	1	1	1

Bit 7 - Reserved

This bit-field must be set to “0”, in order for the XRT72L13 M13 device to function properly.

Bit 6 - Reserved

This bit-field must be set to “0” in order for the XRT72L13 M13 device to function properly.

Bit 5 - M12 Bypass

This “Read/Write” bit field permits the user to bypass M12 Multiplexer/De-Multiplexer # 4. By doing this the following will happen.

In the Transmit Direction

- The XRT72L13 M13 device will accept a DS2 clock signal (6.312MHz) via the TxDS1Clk15 input pin.
- The XRT72L13 M13 device will accept a DS2 signal via the TxDS1Data_15 input pin

In the Receive Direction

- The XRT72L13 M13 device will output a DS2 clock signal (6.312MHz) via the RxDS1Clk15 output pin.
- XRT72L13 M13 device will output the contents of DS2 Channel # 4 via the RxDS1Data15 output pin.

Setting this bit-field to “1” configures M12 MUX # 4 and M12 DEMUX # 4 to be bypassed.

Setting this bit-field to “0” enables M12 MUX # 4 and M12 DEMUX # 4.

Bit 4 - M12 G.747

This “Read/Write” bit-field permits the user to configure M12 MUX # 4 and DEMUX # 4 to support either a DS2 signal or an ITU-T G.747 signal.

Setting this bit-field to “0” configures M12 # 4 to support DS2. In this mode, the M12 MUX will accept four DS1 signals (via TxDS1Data12 thru TXDS1Data15) and will muitiplex these signals into a DS2 signal. Likewise, the M12 DEMUX will accept an incoming DS2 signal (from the M23 DEMUX) and will de-multiplex this signal into 4 DS1 signals. These four DS1 signals will be output via the “RxDS1Data12” thru “RxDS1Data15” output pins.

Setting this bit-field to “1” configures M12 # 4 to support ITU-T G.747. In this mode, the M12 MUX will accept 3 E1 signals (via TxDS1Data12 thru TxDS1Data14) and will multiplex these signals into an ITU-T G.747 signal. Likewise, the M12 DEMUX will accept an incoming ITU-T G.747 signal (from the M23 DEMUX) and will de-multiplexe this signal into 3 E1 signals. These three E1 signals will output via the “RxDS1Data12” thru “RxDS1Data14” output pins.

Bit 3 - M12G.747 Reserved

Bit 2 - M12 FERF

This “Read/Write” bit-field permits the user to force M12 MUX # 4 to transmit a “FERF” (Far-End-Receive Failure) indicator to the M23 MUX (and in turn to the remote terminal equipment).

Setting this bit-field to “1” configures the M12 MUX to set the “X-bits” (within the “outbound” DS2 data stream) to “0”. This signaling will be interpreted (by the remote terminal equipment) as a FERF indicator.

Settiing this bit-field to “0” configures the M12 MUX to set the “X-bits” (within the “outbound” DS2 data stream) to “1”. This signaling will be interpreted (by the remote terminal equipment) as an indication of no FERF.

Bits 1 and 0 M12 LB Code[1:0]

2.3.2.28 M12 DS2 # 5 Configuration Register)

M12 DS2 # 5 CONFIGURATION REGISTER (ADDRESS = 0X1E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved 7	Reserved 6	M12 Bypass	M12 G.747	M12 G.747 Res	M12 FERF	M12LBCode[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	1	1	1

Bit 7 - Reserved

This bit-field must be set to “0”, in order for the XRT72L13 M13 device to function properly.

Bit 6 - Reserved

This bit-field must be set to “0” in order for the XRT72L13 M13 device to function properly.

Bit 5 - M12 Bypass

This “Read/Write” bit field permits the user to bypass M12 Multiplexer/De-Multiplexer # 5. By doing this the following will happen.

In the Transmit Direction

- The XRT72L13 M13 device will accept a DS2 clock signal (6.312MHz) via the TxDS1Clk19 input pin.
- The XRT72L13 M13 device will accept a DS2 signal via the TxDS1Data_19 input pin

In the Receive Direction

- The XRT72L13 M13 device will output a DS2 clock signal (6.312MHz) via the RxDS1Clk19 output pin.
- XRT72L13 M13 device will output the contents of DS2 Channel # 2 via the RxDS1Data19 output pin.

Setting this bit-field to “1” configures M12 MUX # 5 and M12 DEMUX # 5 to be bypassed.

Setting this bit-field to “0” enables M12 MUX # 5 and M12 DEMUX # 5.

Bit 4 - M12 G.747

This “Read/Write” bit-field permits the user to configure M12 MUX # 5 and DEMUX # 5 to support either a DS2 signal or an ITU-T G.747 signal.

Setting this bit-field to “0” configures M12 # 5 to support DS2. In this mode, the M12 MUX will accept four DS1 signals (via TxDS1Data16 thru TXDS1Data19) and will muitiplex these signals into a DS2 signal. Likewise, the M12 DEMUX will accept an incoming

DS2 signal (from the M23 DEMUX) and will de-multiplex this signal into 4 DS1 signals. These four DS1 signals will be output via the "RxDS1Data16" thru "RxDS1Data19" output pins.

Setting this bit-field to "1" configures M12 # 5 to support ITU-T G.747. In this mode, the M12 MUX will accept 3 E1 signals (via TxDS1Data16 thru TxDS1Data18) and will multiplex these signals into an ITU-T G.747 signal. Likewise, the M12 DEMUX will accept an incoming ITU-T G.747 signal (from the M23 DEMUX) and will de-multiplexe this signal into 3 E1 signals. These three E1 signals will output via the "RxDS1Data16" thru "RxDS1Data18" output pins.

Bit 3 - M12G.747 Reserved

Bit 2 - M12 FERF

This "Read/Write" bit-field permits the user to force M12 MUX # 5 to transmit a "FERF" (Far-End-Receive Failure) indicator to the M23 MUX (and in turn to the remote terminal equipment).

Setting this bit-field to "1" configures the M12 MUX to set the "X-bits" (within the "outbound" DS2 data stream) to "0". This signaling will be interpreted (by the remote terminal equipment) as a FERF indicator.

Settiing this bit-field to "0" configures the M12 MUX to set the "X-bits" (within the "outbound" DS2 data stream) to "1". This signaling will be interpreted (by the remote terminal equipment) as an indication of no FERF.

Bits 1 and 0 M12 LB Code[1:0]

2.3.2.29 M12 DS2 # 6 Configuration Register)

M12 DS2 # 6 CONFIGURATION REGISTER (ADDRESS = 0X1F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved 7	Reserved 6	M12 Bypass	M12 G.747	M12 G.747 Res	M12 FERF	M12LBCode[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	1	1	1

Bit 7 - Reserved

This bit-field must be set to "0", in order for the XRT72L13 M13 device to function properly.

Bit 6 - Reserved

This bit-field must be set to "0" in order for the XRT72L13 M13 device to function properly.

Bit 5 - M12 Bypass

This "Read/Write" bit field permits the user to bypass M12 Multiplexer/De-Multiplexer # 6. By doing this the following will happen.

In the Transmit Direction

- The XRT72L13 M13 device will accept a DS2 clock signal (6.312MHz) via the TxDS1Clk23 input pin.
- The XRT72L13 M13 device will accept a DS2 signal via the TxDS1Data_23 input pin

In the Receive Direction

- The XRT72L13 M13 device will output a DS2 clock signal (6.312MHz) via the RxDS1Clk23 output pin.
- XRT72L13 M13 device will output the contents of DS2 Channel # 6 via the RxDS1Data23 output pin.

Setting this bit-field to "1" configures M12 MUX # 6 and M12 DEMUX # 6 to be bypassed.

Setting this bit-field to "0" enables M12 MUX # 6 and M12 DEMUX # 6.

Bit 4 - M12 G.747

This "Read/Write" bit-field permits the user to configure M12 MUX # 6 and DEMUX # 6 to support either a DS2 signal or an ITU-T G.747 signal.

Setting this bit-field to "0" configures M12 # 6 to support DS2. In this mode, the M12 MUX will accept four DS1 signals (via TxDS1Data20 thru TXDS1Data23) and will muitiplex these signals into a DS2 signal. Likewise, the M12 DEMUX will accept an incoming DS2 signal (from the M23 DEMUX) and will de-multiplex this signal into 4 DS1 signals. These four DS1 signals will be output via the "RxDS1Data20" thru "RxDS1Data23" output pins.

Setting this bit-field to "1" configures M12 # 6 to support ITU-T G.747. In this mode, the M12 MUX will accept 3 E1 signals (via TxDS1Data20 thru TxDS1Data22) and will multiplex these signals into an ITU-T G.747 signal. Likewise, the M12 DEMUX will accept an incoming ITU-T G.747 signal (from the M23 DEMUX) and will de-multiplexe this signal into 3 E1 signals. These three E1 signals will output via the "RxDS1Data20" thru "RxDS1Data22" output pins.

Bit 3 - M12G.747 Reserved

Bit 2 - M12 FERF

This "Read/Write" bit-field permits the user to force M12 MUX # 6 to transmit a "FERF" (Far-End-Receive Failure) indicator to the M23 MUX (and in turn to the remote terminal equipment).

Setting this bit-field to “1” configures the M12 MUX to set the “X-bits” (within the “outbound” DS2 data stream) to “0”. This signaling will be interpreted (by the remote terminal equipment) as a FERF indicator.

Settiing this bit-field to “0” configures the M12 MUX to set the “X-bits” (within the “outbound” DS2 data stream) to “1”. This signaling will be interpreted (by the remote terminal equipment) as an indication of no FERF.

Bits 1 and 0 M12 LB Code[1:0]

2.3.2.30 M12 DS2 # 7 Configuration Register)

M12 DS2 # 7 CONFIGURATION REGISTER (ADDRESS = 0X20)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved 7	Reserved 6	M12 Bypass	M12 G.747	M12 G.747 Res	M12 FERF	M12LBCode[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	1	1	1

Bit 7 - Reserved

This bit-field must be set to “0”, in order for the XRT72L13 M13 device to function properly.

Bit 6 - Reserved

This bit-field must be set to “0” in order for the XRT72L13 M13 device to function properly.

Bit 5 - M12 Bypass

This “Read/Write” bit field permits the user to bypass M12 Multiplexer/De-Multiplexer # 6. By doing this the following will happen.

In the Transmit Direction

- The XRT72L13 M13 device will accept a DS2 clock signal (6.312MHz) via the TxDS1Clk23 input pin.
- The XRT72L13 M13 device will accept a DS2 signal via the TxDS1Data_23 input pin

In the Receive Direction

- The XRT72L13 M13 device will output a DS2 clock signal (6.312MHz) via the RxDS1Clk23 output pin.
- XRT72L13 M13 device will output the contents of DS2 Channel # 6 via the RxDS1Data23 output pin.

Setting this bit-field to “1” configures M12 MUX # 6 and M12 DEMUX # 6 to be bypassed.

Setting this bit-field to “0” enables M12 MUX # 6 and M12 DEMUX # 6.

Bit 4 - M12 G.747

This “Read/Write” bit-field permits the user to configure M12 MUX # 6 and DEMUX # 6 to support either a DS2 signal or an ITU-T G.747 signal.

Setting this bit-field to “0” configures M12 # 6 to support DS2. In this mode, the M12 MUX will accept four DS1 signals (via TxDS1Data20 thru TXDS1Data23) and will muitiplex these signals into a DS2 signal. Likewise, the M12 DEMUX will accept an incoming DS2 signal (from the M23 DEMUX) and will de-multiplex this signal into 4 DS1 signals. These four DS1 signals will be output via the “RxDS1Data20” thru “RxDS1Data23” output pins.

Setting this bit-field to “1” configures M12 # 6 to support ITU-T G.747. In this mode, the M12 MUX will accept 3 E1 signals (via TxDS1Data20 thru TxDS1Data22) and will multiplex these signals into an ITU-T G.747 signal. Likewise, the M12 DEMUX will accept an incoming ITU-T G.747 signal (from the M23 DEMUX) and will de-multiplexe this signal into 3 E1 signals. These three E1 signals will output via the “RxDS1Data20” thru “RxDS1Data22” output pins.

Bit 3 - M12G.747 Reserved

Bit 2 - M12 FERF

This “Read/Write” bit-field permits the user to force M12 MUX # 6 to transmit a “FERF” (Far-End-Receive Failure) indicator to the M23 MUX (and in turn to the remote terminal equipment).

Setting this bit-field to “1” configures the M12 MUX to set the “X-bits” (within the “outbound” DS2 data stream) to “0”. This signaling will be interpreted (by the remote terminal equipment) as a FERF indicator.

Settiing this bit-field to “0” configures the M12 MUX to set the “X-bits” (within the “outbound” DS2 data stream) to “1”. This signaling will be interpreted (by the remote terminal equipment) as an indication of no FERF.

Bits 1 and 0 M12 LB Code[1:0]

2.3.2.31 M12 DS2 # 1 AIS Register)

M12 DS2 # 1 AIS REGISTER (ADDRESS = 0X21)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Insert AIS Rx DS1 Channel 3	Insert AIS Rx DS1 Channel 2	Insert AIS Rx DS1 Channel 1	Insert AIS Rx DS1 Channel 0	Insert AIS Tx DS1 Channel 3	Insert AIS Tx DS1 Channel 2	Insert AIS Tx DS1 Channel 1	Insert AIS Tx DS1 Channel 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	1	1	1

Bit 7 - Insert AIS Rx DS1 Channel 3

This “Read/Write” bit-field permits the user to configure the contents of the “inbound” DS1 Channel 3 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits data to be output (via the RxDS1Data3 output pin, as demultiplexed via the inbound DS2 and DS3 data streams.

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 6 - Insert AIS Rx DS1 Channel 2

This “Read/Write” bit-field permits the user to configure the contents of the “inbound” DS1 Channel 2 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits data to be output (via the RxDS1Data2 output pin, as demultiplexed via the inbound DS2 and DS3 data streams.

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 5 - Insert AIS Rx DS1 Channel 1

This “Read/Write” bit-field permits the user to configure the contents of the “inbound” DS1 Channel 1 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits data to be output (via the RxDS1Data1 output pin, as demultiplexed via the inbound DS2 and DS3 data streams.

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 4 - Insert AIS Rx DS1 Channel 0

This “Read/Write” bit-field permits the user to configure the contents of the “inbound” DS1 Channel 0 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits data to be output (via the RxDS1Data0 output pin, as demultiplexed via the inbound DS2 and DS3 data streams.

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 3 - Insert AIS Tx DS1 Channel 3

This “Read/Write” bit-field permits the user to configure the contents of the “output” DS1 Channel 3 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits the contents of DS1 Channel 3 to be transmitted as received (via the TxDS1Data3 input pin).

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 2 - Insert AIS Tx DS1 Channel 2

This “Read/Write” bit-field permits the user to configure the contents of the “output” DS1 Channel 3 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits the contents of DS1 Channel 2 to be transmitted as received (via the TxDS1Data2 input pin).

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 1 - Insert AIS Tx DS1 Channel 1

This “Read/Write” bit-field permits the user to configure the contents of the “output” DS1 Channel 1 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits the contents of DS1 Channel 1 to be transmitted as received (via the TxDS1Data1 input pin).

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 0 - Insert AIS Tx DS1 Channel 0

This “Read/Write” bit-field permits the user to configure the contents of the “output” DS1 Channel 0 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits the contents of DS1 Channel 0 to be transmitted as received (via the TxDS1Data0 input pin).

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

2.3.2.32 M12 DS2 # 2 AIS Register)

M12 DS2 # 2 AIS REGISTER (ADDRESS = 0X22)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Insert AIS Rx DS1 Channel 7	Insert AIS Rx DS1 Channel 6	Insert AIS Rx DS1 Channel 5	Insert AIS Rx DS1 Channel 4	Insert AIS Tx DS1 Channel 7	Insert AIS Tx DS1 Channel 6	Insert AIS Tx DS1 Channel 5	Insert AIS Tx DS1 Channel 4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	1	1	1

Bit 7 - Insert AIS Rx DS1 Channel 7

This “Read/Write” bit-field permits the user to configure the contents of the “inbound” DS1 Channel 7 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits data to be output (via the RxDS1Data7 output pin, as demultiplexed via the inbound DS2 and DS3 data streams.

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 6 - Insert AIS Rx DS1 Channel 6

This “Read/Write” bit-field permits the user to configure the contents of the “inbound” DS1 Channel 6 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits data to be output (via the RxDS1Data6 output pin, as demultiplexed via the inbound DS2 and DS3 data streams.

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 5 - Insert AIS Rx DS1 Channel 5

This “Read/Write” bit-field permits the user to configure the contents of the “inbound” DS1 Channel 5 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits data to be output (via the RxDS1Data5 output pin, as demultiplexed via the inbound DS2 and DS3 data streams.

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 4 - Insert AIS Rx DS1 Channel 4

This “Read/Write” bit-field permits the user to configure the contents of the “inbound” DS1 Channel 4 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits data to be output (via the RxDS1Data4 output pin, as demultiplexed via the inbound DS2 and DS3 data streams.

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 3 - Insert AIS Tx DS1 Channel 7

This “Read/Write” bit-field permits the user to configure the contents of the “output” DS1 Channel 7 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits the contents of DS1 Channel 7 to be transmitted as received (via the TxDS1Data7 input pin).

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 2 - Insert AIS Tx DS1 Channel 6

This “Read/Write” bit-field permits the user to configure the contents of the “output” DS1 Channel 6 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits the contents of DS1 Channel 6 to be transmitted as received (via the TxDS1Data2 input pin).

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 1 - Insert AIS Tx DS1 Channel 5

This “Read/Write” bit-field permits the user to configure the contents of the “output” DS1 Channel 5 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits the contents of DS1 Channel 5 to be transmitted as received (via the TxDS1Data5 input pin).

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 0 - Insert AIS Tx DS1 Channel 4

This “Read/Write” bit-field permits the user to configure the contents of the “output” DS1 Channel 4 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits the contents of DS1 Channel 4 to be transmitted as received (via the TxDS1Data4 input pin).

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

2.3.2.33 M12 DS2 # 3 AIS Register)

M12 DS2 # 3 AIS REGISTER (ADDRESS = 0X23)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Insert AIS Rx DS1 Channel 11	Insert AIS Rx DS1 Channel 10	Insert AIS Rx DS1 Channel 9	Insert AIS Rx DS1 Channel 8	Insert AIS Tx DS1 Channel 11	Insert AIS Tx DS1 Channel 10	Insert AIS Tx DS1 Channel 9	Insert AIS Tx DS1 Channel 8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	1	1	1

Bit 7 - Insert AIS Rx DS1 Channel 11

This “Read/Write” bit-field permits the user to configure the contents of the “inbound” DS1 Channel 11 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits data to be output (via the RxDS1Data11 output pin, as demultiplexed via the inbound DS2 and DS3 data streams.

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 6 - Insert AIS Rx DS1 Channel 10

This “Read/Write” bit-field permits the user to configure the contents of the “inbound” DS1 Channel 10 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits data to be output (via the RxDS1Data10 output pin, as demultiplexed via the inbound DS2 and DS3 data streams.

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 5 - Insert AIS Rx DS1 Channel 9

This “Read/Write” bit-field permits the user to configure the contents of the “inbound” DS1 Channel 9 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits data to be output (via the RxDS1Data9 output pin, as demultiplexed via the inbound DS2 and DS3 data streams.

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 4 - Insert AIS Rx DS1 Channel 8

This “Read/Write” bit-field permits the user to configure the contents of the “inbound” DS1 Channel 8 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits data to be output (via the RxDS1Data8 output pin, as demultiplexed via the inbound DS2 and DS3 data streams.

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 3 - Insert AIS Tx DS1 Channel 11

This “Read/Write” bit-field permits the user to configure the contents of the “outbound” DS1 Channel 11 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits the contents of DS1 Channel 11 to be transmitted as received (via the TxDS1Data11 input pin).

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 2 - Insert AIS Tx DS1 Channel 10

This “Read/Write” bit-field permits the user to configure the contents of the “outbound” DS1 Channel 10 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits the contents of DS1 Channel 10 to be transmitted as received (via the TxDS1Data10 input pin).

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 1 - Insert AIS Tx DS1 Channel 9

This “Read/Write” bit-field permits the user to configure the contents of the “outbound” DS1 Channel 9 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits the contents of DS1 Channel 8 to be transmitted as received (via the TxDS1Data9 input pin).

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 0 - Insert AIS Tx DS1 Channel 8

This “Read/Write” bit-field permits the user to configure the contents of the “outbound” DS1 Channel 8 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits the contents of DS1 Channel 8 to be transmitted as received (via the TxDS1Data8 input pin).

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

2.3.2.34 M12 DS2 # 4 AIS Register)

M12 DS2 # 4 AIS REGISTER (ADDRESS = 0X24)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Insert AIS Rx DS1 Channel 15	Insert AIS Rx DS1 Channel 14	Insert AIS Rx DS1 Channel 13	Insert AIS Rx DS1 Channel 12	Insert AIS Tx DS1 Channel 15	Insert AIS Tx DS1 Channel 14	Insert AIS Tx DS1 Channel 13	Insert AIS Tx DS1 Channel 12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	1	1	1

Bit 7 - Insert AIS Rx DS1 Channel 15

This “Read/Write” bit-field permits the user to configure the contents of the “inbound” DS1 Channel 15 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits data to be output (via the RxDS1Data15 output pin, as demultiplexed via the inbound DS2 and DS3 data streams.

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 6 - Insert AIS Rx DS1 Channel 14

This “Read/Write” bit-field permits the user to configure the contents of the “inbound” DS1 Channel 14 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits data to be output (via the RxDS1Data14 output pin, as demultiplexed via the inbound DS2 and DS3 data streams.

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 5 - Insert AIS Rx DS1 Channel 13

This “Read/Write” bit-field permits the user to configure the contents of the “inbound” DS1 Channel 13 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits data to be output (via the RxDS1Data13 output pin, as demultiplexed via the inbound DS2 and DS3 data streams.

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 4 - Insert AIS Rx DS1 Channel 12

This “Read/Write” bit-field permits the user to configure the contents of the “inbound” DS1 Channel 12 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits data to be output (via the RxDS1Data12 output pin, as demultiplexed via the inbound DS2 and DS3 data streams.

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 3 - Insert AIS Tx DS1 Channel 15

This “Read/Write” bit-field permits the user to configure the contents of the “outbound” DS1 Channel 15 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits the contents of DS1 Channel 15 to be transmitted as received (via the TxDS1Data15 input pin).

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 2 - Insert AIS Tx DS1 Channel 14

This “Read/Write” bit-field permits the user to configure the contents of the “outbound” DS1 Channel 14 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits the contents of DS1 Channel 14 to be transmitted as received (via the TxDS1Data14 input pin).

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 1 - Insert AIS Tx DS1 Channel 13

This “Read/Write” bit-field permits the user to configure the contents of the “outbound” DS1 Channel 13 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits the contents of DS1 Channel 13 to be transmitted as received (via the TxDS1Data13 input pin).

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 0 - Insert AIS Tx DS1 Channel 12

This “Read/Write” bit-field permits the user to configure the contents of the “outbound” DS1 Channel 12 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits the contents of DS1 Channel 12 to be transmitted as received (via the TxDS1Data12 input pin).

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

2.3.2.35 M12 DS2 # 5 AIS Register)

M12 DS2 # 5 AIS REGISTER (ADDRESS = 0X25)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Insert AIS Rx DS1 Channel 19	Insert AIS Rx DS1 Channel 18	Insert AIS Rx DS1 Channel 17	Insert AIS Rx DS1 Channel 16	Insert AIS Tx DS1 Channel 19	Insert AIS Tx DS1 Channel 18	Insert AIS Tx DS1 Channel 17	Insert AIS Tx DS1 Channel 16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	1	1	1

Bit 7 - Insert AIS Rx DS1 Channel 19

This “Read/Write” bit-field permits the user to configure the contents of the “inbound” DS1 Channel 19 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits data to be output (via the RxDS1Data19 output pin, as demultiplexed via the inbound DS2 and DS3 data streams.

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 6 - Insert AIS Rx DS1 Channel 18

This “Read/Write” bit-field permits the user to configure the contents of the “inbound” DS1 Channel 18 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits data to be output (via the RxDS1Data18 output pin, as demultiplexed via the inbound DS2 and DS3 data streams.

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 5 - Insert AIS Rx DS1 Channel 17

This “Read/Write” bit-field permits the user to configure the contents of the “inbound” DS1 Channel 17 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits data to be output (via the RxDS1Data17 output pin, as demultiplexed via the inbound DS2 and DS3 data streams.

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 4 - Insert AIS Rx DS1 Channel 16

This “Read/Write” bit-field permits the user to configure the contents of the “inbound” DS1 Channel 16 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits data to be output (via the RxDS1Data16 output pin, as demultiplexed via the inbound DS2 and DS3 data streams.

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 3 - Insert AIS Tx DS1 Channel 19

This “Read/Write” bit-field permits the user to configure the contents of the “outbound” DS1 Channel 19 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits the contents of DS1 Channel 19 to be transmitted as received (via the TxDS1Data19 input pin).

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 2 - Insert AIS Tx DS1 Channel 18

This “Read/Write” bit-field permits the user to configure the contents of the “outbound” DS1 Channel 18 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits the contents of DS1 Channel 18 to be transmitted as received (via the TxDS1Data18 input pin).

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 1 - Insert AIS Tx DS1 Channel 17

This “Read/Write” bit-field permits the user to configure the contents of the “outbound” DS1 Channel 17 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits the contents of DS1 Channel 17 to be transmitted as received (via the TxDS1Data17 input pin).

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 0 - Insert AIS Tx DS1 Channel 16

This “Read/Write” bit-field permits the user to configure the contents of the “outbound” DS1 Channel 16 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits the contents of DS1 Channel 16 to be transmitted as received (via the TxDS1Data16 input pin).

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

2.3.2.36 M12 DS2 # 6 AIS Register)

M12 DS2 # 6 AIS REGISTER (ADDRESS = 0X26)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Insert AIS Rx DS1 Channel 23	Insert AIS Rx DS1 Channel 22	Insert AIS Rx DS1 Channel 21	Insert AIS Rx DS1 Channel 20	Insert AIS Tx DS1 Channel 23	Insert AIS Tx DS1 Channel 22	Insert AIS Tx DS1 Channel 21	Insert AIS Tx DS1 Channel 20
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	1	1	1

Bit 7 - Insert AIS Rx DS1 Channel 23

This “Read/Write” bit-field permits the user to configure the contents of the “inbound” DS1 Channel 23 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits data to be output (via the RxDS1Data23 output pin, as demultiplexed via the inbound DS2 and DS3 data streams.

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 6 - Insert AIS Rx DS1 Channel 22

This “Read/Write” bit-field permits the user to configure the contents of the “inbound” DS1 Channel 22 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits data to be output (via the RxDS1Data22 output pin, as demultiplexed via the inbound DS2 and DS3 data streams.

Bit 5 - insert AIS Rx DS1 Channel 21

This “Read/Write” bit-field permits the user to configure the contents of the “inbound” DS1 Channel 21 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits data to be output (via the RxDS1Data21 output pin), as demultiplexed via the inbound DS2 and DS3 data streams.

Bit 4 - Insert AIS Rx DS1 Channel 20

This “Read/Write” bit-field permits the user to configure the contents of the “inbound” DS1 Channel 20 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits data to be output (via the RxDS1Data20 output pin), as demultiplexed via the inbound DS2 and DS3 data streams.

Bit 3 - Insert AIS Tx DS1 Channel 23

This “Read/Write” bit-field permits the user to configure the contents of the “outbound” DS1 Channel 23 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits the contents of DS1 Channel 23 to be transmitted as received (via the TxDS1Data23 input pin).

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 2 - Insert AIS Tx DS1 Channel 22

This “Read/Write” bit-field permits the user to configure the contents of the “outbound” DS1 Channel 22 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits the contents of DS1 Channel 22 to be transmitted as received (via the TxDS1Data22 input pin).

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 1 - Insert AIS Tx DS1 Channel 21

This “Read/Write” bit-field permits the user to configure the contents of the “outbound” DS1 Channel 21 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits the contents of DS1 Channel 21 to be transmitted as received (via the TxDS1Data21 input pin).

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 0 - Insert AIS Tx DS1 Channel 20

This “Read/Write” bit-field permits the user to configure the contents of the “outbound” DS1 Channel 20 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits the contents of DS1 Channel 20 to be transmitted as received (via the TxDS1Data20 input pin).

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

2.3.2.37 M12 DS2 # 7 AIS Register)

M12 DS2 # 7 AIS REGISTER (ADDRESS = 0X27)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Insert AIS Rx DS1 Channel 27	Insert AIS Rx DS1 Channel 26	Insert AIS Rx DS1 Channel 25	Insert AIS Rx DS1 Channel 24	Insert AIS Tx DS1 Channel 27	Insert AIS Tx DS1 Channel 26	Insert AIS Tx DS1 Channel 25	Insert AIS Tx DS1 Channel 24
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	1	1	1

Bit 7 - Insert AIS Rx DS1 Channel 27

This “Read/Write” bit-field permits the user to configure the contents of the “inbound” DS1 Channel 27 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits data to be output (via the RxDS1Data27 output pin), as demultiplexed via the inbound DS2 and DS3 data streams.

Bit 6 - Insert AIS Rx DS1 Channel 26

This “Read/Write” bit-field permits the user to configure the contents of the “inbound” DS1 Channel 26 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits data to be output (via the RxDS1Data26 output pin), as demultiplexed via the inbound DS2 and DS3 data streams.

Bit 5 - Insert AIS Rx DS1 Channel 25

This “Read/Write” bit-field permits the user to configure the contents of the “inbound” DS1 Channel 25 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits data to be output (via the RxDS1Data25 output pin), as demultiplexed via the inbound DS2 and DS3 data streams.

Bit 4 - Insert AIS Rx DS1 Channel 24

This “Read/Write” bit-field permits the user to configure the contents of the “inbound” DS1 Channel 24 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits data to be output (via the RxDS1Data24 output pin), as demultiplexed via the inbound DS2 and DS3 data streams.

Bit 3 - Insert AIS Tx DS1 Channel 27

This “Read/Write” bit-field permits the user to configure the contents of the “outbound” DS1 Channel 27 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits the contents of DS1 Channel 27 to be transmitted as received (via the TxDS1Data27 input pin).

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 2 - Insert AIS Tx DS1 Channel 26

This “Read/Write” bit-field permits the user to configure the contents of the “outbound” DS1 Channel 26 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits the contents of DS1 Channel 26 to be transmitted as received (via the TxDS1Data26 input pin).

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 1 - Insert AIS Tx DS1 Channel 25

This “Read/Write” bit-field permits the user to configure the contents of the “outbound” DS1 Channel 25 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits the contents of DS1 Channel 25 to be transmitted as received (via the TxDS1Data25 input pin).

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 0 - Insert AIS Tx DS1 Channel 24

This “Read/Write” bit-field permits the user to configure the contents of the “outbound” DS1 Channel 24 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits the contents of DS1 Channel 24 to be transmitted as received (via the TxDS1Data24 input pin).

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

2.3.2.38 M12 DS2 # 1 Loopback Request Register)

M12 DS2 # 1 LOOP-BACK REGISTER (ADDRESS = 0X28)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Loop-back Activation DS1 Channel 3	Loop-back Activation DS1 Channel 2	Loop-back Activation DS1 Channel 1	Loop-back Activation DS1 Channel 0	Loop-back Request DS1 Channel 3	Loop-back Request DS1 Channel 2	Loop-back Request DS1 Channel 1	Loop-back Request DS1 Channel 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit 7 - Loop-back Activation - DS1 Channel 3

This “Read/Write” bit-field permits the user to configure DS1 Channel 3 into Remote Loop-back Mode. When this loop-back is configured, then the “RxDS1Data_3” signal will internally be “looped-back” into the “TxDS1Data_3” path. Further, the “RxDS1Clock_3” clock signal will also be internally looped back into the “RxDS1Clock_3” signal path.

Setting this bit-field to “1” enables this loop-back mode. Conversely, setting this bit-field to “0” disables this loop-back mode.

NOTE: *This bit-field is ignored if the XRT72L13 has been configured to operate in the “ITU-T G.747” Mode.*

Bit 6 - Loop-back Activation - DS1 Channel 2

This “Read/Write” bit-field permits the user to configure DS1 Channel 2 into Remote Loop-back Mode. When this loop-back is configured, then the “RxDS1Data_2” signal will internally be “looped-back” into the “TxDS1Data_2” path. Further, the “RxDS1Clock_2” clock signal will also be internally looped back into the “RxDS1Clock_2” signal path.

Setting this bit-field to “1” enables this loop-back mode. Conversely, setting this bit-field to “0” disables this loop-back mode.

Bit 5 - Loop-back Activation - DS1 Channel 1

This “Read/Write” bit-field permits the user to configure DS1 Channel 1 into Remote Loop-back Mode. When this loop-back is configured, then the “RxDS1Data_1” signal will internally be “looped-back” into the “TxDS1Data_1” path. Further, the “RxDS1Clock_1” clock signal will also be internally looped back into the “RxDS1Clock_1” signal path.

Setting this bit-field to “1” enables this loop-back mode. Conversely, setting this bit-field to “0” disables this loop-back mode.

Bit 4 - Loop-back Activation - DS1 Channel 0

This “Read/Write” bit-field permits the user to configure DS1 Channel 0 into Remote Loop-back Mode. When this loop-back is configured, then the “RxDS1Data_0” signal will internally be “looped-back” into the “TxDS1Data_0” path. Further, the “RxDS1Clock_0” clock signal will also be internally looped back into the “RxDS1Clock_0” signal path.

Setting this bit-field to “1” enables this loop-back mode. Conversely, setting this bit-field to “0” disables this loop-back mode.

Bit 3 - Loop-back Request - DS1 Channel 3

This “Read/Write” bit-field permits the user to configure the XRT72L13 to transmit a “DS1 Channel 3 - Loop-back Request” signal to the Remote Terminal Equipment. When the Remote Terminal Equipment receives this request, it is expected to respond by configuring its own DS1 Channel 3 signal into Loop-back Mode.

NOTE: *This bit-field is ignored if the XRT72L13 has been configured to operate in the “ITU-T G.747” Mode.*

Bit 2 - Loop-back Request - DS1 Channel 2

This “Read/Write” bit-field permits the user to configure the XRT72L13 to transmit a “DS1 Channel 2 - Loop-back Request” signal to the Remote Terminal Equipment. When the Remote Terminal Equipment receives this request, it is expected to respond by configuring its own DS1 Channel 2 signal into Loop-back Mode.

NOTE: *This bit-field is ignored if the XRT72L13 has been configured to operate in the “ITU-T G.747” Mode.*

Bit 1 - Loop-back Request - DS1 Channel 1

This “Read/Write” bit-field permits the user to configure the XRT72L13 to transmit a “DS1 Channel 1 - Loop-back Request” signal to the Remote Terminal Equipment. When the Remote Terminal Equipment receives this request, it is expected to respond by configuring its own DS1 Channel 1 signal into Loop-back Mode.

NOTE: *This bit-field is ignored if the XRT72L13 has been configured to operate in the “ITU-T G.747” Mode.*

Bit 0 - Loop-back Request - DS1 Channel 0

This “Read/Write” bit-field permits the user to configure the XRT72L13 to transmit a “DS1 Channel 0 - Loop-back Request” signal to the Remote Terminal Equipment. When the Remote Terminal Equipment receives this request, it is expected to respond by configuring its own DS1 Channel 0 signal into Loop-back Mode.

NOTE: *This bit-field is ignored if the XRT72L13 has been configured to operate in the “ITU-T G.747” Mode.*

2.3.2.39 M12 DS2 # 2 Loopback Request Register)

M12 DS2 # 2 LOOP-BACK REGISTER (ADDRESS = 0X29)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Loop-back Activation DS1 Channel 7	Loop-back Activation DS1 Channel 6	Loop-back Activation DS1 Channel 5	Loop-back Activation DS1 Channel 4	Loop-back Request DS1 Channel 7	Loop-back Request DS1 Channel 6	Loop-back Request DS1 Channel 5	Loop-back Request DS1 Channel 4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit 7 - Loop-back Activation - DS1 Channel 7

This “Read/Write” bit-field permits the user to configure DS1 Channel 7 into Remote Loop-back Mode. When this loop-back is configured, then the “RxDS1Data_7” signal will internally be “looped-back” into the “TxDS1Data_7” path. Further, the “RxDS1Clock_7” clock signal will also be internally looped back into the “RxDS1Clock_7” signal path.

Setting this bit-field to “1” enables this loop-back mode. Conversely, setting this bit-field to “0” disables this loop-back mode.

NOTE: *This bit-field is ignored if the XRT72L13 has been configured to operate in the “ITU-T G.747” Mode.*

Bit 6 - Loop-back Activation - DS1 Channel 6

This “Read/Write” bit-field permits the user to configure DS1 Channel 6 into Remote Loop-back Mode. When this loop-back is configured, then the “RxDS1Data_6” signal will internally be “looped-back” into the “TxDS1Data_6” path. Further, the “RxDS1Clock_6” clock signal will also be internally looped back into the “RxDS1Clock_6” signal path.

Setting this bit-field to “1” enables this loop-back mode. Conversely, setting this bit-field to “0” disables this loop-back mode.

Bit 5 - Loop-back Activation - DS1 Channel 5

This “Read/Write” bit-field permits the user to configure DS1 Channel 5 into Remote Loop-back Mode. When this loop-back is configured, then the “RxDS1Data_5” signal will internally be “looped-back” into the “TxDS1Data_5” path. Further, the “RxDS1Clock_5” clock signal will also be internally looped back into the “RxDS1Clock_5” signal path.

Setting this bit-field to “1” enables this loop-back mode. Conversely, setting this bit-field to “0” disables this loop-back mode.

Bit 4 - Loop-back Activation - DS1 Channel 4

This “Read/Write” bit-field permits the user to configure DS1 Channel 4 into Remote Loop-back Mode. When this loop-back is configured, then the “RxDS1Data_4” signal will internally be “looped-back” into the “TxDS1Data_4” path. Further, the “RxDS1Clock_4” clock signal will also be internally looped back into the “RxDS1Clock_4” signal path.

Setting this bit-field to “1” enables this loop-back mode. Conversely, setting this bit-field to “0” disables this loop-back mode.

Bit 3 - Loop-back Request - DS1 Channel 7

This “Read/Write” bit-field permits the user to configure the XRT72L13 to transmit a “DS1 Channel 7 - Loop-back Request” signal to the Remote Terminal Equipment. When the Remote Terminal Equipment receives this request, it is expected to respond by configuring its own DS1 Channel 7 signal into Loop-back Mode.

NOTE: *This bit-field is ignored if the XRT72L13 has been configured to operate in the “ITU-T G.747” Mode.*

Bit 2 - Loop-back Request - DS1 Channel 6

This “Read/Write” bit-field permits the user to configure the XRT72L13 to transmit a “DS1 Channel 6 - Loop-back Request” signal to the Remote Terminal Equipment. When the Remote Terminal Equipment receives this request, it is expected to respond by configuring its own DS1 Channel 6 signal into Loop-back Mode.

NOTE: *This bit-field is ignored if the XRT72L13 has been configured to operate in the “ITU-T G.747” Mode.*

Bit 1 - Loop-back Request - DS1 Channel 5

This “Read/Write” bit-field permits the user to configure the XRT72L13 to transmit a “DS1 Channel 5 - Loop-back Request” signal to the Remote Terminal Equipment. When the Remote Terminal Equipment receives this request, it is expected to respond by configuring its own DS1 Channel 5 signal into Loop-back Mode.

NOTE: *This bit-field is ignored if the XRT72L13 has been configured to operate in the “ITU-T G.747” Mode.*

Bit 0 - Loop-back Request - DS1 Channel 4

This “Read/Write” bit-field permits the user to configure the XRT72L13 to transmit a “DS1 Channel 4 - Loop-back Request” signal to the Remote Terminal Equipment. When the Remote Terminal Equipment receives this request, it is expected to respond by configuring its own DS1 Channel 4 signal into Loop-back Mode.

NOTE: *This bit-field is ignored if the XRT72L13 has been configured to operate in the “ITU-T G.747” Mode.*

2.3.2.40 M12 DS2 # 3 Loopback Request Register)

M12 DS2 # 3 LOOP-BACK REGISTER (ADDRESS = 0X2A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Loop-back Activation DS1 Channel 11	Loop-back Activation DS1 Channel 10	Loop-back Activation DS1 Channel 9	Loop-back Activation DS1 Channel 8	Loop-back Request DS1 Channel 11	Loop-back Request DS1 Channel 10	Loop-back Request DS1 Channel 9	Loop-back Request DS1 Channel 8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit 7 - Loop-back Activation - DS1 Channel 11

This “Read/Write” bit-field permits the user to configure DS1 Channel 11 into Remote Loop-back Mode.

When this loop-back is configured, then the "RxDS1Data_11" signal will internally be "looped-back" into the "TxDS1Data_11" path. Further, the "RxDS1Clock_11" clock signal will also be internally looped back into the "RxDS1Clock_11" signal path.

Setting this bit-field to "1" enables this loop-back mode. Conversely, setting this bit-field to "0" disables this loop-back mode.

NOTE: *This bit-field is ignored if the XRT72L13 has been configured to operate in the "ITU-T G.747" Mode.*

Bit 6 - Loop-back Activation - DS1 Channel 10

This "Read/Write" bit-field permits the user to configure DS1 Channel 10 into Remote Loop-back Mode. When this loop-back is configured, then the "RxDS1Data_10" signal will internally be "looped-back" into the "TxDS1Data_10" path. Further, the "RxDS1Clock_10" clock signal will also be internally looped back into the "RxDS1Clock_10" signal path.

Setting this bit-field to "1" enables this loop-back mode. Conversely, setting this bit-field to "0" disables this loop-back mode.

Bit 5 - Loop-back Activation - DS1 Channel 9

This "Read/Write" bit-field permits the user to configure DS1 Channel 9 into Remote Loop-back Mode. When this loop-back is configured, then the "RxDS1Data_9" signal will internally be "looped-back" into the "TxDS1Data_9" path. Further, the "RxDS1Clock_9" clock signal will also be internally looped back into the "RxDS1Clock_9" signal path.

Setting this bit-field to "1" enables this loop-back mode. Conversely, setting this bit-field to "0" disables this loop-back mode.

Bit 4 - Loop-back Activation - DS1 Channel 8

This "Read/Write" bit-field permits the user to configure DS1 Channel 8 into Remote Loop-back Mode. When this loop-back is configured, then the "RxDS1Data_8" signal will internally be "looped-back" into the "TxDS1Data_8" path. Further, the "RxDS1Clock_8" clock signal will also be internally looped back into the "RxDS1Clock_8" signal path.

Setting this bit-field to "1" enables this loop-back mode. Conversely, setting this bit-field to "0" disables this loop-back mode.

Bit 3 - Loop-back Request - DS1 Channel 11

This "Read/Write" bit-field permits the user to configure the XRT72L13 to transmit a "DS1 Channel 11 - Loop-back Request" signal to the Remote Terminal Equipment. When the Remote Terminal Equipment receives this request, it is expected to respond by configuring its own DS1 Channel 11 signal into Loop-back Mode.

NOTE: *This bit-field is ignored if the XRT72L13 has been configured to operate in the "ITU-T G.747" Mode.*

Bit 2 - Loop-back Request - DS1 Channel 10

This "Read/Write" bit-field permits the user to configure the XRT72L13 to transmit a "DS1 Channel 10 - Loop-back Request" signal to the Remote Terminal Equipment. When the Remote Terminal Equipment receives this request, it is expected to respond by configuring its own DS1 Channel 10 signal into Loop-back Mode.

NOTE: *This bit-field is ignored if the XRT72L13 has been configured to operate in the "ITU-T G.747" Mode.*

Bit 1 - Loop-back Request - DS1 Channel 9

This "Read/Write" bit-field permits the user to configure the XRT72L13 to transmit a "DS1 Channel 9 - Loop-back Request" signal to the Remote Terminal Equipment. When the Remote Terminal Equipment receives this request, it is expected to respond by configuring its own DS1 Channel 9 signal into Loop-back Mode.

NOTE: *This bit-field is ignored if the XRT72L13 has been configured to operate in the "ITU-T G.747" Mode.*

Bit 0 - Loop-back Request - DS1 Channel 8

This "Read/Write" bit-field permits the user to configure the XRT72L13 to transmit a "DS1 Channel 8 - Loop-back Request" signal to the Remote Terminal Equipment. When the Remote Terminal Equipment receives this request, it is expected to respond by configuring its own DS1 Channel 8 signal into Loop-back Mode.

NOTE: *This bit-field is ignored if the XRT72L13 has been configured to operate in the "ITU-T G.747" Mode.*

2.3.2.41 M12 DS2 # 4 Loop-back Request Register

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M12 DS2 # 4 LOOP-BACK REGISTER (ADDRESS = 0X2B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Loop-back Activation DS1 Channel 15	Loop-back Activation DS1 Channel 14	Loop-back Activation DS1 Channel 13	Loop-back Activation DS1 Channel 12	Loop-back Request DS1 Channel 15	Loop-back Request DS1 Channel 14	Loop-back Request DS1 Channel 13	Loop-back Request DS1 Channel 12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit 7 - Loop-back Activation - DS1 Channel 15

This “Read/Write” bit-field permits the user to configure DS1 Channel 15 into Remote Loop-back Mode. When this loop-back is configured, then the “RxDS1Data_15” signal will internally be “looped-back” into the “TxDS1Data_15” path. Further, the “RxDS1Clock_15” clock signal will also be internally looped back into the “RxDS1Clock_15” signal path.

Setting this bit-field to “1” enables this loop-back mode. Conversely, setting this bit-field to “0” disables this loop-back mode.

NOTE: *This bit-field is ignored if the XRT72L13 has been configured to operate in the “ITU-T G.747” Mode.*

Bit 6 - Loop-back Activation - DS1 Channel 14

This “Read/Write” bit-field permits the user to configure DS1 Channel 14 into Remote Loop-back Mode. When this loop-back is configured, then the “RxDS1Data_14” signal will internally be “looped-back” into the “TxDS1Data_14” path. Further, the “RxDS1Clock_14” clock signal will also be internally looped back into the “RxDS1Clock_14” signal path.

Setting this bit-field to “1” enables this loop-back mode. Conversely, setting this bit-field to “0” disables this loop-back mode.

Bit 5 - Loop-back Activation - DS1 Channel 13

This “Read/Write” bit-field permits the user to configure DS1 Channel 13 into Remote Loop-back Mode. When this loop-back is configured, then the “RxDS1Data_13” signal will internally be “looped-back” into the “TxDS1Data_13” path. Further, the “RxDS1Clock_13” clock signal will also be internally looped back into the “RxDS1Clock_13” signal path.

Setting this bit-field to “1” enables this loop-back mode. Conversely, setting this bit-field to “0” disables this loop-back mode.

Bit 4 - Loop-back Activation - DS1 Channel 12

This “Read/Write” bit-field permits the user to configure DS1 Channel 12 into Remote Loop-back Mode. When this loop-back is configured, then the “RxDS1Data_12” signal will internally be “looped-back” into the “TxDS1Data_12” path. Further, the “RxDS1Clock_12” clock signal will also be internally looped back into the “RxDS1Clock_12” signal path.

Setting this bit-field to “1” enables this loop-back mode. Conversely, setting this bit-field to “0” disables this loop-back mode.

Bit 3 - Loop-back Request - DS1 Channel 15

This “Read/Write” bit-field permits the user to configure the XRT72L13 to transmit a “DS1 Channel 15 - Loop-back Request” signal to the Remote Terminal Equipment. When the Remote Terminal Equipment receives this request, it is expected to respond by configuring its own DS1 Channel 15 signal into Loop-back Mode.

NOTE: *This bit-field is ignored if the XRT72L13 has been configured to operate in the “ITU-T G.747” Mode.*

Bit 2 - Loop-back Request - DS1 Channel 14

This “Read/Write” bit-field permits the user to configure the XRT72L13 to transmit a “DS1 Channel 14 - Loop-back Request” signal to the Remote Terminal Equipment. When the Remote Terminal Equipment receives this request, it is expected to respond by configuring its own DS1 Channel 14 signal into Loop-back Mode.

NOTE: *This bit-field is ignored if the XRT72L13 has been configured to operate in the “ITU-T G.747” Mode.*

Bit 1 - Loop-back Request - DS1 Channel 13

This “Read/Write” bit-field permits the user to configure the XRT72L13 to transmit a “DS1 Channel 13 - Loop-back Request” signal to the Remote Terminal Equipment. When the Remote Terminal Equipment receives this request, it is expected to respond by configuring its own DS1 Channel 13 signal into Loop-back Mode.

NOTE: *This bit-field is ignored if the XRT72L13 has been configured to operate in the “ITU-T G.747” Mode.*

Bit 0 - Loop-back Request - DS1 Channel 12

This “Read/Write” bit-field permits the user to configure the XRT72L13 to transmit a “DS1 Channel 12 - Loop-back Request” signal to the Remote Terminal Equipment. When the Remote Terminal Equipment receives this request, it is expected to respond by configuring its own DS1 Channel 12 signal into Loop-back Mode.

NOTE: *This bit-field is ignored if the XRT72L13 has been configured to operate in the “ITU-T G.747” Mode.*

2.3.2.42 M12 DS2 # 5 Loopback Request Register)

M12 DS2 # 5 LOOP-BACK REGISTER (ADDRESS = 0X2C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Loop-back Activation DS1 Channel 19	Loop-back Activation DS1 Channel 18	Loop-back Activation DS1 Channel 17	Loop-back Activation DS1 Channel 16	Loop-back Request DS1 Channel 19	Loop-back Request DS1 Channel 18	Loop-back Request DS1 Channel 17	Loop-back Request DS1 Channel 16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit 7 - Loop-back Activation - DS1 Channel 19

This “Read/Write” bit-field permits the user to configure DS1 Channel 19 into Remote Loop-back Mode. When this loop-back is configured, then the “RxDS1Data_19” signal will internally be “looped-back” into the “TxDS1Data_19” path. Further, the “RxDS1Clock_19” clock signal will also be internally looped back into the “RxDS1Clock_19” signal path.

Setting this bit-field to “1” enables this loop-back mode. Conversely, setting this bit-field to “0” disables this loop-back mode.

NOTE: *This bit-field is ignored if the XRT72L13 has been configured to operate in the “ITU-T G.747” Mode.*

Bit 6 - Loop-back Activation - DS1 Channel 18

This “Read/Write” bit-field permits the user to configure DS1 Channel 18 into Remote Loop-back Mode. When this loop-back is configured, then the “RxDS1Data_18” signal will internally be “looped-back” into the “TxDS1Data_18” path. Further, the “RxDS1Clock_18” clock signal will also be internally looped back into the “RxDS1Clock_18” signal path.

Setting this bit-field to “1” enables this loop-back mode. Conversely, setting this bit-field to “0” disables this loop-back mode.

Bit 5 - Loop-back Activation - DS1 Channel 17

This “Read/Write” bit-field permits the user to configure DS1 Channel 17 into Remote Loop-back Mode. When this loop-back is configured, then the “RxDS1Data_17” signal will internally be “looped-back” into the “TxDS1Data_17” path. Further, the “RxDS1Clock_17” clock signal will also be internally looped back into the “RxDS1Clock_17” signal path.

Setting this bit-field to “1” enables this loop-back mode. Conversely, setting this bit-field to “0” disables this loop-back mode.

Bit 4 - Loop-back Activation - DS1 Channel 16

This “Read/Write” bit-field permits the user to configure DS1 Channel 16 into Remote Loop-back Mode. When this loop-back is configured, then the “RxDS1Data_16” signal will internally be “looped-back” into the “TxDS1Data_16” path. Further, the “RxDS1Clock_16” clock signal will also be internally looped back into the “RxDS1Clock_16” signal path.

Setting this bit-field to “1” enables this loop-back mode. Conversely, setting this bit-field to “0” disables this loop-back mode.

Bit 3 - Loop-back Request - DS1 Channel 19

This “Read/Write” bit-field permits the user to configure the XRT72L13 to transmit a “DS1 Channel 19 - Loop-back Request” signal to the Remote Terminal Equipment. When the Remote Terminal Equipment receives this request, it is expected to respond by configuring its own DS1 Channel 19 signal into Loop-back Mode.

NOTE: *This bit-field is ignored if the XRT72L13 has been configured to operate in the “ITU-T G.747” Mode.*

Bit 2 - Loop-back Request - DS1 Channel 18

This “Read/Write” bit-field permits the user to configure the XRT72L13 to transmit a “DS1 Channel 18 - Loop-back Request” signal to the Remote Terminal Equipment. When the Remote Terminal Equipment receives this request, it is expected to respond by configuring its own DS1 Channel 18 signal into Loop-back Mode.

NOTE: *This bit-field is ignored if the XRT72L13 has been configured to operate in the “ITU-T G.747” Mode.*

Bit 1 - Loop-back Request - DS1 Channel 17

This “Read/Write” bit-field permits the user to configure the XRT72L13 to transmit a “DS1 Channel 17 - Loop-back Request” signal to the Remote Terminal Equipment. When the Remote Terminal Equipment receives this request, it is expected to respond by configuring its own DS1 Channel 17 signal into Loop-back Mode.

NOTE: *This bit-field is ignored if the XRT72L13 has been configured to operate in the “ITU-T G.747” Mode.*

Bit 0 - Loop-back Request - DS1 Channel 16

This “Read/Write” bit-field permits the user to configure the XRT72L13 to transmit a “DS1 Channel 16 - Loop-back Request” signal to the Remote Terminal Equipment. When the Remote Terminal Equipment receives this request, it is expected to respond by configuring its own DS1 Channel 16 signal into Loop-back Mode.

NOTE: *This bit-field is ignored if the XRT72L13 has been configured to operate in the “ITU-T G.747” Mode.*

2.3.2.43 M12 DS2 # 6 Loopback Request Register)

M12 DS2 # 6 LOOP-BACK REGISTER (ADDRESS = 0X2D)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Loop-back Activation DS1 Channel 23	Loop-back Activation DS1 Channel 22	Loop-back Activation DS1 Channel 21	Loop-back Activation DS1 Channel 20	Loop-back Request DS1 Channel 23	Loop-back Request DS1 Channel 22	Loop-back Request DS1 Channel 21	Loop-back Request DS1 Channel 20
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit 7 - Loop-back Activation - DS1 Channel 23

This “Read/Write” bit-field permits the user to configure DS1 Channel 23 into Remote Loop-back Mode. When this loop-back is configured, then the “RxDS1Data_23” signal will internally be “looped-back” into the “TxDS1Data_23” path. Further, the “RxDS1Clock_23” clock signal will also be internally looped back into the “RxDS1Clock_23” signal path.

Setting this bit-field to “1” enables this loop-back mode. Conversely, setting this bit-field to “0” disables this loop-back mode.

NOTE: *This bit-field is ignored if the XRT72L13 has been configured to operate in the “ITU-T G.747” Mode.*

Bit 6 - Loop-back Activation - DS1 Channel 22

This “Read/Write” bit-field permits the user to configure DS1 Channel 22 into Remote Loop-back Mode. When this loop-back is configured, then the “RxDS1Data_22” signal will internally be “looped-back” into the “TxDS1Data_22” path. Further, the “RxDS1Clock_22” clock signal will also be internally looped back into the “RxDS1Clock_22” signal path.

Setting this bit-field to “1” enables this loop-back mode. Conversely, setting this bit-field to “0” disables this loop-back mode.

Bit 5 - Loop-back Activation - DS1 Channel 21

This “Read/Write” bit-field permits the user to configure DS1 Channel 21 into Remote Loop-back Mode. When this loop-back is configured, then the “RxDS1Data_21” signal will internally be “looped-back” into the “TxDS1Data_21” path. Further, the “RxDS1Clock_21” clock signal will also be internally looped back into the “RxDS1Clock_21” signal path.

Setting this bit-field to “1” enables this loop-back mode. Conversely, setting this bit-field to “0” disables this loop-back mode.

Bit 4 - Loop-back Activation - DS1 Channel 20

This “Read/Write” bit-field permits the user to configure DS1 Channel 20 into Remote Loop-back Mode. When this loop-back is configured, then the “RxDS1Data_20” signal will internally be “looped-back” into the “TxDS1Data_20” path. Further, the “RxDS1Clock_20” clock signal will also be internally looped back into the “RxDS1Clock_20” signal path.

Setting this bit-field to “1” enables this loop-back mode. Conversely, setting this bit-field to “0” disables this loop-back mode.

Bit 3 - Loop-back Request - DS1 Channel 23

This “Read/Write” bit-field permits the user to configure the XRT72L13 to transmit a “DS1 Channel 23 - Loop-back Request” signal to the Remote Terminal Equipment. When the Remote Terminal Equipment receives this request, it is expected to respond by configuring its own DS1 Channel 23 signal into Loop-back Mode.

NOTE: *This bit-field is ignored if the XRT72L13 has been configured to operate in the “ITU-T G.747” Mode.*

Bit 2 - Loop-back Request - DS1 Channel 22

This “Read/Write” bit-field permits the user to configure the XRT72L13 to transmit a “DS1 Channel 22 - Loop-back Request” signal to the Remote Terminal Equipment. When the Remote Terminal Equipment receives this request, it is expected to respond by configuring its own DS1 Channel 22 signal into Loop-back Mode.

NOTE: *This bit-field is ignored if the XRT72L13 has been configured to operate in the “ITU-T G.747” Mode.*

Bit 1 - Loop-back Request - DS1 Channel 21

This “Read/Write” bit-field permits the user to configure the XRT72L13 to transmit a “DS1 Channel 21 - Loop-back Request” signal to the Remote Terminal Equipment. When the Remote Terminal Equipment receives this request, it is expected to respond by configuring its own DS1 Channel 21 signal into Loop-back Mode.

NOTE: *This bit-field is ignored if the XRT72L13 has been configured to operate in the “ITU-T G.747” Mode.*

Bit 0 - Loop-back Request - DS1 Channel 20

This “Read/Write” bit-field permits the user to configure the XRT72L13 to transmit a “DS1 Channel 20 - Loop-back Request” signal to the Remote Terminal Equipment. When the Remote Terminal Equipment receives this request, it is expected to respond by configuring its own DS1 Channel 20 signal into Loop-back Mode.

NOTE: *This bit-field is ignored if the XRT72L13 has been configured to operate in the “ITU-T G.747” Mode.*

2.3.2.44 M12 DS2 # 7 Loopback Request Register)

M12 DS2 # 7 LOOP-BACK REGISTER (ADDRESS = 0X28)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Loop-back Activation DS1 Channel 27	Loop-back Activation DS1 Channel 26	Loop-back Activation DS1 Channel 25	Loop-back Activation DS1 Channel 24	Loop-back Request DS1 Channel 27	Loop-back Request DS1 Channel 26	Loop-back Request DS1 Channel 25	Loop-back Request DS1 Channel 24
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit 7 - Loop-back Activation - DS1 Channel 27

This “Read/Write” bit-field permits the user to configure DS1 Channel 27 into Remote Loop-back Mode. When this loop-back is configured, then the “RxDS1Data_27” signal will internally be “looped-back” into the “TxDS1Data_27” path. Further, the “RxDS1Clock_27” clock signal will also be internally looped back into the “RxDS1Clock_27” signal path.

Setting this bit-field to “1” enables this loop-back mode. Conversely, setting this bit-field to “0” disables this loop-back mode.

NOTE: *This bit-field is ignored if the XRT72L13 has been configured to operate in the “ITU-T G.747” Mode.*

Bit 6 - Loop-back Activation - DS1 Channel 26

This “Read/Write” bit-field permits the user to configure DS1 Channel 26 into Remote Loop-back Mode. When this loop-back is configured, then the “RxDS1Data_26” signal will internally be “looped-back” into the “TxDS1Data_26” path. Further, the “RxDS1Clock_26” clock signal will also be internally looped back into the “RxDS1Clock_26” signal path.

Setting this bit-field to “1” enables this loop-back mode. Conversely, setting this bit-field to “0” disables this loop-back mode.

Bit 5 - Loop-back Activation - DS1 Channel 25

This “Read/Write” bit-field permits the user to configure DS1 Channel 25 into Remote Loop-back Mode. When this loop-back is configured, then the “RxDS1Data_25” signal will internally be “looped-back” into the “TxDS1Data_25” path. Further, the “RxDS1Clock_25” clock signal will also be internally looped back into the “RxDS1Clock_25” signal path.

Setting this bit-field to “1” enables this loop-back mode. Conversely, setting this bit-field to “0” disables this loop-back mode.

Bit 4 - Loop-back Activation - DS1 Channel 24

This “Read/Write” bit-field permits the user to configure DS1 Channel 24 into Remote Loop-back Mode. When this loop-back is configured, then the “RxDS1Data_24” signal will internally be “looped-back” into the “TxDS1Data_24” path. Further, the “RxDS1Clock_24” clock signal will also be internally looped back into the “RxDS1Clock_24” signal path.

Setting this bit-field to “1” enables this loop-back mode. Conversely, setting this bit-field to “0” disables this loop-back mode.

Bit 3 - Loop-back Request - DS1 Channel 27

This “Read/Write” bit-field permits the user to configure the XRT72L13 to transmit a “DS1 Channel 27 - Loop-back Request” signal to the Remote Terminal Equipment. When the Remote Terminal Equipment receives this request, it is expected to respond by configuring its own DS1 Channel 27 signal into Loop-back Mode.

NOTE: *This bit-field is ignored if the XRT72L13 has been configured to operate in the “ITU-T G.747” Mode.*

Bit 2 - Loop-back Request - DS1 Channel 26

This “Read/Write” bit-field permits the user to configure the XRT72L13 to transmit a “DS1 Channel 26 - Loop-back Request” signal to the Remote Terminal Equipment. When the Remote Terminal Equipment receives this request, it is expected to respond by configuring its own DS1 Channel 26 signal into Loop-back Mode.

NOTE: *This bit-field is ignored if the XRT72L13 has been configured to operate in the “ITU-T G.747” Mode.*

Bit 1 - Loop-back Request - DS1 Channel 25

This “Read/Write” bit-field permits the user to configure the XRT72L13 to transmit a “DS1 Channel 25 - Loop-back Request” signal to the Remote Terminal Equipment. When the Remote Terminal Equipment receives this request, it is expected to respond by configuring its own DS1 Channel 25 signal into Loop-back Mode.

NOTE: *This bit-field is ignored if the XRT72L13 has been configured to operate in the “ITU-T G.747” Mode.*

Bit 0 - Loop-back Request - DS1 Channel 24

This “Read/Write” bit-field permits the user to configure the XRT72L13 to transmit a “DS1 Channel 24 - Loop-back Request” signal to the Remote Terminal Equipment. When the Remote Terminal Equipment receives this request, it is expected to respond by configuring its own DS1 Channel 24 signal into Loop-back Mode.

NOTE: *This bit-field is ignored if the XRT72L13 has been configured to operate in the “ITU-T G.747” Mode.*

2.3.2.45 Tx DS3 Configuration Register)

TX DS3 CONFIGURATION REGISTER (ADDRESS = 0X30)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Tx Yellow Alarm	Tx X Bits	Tx Idle	Tx AIS	Tx LOS	FERF on LOS	FERF on OOF	FERF on AIS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	1	1	1

Bit 7 - Tx Yellow Alarm

This "Read/Write" bit-field allows the local µP to command the Transmit DS3 Framer to transmit a "Yellow Alarm" (e.g., X bits are all "0") in the outgoing DS3 data stream.

Writing a "0" to this bit-field disables this feature (the default condition). In this condition, the X-bits in the out-bound DS3 frame, are internally generated (based upon receiver conditions).

Writing a "1" to this bit-field invokes this command. In this condition, the Transmit DS3 Framer will override the internally-generated X-bits and force all of the X-bits of each outbound DS3 frame to "0".

NOTE: *For more information in this feature, please see Section _.*

NOTE: *This bit-setting is ignored if Bits 3, 4 or 5 (within this register) are set to "1".*

Bit 6 - Tx X-Bit (Force X bits to "1")

This "Read/Write" bit-field allows the user to command the Transmit DS3 Framer to force all of the X-bits, in the outbound DS3 Frames, to "1".

Writing a "0" to this bit-field disables this feature (the default condition). In this case, the Transmit DS3 Framer will generate X-bits based upon the receive conditions.

Writing a "1" to this bit-field invokes this command. In this case, the Transmit DS3 Framer will overwrite the internally-generated X-bits and set them all to "1".

NOTE: *For more information on this feature, please see Section _.*

NOTE: *This bit-setting is ignored if Bits 3, 4, 5, or 7 (within this register) are set to "1".*

Bit 5 - Tx Idle (Pattern)

This "Read/Write" bit-field allows the user to command the Transmit DS3 Framer to transmit the "Idle Condition" pattern. If the user invokes this command, then the Transmit DS3 Framer will force the outbound DS3 Frames to have the following patterns.

- Valid M-bits, F-bits and P-bits
- The three CP-Bits (F-frame #3) are "0"
- The X-bits are set to "1"
- A repeating "1100..." pattern in written into the payload portion of the DS3 Frames.

Writing a "1" to this bit-field invokes this command. Writing a "0" allows the Transmit DS3 Framer to function normally (e.g., the Transmit DS3 Framer will transmit its payload and internally generated overhead bits).

NOTE: *For more information on this feature, please see Section _.*

NOTE: *This bit-setting is ignored if Bits 3 or 4 (within this register) are set to "1".*

Bit 4 - Tx AIS (Pattern)

This "Read/Write" bit-field allows the user to command the Transmit DS3 Framer to transmit an "AIS" pattern. If the user invokes this command, then the Transmit DS3 Framer will force the outbound DS3 frames to have the following patterns.

- Valid M-bits, F-bits, and P-bits
- All C-bits are set to '0'
- All X-bits are set to '1'
- A repeating '1010...' pattern is written into the payload of the DS3 Frames.

Writing a "1' to this bit-field invokes this command. Writing a "0" allows the Transmit DS3 Framer to function normally (e.g., the Transmit DS3 Framer will transmit its payload and internally generated overhead bits).

NOTE: *For more information on this feature, please see Section _.*

Bit 3 - Tx LOS (Loss of Signal)

This "Read/Write" bit-field allows the user to command the Transmit DS3 Framer to simulate an "LOS Condition". If the user invokes this command, then the Transmit DS3 Framer will stop sending "mark" pulses out on the line; and will transmit an all-zero pattern.

Writing a '0' to this bit-field disables (or shuts off) this feature, thereby allowing internally generated DS3 Frames to be generated and transmitted over the line.

Writing a '1' to this bit-field invokes this command, causing the Transmit DS3 Framing to generate an all '0' pattern.

NOTE: *For more information on this feature, please see Section _.*

Bit 2 - FERF on LOS

This "Read/Write" bit-field allows the user to configure the Transmit DS3 Framer to generate a "Yellow Alarm" if the Near-End Receive DS3 Framer detects a "LOS" (Loss of Signal) Condition.

Writing a "1" to this bit-field enables this feature. Writing a "0" to this bit-field disables this feature.

NOTE: *For more information on this feature, please see Section _.*

Bit 1 - FERF on OOF

This "Read/Write" bit-field allows the user to configure the Transmit DS3 Framer to generate a "Yellow Alarm" if the Near-End Receive DS3 Framer detects an "OOF (Out-of-Frame) Condition".

Writing a "1" to this bit-field enables this feature. Writing a "0" to this bit-field disables this feature.

NOTE: *For more information on this feature, please see Section _.*

Bit 0 - FERF on AIS

This "Read/Write" bit-field allows the user to configure the Transmit DS3 Framer to generate a "Yellow Alarm" if the Near-End Receive DS3 Framer detects an AIS (Alarm Indication Signal) Condition.

Writing a "1" to this bit-field enables this feature. Writing a "0" to this bit-field disables this feature.

NOTE: *For more information on this feature, please see Section _.*

2.3.2.46 TxDS3 FEAC Configuration and Status Register)

TRANSMIT DS3 CONFIGURATION & STATUS REGISTER (ADDRESS = 0X31)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			Tx FEAC Interrupt Enable	TxFEAC Interrupt Status	TxFEAC Enable	TxFEAC Go	TxFEAC Busy
RO	RO	RO	R/W	RUR	R/W	R/W	RO
0	0	0	0	0	0	0	0

Bit 4 - Tx FEAC Interrupt Enable

This “Read-Write” bit-field permits the user to enable or disable the “Transmit FEAC” Interrupt.

Setting this bit-field to “0” disables this interrupt.

Conversely, setting this bit-field to “1” enables this interrupt.

Bit 3 - TxFEAC Interrupt Status

This "Read-Only" bit-field indicates whether or not the "FEAC Message Transmission Complete" interrupt has occurred since the last read of this register. This interrupt will occur once the Transmit FEAC Processor has finished its 10th transmission of the 16 bit FEAC Message (6 bit FEAC Code word + 10 framing bits). The purpose of this interrupt is to let the local µP know that the Transmit FEAC Processor has completed its transmission of its latest FEAC Message and is now ready to transmit another FEAC Message.

If this bit-field is "0", then the "FEAC Message Transmission Complete" interrupt has NOT occurred since the last read of this register.

If this bit-field is "1", then the "FEAC Message Transmission Complete" interrupt has occurred since the last read of this register.

NOTE: *For more information on the Transmit FEAC Processor, please see Section _.*

Bit 2 - TxFEAC Enable

This "Read/Write" bit-field allows the user to enable or disable the Transmit FEAC Processor. The Transmit FEAC Processor will NOT function until it has been enabled.

Writing a "0" to this bit-field disables the Transmit FEAC Processor. Writing a "1" to this bit-field enables the Transmit FEAC Processor.

Bit 1 - TxFEAC Go

This bit-field allows the user to invoke the "Transmit FEAC Message" command. Once this command has been invoked, the Transmit FEAC Processor will do the following:

- Encapsulate the 6 bit FEAC code word, from the Tx DS3 FEAC Register (Address = 0x1D) into a 16 bit FEAC Message
- Serially transmit this 16-bit FEAC Message to the far-end receiver via the "outbound" DS3 datastream, 10 consecutive times.

NOTE: *For more information on the Transmit FEAC Processor, please see Section _.*

Bit 0 - TxFEAC Busy

This "Read-Only" bit-field allows the local µP to "poll" and determine if the Transmit FEAC Processor has completed its 10th transmission of the 16-bit FEAC Message. This bit-field will contain a "1", if the Transmit FEAC Processor is still transmitting the FEAC Message. This bit-field will toggle to "0", once the Transmit FEAC Processor has completed its 10th transmission of the FEAC Message.

NOTE: *For more information on the Transmit FEAC Processor, please see Section _.*

2.3.2.47 TxDS3 FEAC Register

)

TX DS3 FEAC REGISER (ADDRESS = 0X32)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	TxFEAC[5:0]						Not Used
RO	R/W	R/W	R/W	R/W	R/W	R/W	RO
0	1	1	1	1	1	1	0

This register contains a six (6) bit "read/write" field that allows the user to write in the six-bit FEAC code word, that he/she wishes to transmit to the "Far End Receive FEAC Processor", via the outgoing DS3 data stream. The Transmit FEAC Processor will encapsulate this six-bit code into a 16-bit FEAC message, and will proceed to transmit this message to the "Far End Receiver" via the FEAC bit-field within each out-going DS3 frame.

NOTE: *For more information on the operation of the Transmit FEAC Processor, please see Section _.*

2.3.2.48 TxDS3 LAPD Configuration Register)

TXDS3 LAPD CONFIGURATION REGISTER (ADDRESS = 0X33)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used				Auto Retransmit	Not Used	TxLAPD Msg Length	TxLAPD Enable
RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	1	0	0	0

Bit 3 - Auto Retransmit

This "Read/Write" bit-field allows the user to configure the LAPD Transmitter to either transmit the LAPD

Message frame only once; or repeatedly at one-second intervals.

Writing a "0" to this bit-field configures the LAPD Transmitter to transmit the LAPD Message frame once. Afterwards, the LAPD Transmitter will halt transmission, until it has commanded to transmit another LAPD Message frame.

Writing a "1" to this bit-field configures the LAPD Transmitter to transmit the LAPD Message frame repeatedly at one second intervals. In this configuration, the LAPD Transmitter will repeat its transmission of the LAPD Message frame until it has been disabled.

Bit 1 - TxLAPD Message Length Select

This "Read/Write" bit-field permits the user to select the length of the "outbound" LAPD Message frame.

Setting this bit-field to "0" configures the "outbound" LAPD Message frame to be 76 bytes in length. Setting this bit-field to "1" configures the "outbound" LAPD Message frame to be 82 bytes in length.

Bit 0 - TxLAPD Enable

This "Read/Write" bit-field allows the user to enable or disable the LAPD Transmitter. The LAPD Transmitter must be enabled before it can be commanded to transmit a LAPD Message frame (containing a PMDL message) via the outbound DS3 frames, to the "Far-End" Terminal.

Writing a "0" disables the LAPD Transmitter (default condition). Writing a "1" enables the LAPD Transmitter.

NOTE: *For information on the LAPD Transmitter, please see Section _.*

2.3.2.49 TxDS3 LAPD Status/Interrupt Register)

TXDS3 LAPD STATUS AND INTERRUPT REGISTER (ADDRESS = 0X34)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used				TxDL Start	TxDL Busy	TxLAPD Interrupt Enable	TxLAPD Interrupt Status
RO	RO	RO	RO	R/W	RO	R/W	RUR
0	0	0	0	0	0	0	0

Bit 3 - TxDL Start

This "Read/Write" bit-field allows the user to invoke the "Transmit LAPD Message" command. Once the user invokes this command, the LAPD Transmitter will do the following:

- Read in the PMDL Message from the "Transmit LAPD Message" Buffer.
- Encapsulate the PMDL Message into a complete LAPD Message frame by including the necessary header and trailer bytes (e.g., flag sequence bytes, SAPI, CR, EA values, etc.).
- Compute the frame check sequence word (16 bit value)
- Insert the Frame Check Sequence value into the 2 octet slot after the payload section of the Message.
- Proceed to transmit the LAPD Message Frame to the "far end" terminal via the outgoing DS3 frames.

Writing a "1" to this bit-field start the transmission of the LAPD Message Frame, via the LAPD Transmitter.

NOTE: *For more information on the LAPD Transmitter, please see Section _.*

Bit 2 - TxDL Busy

This "Read-Only" bit-field allows the local µP to "poll" and determine if the LAPD Transmitter has completed its transmission of the LAPD Message frame. This bit-field will contain a "1", if the LAPD Transmitter is still transmitting the LAPD Message frame to the "far-end" terminal. This bit-field will toggle to "0", once the LAPD Transmitter has completed its transmission of the LAPD Message frame.

NOTE: *For more information on the LAPD Transmitter, please see Section _.*

Bit 1 - TxLAPD Interrupt Enable

This "Read/Write" bit-field allows the user to enable or disable the "LAPD Message Frame Transmission Complete" interrupt.

Writing a "0" to this bit-field disables this interrupt. Writing a "1" to this bit-field enables this interrupt.

Bit 0 - TxLAPD Interrupt Status

This "Reset Upon Read" bit-field indicates whether or not the "LAPD Message frame Transmission Complete" interrupt has occurred since the last read of this register. The purpose of this interrupt is to let the local µP know that the LAPD Transmitter has completed its transmission of the LAPD Message frame (containing the latest PMDL message); and is now ready to transmit another LAPD Message frame.

A "0" in this bit-field indicates that the "LAPD Message frame Transmission Complete" interrupt has not

occurred since the read of this register. A "1" in this bit-field indicates that this interrupt has occurred since the last read of this register.

NOTE: For more information on the LAPD Transmitter, please see Section _.

2.3.2.50 TxDS3 M-Bit Mask Register)

TXDS3 M-BIT MASK REGISTER (ADDRESS = 0X35)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxFEBEDat[2:0]			FEBE Reg Enable	Tx Error P-Bit	MBit Mask[2]	MBit Mask[1]	MBit Mask[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit 7 - 5: TxFEBEDat[2:0]

These three (3) "read/write" bit-fields, along with Bit 4 of this register, allows the user to configure and transmit his/her choice for FEBE bits in each outgoing DS3 Frame. The user will write his/her value for the FEBE bits into these bit-fields. The Transmit DS3 Framer will insert these values into the FEBE bit-fields of each outgoing DS3 Frame, once the user has written a "1" to Bit 4 (FEBE Register Enable).

NOTE: For more information on this feature, please see Section _.

Bit 4 - FEBE Register Enable

This "Read/Write" bit-field allows the user to configure the Transmit DS3 Framer to insert the contents of TxFEBEDat[2:0] into the FEBE bit-fields each outgoing DS3 Frame.

Writing a "0" to this bit-field disables this feature (e.g., the Transmit DS3 Framer will transmit the internally generated FEBE bits). Writing a "1" to this bit-field enables this features (e.g., the internally generated FEBE bits are overwritten by the contents of the TxFEBEDat[2:0] bit-field).

NOTE: For more information on this feature, please see Section _.

Bit 3 - Transmit Erred P-Bit

This "Read/Write bit-field allows the user to insert errors into the P-bits of the outgoing DS3 frames (via the Transmit DS3 Framer block). If the user enables this feature, then the Transmit DS3 Framer will proceed to invert each and every P-bit, from its computed value, prior to transmission to the "Far-end" Terminal.

Writing a "0" to this bit-field (the default condition) disables this feature (e.g., the correct P-bits are sent). Writing a "1" to this bit-field enables this feature (e.g., the incorrect P-bits are sent).

NOTE: For more information on this feature, please see Section _.

Bit 2 - 0 M-Bit Mask[2:0]

These "Read/Write" bit-fields allow the user to insert errors in the M-bits for Test and Diagnostic purposes. The Transmit DS3 Framer automatically performs an XOR operation on the actual contents of the M-bit fields to these register bit-fields. Therefore, for every '1' that exists in these bit-fields, will result in a change of state of the corresponding M-bit, prior to being transmitted to the Far End Receive DS3 Framer.

If the user wishes to operate the Transmit DS3 Framer in the normal mode (e.g., when no errors are being injected into the M-bit fields of the outbound DS3 Frame), then he/she must ensure that these bit-fields are all '0'.

2.3.2.51 Tx DS3 F-Bit Mask1 Register)

TX DS3 F-BIT MASK REGISTER - 1 (ADDRESS = 0X36)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used				FBit Mask[27]	FBit Mask[26]	FBit Mask[25]	FBit Mask[24]
RO	RO	RO	RO	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bits 3 - 0 F-Bit Mask[27:24]

These "Read/Write" bit-fields allow the user to insert errors into the first four F-bits of a DS3 M-frame, for test and diagnostic purposes. The Transmit DS3 Framer block (within the chip) automatically performs an XOR operation on the actual contents of these F-bit fields to these register bit-fields. Therefore, for every "1" that exists in these bit-fields, this will result in a change of state for the corresponding F-bit, prior to

being transmitted to the Far-End Receive DS3 Framer.

If the user wishes to operate the Transmit DS3 Framer block in the normal mode (e.g., when no errors are being injected into these F-bit fields of the outbound DS3 frames), then he/she must ensure that all of these bit-fields are "0s".

2.3.2.52 TxDS3 F-Bit Mask2 Register)

TXDS3 F-BIT MASK REGISTER - 2 (ADDRESS = 0X37)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FBit Mask[23]	FBit Mask[22]	FBit Mask[21]	FBit Mask[20]	FBit Mask[19]	FBit Mask[18]	FBit Mask[17]	FBit Mask[16]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bits 7 - 0 F-Bit Mask[23:16]

These "Read/Write" bit-fields allow the user to insert errors into the fifth through twelfth F-bits of a DS3 M-frame, for test and diagnostic purposes. The Transmit DS3 Framer block automatically performs an XOR operation on the actual contents of these F-bit fields to these register bit-fields. Therefore, for every "1" that exists in these bit-fields, this will result in a change of state for the corresponding F-bit, prior to being transmitted to the Remote Receive DS3 Framer.If the user wishes to operate the Transmit DS3 Framer block in the normal mode (e.g., when no errors are being injected into these F-bit fields of the outbound DS3 frames), then he/she must ensure that all of these bit-fields are "0s".

2.3.2.53 TxDS3 F-Bit Mask3 Register)

TX DS3 F-BIT MASK REGISTER - 3 (ADDRESS = 0X38)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FBit Mask[15]	FBit Mask[14]	FBit Mask[13]	FBit Mask[12]	FBit Mask[11]	FBit Mask[10]	FBit Mask[9]	FBit Mask[8]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bits 7 - 0 F-Bit Mask[15:8]

These "Read/Write" bit-fields allow the user to insert errors into the thirteenth through twentieth F-bits of a DS3 M-frame, for test and diagnostic purposes. The Transmit DS3 Framer automatically performs an XOR operation on the actual contents of these F-bit fields to these register bit-fields. Therefore, for every "1" that exists in these bit-fields, this will result in a change of state for the corresponding F-bit, prior to being transmitted to the Far-End Receive DS3 Framer.

If the user wishes to operate the Transmit DS3 Framer in the normal mode (e.g., when no errors are being injected into these F-bit fields of the outbound DS3 frames), then he/she must ensure that all of these bit-fields are "0s".

2.3.2.54 TxDS3 F-Bit Mask4 Register)

TXDS3 F-BIT MASK REGISTER - 4 (ADDRESS = 0X39)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FBit Mask[7]	FBit Mask[6]	FBit Mask[5]	FBit Mask[4]	FBit Mask[3]	FBit Mask[2]	FBit Mask[1]	FBit Mask[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bits 7 - 0 F-Bit Mask[7:0]

These "Read/Write" bit-fields allow the user to insert errors into the last eight F-bits of a DS3 M-frame, for test and diagnostic purposes. The Transmit DS3 Framer automatically performs an XOR operation on the actual contents of these F-bit fields to these register bit-fields. Therefore, for every "1" that exists in these bit-fields, this will result in a change of state for the corresponding F-bit, prior to being transmitted to the Far-End Receive DS3 Framer.

If the user wishes to operate the Transmit DS3 Framer in the normal mode (e.g., when no errors are being injected into these F-bit fields of the outbound DS3

2.3.2.55 DS2 # 1 Framer Configuration Register)

DS2 # 1 FRAMER CONFIGURATION REGISTER (ADDRESS = 0X3A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	ONE AND ONLY	DS2 MSYNC Algo	DS2 FSYNC Algo	DS2 FOOF Algo	DS2 MOOF Algo	DS2 MOOF Disable	DS2 Reframe]
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit 6 - ONE AND ONLY

Bit 5 - DS2 MSYNC - Algo

This “Read/Write” bit-field permits the user to define the “M-Bit Sync Declaration” Criteria for Receive DS2 Framer - Channel 1.

Setting this bit-field to “0” configures the Receive DS2 Framer (for Channel 1) to declare “M-SYNC” if it receives 4 consecutive, correct M-bits.

Setting this bit-field to “1” configures the Receive DS2 Framer (for Channel 1) to declare “M-SYNC” if it receives 8 consecutive, correct M-bits.

Bit 4 - DS2 FSYNC - Algo

This “Read/Write” bit-field permits the user to define the “F-Bit Sync Declaration” Criteria for Receive DS2 Framer - Channel 1.

Setting this bit-field to “0” configures the Receive DS2 Framer (for Channel 1) to declare “F-SYNC” if it receives 8 consecutive, correct F-bits.

Setting this bit-field to “1” configures the Receive DS2 Framer (for Channel 1) to declare “F-SYNC” if it receives 16 consecutive, correct F-bits.

Bit 3 - DS2 FOOF - Algo

This “Read/Write” bit-field permits the user to define the “Receive DS2 Out-of-Frame Declaration” criteria, for DS2 Channel 1.

Setting this bit-field to “1” configures the Receive DS2 Framer (for Channel 1) to declare an “OOF” (Out-of-Frame) condition when 2 out of the last 5 received F-bits are errored.

Setting this bit-field to “0” configures the Receive DS2 Framer (for Channel 1) to declare an “OOF” (Out-of-Frame) condition when 2 out of the last 4 received F-bits are errored.

Bit 2 - DS2 MOOF Algo

This “Read/Write” bit-field permits the user to define the “Receive DS2 Out-of-Frame Declaration” criteria, for DS2 Channel 1.

Setting this bit-field to “1” configures the Receive DS2 Framer (for Channel 1) to declare an “OOF” (Out-of-Frame) condition when at least one M-bit error is detected within 3 out of the last 4 received DS2 frames.

Setting this bit-field to “0” configures the Receive DS2 Framer (for Channel 1) to declare an “OOF” (Out-of-Frame) condition when at least one M-bit error is detected within 2 out of the last 4 received DS2 frames.

NOTE: *This bit-field is ignored if Bit 1 (within this register is set to “1”.*

Bit 1 - DS2 MOOF Disable

This “Read/Write” bit-field permits the user to configure Receive DS2 Framer # 1 to evaluate M-bits as a part of the “Receive DS2 Out-of Frame Declaration” criteria.

Setting this bit-field to “0” configures Receive DS2 Framer # 1 to check for M-bit errors and declare an OOF condition, per the settings within the “DS2 MOOF Algo” bit-field (Bit 2, within this register).

Setting this bit-field to “1” configures Receive DS2 Framer # 1 to NOT check for M-bits errors, as a part of the “Receive DS2 Out-of Frame Declaration” criteria.

Bit 0 - DS2 Reframe

This “Read/Write” bit-field permits the user to force (via software) Receive DS2 Framer # 1 to execute a “Re-Frame” procedure.

A “0” to “1” transition, within this bit-field will cause Receive DS2 Framer # 1 to execute a “re-frame” operation.

2.3.2.56 DS2 # 2 Framer Configuration Register)

DS2 # 2 FRAMER CONFIGURATION REGISTER (ADDRESS = 0X3B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	ONE AND ONLY	DS2 MSYNC Algo	DS2 FSYNC Algo	DS2 FOOF Algo	DS2 MOOF Algo	DS2 MOOF Disable	DS2 Reframe]
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit 6 - ONE AND ONLY

Bit 5 - DS2 MSYNC - Algo

This “Read/Write” bit-field permits the user to define the “M-Bit Sync Declaration” Criteria for Receive DS2 Framer - Channel 2.

Setting this bit-field to “0” configures the Receive DS2 Framer (for Channel 2) to declare “M-SYNC” if it receives 4 consecutive, correct M-bits.

Setting this bit-field to “1” configures the Receive DS2 Framer (for Channel 2) to declare “M-SYNC” if it receives 8 consecutive, correct M-bits.

Bit 4 - DS2 FSYNC - Algo

This “Read/Write” bit-field permits the user to define the “F-Bit Sync Declaration” Criteria for Receive DS2 Framer - Channel 2.

Setting this bit-field to “0” configures the Receive DS2 Framer (for Channel 2) to declare “F-SYNC” if it receives 8 consecutive, correct F-bits.

Setting this bit-field to “1” configures the Receive DS2 Framer (for Channel 2) to declare “F-SYNC” if it receives 16 consecutive, correct F-bits.

Bit 3 - DS2 FOOF - Algo

This “Read/Write” bit-field permits the user to define the “Receive DS2 Out-of-Frame Declaration” criteria, for DS2 Channel 2.

Setting this bit-field to “1” configures the Receive DS2 Framer (for Channel 2) to declare an “OOF” (Out-of-Frame) condition when 2 out of the last 5 received F-bits are errored.

Setting this bit-field to “0” configures the Receive DS2 Framer (for Channel 2) to declare an “OOF” (Out-of-Frame) condition when 2 out of the last 4 received F-bits are errored.

Bit 2 - DS2 MOOF Algo

This “Read/Write” bit-field permits the user to define the “Receive DS2 Out-of-Frame Declaration” criteria, for DS2 Channel 2.

Setting this bit-field to “1” configures the Receive DS2 Framer (for Channel 2) to declare an “OOF” (Out-of-Frame) condition when at least one M-bit error is detected within 3 out of the last 4 received DS2 frames.

Setting this bit-field to “0” configures the Receive DS2 Framer (for Channel 2) to declare an “OOF” (Out-of-Frame) condition when at least one M-bit error is detected within 2 out of the last 4 received DS2 frames.

NOTE: *This bit-field is ignored if Bit 1 (within this register is set to “1”.*

Bit 1 - DS2 MOOF Disable

This “Read/Write” bit-field permits the user to configure Receive DS2 Framer # 2 to evaluate M-bits as a part of the “Receive DS2 Out-of Frame Declaration” criteria.

Setting this bit-field to “0” configures Receive DS2 Framer # 2 to check for M-bit errors and declare an OOF condition, per the settings within the “DS2 MOOF Algo” bit-field (Bit 2, within this register).

Setting this bit-field to “1” configures Receive DS2 Framer # 2 to NOT check for M-bits errors, as a part of the “Receive DS2 Out-of Frame Declaration” criteria.

Bit 0 - DS2 Reframe

This “Read/Write” bit-field permits the user to force (via software) Receive DS2 Framer # 2 to execute a “Re-Frame” procedure.

A “0” to “1” transition, within this bit-field will cause Receive DS2 Framer # 2 to execute a “re-frame” operation.

2.3.2.57 DS2 # 3 Framer Configuration Register)

DS2 # 3 FRAMER CONFIGURATION REGISTER (ADDRESS = 0X3C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	ONE AND ONLY	DS2 MSYNC Algo	DS2 FSYNC Algo	DS2 FOOF Algo	DS2 MOOF Algo	DS2 MOOF Disable	DS2 Reframe]
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit 6 - ONE AND ONLY

Bit 5 - DS2 MSYNC - Algo

This “Read/Write” bit-field permits the user to define the “M-Bit Sync Declaration” Criteria for Receive DS2 Framer - Channel 3.

Setting this bit-field to “0” configures the Receive DS2 Framer (for Channel 3) to declare “M-SYNC” if it receives 4 consecutive, correct M-bits.

Setting this bit-field to “1” configures the Receive DS2 Framer (for Channel 3) to declare “M-SYNC” if it receives 8 consecutive, correct M-bits.

Bit 4 - DS2 FSYNC - Algo

This “Read/Write” bit-field permits the user to define the “F-Bit Sync Declaration” Criteria for Receive DS2 Framer - Channel 3.

Setting this bit-field to “0” configures the Receive DS2 Framer (for Channel 3) to declare “F-SYNC” if it receives 8 consecutive, correct F-bits.

Setting this bit-field to “1” configures the Receive DS2 Framer (for Channel 3) to declare “F-SYNC” if it receives 16 consecutive, correct F-bits.

Bit 3 - DS2 FOOF - Algo

This “Read/Write” bit-field permits the user to define the “Receive DS2 Out-of-Frame Declaration” criteria, for DS2 Channel 3.

Setting this bit-field to “1” configures the Receive DS2 Framer (for Channel 3) to declare an “OOF” (Out-of-Frame) condition when 2 out of the last 5 received F-bits are errored.

Setting this bit-field to “0” configures the Receive DS2 Framer (for Channel 3) to declare an “OOF” (Out-of-Frame) condition when 2 out of the last 4 received F-bits are errored.

Bit 2 - DS2 MOOF Algo

This “Read/Write” bit-field permits the user to define the “Receive DS2 Out-of-Frame Declaration” criteria, for DS2 Channel 3.

Setting this bit-field to “1” configures the Receive DS2 Framer (for Channel 3) to declare an “OOF” (Out-of-Frame) condition when at least one M-bit error is detected within 3 out of the last 4 received DS2 frames.

Setting this bit-field to “0” configures the Receive DS2 Framer (for Channel 3) to declare an “OOF” (Out-of-Frame) condition when at least one M-bit error is detected within 2 out of the last 4 received DS2 frames.

NOTE: *This bit-field is ignored if Bit 1 (within this register is set to “1”.*

Bit 1 - DS2 MOOF Disable

This “Read/Write” bit-field permits the user to configure Receive DS2 Framer # 3 to evaluate M-bits as a part of the “Receive DS2 Out-of Frame Declaration” criteria.

Setting this bit-field to “0” configures Receive DS2 Framer # 3 to check for M-bit errors and declare an OOF condition, per the settings within the “DS2 MOOF Algo” bit-field (Bit 2, within this register).

Setting this bit-field to “1” configures Receive DS2 Framer # 3 to NOT check for M-bits errors, as a part of the “Receive DS2 Out-of Frame Declaration” criteria.

Bit 0 - DS2 Reframe

This “Read/Write” bit-field permits the user to force (via software) Receive DS2 Framer # 3 to execute a “Re-Frame” procedure.

A “0” to “1” transition, within this bit-field will cause Receive DS2 Framer # 3 to execute a “re-frame” operation.

2.3.2.58 DS2 # 4 Framer Configuration Register)

DS2 # 4 FRAMER CONFIGURATION REGISTER (ADDRESS = 0X3D)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	ONE AND ONLY	DS2 MSYNC Algo	DS2 FSYNC Algo	DS2 FOOF Algo	DS2 MOOF Algo	DS2 MOOF Disable	DS2 Reframe]
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit 6 - ONE AND ONLY

Bit 5 - DS2 MSYNC - Algo

This “Read/Write” bit-field permits the user to define the “M-Bit Sync Declaration” Criteria for Receive DS2 Framer - Channel 4.

Setting this bit-field to “0” configures the Receive DS2 Framer (for Channel 4) to declare “M-SYNC” if it receives 4 consecutive, correct M-bits.

Setting this bit-field to “1” configures the Receive DS2 Framer (for Channel 4) to declare “M-SYNC” if it receives 8 consecutive, correct M-bits.

Bit 4 - DS2 FSYNC - Algo

This “Read/Write” bit-field permits the user to define the “F-Bit Sync Declaration” Criteria for Receive DS2 Framer - Channel 4.

Setting this bit-field to “0” configures the Receive DS2 Framer (for Channel 4) to declare “F-SYNC” if it receives 8 consecutive, correct F-bits.

Setting this bit-field to “1” configures the Receive DS2 Framer (for Channel 4) to declare “F-SYNC” if it receives 16 consecutive, correct F-bits.

Bit 3 - DS2 FOOF - Algo

This “Read/Write” bit-field permits the user to define the “Receive DS2 Out-of-Frame Declaration” criteria, for DS2 Channel 4.

Setting this bit-field to “1” configures the Receive DS2 Framer (for Channel 4) to declare an “OOF” (Out-of-Frame) condition when 2 out of the last 5 received F-bits are errored.

Setting this bit-field to “0” configures the Receive DS2 Framer (for Channel 4) to declare an “OOF” (Out-of-Frame) condition when 2 out of the last 4 received F-bits are errored.

Bit 2 - DS2 MOOF Algo

This “Read/Write” bit-field permits the user to define the “Receive DS2 Out-of-Frame Declaration” criteria, for DS2 Channel 4.

Setting this bit-field to “1” configures the Receive DS2 Framer (for Channel 4) to declare an “OOF” (Out-of-Frame) condition when at least one M-bit error is detected within 3 out of the last 4 received DS2 frames.

Setting this bit-field to “0” configures the Receive DS2 Framer (for Channel 4) to declare an “OOF” (Out-of-Frame) condition when at least one M-bit error is detected within 2 out of the last 4 received DS2 frames.

NOTE: *This bit-field is ignored if Bit 1 (within this register is set to “1”.*

Bit 1 - DS2 MOOF Disable

This “Read/Write” bit-field permits the user to configure Receive DS2 Framer # 4 to evaluate M-bits as a part of the “Receive DS2 Out-of Frame Declaration” criteria.

Setting this bit-field to “0” configures Receive DS2 Framer # 4 to check for M-bit errors and declare an OOF condition, per the settings within the “DS2 MOOF Algo” bit-field (Bit 2, within this register).

Setting this bit-field to “1” configures Receive DS2 Framer # 4 to NOT check for M-bits errors, as a part of the “Receive DS2 Out-of Frame Declaration” criteria.

Bit 0 - DS2 Reframe

This “Read/Write” bit-field permits the user to force (via software) Receive DS2 Framer # 4 to execute a “Re-Frame” procedure.

A “0” to “1” transition, within this bit-field will cause Receive DS2 Framer # 4 to execute a “re-frame” operation.

2.3.2.59 DS2 # 5 Framer Configuration Register)

DS2 # 5 FRAMER CONFIGURATION REGISTER (ADDRESS = 0X3E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	ONE AND ONLY	DS2 MSYNC Algo	DS2 FSYNC Algo	DS2 FOOF Algo	DS2 MOOF Algo	DS2 MOOF Disable	DS2 Reframe]
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit 6 - ONE AND ONLY

Bit 5 - DS2 MSYNC - Algo

This “Read/Write” bit-field permits the user to define the “M-Bit Sync Declaration” Criteria for Receive DS2 Framer - Channel 5.

Setting this bit-field to “0” configures the Receive DS2 Framer (for Channel 5) to declare “M-SYNC” if it receives 4 consecutive, correct M-bits.

Setting this bit-field to “1” configures the Receive DS2 Framer (for Channel 5) to declare “M-SYNC” if it receives 8 consecutive, correct M-bits.

Bit 4 - DS2 FSYNC - Algo

This “Read/Write” bit-field permits the user to define the “F-Bit Sync Declaration” Criteria for Receive DS2 Framer - Channel 5.

Setting this bit-field to “0” configures the Receive DS2 Framer (for Channel 5) to declare “F-SYNC” if it receives 8 consecutive, correct F-bits.

Setting this bit-field to “1” configures the Receive DS2 Framer (for Channel 5) to declare “F-SYNC” if it receives 16 consecutive, correct F-bits.

Bit 3 - DS2 FOOF - Algo

This “Read/Write” bit-field permits the user to define the “Receive DS2 Out-of-Frame Declaration” criteria, for DS2 Channel 5.

Setting this bit-field to “1” configures the Receive DS2 Framer (for Channel 5) to declare an “OOF” (Out-of-Frame) condition when 2 out of the last 5 received F-bits are errored.

Setting this bit-field to “0” configures the Receive DS2 Framer (for Channel 5) to declare an “OOF” (Out-of-Frame) condition when 2 out of the last 4 received F-bits are errored.

Bit 2 - DS2 MOOF Algo

This “Read/Write” bit-field permits the user to define the “Receive DS2 Out-of-Frame Declaration” criteria, for DS2 Channel 5.

Setting this bit-field to “1” configures the Receive DS2 Framer (for Channel 5) to declare an “OOF” (Out-of-Frame) condition when at least one M-bit error is detected within 3 out of the last 4 received DS2 frames.

Setting this bit-field to “0” configures the Receive DS2 Framer (for Channel 5) to declare an “OOF” (Out-of-Frame) condition when at least one M-bit error is detected within 2 out of the last 4 received DS2 frames.

NOTE: *This bit-field is ignored if Bit 1 (within this register is set to “1”.*

Bit 1 - DS2 MOOF Disable

This “Read/Write” bit-field permits the user to configure Receive DS2 Framer # 5 to evaluate M-bits as a part of the “Receive DS2 Out-of Frame Declaration” criteria.

Setting this bit-field to “0” configures Receive DS2 Framer # 5 to check for M-bit errors and declare an OOF condition, per the settings within the “DS2 MOOF Algo” bit-field (Bit 2, within this register).

Setting this bit-field to “1” configures Receive DS2 Framer # 5 to NOT check for M-bits errors, as a part of the “Receive DS2 Out-of Frame Declaration” criteria.

Bit 0 - DS2 Reframe

This “Read/Write” bit-field permits the user to force (via software) Receive DS2 Framer # 5 to execute a “Re-Frame” procedure.

A “0” to “1” transition, within this bit-field will cause Receive DS2 Framer # 5 to execute a “re-frame” operation.

2.3.2.60 DS2 # 6 Framer Configuration Register)

DS2 # 6 FRAMER CONFIGURATION REGISTER (ADDRESS = 0X3F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	ONE AND ONLY	DS2 MSYNC Algo	DS2 FSYNC Algo	DS2 FOOF Algo	DS2 MOOF Algo	DS2 MOOF Disable	DS2 Reframe]
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit 6 - ONE AND ONLY

Bit 5 - DS2 MSYNC - Algo

This “Read/Write” bit-field permits the user to define the “M-Bit Sync Declaration” Criteria for Receive DS2 Framer - Channel 6.

Setting this bit-field to “0” configures the Receive DS2 Framer (for Channel 6) to declare “M-SYNC” if it receives 4 consecutive, correct M-bits.

Setting this bit-field to “1” configures the Receive DS2 Framer (for Channel 6) to declare “M-SYNC” if it receives 8 consecutive, correct M-bits.

Bit 4 - DS2 FSYNC - Algo

This “Read/Write” bit-field permits the user to define the “F-Bit Sync Declaration” Criteria for Receive DS2 Framer - Channel 6.

Setting this bit-field to “0” configures the Receive DS2 Framer (for Channel 6) to declare “F-SYNC” if it receives 8 consecutive, correct F-bits.

Setting this bit-field to “1” configures the Receive DS2 Framer (for Channel 6) to declare “F-SYNC” if it receives 16 consecutive, correct F-bits.

Bit 3 - DS2 FOOF - Algo

This “Read/Write” bit-field permits the user to define the “Receive DS2 Out-of-Frame Declaration” criteria, for DS2 Channel 6.

Setting this bit-field to “1” configures the Receive DS2 Framer (for Channel 6) to declare an “OOF” (Out-of-Frame) condition when 2 out of the last 5 received F-bits are errored.

Setting this bit-field to “0” configures the Receive DS2 Framer (for Channel 6) to declare an “OOF” (Out-of-Frame) condition when 2 out of the last 4 received F-bits are errored.

Bit 2 - DS2 MOOF Algo

This “Read/Write” bit-field permits the user to define the “Receive DS2 Out-of-Frame Declaration” criteria, for DS2 Channel 6.

Setting this bit-field to “1” configures the Receive DS2 Framer (for Channel 6) to declare an “OOF” (Out-of-Frame) condition when at least one M-bit error is detected within 3 out of the last 4 received DS2 frames.

Setting this bit-field to “0” configures the Receive DS2 Framer (for Channel 6) to declare an “OOF” (Out-of-Frame) condition when at least one M-bit error is detected within 2 out of the last 4 received DS2 frames.

NOTE: *This bit-field is ignored if Bit 1 (within this register is set to “1”.*

Bit 1 - DS2 MOOF Disable

This “Read/Write” bit-field permits the user to configure Receive DS2 Framer # 6 to evaluate M-bits as a part of the “Receive DS2 Out-of Frame Declaration” criteria.

Setting this bit-field to “0” configures Receive DS2 Framer # 6 to check for M-bit errors and declare an OOF condition, per the settings within the “DS2 MOOF Algo” bit-field (Bit 2, within this register).

Setting this bit-field to “1” configures Receive DS2 Framer # 6 to NOT check for M-bits errors, as a part of the “Receive DS2 Out-of Frame Declaration” criteria.

Bit 0 - DS2 Reframe

This “Read/Write” bit-field permits the user to force (via software) Receive DS2 Framer # 6 to execute a “Re-Frame” procedure.

A “0” to “1” transition, within this bit-field will cause Receive DS2 Framer # 6 to execute a “re-frame” operation.

2.3.2.61 DS2 # 7 Framer Configuration Register)

DS2 # 7 FRAMER CONFIGURATION REGISTER (ADDRESS = 0X40)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	ONE AND ONLY	DS2 MSYNC Algo	DS2 FSYNC Algo	DS2 FOOF Algo	DS2 MOOF Algo	DS2 MOOF Disable	DS2 Reframe]
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit 6 - ONE AND ONLY

Bit 5 - DS2 MSYNC - Algo

This “Read/Write” bit-field permits the user to define the “M-Bit Sync Declaration” Criteria for Receive DS2 Framer - Channel 7.

Setting this bit-field to “0” configures the Receive DS2 Framer (for Channel 7) to declare “M-SYNC” if it receives 4 consecutive, correct M-bits.

Setting this bit-field to “1” configures the Receive DS2 Framer (for Channel 7) to declare “M-SYNC” if it receives 8 consecutive, correct M-bits.

Bit 4 - DS2 FSYNC - Algo

This “Read/Write” bit-field permits the user to define the “F-Bit Sync Declaration” Criteria for Receive DS2 Framer - Channel 7.

Setting this bit-field to “0” configures the Receive DS2 Framer (for Channel 7) to declare “F-SYNC” if it receives 8 consecutive, correct F-bits.

Setting this bit-field to “1” configures the Receive DS2 Framer (for Channel 7) to declare “F-SYNC” if it receives 16 consecutive, correct F-bits.

Bit 3 - DS2 FOOF - Algo

This “Read/Write” bit-field permits the user to define the “Receive DS2 Out-of-Frame Declaration” criteria, for DS2 Channel 7.

Setting this bit-field to “1” configures the Receive DS2 Framer (for Channel 7) to declare an “OOF” (Out-of-Frame) condition when 2 out of the last 5 received F-bits are errored.

Setting this bit-field to “0” configures the Receive DS2 Framer (for Channel 7) to declare an “OOF” (Out-of-Frame) condition when 2 out of the last 4 received F-bits are errored.

Bit 2 - DS2 MOOF Algo

This “Read/Write” bit-field permits the user to define the “Receive DS2 Out-of-Frame Declaration” criteria, for DS2 Channel 7.

Setting this bit-field to “1” configures the Receive DS2 Framer (for Channel 7) to declare an “OOF” (Out-of-Frame) condition when at least one M-bit error is detected within 3 out of the last 4 received DS2 frames.

Setting this bit-field to “0” configures the Receive DS2 Framer (for Channel 7) to declare an “OOF” (Out-of-Frame) condition when at least one M-bit error is detected within 2 out of the last 4 received DS2 frames.

NOTE: *This bit-field is ignored if Bit 1 (within this register is set to “1”.*

Bit 1 - DS2 MOOF Disable

This “Read/Write” bit-field permits the user to configure Receive DS2 Framer # 7 to evaluate M-bits as a part of the “Receive DS2 Out-of Frame Declaration” criteria.

Setting this bit-field to “0” configures Receive DS2 Framer # 7 to check for M-bit errors and declare an OOF condition, per the settings within the “DS2 MOOF Algo” bit-field (Bit 2, within this register).

Setting this bit-field to “1” configures Receive DS2 Framer # 7 to NOT check for M-bits errors, as a part of the “Receive DS2 Out-of Frame Declaration” criteria.

Bit 0 - DS2 Reframe

This “Read/Write” bit-field permits the user to force (via software) Receive DS2 Framer # 7 to execute a “Re-Frame” procedure.

A “0” to “1” transition, within this bit-field will cause Receive DS2 Framer # 7 to execute a “re-frame” operation.

2.3.2.62 PMON LCV Event Count Register - MSB

PMON LCV EVENT COUNT REGISTER - MSB (ADDRESS = 0X50)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LCV Count - High Byte							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

This "Reset-upon-Read" register, along with the "PMON LCV Event Count Register - LSB" (Address = 0x51) contains a 16-bit representation of the number of "Line Code Violations" that have been detected by the Receive DS3 Framer block (within the chip), since the last read of these registers. This register contains the MSB (or Upper-Byte) value of this 16 bit expression.

2.3.2.63 PMON LCV Event Count Register - LSB

PMON LCV EVENT COUNT REGISTER - LSB (ADDRESS = 0X51)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LCV Count - Low Byte							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

This "Reset-upon-Read" register, along with the "PMON LCV Event Count Register - LSB" (Address = 0x50) contains a 16-bit representation of the number of "Line Code Violations" that have been detected by the Receive DS3 Framer block (within the chip), since the last read of these registers. This register contains the LSB (or Lower-Byte) value of this 16 bit expression.

2.3.2.64 PMON Framing Bit Error Event Count Register - MSB

PMON FRAMING BIT ERROR COUNT REGISTER - MSB (ADDRESS = 0X52)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Framing Bit Error Count - High Byte							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

This "Reset-upon-Read" register, along with the "PMON Framing Bit Error Count Register - LSB" (Address = 0x53) contains a 16-bit representation of the number of "Framing Bit Errors" that have been detected by the Receive DS3 Framer block (within the chip), since the last read of these registers. This register contains the MSB (or Upper-Byte) value of this 16 bit expression.

2.3.2.65 PMON Framing Bit Error Event Count Register - LSB

PMON FRAMING BIT ERROR COUNT REGISTER - LSB (ADDRESS = 0X53)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Framing Bit Error Count - Low Byte							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

This "Reset-upon-Read" register, along with the "PMON Framing Bit Error Count Register - MSB" (Address = 0x52) contains a 16-bit representation of the number of "Framing Bit Errors" that have been detect-

ed by the Receive DS3 Framer block (within the chip), since the last read of these registers. This register contains the LSB (or Lower-Byte) value of this 16 bit expression.

2.3.2.66 PMON P-Bit Error Event Count Register - MSB

PMON P-BIT ERROR COUNT REGISTER - MSB (ADDRESS = 0X54)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P-Bit Error Count - High Byte							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

This "Reset-upon-Read" register, along with the "PMON P-Bit Error Count Register - LSB" (Address = 0x55) contains a 16-bit representation of the number of "P-bit Errors that have been detected by the Receive DS3 Framer block (within the chip), since the last read of these registers. This register contains the MSB (or Upper-Byte) value of this 16 bit expression.

2.3.2.67 PMON P-Bit Error Event Count Register - LSB

PMON P-BIT ERROR COUNT REGISTER - LSB (ADDRESS = 0X55)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P-Bit Error Count - Low Byte							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

This "Reset-upon-Read" register, along with the "PMON P-Bit Error Count Register - MSB" (Address = 0x54) contains a 16-bit representation of the number of "P-bit Errors that have been detected by the Receive DS3 Framer block (within the chip), since the last read of these registers. This register contains the LSB (or Lower-Byte) value of this 16 bit expression.

2.3.2.68 PMON FEBE Event Count Register - MSB

PMON FEBE EVENT COUNT REGISTER - MSB (ADDRESS = 0X56)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FEBE Event Count - High Byte							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

This "Reset-upon-Read" register, along with the "PMON FEBE Event Count Register - LSB" (Address = 0x57) contains a 16-bit representation of the number of "FEBE Events that have been detected by the Receive DS3 Framer block (within the chip), since the last read of these registers. This register contains the MSB (or Upper-Byte) value of this 16 bit expression.

2.3.2.69 PMON FEBE Event Count Register - LSB

PMON FEBE EVENT COUNT REGISTER - LSB (ADDRESS = 0X57)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FEBE Event Count - Low Byte							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

This "Reset-upon-Read" register, along with the "PMON FEBE Event Count Register - MSB" (Address = 0x56) contains a 16-bit representation of the number of "FEBE Events that have been detected by the Receive DS3 Framer block (within the chip), since the

last read of these registers. This register contains the LSB (or Lower-Byte) value of this 16 bit expression.

2.3.2.70 PMON CP-Bit Error Event Count Register - MSB

PMON CP-BIT ERROR COUNT REGISTER - MSB (ADDRESS = 0X58)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CP-Bit Error Count - High Byte							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

This "Reset-upon-Read" register, along with the "PMON CP-Bit Error Count Register - LSB" (Address = 0x59) contains a 16-bit representation of the number of "CP-bit Errors that have been detected by the Receive DS3 Framer block (within the chip), since the last read of these registers. This register contains the MSB (or Upper-Byte) value of this 16 bit expression.

2.3.2.71 PMON CP-Bit Error Event Count Register - LSB

PMON CP-BIT ERROR COUNT REGISTER - LSB (ADDRESS = 0X59)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CP-Bit Error Count - Low Byte							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

This "Reset-upon-Read" register, along with the "PMON CP-Bit Error Count Register - MSB" (Address = 0x58) contains a 16-bit representation of the number of "CP-bit Errors that have been detected by the Receive DS3 Framer block (within the chip), since the last read of these registers. This register contains the MSB (or Upper-Byte) value of this 16 bit expression.

2.3.2.72 PMON DS2 # 1 Framing Bit Error Count Register

PMON DS2 # 1 FRAMING BIT ERROR COUNT REGISTER (ADDRESS = 0X5A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DS2 # 1 Framing-Bit Error Count							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

This “Reset-upon Read” register contains an 8-bit representation of the number of “F” or “M-” bit errors that have been detected by Receive DS2 Framer # 1 (within the chip), since the last read of this register.

2.3.2.73 PMON DS2 # 2 Framing Bit Error Count Register

PMON DS2 # 2 FRAMING BIT ERROR COUNT REGISTER (ADDRESS = 0X5B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DS2 # 2 Framing-Bit Error Count							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

This “Reset-upon Read” register contains an 8-bit representation of the number of “F” or “M-” bit errors that have been detected by Receive DS2 Framer # 2 (within the chip), since the last read of this register.

2.3.2.74 PMON DS2 # 3 Framing Bit Error Count Register

PMON DS2 # 3 FRAMING BIT ERROR COUNT REGISTER (ADDRESS = 0X5C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DS2 # 3 Framing-Bit Error Count							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

This “Reset-upon Read” register contains an 8-bit representation of the number of “F” or “M-” bit errors that have been detected by Receive DS2 Framer # 3 (within the chip), since the last read of this register.

2.3.2.75 PMON DS2 # 4 Framing Bit Error Count Register

PMON DS2 # 4 FRAMING BIT ERROR COUNT REGISTER (ADDRESS = 0X5D)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DS2 # 4 Framing-Bit Error Count							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

This “Reset-upon Read” register contains an 8-bit representation of the number of “F” or “M-” bit errors that have been detected by Receive DS2 Framer # 4 (within the chip), since the last read of this register.

2.3.2.76 PMON DS2 # 5 Framing Bit Error Count Register

PMON DS2 # 5 FRAMING BIT ERROR COUNT REGISTER (ADDRESS = 0X5E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DS2 # 5 Framing-Bit Error Count							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

This “Reset-upon Read” register contains an 8-bit representation of the number of “F” or “M-” bit errors that have been detected by Receive DS2 Framer # 5 (within the chip), since the last read of this register.

2.3.2.77 PMON DS2 # 6 Framing Bit Error Count Register

PMON DS2 # 6 FRAMING BIT ERROR COUNT REGISTER (ADDRESS = 0X5F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DS2 # 6 Framing-Bit Error Count							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

This “Reset-upon Read” register contains an 8-bit representation of the number of “F” or “M-” bit errors that have been detected by Receive DS2 Framer # 6 (within the chip), since the last read of this register.

2.3.2.78 PMON DS2 # 7 Framing Bit Error Counter

PMON DS2 # 7 FRAMING BIT ERROR COUNT REGISTER (ADDRESS = 0X60)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DS2 # 7 Framing-Bit Error Count							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

This “Reset-upon Read” register contains an 8-bit representation of the number of “F” or “M-” bit errors that have been detected by Receive DS2 Framer # 7 (within the chip), since the last read of this register.

2.3.2.79 PMON ITU-T G.747 # 1 Parity Bit Error Count Register

PMON ITU-T G.747 # 1 P- BIT ERROR COUNT REGISTER (ADDRESS = 0X61)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ITU-T G.747 # 1 P-Bit Error Count							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

This “Reset-upon-Read” register contains an 8-bit representation of the number of “P” bit errors that have been detected by Receive G.747 Framer # 1 (within the chip) since the last read of this register.

NOTE: *This register is only applicable if the XRT72L13 has been configured to operate in the ITU-T G.747 Mode.*

2.3.2.80 PMON ITU-T G.747 # 2 Parity Bit Error Count Register

PMON ITU-T G.747 # 2 P- BIT ERROR COUNT REGISTER (ADDRESS = 0X62)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ITU-T G.747 # 2 P-Bit Error Count							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

This “Reset-upon-Read” register contains an 8-bit representation of the number of “P” bit errors that have been detected by Receive G.747 Framer # 2 (within the chip) since the last read of this register.

NOTE: *This register is only applicable if the XRT72L13 has been configured to operate in the ITU-T G.747 Mode.*

2.3.2.81 PMON ITU-T G.747 # 3 Parity Bit Error Count Register

PMON ITU-T G.747 # 3 P- BIT ERROR COUNT REGISTER (ADDRESS = 0X63)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ITU-T G.747 # 3 P-Bit Error Count							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

This “Reset-upon-Read” register contains an 8-bit representation of the number of “P” bit errors that have been detected by Receive G.747 Framer # 3 (within the chip) since the last read of this register.

NOTE: *This register is only applicable if the XRT72L13 has been configured to operate in the ITU-T G.747 Mode.*

2.3.2.82 PMON ITU-T G.747 # 4 Parity Bit Error Count Register

PMON ITU-T G.747 # 4 P- BIT ERROR COUNT REGISTER (ADDRESS = 0X64)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ITU-T G.747 # 4 P-Bit Error Count							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

This "Reset-upon-Read" register contains an 8-bit representation of the number of "P" bit errors that have been detected by Receive G.747 Framer # 4 (within the chip) since the last read of this register.

NOTE: *This register is only applicable if the XRT72L13 has been configured to operate in the ITU-T G.747 Mode.*

2.3.2.83 PMON ITU-T G.747 # 5 Parity Bit Error Count Register

PMON ITU-T G.747 # 5 P- BIT ERROR COUNT REGISTER (ADDRESS = 0X65)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ITU-T G.747 # 5 P-Bit Error Count							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

This "Reset-upon-Read" register contains an 8-bit representation of the number of "P" bit errors that have been detected by Receive G.747 Framer # 5 (within the chip) since the last read of this register.

NOTE: *This register is only applicable if the XRT72L13 has been configured to operate in the ITU-T G.747 Mode.*

2.3.2.84 PMON ITU-T G.747 # 6 Parity Bit Error Count Register

PMON ITU-T G.747 # 6 P- BIT ERROR COUNT REGISTER (ADDRESS = 0X66)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ITU-T G.747 # 6 P-Bit Error Count							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

This "Reset-upon-Read" register contains an 8-bit representation of the number of "P" bit errors that have been detected by Receive G.747 Framer # 6 (within the chip) since the last read of this register.

NOTE: *This register is only applicable if the XRT72L13 has been configured to operate in the ITU-T G.747 Mode.*

2.3.2.85 PMON ITU-T G.747 # 7 Parity Bit Error Count Register

PMON ITU-T G.747 # 7 P- BIT ERROR COUNT REGISTER (ADDRESS = 0X67)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ITU-T G.747 # 7 P-Bit Error Count							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

This "Reset-upon-Read" register contains an 8-bit representation of the number of "P" bit errors that have been detected by Receive G.747 Framer # 7 (within the chip) since the last read of this register.

NOTE: *This register is only applicable if the XRT72L13 has been configured to operate in the ITU-T G.747 Mode.*

2.3.2.86 PMON Holding Register

PMON HOLDING REGISTER (ADDRESS = 0X6C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON Holding Value							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

Each of the PMON registers are 16 bit "Reset-upon-Read" registers. More specifically, whenever the Microprocessor intends to read a PMON register, there are two things to bear in mind.

1. This Microprocessor is going to require two read accesses in order read out the full 16-bit expression of these PMON registers.
2. The entire 16-bit expression (of a given PMON register) is going to be reset, immediately after the Microprocessor has completed its first read access to the PMON register.

Hence, the contents of the other byte (of the partially read PMON register) will reside within the PMON Holding register.

2.3.2.87 One Second Error Status Register

ONE SECOND ERROR STATUS REGISTER (ADDRESS = 0X6D)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
						Errored Second	Severely Errored Second
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

Bit 1 - Errored Second

This “Read-Only” bit-field indicates whether or not there was at least one error within the last one second accumulation period.

If no error has occurred (within the last one second accumulation period) then this bit-field will be set to “0”. Conversely, if at least one error has occurred (within the last one second accumulation period) then this bit-field will be set to “1”.

Bit 0 - Severely Errored Second

This “Read-Only” bit-field indicates whether or not the error-rate, in the last one second interval was greater than 1e-3.

If the bit error rate (within the last one second accumulation period) is less than 1e-3, then this bit-field will be set to “0”. Conversely, if the bit-error rate (within the last one second accumulation period) is greater than 1e-3, then this bit-field will be set to “1”.

2.3.2.88 LCV One Second Accumulator Register - MSB

LCV - ONE SECOND ACCUMULATOR REGISTER - MSB (ADDRESS = 0X6E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LCV - One Second Count - High Byte							
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

This "Read-Only" register, along with the "LCV - One Second Accumulator Register - LSB" (Address = 0x6F) contains a 16-bit representation of the number of "LCV (Line Code Violation) Events that have been detected by the Receive DS3 Framer block, within the last one-second sampling period. This register contains the MSB (or Upper-Byte) value of this 16 bit expression.

2.3.2.89 LCV One Second Accumulator Register - LSB

LCV - ONE SECOND ACCUMULATOR REGISTER - LSB (ADDRESS = 0X6F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LCV - One Second Count - Low Byte							
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

This "Read-Only" register, along with the "LCV - One Second Accumulator Register - MSB" (Address = 0x6E) contains a 16-bit representation of the number of "LCV (Line Code Violation) Events that have been detected by the Receive DS3 Framer block, within the last one second sampling period. This register contains the LSB (or Lower-Byte) value of this 16 bit expression.

2.3.2.90 P-Bit Error One Second Accumulator Register - MSB

P-BIT ERRORS - ONE SECOND ACCUMULATOR REGISTER - MSB (ADDRESS = 0X70)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Frame Parity Error Count - High Byte							
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

This "Read-Only" register, along with the "Frame Parity Errors - One Second Accumulator Register - LSB" (Address = 0x71) contains a 16-bit representation of the number of "P-bit" Errors that have been detected by the Receive DS3 Framer block, within the last one second sampling period. This register contains the MSB (or Upper-Byte) value of this 16 bit expression.

2.3.2.91 P-Bit Error One Second Accumulator Register - LSB

P-BIT ERRORS - ONE SECOND ACCUMULATOR REGISTER - LSB (ADDRESS = 0X71)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Frame Parity Error Count - Low Byte							
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

This "Read-Only" register, along with the "Frame Parity Errors - One Second Accumulator Register - MSB" (Address = 0x70) contains a 16-bit representation of the number of "P-bit" Errors that have been detected by the Receive DS3 Framer block, within the last one-second sampling period. This register contains the LSB (or Lower-Byte) value of this 16 bit expression.

2.3.2.92 CP-Bit Error One Second Accumulator Register - MSB

CP-BIT ERRORS - ONE SECOND ACCUMULATOR REGISTER - MSB (ADDRESS = 0X72)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CP Bit Error Count - High Byte							
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

This “Read-Only” register, along with the “Frame CP-Bit Error - One Second Accumulator Register - LSB” (Address = 0x73) contains a 16-bit representation of the number of “CP Bit Errors” tjhat have been detected by the Receive DS3 Framer block, within the last one-second sampling period. This register contains the MSB (or Upper Byte) value of this 16-bit expression.

2.3.2.93 CP-Bit Error One Second Accumulator Register - LSB

CP-BIT ERRORS - ONE SECOND ACCUMULATOR REGISTER - LSB (ADDRESS = 0X73)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CP Bit Error Count - Low Byte							
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

This “Read-Only” register, along with the “Frame CP-Bit Error - One Second Accumulator Register - MSB” (Address = 0x72) contains a 16-bit representation of the number of “CP Bit Errors” tjhat have been detected by the Receive DS3 Framer block, within the last one-second sampling period. This register contains the LSB (or Lower Byte) value of this 16-bit expression.

2.3.2.94 Line Interface Drive Register

LINE INTERFACE DRIVE REGISTER (ADDRESS = 0X80)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
		REQB	TAOS	ENCODIS	TxLEV	RLOOP	LLOOP
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	1	0	0	0

Bit 5 - REQB - (Receive Equalization Bypass Control)

This "Read/Write" bit-field allows the user to control the state of the REQB output pin of the XRT72L13. This output pin is intended to be connected to the REQB input pins of the XRT7300 DS3/E3 LIU IC. If the user forces this signal to toggle "high", then the Receive Equalizer (within the XRT7300) will be disabled. Conversely, if the user forces this signal to toggle "low", then the Receive Equalizer (within the XRT7300) will be enabled.

Writing a "1" to this bit-field causes the Framer device to toggle the REQB output pin "high". Writing a "0" to this bit-field causes the Framer device to toggle the REQB output pin "low".

For information on the criteria that should be used when deciding whether to bypass the equalization circuitry or not, please consult the "XRT7300 DS3/E3/STS-1 LIU IC" data sheet.

NOTE: *If the customer is not using the XRT7300 DS3/E3/STS-1 LIU IC, then he/she can use this bit-field and the REQB output pin for other purposes.*

Bit 4 - TAOS - (Transmit All Ones Signal)

This "Read/Write" bit-field allows the user to control the state of the TAOS output pin of the XRT72L13. This output pin is intended to be connected to the TAOS input pin of the XRT7300 DS3/E3/STS-1 LIU IC. If the user forces this signal to toggle "high", then the XRT7300 LIU device will transmit an "All Ones" pattern onto the line. Conversely, if the user commands this output signal to toggle "low" then the XRT7300 LIU IC will proceed to transmit data based upon the pattern that it receives via the TxPOS and TxNEG output pins (of the Framer IC).

Writing a "1" to this bit-field will cause the TAOS output pin to toggle "high". Writing a "0" to this bit-field will cause this output pin to toggle "low".

NOTE: *If the customer is not using the XRT7300 DS3/E3/STS-1 LIU IC, then he/she can use this bit-field, and the TAOS output pin for other purposes.*

Bit 3 - Encodis - (B3ZS Encoder Disable)

This "Read/Write" bit-field allows the user to control the state of the Encodis output pin of the XRT72L13 M13 device. This output pin is intended to be connected to the Encodis input pin of the XRT7300 DS3/E3/STS-1 LIU IC. If the user forces this signal to toggle "high", then the "internal B3ZS/HDB3 encoder" (within the XRT7300) will be disabled. Conversely, if the user command this output signal to toggle "low", then the "internal B3ZS/HDB3 encoder" (within the XRT7300) will be enabled.

Writing a "1" to this bit-field causes the Framer IC to toggle the "Encodis" output pin "high". Writing a "0" to this bit-field will cause the Framer IC to toggle this output pin "low".

NOTES:

1. *The B3ZS/HDB3 encoder, within the XRT7300, is not to be confused with the B3ZS/HDB3 encoding capable that exists within the Transmit Section of the Framer IC.*

2. *The user is advised to disabled the B3ZS/HDB3 encoder (within the XRT7300 IC) if the XRT72L13 is configured to operate in the B3ZS/HDB3 line code.*
3. *If the customer is not using the XRT7300 DS3/E3/STS-1 LIU IC, then he/she can use this bit-field and the "Encodis" output pin for other purposes.*
4. *It is permissible to tie the "Encodis" output pin of the XRT 72L13 DS3 Framer IC to both the "Encodis" and "Decodis" input pins of the XRT7300.*

Bit 2 - TxLev - (Transmit Output Line Build-Out Select Output)

This "Read/Write" bit-field allows the user to control the state of the "TxLev" output pin of the XRT72L13. This output pin is intended to be connected to the TxLev input pin of the XRT7300 DS3/E3/STS-1 LIU IC. If the user commands this signal to toggle "high", then the XRT7300 DS3/E3/STS-1 LIU IC will disable the "Transmit Line Build-Out" circuitry, and will transmit unshaped (square-wave) pulses onto the line. If the user commands this signal to toggle "low", then the XRT7300 DS3/E3 LIU IC will enable the "Transmit Line Build-Out" circuitry, and will transmit shaped pulses onto the line.

In order to insure that the transmit output pulses of the XRT7300 meet the "DSX-3 Isolated Pulse Template Requirements (per Bellcore GR-499-CORE), the user is advised to set this bit-field to "0", if the length of cable (between the XRT7300 transmit output and the DSX-3 Cross Connect System) is greater than 225 feet.

Conversely, the user is advised to set this bit-field to "1", if the length of cable (between the XRT7300 transmit output and the DSX-3 Cross Connect system) is less than 225 feet.

Writing a "1" to this bit-field commands the Framer to toggle the TxLev output "high". Writing a "0" to this bit-field commands the Framer to toggle this output signal "low".

Bit 1 - RLOOP - (Remote Loopback)

This "Read/Write" bit-field allows the user to control the state of the RLOOP output pin of the XRT72L13 M13 device. This output pin is intended to be connected to the "RLOOP" input pin of the XRT7300 DS3/E3 LIU IC.

In the XRT7300 DS3/E3 LIU IC, the state of the "RLOOP" and the "LLOOP" pins are used to dictate which loop-back mode the XRT7300 will operate in. The following table presents the relationship between the state of these two input pins (or bit-fields) and the resulting loop-back modes.

RLOOP	LLOOP	RESULTING LOOP-BACK MODE OF THE XRT7300
0	0	Normal Operation (No Loop-back Mode)
0	1	Analog Local Loop-back Mode
1	0	Remote Loop-back Mode
1	1	Digital Local Loop-back Mode

Writing a "1" into this bit-field commands the Framer IC to toggle the "RLOOP" output signal "high". Writing a "0" into this bit-field commands the Framer IC to toggle this output signal "low".

For a detailed description of the XRT7300 DS3/E3 LIU's operation, during each of these above-mentioned loop-back modes, please consult the "XRT7300 DS3/E3/STS-1 LIU IC" Data Sheet.

NOTE: *If the customer is not using the XRT7300 DS3/E3/STS-1 LIU IC, then he/she can use this bit-field and the "RLOOP" output pin for other purposes.*

Bit 0 - LLOOP - (Local Loop-back)

This "Read/Write" bit-field allows the user to control the state of the LLOOP output pin of the XRT72L13 M13 device. This output pin is intended to be connected to the LLOOP input pin of the XRT7300 DS3/E3 LIU IC.

In the XRT7300 DS3/E3 LIU IC, the state of the "RLOOP" and the "LLOOP" pins are used to dictate which loop-back mode the XRT7300 will operate in. The following table presents the relationship between the state of these two input pins (or bit-fields) and the resulting loop-back modes.

RLOOP	LLOOP	RESULTING LOOP-BACK MODE OF THE XRT7300
0	0	Normal Operation (No Loop-back Mode)
0	1	Analog Local Loop-back Mode
1	0	Remote Loop-back Mode

RLOOP	LLOOP	RESULTING LOOP-BACK MODE OF THE XRT7300
1	1	Digital Local Loop-back Mode

Writing a "1" into this bit-field commands the XRT72L13 M13 device to toggle the "LLOOP" output signal "high". Writing a "0" into this bit-field commands the XRT72L13 M13 device to toggle this output signal "low".

For a detailed description of the XRT7300 DS3/E3 LIU's operation, during each of these above-mentioned loop-back modes, please consult the "XRT7300 DS3/E3/STS-1 LIU IC" Data Sheet.

NOTE: *If the customer is not using the XRT7300 DS3/E3/STS-1 LIU IC, then he/she can use this bit-field and the "LLOOP" output pin for other purposes.*

2.3.2.95 Line Interface Scan Register

LINE INTERFACE SCAN REGISTER (ADDRESS = 0X81)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
					DMO	RLOL	RLOS
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

Bit 2 - DMO - (Drive Monitor Output)

This "Read-Only" bit-field indicates the logic state of the DMO input pin of the XRT72L13 M13 device. This input pin is intended to be connected to the DMO output pin of the XRT7300 DS3/E3 LIU IC. If this bit-field contains a logic "1", then the DMO input pin is "high". The XRT7300 DS3/E3 LIU IC will set this pin "high" if the drive monitor circuitry (within the XRT7300) has not detected any bipolar signals at the MTIP and MRING inputs (of the XRT7300) within the last 128 $\pm$ 32 bit periods.

Conversely, if this bit-field contains a logic "0", then the DMO input pin is "high". The XRT7300 DS3/E3 LIU IC will set this pin "low" if bipolar signals are being detected at the MTIP and MRING input pins.

NOTE: *If this customer is not using the XRT7300 DS3/E3 LIU IC, then he/she can use this input pin for a variety of other purposes.*

Bit 1 - RLOL - (Receive Loss of Lock)

This "Read-Only" bit-field indicates the logic state of the RLOL input pin of the XRT72L13 M13 device. This input pin is intended to be connected to the RLOL output pin of the XRT7300 DS3/E3 LIU IC. If this bit-field contains a logic "1", then the RLOL input pin is "high". The XRT7300 DS3/E3 LIU IC will set this pin "high" if the clock recovery phase-locked-loop circuitry (within the XRT7300) has lost "lock" with the incoming DS3/E3 data-stream and is not properly recovering clock and data.

Conversely, if this bit-field contains a logic "0", then the RLOL input pin is "low". The XRT7300 DS3/E3 LIU IC will hold this pin "low" as long as this "clock recovery phase-locked-loop" circuitry (within the XRT7300) is properly "locked" onto the incoming DS3 data-stream, and is properly recovering clock and data from this data-stream.

For more information on the operation of the XRT7300 DS3/E3/STS-1 LIU IC, please consult the "XRT7300 DS3/E3/STS-1 LIU IC" data sheet.

NOTE: *If the customer is not using the XRT7300 DS3/E3/STS-1 IC, then he/she can use this bit-field, and the RLOL input pin for other purposes.*

Bit 0 - RLOS - (Receive Loss of Signal)

This "Read-Only" bit-field indicates the logic state of the RLOS input pin of the XRT72L13 M13 device. This input pin is intended to be connected to the RLOS output pin of the XRT7300 DS3/E3 LIU IC. If this bit-field contains a logic "1", then the RLOS input pin is "high". The XRT7300 will toggle this signal "high" if it (the XRT7300 LIU IC) is currently declaring an LOS (Loss of Signal) condition.

Conversely, if this bit-field contains a logic "0", then the RLOS input pin is "low". The XRT7300 will hold this signal "low" if it is NOT currently declaring an LOS (Loss of Signal) condition.

For more information on the LOS Declaration and Clearance criteria of the XRT7300, please consult the "XRT7300 DS3/E3/STS-1 LIU IC" data sheet.

NOTE: *Asserting the RLOS input pin will cause the XRT 72L13 DS3 Framer IC to generate the "Change in LOS Condition" interrupt and declare an "LOS" (Loss of Signal) condition. Therefore, this input pin should not be used as a general purpose input.*

2.3.2.96 M23 RxDS2 Loopback Request Interrupt Enable Register

M23 RXDS2 LOOP-BACK REQUEST INTERRUPT ENABLE REGISTER (ADDRESS = 0X90)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	M23 # 7 Loopback Request Interrupt Enable	M23 # 6 Loopback Request Interrupt Enable	M23 # 5 Loopback Request Interrupt Enable	M23 # 4 Loopback Request Interrupt Enable	M23 # 3 Loopback Request Interrupt Enable	M23 # 2 Loopback Request Interrupt Enable	M23 # 1 Loopback Request Interrupt Enable
RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit 6 - M23 # 7 Loopback Request Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “Receive DS2 Channel # 7 Loop-back Request” Interrupt.

Setting this bit-field to “1” enables this interrupt. Setting this bit-field to “0” disables this interrupt.

Bit 5 - M23 # 6 Loopback Request Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “Receive DS2 Channel # 6 Loop-back Request” Interrupt.

Setting this bit-field to “1” enables this interrupt. Setting this bit-field to “0” disables this interrupt.

Bit 4 - M23 # 5 Loopback Request Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “Receive DS2 Channel # 5 Loop-back Request” Interrupt.

Setting this bit-field to “1” enables this interrupt. Setting this bit-field to “0” disables this interrupt.

Bit 3 - M23 # 4 Loopback Request Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “Receive DS2 Channel # 4 Loop-back Request” Interrupt.

Setting this bit-field to “1” enables this interrupt. Setting this bit-field to “0” disables this interrupt.

Bit 2 - M23 # 3 Loopback Request Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “Receive DS2 Channel # 3 Loop-back Request” Interrupt.

Setting this bit-field to “1” enables this interrupt. Setting this bit-field to “0” disables this interrupt.

Bit 1 - M23 # 2 Loopback Request Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “Receive DS2 Channel # 2 Loop-back Request” Interrupt.

Setting this bit-field to “1” enables this interrupt. Setting this bit-field to “0” disables this interrupt.

Bit 0 - M23 # 1 Loopback Request Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “Receive DS2 Channel # 1 Loop-back Request” Interrupt.

Setting this bit-field to “1” enables this interrupt. Setting this bit-field to “0” disables this interrupt.

2.3.2.97 M23 RxDS2 Loopback Request Interrupt Register

M23 RXDS2 CHANGE IN LOOP-BACK REQUEST STATE - INTERRUPT REGISTER (ADDRESS = 0X91)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	Change in Loop-back Request Interrupt Status M23 # 7	Change in Loop-back Request Interrupt Status M23 # 6	Change in Loop-back Request Interrupt Status M23 # 5	Change in Loop-back Request Interrupt Status M23 # 4	Change in Loop-back Request Interrupt Status M23 # 3	Change in Loop-back Request Interrupt Status M23 # 2	Change in Loop-back Request Interrupt Status M23 # 1
RO	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

Bit 6 - Change in Loop-back Request Interrupt Status, M23 # 7.

This “Reset-upon-Read” bit-field indicates whether or not there has been a change in the “Loop-back Request Status” for DS2 Channel # 7.

This bit-field will be set to “0” if there has been no change in the “Loop-back Request Status” for DS2 Channel # 7. Conversely, this bit-field will set to “1” anytime there has been a change in the “Loop-back Request Status” for DS2 Channel # 7.

NOTE: *This bit-field will be asserted in response to either of the following conditions.*

1. The “Loop-back Request Status” for DS2 Channel 7 has transitioned from the active to the inactive state.
2. The Loop-back Request Status” for DS2 Channel 7 has transition from the inactive to the active state.

Bit 5 - Change in Loop-back Request Interrupt Status, M23 # 6.

This “Reset-upon-Read” bit-field indicates whether or not there has been a change in the “Loop-back Request Status” for DS2 Channel # 6.

This bit-field will be set to “0” if there has been no change in the “Loop-back Request Status” for DS2 Channel # 6. Conversely, this bit-field will set to “1” anytime there has been a change in the “Loop-back Request Status” for DS2 Channel # 6.

NOTE: *This bit-field will be asserted in response to either of the following conditions.*

1. The “Loop-back Request Status” for DS2 Channel 6 has transitioned from the active to the inactive state.
2. The Loop-back Request Status” for DS2 Channel 6 has transition from the inactive to the active state.

Bit 4 - Change in Loop-back Request Interrupt Status, M23 # 5.

This “Reset-upon-Read” bit-field indicates whether or not there has been a change in the “Loop-back Request Status” for DS2 Channel # 5.

This bit-field will be set to “0” if there has been no change in the “Loop-back Request Status” for DS2 Channel # 5. Conversely, this bit-field will set to “1” anytime there has been a change in the “Loop-back Request Status” for DS2 Channel # 5.

NOTE: *This bit-field will be asserted in response to either of the following conditions.*

1. The “Loop-back Request Status” for DS2 Channel 5 has transitioned from the active to the inactive state.
2. The Loop-back Request Status” for DS2 Channel 5 has transition from the inactive to the active state.

Bit 3 - Change in Loop-back Request Interrupt Status, M23 # 4.

This “Reset-upon-Read” bit-field indicates whether or not there has been a change in the “Loop-back Request Status” for DS2 Channel # 4.

This bit-field will be set to “0” if there has been no change in the “Loop-back Request Status” for DS2 Channel # 4. Conversely, this bit-field will set to “1” anytime there has been a change in the “Loop-back Request Status” for DS2 Channel # 4.

NOTE: *This bit-field will be asserted in response to either of the following conditions.*

1. The “Loop-back Request Status” for DS2 Channel 4 has transitioned from the active to the inactive state.
2. The Loop-back Request Status” for DS2 Channel 4 has transition from the inactive to the active state.

Bit 2- Change in Loop-back Request Interrupt Status, M23 # 3

This “Reset-upon-Read” bit-field indicates whether or not there has been a change in the “Loop-back Request Status” for DS2 Channel # 3.

This bit-field will be set to “0” if there has been no change in the “Loop-back Request Status” for DS2 Channel # 3. Conversely, this bit-field will set to “1” anytime there has been a change in the “Loop-back Request Status” for DS2 Channel # 3.

NOTE: *This bit-field will be asserted in response to either of the following conditions.*

1. The “Loop-back Request Status” for DS2 Channel 3 has transitioned from the active to the inactive state.
2. The Loop-back Request Status” for DS2 Channel 3 has transition from the inactive to the active state.

Bit 1 - Change in Loop-back Request Interrupt Status, M23 # 2

This “Reset-upon-Read” bit-field indicates whether or not there has been a change in the “Loop-back Request Status” for DS2 Channel # 2.

This bit-field will be set to “0” if there has been no change in the “Loop-back Request Status” for DS2 Channel # 2. Conversely, this bit-field will set to “1” anytime there has been a change in the “Loop-back Request Status” for DS2 Channel # 2.

NOTE: *This bit-field will be asserted in response to either of the following conditions.*

1. The “Loop-back Request Status” for DS2 Channel 2 has transitioned from the active to the inactive state.
2. The Loop-back Request Status” for DS2 Channel 2 has transition from the inactive to the active state.

Bit 0 - Change in Loop-back Request Interrupt Status, M23 # 1.

This “Reset-upon-Read” bit-field indicates whether or not there has been a change in the “Loop-back Request Status” for DS2 Channel # 1.

This bit-field will be set to “0” if there has been no change in the “Loop-back Request Status” for DS2 Channel # 1. Conversely, this bit-field will set to “1” anytime there has been a change in the “Loop-back Request Status” for DS2 Channel # 1.

NOTE: *This bit-field will be asserted in response to either of the following conditions.*

1. The “Loop-back Request Status” for DS2 Channel 1 has transitioned from the active to the inactive state.
2. The Loop-back Request Status” for DS2 Channel 1 has transition from the inactive to the active state.

2.3.2.98 M23 RxDS2 Loopback Request Status Register.

M23 RXDS2 LOOP-BACK REQUEST STATUS - INTERRUPT REGISTER (ADDRESS = 0X92)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	Loop-back Request Status M23 # 7	Loop-back Request Status M23 # 6	Loop-back Request Status M23 # 5	Loop-back Request Status M23 # 4	Loop-back Request Status M23 # 3	Loop-back Request Status M23 # 2	Loop-back Request Status M23 # 1
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

Bit 6 - Loop-back Request Status - M23 # 7

This “Read-Only” bit-field reflect the current Loop-back Request state of M23 # 7.

This bit-field will be set to “1” if the “Loop-back Request” for M23 # 7 is currently active.

Conversely, this bit-field will be set to “0” if the “Loop-back Request” for M23 # 7 is currently inactive.

Bit 5 - Loop-back Request Status - M23 # 6

This “Read-Only” bit-field reflect the current Loop-back Request state of M23 # 6.

This bit-field will be set to “1” if the “Loop-back Request” for M23 # 6 is currently active.

Conversely, this bit-field will be set to “0” if the “Loop-back Request” for M23 # 6 is currently inactive.

Bit 4 - Loop-back Request Status - M23 # 5

This “Read-Only” bit-field reflect the current Loop-back Request state of M23 # 5.

This bit-field will be set to “1” if the “Loop-back Request” for M23 # 5 is currently active.

Conversely, this bit-field will be set to “0” if the “Loop-back Request” for M23 # 5 is currently inactive.

Bit 3 - Loop-back Request Status - M23 # 4

This “Read-Only” bit-field reflect the current Loop-back Request state of M23 # 4.

This bit-field will be set to “1” if the “Loop-back Request” for M23 # 4 is currently active.

Conversely, this bit-field will be set to “0” if the “Loop-back Request” for M23 # 4 is currently inactive.

Bit 2 - Loop-back Request Status - M23 # 3

This “Read-Only” bit-field reflect the current Loop-back Request state of M23 # 3.

This bit-field will be set to “1” if the “Loop-back Request” for M23 # 3 is currently active.

Conversely, this bit-field will be set to “0” if the “Loop-back Request” for M23 # 3 is currently inactive.

Bit 1 - Loop-back Request Status - M23 # 2

This “Read-Only” bit-field reflect the current Loop-back Request state of M23 # 2.

This bit-field will be set to “1” if the “Loop-back Request” for M23 # 2 is currently active.

Conversely, this bit-field will be set to “0” if the “Loop-back Request” for M23 # 2 is currently inactive.

Bit 0 - Loop-back Request Status - M23 # 1

This “Read-Only” bit-field reflect the current Loop-back Request state of M23 # 1.

This bit-field will be set to “1” if the “Loop-back Request” for M23 # 1 is currently active.

Conversely, this bit-field will be set to “0” if the “Loop-back Request” for M23 # 1 is currently inactive.

2.3.2.99 M12 DS2 # 1 Loopback Interrupt/Interrupt Enable Register

M12 DS2 # 1 LOOP-BACK INTERRUPT/INTERRUPT ENABLE REGISTER (ADDRESS = 0X93)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DS1 Channel 3 Loop-back Request Interrupt Status	DS1 Channel 2 Loop-back Request Interrupt Status	DS1 Channel 1 Loop-back Request Interrupt Status	DS1 Channel 0 Loop-back Request Interrupt Status	DS1 Channel 3 Loop-back Request Interrupt Enable	DS1 Channel 2 Loop-back Request Interrupt Enable	DS1 Channel 1 Loop-back Request Interrupt Enable	DS1 Channel 0 Loop-back Request Interrupt Enable
RUR	RUR	RUR	RUR	R/W	R/W	R/W/	R/W
0	0	0	0	0	0	0	0

Bit 7 - DS1 Channel 3 Loop-back Request Interrupt Status

This “Reset-upon-Read” bit-field indicates whether the “DS1 Channel 3 Loop-back Request” interrupt has occurred or not.

This bit-field will be set to “1” if the “DS1 Channel 3 Loop-back Request Interrupt” has occurred since the last read of this register.

This bit-field will be set to “0” if the “DS1 Channel 3 Loop-back Request” interrupt has NOT occurred since the last read of this register.

NOTE: *This bit-field is ignored if the XRT72L13 is configured to operate in the “ITU-T G.747 Mode”.*

Bit 6 - DS1 Channel 2 Loop-back Request Interrupt Status

This “Reset-upon-Read” bit-field indicates whether the “DS1 Channel 2 Loop-back Request” interrupt has occurred or not.

This bit-field will be set to “1” if the “DS1 Channel 2 Loop-back Request Interrupt” has occurred since the last read of this register.

This bit-field will be set to “0” if the “DS1 Channel 2 Loop-back Request” interrupt has NOT occurred since the last read of this register.

Bit 5 - DS1 Channel 1 Loop-back Request Interrupt Status

This “Reset-upon-Read” bit-field indicates whether the “DS1 Channel 1 Loop-back Request” interrupt has occurred or not.

This bit-field will be set to “1” if the “DS1 Channel 1 Loop-back Request Interrupt” has occurred since the last read of this register.

This bit-field will be set to “0” if the “DS1 Channel 1 Loop-back Request” interrupt has NOT occurred since the last read of this register.

Bit 4 - DS1 Channel 0 Loop-back Request Interrupt Status

This “Reset-upon-Read” bit-field indicates whether the “DS1 Channel 0 Loop-back Request” interrupt has occurred or not.

This bit-field will be set to “1” if the “DS1 Channel 0 Loop-back Request Interrupt” has occurred since the last read of this register.

This bit-field will be set to “0” if the “DS1 Channel 0 Loop-back Request” interrupt has NOT occurred since the last read of this register.

Bit 3 - DS1 Channel 3 Loop-back Request Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS1 Channel 3 Loop-back Request” Interrupt.

Setting this bit to “0” disables this interrupt. Conversely, setting this bit to “1” enables this interrupt.

NOTE: *This bit-field is ignored if the XRT72L13 is configured to operate in the “ITU-T G.747 Mode”.*

Bit 2 - DS1 Channel 2 Loop-back Request Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS1 Channel 2 Loop-back Request” Interrupt.

Setting this bit to “0” disables this interrupt. Conversely, setting this bit to “1” enables this interrupt.

Bit 1 - DS1 Channel 1 Loop-back Request Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS1 Channel 1 Loop-back Request” Interrupt.

Setting this bit to “0” disables this interrupt. Conversely, setting this bit to “1” enables this interrupt.

Bit 0 - DS1 Channel 0 Loop-back Request Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS1 Channel 0 Loop-back Request” Interrupt.

Setting this bit to “0” disables this interrupt. Conversely, setting this bit to “1” enables this interrupt.

2.3.2.100 M12 DS2 # 1 Loopback Status Register

M12 DS2 # 1 LOOP-BACK STATUS REGISTER (ADDRESS = 0X94)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				DS1 Channel # 3 Loopback Status	DS1 Channel # 2 Loopback Status	DS1 Channel # 1 Loopback Status	DS1 Channel # 0 Loopback Status
R/O	R/O	R/O	/RO	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

Bit 3 - DS1 Channel # 3 Loop-back Status

This “Read-Only” bit-field indicates whether or not a loop-back request has been detected for DS1 Channel # 3.

This bit-field will be set to “1” if a loop-back request has been detected for DS1 Channel # 3. Conversely, this bit-field will be set to “0” if a loop-back request has NOT been detected for DS1 Channel # 3.

NOTE: *This bit-field is invalid if the XRT72L13 M13 device is operating in the “ITU-T G.747” Mode.*

Bit 2 - DS1 Channel # 2 Loop-back Status

This “Read-Only” bit-field indicates whether or not a loop-back request has been detected for DS1 Channel # 2.

This bit-field will be set to “1” if a loop-back request has been detected for DS1 Channel # 2. Conversely, this bit-field will be set to “0” if a loop-back request has NOT been detected for DS1 Channel # 2.

Bit 1 - DS1 Channel # 1 Loop-back Status

This “Read-Only” bit-field indicates whether or not a loop-back request has been detected for DS1 Channel # 1.

This bit-field will be set to “1” if a loop-back request has been detected for DS1 Channel # 1. Conversely, this bit-field will be set to “0” if a loop-back request has NOT been detected for DS1 Channel # 1.

Bit 0 - DS1 Channel # 0 Loop-back Status

This “Read-Only” bit-field indicates whether or not a loop-back request has been detected for DS1 Channel # 0.

This bit-field will be set to “1” if a loop-back request has been detected for DS1 Channel # 0. Conversely, this bit-field will be set to “0” if a loop-back request has NOT been detected for DS1 Channel # 0.

2.3.2.101 M12 DS2 # 2 Loopback Interrupt/Interrupt Enable Register

M12 DS2 # 2 LOOP-BACK INTERRUPT/INTERRUPT ENABLE REGISTER (ADDRESS = 0X95)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DS1 Channel 7 Loop-back Request Interrupt Status	DS1 Channel 6 Loop-back Request Interrupt Status	DS1 Channel 5 Loop-back Request Interrupt Status	DS1 Channel 4 Loop-back Request Interrupt Status	DS1 Channel 7 Loop-back Request Interrupt Enable	DS1 Channel 6 Loop-back Request Interrupt Enable	DS1 Channel 5 Loop-back Request Interrupt Enable	DS1 Channel 4 Loop-back Request Interrupt Enable
RUR	RUR	RUR	RUR	R/W	R/W	R/W/	R/W
0	0	0	0	0	0	0	0

Bit 7 - DS1 Channel 7 Loop-back Request Interrupt Status

This “Reset-upon-Read” bit-field indicates whether the “DS1 Channel 7 Loop-back Request” interrupt has occurred or not.

This bit-field will be set to “1” if the “DS1 Channel 7 Loop-back Request Interrupt” has occurred since the last read of this register.

This bit-field will be set to “0” if the “DS1 Channel 7 Loop-back Request” interrupt has NOT occurred since the last read of this register.

NOTE: This bit-field is ignored if the XRT72L13 is configured to operate in the “ITU-T G.747 Mode”.

Bit 6 - DS1 Channel 6 Loop-back Request Interrupt Status

This “Reset-upon-Read” bit-field indicates whether the “DS1 Channel 6 Loop-back Request” interrupt has occurred or not.

This bit-field will be set to “1” if the “DS1 Channel 6 Loop-back Request Interrupt” has occurred since the last read of this register.

This bit-field will be set to “0” if the “DS1 Channel 6 Loop-back Request” interrupt has NOT occurred since the last read of this register.

Bit 5 - DS1 Channel 5 Loop-back Request Interrupt Status

This “Reset-upon-Read” bit-field indicates whether the “DS1 Channel 5 Loop-back Request” interrupt has occurred or not.

This bit-field will be set to “1” if the “DS1 Channel 5 Loop-back Request Interrupt” has occurred since the last read of this register.

This bit-field will be set to “0” if the “DS1 Channel 5 Loop-back Request” interrupt has NOT occurred since the last read of this register.

Bit 4 - DS1 Channel 4 Loop-back Request Interrupt Status

This “Reset-upon-Read” bit-field indicates whether the “DS1 Channel 4 Loop-back Request” interrupt has occurred or not.

This bit-field will be set to “1” if the “DS1 Channel 4 Loop-back Request Interrupt” has occurred since the last read of this register.

This bit-field will be set to “0” if the “DS1 Channel 4 Loop-back Request” interrupt has NOT occurred since the last read of this register.

Bit 3 - DS1 Channel 7 Loop-back Request Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS1 Channel 7 Loop-back Request” Interrupt.

Setting this bit to “0” disables this interrupt. Conversely, setting this bit to “1” enables this interrupt.

Bit 2 - DS1 Channel 6 Loop-back Request Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS1 Channel 6 Loop-back Request” Interrupt.

Setting this bit to “0” disables this interrupt. Conversely, setting this bit to “1” enables this interrupt.

Bit 1 - DS1 Channel 5 Loop-back Request Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS1 Channel 5 Loop-back Request” Interrupt.

Setting this bit to “0” disables this interrupt. Conversely, setting this bit to “1” enables this interrupt.

Bit 0 - DS1 Channel 4 Loop-back Request Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS1 Channel 4 Loop-back Request” Interrupt.

Setting this bit to “0” disables this interrupt. Conversely, setting this bit to “1” enables this interrupt.

2.3.2.102 M12 DS2 # 2 Loopback Status Register

M12 DS2 # 1 LOOP-BACK STATUS REGISTER (ADDRESS = 0X96)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				DS1 Channel # 7 Loopback Status	DS1 Channel # 6 Loopback Status	DS1 Channel # 5 Loopback Status	DS1 Channel # 4 Loopback Status
R/O	R/O	R/O	/RO	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

Bit 3 - DS1 Channel # 7 Loop-back Status

This “Read-Only” bit-field indicates whether or not a loop-back request has been detected for DS1 Channel # 7.

This bit-field will be set to “1” if a loop-back request has been detected for DS1 Channel # 7. Conversely, this bit-field will be set to “0” if a loop-back request has NOT been detected for DS1 Channel # 7.

NOTE: This bit-field is invalid if the XRT72L13 M13 device is operating in the "ITU-T G.747" Mode.

Bit 2 - DS1 Channel # 6 Loop-back Status

This "Read-Only" bit-field indicates whether or not a loop-back request has been detected for DS1 Channel # 6.

This bit-field will be set to "1" if a loop-back request has been detected for DS1 Channel # 6. Conversely, this bit-field will be set to "0" if a loop-back request has NOT been detected for DS1 Channel # 6.

Bit 1 - DS1 Channel # 5 Loop-back Status

This "Read-Only" bit-field indicates whether or not a loop-back request has been detected for DS1 Channel # 5.

This bit-field will be set to "1" if a loop-back request has been detected for DS1 Channel # 5. Conversely, this bit-field will be set to "0" if a loop-back request has NOT been detected for DS1 Channel # 5.

Bit 0 - DS1 Channel # 4 Loop-back Status

This "Read-Only" bit-field indicates whether or not a loop-back request has been detected for DS1 Channel # 4.

This bit-field will be set to "1" if a loop-back request has been detected for DS1 Channel # 4. Conversely, this bit-field will be set to "0" if a loop-back request has NOT been detected for DS1 Channel # 4.

2.3.2.103 M12 DS2 # 3 Loopback Interrupt/Interrupt Enable Register

M12 DS2 # 3 LOOP-BACK INTERRUPT/INTERRUPT ENABLE REGISTER (ADDRESS = 0X97)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DS1 Channel 11 Loop-back Request Interrupt Status	DS1 Channel 10 Loop-back Request Interrupt Status	DS1 Channel 9 Loop-back Request Interrupt Status	DS1 Channel 8 Loop-back Request Interrupt Status	DS1 Channel 11 Loop-backj Request Interrupt Enable	DS1 Channel 10 Loop-backj Request Interrupt Enable	DS1 Channel 9 Loop-backj Request Interrupt Enable	DS1 Channel 8 Loop-backj Request Interrupt Enable
RUR	RUR	RUR	RUR	R/W	R/W	R/W/	R/W
0	0	0	0	0	0	0	0

Bit 7 - DS1 Channel 11 Loop-back Request Interrupt Status

This "Reset-upon-Read" bit-field indicates whether the "DS1 Channel 11 Loop-back Request" interrupt has occurred or not.

This bit-field will be set to "1" if the "DS1 Channel 11 Loop-back Request Interrupt" has occurred since the last read of this register.

This bit-field will be set to "0" if the "DS1 Channel 11 Loop-back Request" interrupt has NOT occurred since the last read of this register.

NOTE: This bit-field is ignored if the XRT72L13 is configured to operate in the "ITU-T G.747 Mode".

Bit 6 - DS1 Channel 10 Loop-back Request Interrupt Status

This "Reset-upon-Read" bit-field indicates whether the "DS1 Channel 10 Loop-back Request" interrupt has occurred or not.

This bit-field will be set to "1" if the "DS1 Channel 10 Loop-back Request Interrupt" has occurred since the last read of this register.

This bit-field will be set to "0" if the "DS1 Channel 10 Loop-back Request" interrupt has NOT occurred since the last read of this register.

Bit 5 - DS1 Channel 9 Loop-back Request Interrupt Status

This "Reset-upon-Read" bit-field indicates whether the "DS1 Channel 9 Loop-back Request" interrupt has occurred or not.

This bit-field will be set to "1" if the "DS1 Channel 9 Loop-back Request Interrupt" has occurred since the last read of this register.

This bit-field will be set to "0" if the "DS1 Channel 9 Loop-back Request" interrupt has NOT occurred since the last read of this register.

Bit 4 - DS1 Channel 8 Loop-back Request Interrupt Status

This "Reset-upon-Read" bit-field indicates whether the "DS1 Channel 8 Loop-back Request" interrupt has occurred or not.

This bit-field will be set to "1" if the "DS1 Channel 8 Loop-back Request Interrupt" has occurred since the last read of this register.

This bit-field will be set to "0" if the "DS1 Channel 8 Loop-back Request" interrupt has NOT occurred since the last read of this register.

Bit 3 - DS1 Channel 11 Loop-back Request Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS1 Channel 11 Loop-back Request” Interrupt.

Setting this bit to “0” disables this interrupt. Conversely, setting this bit to “1” enables this interrupt.

Bit 2 - DS1 Channel 10 Loop-back Request Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS1 Channel 10 Loop-back Request” Interrupt.

Setting this bit to “0” disables this interrupt. Conversely, setting this bit to “1” enables this interrupt.

Bit 1 - DS1 Channel 9 Loop-back Request Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS1 Channel 9 Loop-back Request” Interrupt.

Setting this bit to “0” disables this interrupt. Conversely, setting this bit to “1” enables this interrupt.

Bit 0 - DS1 Channel 8 Loop-back Request Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS1 Channel 8 Loop-back Request” Interrupt.

Setting this bit to “0” disables this interrupt. Conversely, setting this bit to “1” enables this interrupt.

2.3.2.104 M12 DS2 # 3 Loopback Status Register

M12 DS2 # 1 LOOP-BACK STATUS REGISTER (ADDRESS = 0X98)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				DS1 Channel # 11 Loopback Status	DS1 Channel # 10 Loopback Status	DS1 Channel # 9 Loopback Status	DS1 Channel # 8 Loopback Status
R/O	R/O	R/O	/RO	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

Bit 3 - DS1 Channel # 11 Loop-back Status

This “Read-Only” bit-field indicates whether or not a loop-back request has been detected for DS1 Channel # 11.

This bit-field will be set to “1” if a loop-back request has been detected for DS1 Channel # 11. Conversely, this bit-field will be set to “0” if a loop-back request has NOT been detected for DS1 Channel # 11.

NOTE: *This bit-field is invalid if the XRT72L13 M13 device is operating in the “ITU-T G.747” Mode.*

Bit 2 - DS1 Channel # 10 Loop-back Status

This “Read-Only” bit-field indicates whether or not a loop-back request has been detected for DS1 Channel # 10.

This bit-field will be set to “1” if a loop-back request has been detected for DS1 Channel # 10. Conversely, this bit-field will be set to “0” if a loop-back request has NOT been detected for DS1 Channel # 10.

Bit 1 - DS1 Channel # 9 Loop-back Status

This “Read-Only” bit-field indicates whether or not a loop-back request has been detected for DS1 Channel # 9.

This bit-field will be set to “1” if a loop-back request has been detected for DS1 Channel # 9. Conversely, this bit-field will be set to “0” if a loop-back request has NOT been detected for DS1 Channel # 9.

Bit 0 - DS1 Channel # 8 Loop-back Status

This “Read-Only” bit-field indicates whether or not a loop-back request has been detected for DS1 Channel # 8.

This bit-field will be set to “1” if a loop-back request has been detected for DS1 Channel # 8. Conversely, this bit-field will be set to “0” if a loop-back request has NOT been detected for DS1 Channel # 8.

2.3.2.105 M12 DS2 # 4 Loopback Interrupt/Interrupt Enable Register

M12 DS2 # 4 LOOP-BACK INTERRUPT/INTERRUPT ENABLE REGISTER (ADDRESS = 0X99)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DS1 Channel 15 Loop-back Interrupt	DS1 Channel 14 Loop-back Interrupt	DS1 Channel 13 Loop-back Interrupt	DS1 Channel 12 Loop-back Interrupt	DS1 Channel 15 Loop-backj Interrupt Enable	DS1 Channel 14 Loop-backj Interrupt Enable	DS1 Channel 13 Loop-backj Interrupt Enable	DS1 Channel 12 Loop-backj Interrupt Enable
RUR	RUR	RUR	RUR	R/W	R/W	R/W/	R/W
0	0	0	0	0	0	0	0

Bit 7 - DS1 Channel 15 Loop-back Request Interrupt Status

This “Reset-upon-Read” bit-field indicates whether the “DS1 Channel 15 Loop-back Request” interrupt has occurred or not.

This bit-field will be set to “1” if the “DS1 Channel 15 Loop-back Request Interrupt” has occurred since the last read of this register.

This bit-field will be set to “0” if the “DS1 Channel 15 Loop-back Request” interrupt has NOT occurred since the last read of this register.

NOTE: *This bit-field is ignored if the XRT72L13 is configured to operate in the “ITU-T G.747 Mode”.*

Bit 6 - DS1 Channel 14 Loop-back Request Interrupt Status

This “Reset-upon-Read” bit-field indicates whether the “DS1 Channel 14 Loop-back Request” interrupt has occurred or not.

This bit-field will be set to “1” if the “DS1 Channel 14 Loop-back Request Interrupt” has occurred since the last read of this register.

This bit-field will be set to “0” if the “DS1 Channel 14 Loop-back Request” interrupt has NOT occurred since the last read of this register.

Bit 5 - DS1 Channel 13 Loop-back Request Interrupt Status

This “Reset-upon-Read” bit-field indicates whether the “DS1 Channel 13 Loop-back Request” interrupt has occurred or not.

This bit-field will be set to “1” if the “DS1 Channel 13 Loop-back Request Interrupt” has occurred since the last read of this register.

This bit-field will be set to “0” if the “DS1 Channel 13 Loop-back Request” interrupt has NOT occurred since the last read of this register.

Bit 4 - DS1 Channel 12 Loop-back Request Interrupt Status

This “Reset-upon-Read” bit-field indicates whether the “DS1 Channel 12 Loop-back Request” interrupt has occurred or not.

This bit-field will be set to “1” if the “DS1 Channel 12 Loop-back Request Interrupt” has occurred since the last read of this register.

This bit-field will be set to “0” if the “DS1 Channel 12 Loop-back Request” interrupt has NOT occurred since the last read of this register.

Bit 3 - DS1 Channel 15 Loop-back Request Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS1 Channel 15 Loop-back Request” Interrupt.

Setting this bit to “0” disables this interrupt. Conversely, setting this bit to “1” enables this interrupt.

Bit 2 - DS1 Channel 14 Loop-back Request Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS1 Channel 14 Loop-back Request” Interrupt.

Setting this bit to “0” disables this interrupt. Conversely, setting this bit to “1” enables this interrupt.

Bit 1 - DS1 Channel 13 Loop-back Request Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS1 Channel 13 Loop-back Request” Interrupt.

Setting this bit to “0” disables this interrupt. Conversely, setting this bit to “1” enables this interrupt.

Bit 0 - DS1 Channel 12 Loop-back Request Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS1 Channel 12 Loop-back Request” Interrupt.

Setting this bit to “0” disables this interrupt. Conversely, setting this bit to “1” enables this interrupt.

2.3.2.106 M12 DS2 # 4 Loopback Status Register

M12 DS2 # 1 LOOP-BACK STATUS REGISTER (ADDRESS = 0X9A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				DS1 Channel # 15 Loopback Status	DS1 Channel # 14 Loopback Status	DS1 Channel # 13 Loopback Status	DS1 Channel # 12 Loopback Status
R/O	R/O	R/O	/RO	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

Bit 3 - DS1 Channel # 15 Loop-back Status

This “Read-Only” bit-field indicates whether or not a loop-back request has been detected for DS1 Channel # 15.

This bit-field will be set to “1” if a loop-back request has been detected for DS1 Channel # 15. Conversely, this bit-field will be set to “0” if a loop-back request has NOT been detected for DS1 Channel # 15.

NOTE: *This bit-field is invalid if the XRT72L13 M13 device is operating in the “ITU-T G.747” Mode.*

Bit 2 - DS1 Channel # 14 Loop-back Status

This “Read-Only” bit-field indicates whether or not a loop-back request has been detected for DS1 Channel # 14.

This bit-field will be set to “1” if a loop-back request has been detected for DS1 Channel # 14. Conversely, this bit-field will be set to “0” if a loop-back request has NOT been detected for DS1 Channel # 14.

Bit 1 - DS1 Channel # 13 Loop-back Status

This “Read-Only” bit-field indicates whether or not a loop-back request has been detected for DS1 Channel # 13.

This bit-field will be set to “1” if a loop-back request has been detected for DS1 Channel # 13. Conversely, this bit-field will be set to “0” if a loop-back request has NOT been detected for DS1 Channel # 13.

Bit 0 - DS1 Channel # 12 Loop-back Status

This “Read-Only” bit-field indicates whether or not a loop-back request has been detected for DS1 Channel # 12.

This bit-field will be set to “1” if a loop-back request has been detected for DS1 Channel # 12. Conversely, this bit-field will be set to “0” if a loop-back request has NOT been detected for DS1 Channel # 12.

2.3.2.107 M12 DS2 # 5 Loopback Interrupt/Interrupt Enable Register

M12 DS2 # 5 LOOP-BACK INTERRUPT/INTERRUPT ENABLE REGISTER (ADDRESS = 0X9B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DS1 Channel 19 Loop-back Request Interrupt Status	DS1 Channel 18 Loop-back Request Interrupt Status	DS1 Channel 17 Loop-back Request Interrupt Status	DS1 Channel 16 Loop-back Request Interrupt Status	DS1 Channel 19 Loop-backj Request Interrupt Enable	DS1 Channel 18 Loop-backj Request Interrupt Enable	DS1 Channel 17 Loop-backj Request Interrupt Enable	DS1 Channel 16 Loop-backj Request Interrupt Enable
RUR	RUR	RUR	RUR	R/W	R/W	R/W/	R/W
0	0	0	0	0	0	0	0

Bit 7 - DS1 Channel 19 Loop-back Request Interrupt Status

This “Reset-upon-Read” bit-field indicates whether the “DS1 Channel 19 Loop-back Request” interrupt has occurred or not.

This bit-field will be set to “1” if the “DS1 Channel 19 Loop-back Request Interrupt” has occurred since the last read of this register.

This bit-field will be set to “0” if the “DS1 Channel 19 Loop-back Request” interrupt has NOT occurred since the last read of this register.

NOTE: *This bit-field is ignored if the XRT72L13 is configured to operate in the “ITU-T G.747 Mode”.*

Bit 6 - DS1 Channel 18 Loop-back Request Interrupt Status

This “Reset-upon-Read” bit-field indicates whether the “DS1 Channel 18 Loop-back Request” interrupt has occurred or not.

This bit-field will be set to “1” if the “DS1 Channel 18 Loop-back Request Interrupt” has occurred since the last read of this register.

This bit-field will be set to “0” if the “DS1 Channel 18 Loop-back Request” interrupt has NOT occurred since the last read of this register.

Bit 5 - DS1 Channel 17 Loop-back Request Interrupt Status

This “Reset-upon-Read” bit-field indicates whether the “DS1 Channel 17 Loop-back Request” interrupt has occurred or not.

This bit-field will be set to “1” if the “DS1 Channel 17 Loop-back Request Interrupt” has occurred since the last read of this register.

This bit-field will be set to “0” if the “DS1 Channel 17 Loop-back Request” interrupt has NOT occurred since the last read of this register.

Bit 4 - DS1 Channel 16 Loop-back Request Interrupt Status

This “Reset-upon-Read” bit-field indicates whether the “DS1 Channel 16 Loop-back Request” interrupt has occurred or not.

This bit-field will be set to “1” if the “DS1 Channel 16 Loop-back Request Interrupt” has occurred since the last read of this register.

This bit-field will be set to “0” if the “DS1 Channel 16 Loop-back Request” interrupt has NOT occurred since the last read of this register.

Bit 3 - DS1 Channel 19 Loop-back Request Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS1 Channel 19 Loop-back Request” Interrupt.

Setting this bit to “0” disables this interrupt. Conversely, setting this bit to “1” enables this interrupt.

Bit 2 - DS1 Channel 18 Loop-back Request Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS1 Channel 18 Loop-back Request” Interrupt.

Setting this bit to “0” disables this interrupt. Conversely, setting this bit to “1” enables this interrupt.

Bit 1 - DS1 Channel 17 Loop-back Request Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS1 Channel 17 Loop-back Request” Interrupt.

Setting this bit to “0” disables this interrupt. Conversely, setting this bit to “1” enables this interrupt.

Bit 0 - DS1 Channel 16 Loop-back Request Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS1 Channel 16 Loop-back Request” Interrupt.

Setting this bit to “0” disables this interrupt. Conversely, setting this bit to “1” enables this interrupt.

2.3.2.108 M12 DS2 # 5 LoopbackStatus Register

M12 DS2 # 1 LOOP-BACK STATUS REGISTER (ADDRESS = 0X9C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				DS1 Channel # 19 Loopback Status	DS1 Channel # 18 Loopback Status	DS1 Channel # 17 Loopback Status	DS1 Channel # 16 Loopback Status
R/O	R/O	R/O	/RO	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

Bit 3 - DS1 Channel # 19 Loop-back Status

This “Read-Only” bit-field indicates whether or not a loop-back request has been detected for DS1 Channel # 19.

This bit-field will be set to “1” if a loop-back request has been detected for DS1 Channel # 19. Conversely, this bit-field will be set to “0” if a loop-back request has NOT been detected for DS1 Channel # 19.

NOTE: *This bit-field is invalid if the XRT72L13 M13 device is operating in the “ITU-T G.747” Mode.*

Bit 2 - DS1 Channel # 18 Loop-back Status

This “Read-Only” bit-field indicates whether or not a loop-back request has been detected for DS1 Channel # 18.

This bit-field will be set to “1” if a loop-back request has been detected for DS1 Channel # 18. Converse-

ly, this bit-field will be set to “0” if a loop-back request has NOT been detected for DS1 Channel # 18.

Bit 1 - DS1 Channel # 17 Loop-back Status

This “Read-Only” bit-field indicates whether or not a loop-back request has been detected for DS1 Channel # 17.

This bit-field will be set to “1” if a loop-back request has been detected for DS1 Channel # 17. Conversely, this bit-field will be set to “0” if a loop-back request has NOT been detected for DS1 Channel # 17.

Bit 0 - DS1 Channel # 16 Loop-back Status

This “Read-Only” bit-field indicates whether or not a loop-back request has been detected for DS1 Channel # 16.

This bit-field will be set to “1” if a loop-back request has been detected for DS1 Channel # 16. Conversely, this bit-field will be set to “0” if a loop-back request has NOT been detected for DS1 Channel # 16.

2.3.2.109 M12 DS2 # 6 Loopback Interrupt/Interrupt Enable Register

M12 DS2 # 6 LOOP-BACK INTERRUPT/INTERRUPT ENABLE REGISTER (ADDRESS = 0X9D)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DS1 Channel 23 Loop-back Request Interrupt Status	DS1 Channel 22 Loop-back Request Interrupt Status	DS1 Channel 21 Loop-back Request Interrupt Status	DS1 Channel 20 Loop-back Request Interrupt Status	DS1 Channel 23 Loop-backj Request Interrupt Enable	DS1 Channel 22 Loop-backj Request Interrupt Enable	DS1 Channel 21 Loop-backj Request Interrupt Enable	DS1 Channel 20 Loop-backj Request Interrupt Enable
RUR	RUR	RUR	RUR	R/W	R/W	R/W/	R/W
0	0	0	0	0	0	0	0

Bit 7 - DS1 Channel 23 Loop-back Request Interrupt Status

This “Reset-upon-Read” bit-field indicates whether the “DS1 Channel 23 Loop-back Request” interrupt has occurred or not.

This bit-field will be set to “1” if the “DS1 Channel 23 Loop-back Request Interrupt” has occurred since the last read of this register.

This bit-field will be set to “0” if the “DS1 Channel 23 Loop-back Request” interrupt has NOT occurred since the last read of this register.

NOTE: *This bit-field is ignored if the XRT72L13 is configured to operate in the “ITU-T G.747 Mode”.*

Bit 6 - DS1 Channel 22 Loop-back Request Interrupt Status

This “Reset-upon-Read” bit-field indicates whether the “DS1 Channel 22 Loop-back Request” interrupt has occurred or not.

This bit-field will be set to “1” if the “DS1 Channel 22 Loop-back Request Interrupt” has occurred since the last read of this register.

This bit-field will be set to “0” if the “DS1 Channel 22 Loop-back Request” interrupt has NOT occurred since the last read of this register.

Bit 5 - DS1 Channel 21 Loop-back Request Interrupt Status

This “Reset-upon-Read” bit-field indicates whether the “DS1 Channel 21 Loop-back Request” interrupt has occurred or not.

This bit-field will be set to “1” if the “DS1 Channel 21 Loop-back Request Interrupt” has occurred since the last read of this register.

This bit-field will be set to “0” if the “DS1 Channel 21 Loop-back Request” interrupt has NOT occurred since the last read of this register.

Bit 4 - DS1 Channel 20 Loop-back Request Interrupt Status

This “Reset-upon-Read” bit-field indicates whether the “DS1 Channel 20 Loop-back Request” interrupt has occurred or not.

This bit-field will be set to “1” if the “DS1 Channel 20 Loop-back Request Interrupt” has occurred since the last read of this register.

This bit-field will be set to “0” if the “DS1 Channel 20 Loop-back Request” interrupt has NOT occurred since the last read of this register.

Bit 3 - DS1 Channel 23 Loop-back Request Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS1 Channel 23 Loop-back Request” Interrupt.

Setting this bit to “0” disables this interrupt. Conversely, setting this bit to “1” enables this interrupt.

Bit 2 - DS1 Channel 22 Loop-back Request Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS1 Channel 22 Loop-back Request” Interrupt.

Setting this bit to “0” disables this interrupt. Conversely, setting this bit to “1” enables this interrupt.

Bit 1 - DS1 Channel 21 Loop-back Request Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS1 Channel 21 Loop-back Request” Interrupt.

Setting this bit to “0” disables this interrupt. Conversely, setting this bit to “1” enables this interrupt.

Bit 0 - DS1 Channel 20 Loop-back Request Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS1 Channel 20 Loop-back Request” Interrupt.

Setting this bit to “0” disables this interrupt. Conversely, setting this bit to “1” enables this interrupt.

2.3.2.110 M12 DS2 # 6 Loopback Status Register

M12 DS2 # 1 LOOP-BACK STATUS REGISTER (ADDRESS = 0X9E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				DS1 Channel # 24 Loopback Status	DS1 Channel # 23 Loopback Status	DS1 Channel # 22 Loopback Status	DS1 Channel # 21 Loopback Status
R/O	R/O	R/O	/RO	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

Bit 3 - DS1 Channel # 24 Loop-back Status

This “Read-Only” bit-field indicates whether or not a loop-back request has been detected for DS1 Channel # 24.

This bit-field will be set to “1” if a loop-back request has been detected for DS1 Channel # 24. Conversely, this bit-field will be set to “0” if a loop-back request has NOT been detected for DS1 Channel # 24.

NOTE: *This bit-field is invalid if the XRT72L13 M13 device is operating in the “ITU-T G.747” Mode.*

Bit 2 - DS1 Channel # 23 Loop-back Status

This “Read-Only” bit-field indicates whether or not a loop-back request has been detected for DS1 Channel # 23.

This bit-field will be set to “1” if a loop-back request has been detected for DS1 Channel # 23. Conversely, this bit-field will be set to “0” if a loop-back request has NOT been detected for DS1 Channel # 23.

Bit 1 - DS1 Channel # 22 Loop-back Status

This “Read-Only” bit-field indicates whether or not a loop-back request has been detected for DS1 Channel # 22.

This bit-field will be set to “1” if a loop-back request has been detected for DS1 Channel # 22. Conversely, this bit-field will be set to “0” if a loop-back request has NOT been detected for DS1 Channel # 22.

Bit 0 - DS1 Channel # 21 Loop-back Status

This “Read-Only” bit-field indicates whether or not a loop-back request has been detected for DS1 Channel # 21.

This bit-field will be set to “1” if a loop-back request has been detected for DS1 Channel # 21. Conversely, this bit-field will be set to “0” if a loop-back request has NOT been detected for DS1 Channel # 21.

2.3.2.111 M12 DS2 # 7 Loopback Interrupt/Interrupt Enable Register

M12 DS2 # 7 LOOP-BACK INTERRUPT/INTERRUPT ENABLE REGISTER (ADDRESS = 0X9F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DS1 Channel 27 Loop-back Request Interrupt Status	DS1 Channel 26 Loop-back Request Interrupt Status	DS1 Channel 25 Loop-back Request Interrupt Status	DS1 Channel 24 Loop-back Request Interrupt Status	DS1 Channel 27 Loop-backj Request Interrupt Enable	DS1 Channel 26 Loop-backj Request Interrupt Enable	DS1 Channel 25 Loop-backj Request Interrupt Enable	DS1 Channel 24 Loop-backj Request Interrupt Enable
RUR	RUR	RUR	RUR	R/W	R/W	R/W/	R/W
0	0	0	0	0	0	0	0

Bit 7 - DS1 Channel 27 Loop-back Request Interrupt Status

This “Reset-upon-Read” bit-field indicates whether the “DS1 Channel 27 Loop-back Request” interrupt has occurred or not.

This bit-field will be set to “1” if the “DS1 Channel 27 Loop-back Request Interrupt” has occurred since the last read of this register.

This bit-field will be set to “0” if the “DS1 Channel 27 Loop-back Request” interrupt has NOT occurred since the last read of this register.

NOTE: *This bit-field is ignored if the XRT72L13 is configured to operate in the “ITU-T G.747 Mode”.*

Bit 6 - DS1 Channel 26 Loop-back Request Interrupt Status

This “Reset-upon-Read” bit-field indicates whether the “DS1 Channel 26 Loop-back Request” interrupt has occurred or not.

This bit-field will be set to “1” if the “DS1 Channel 26 Loop-back Request Interrupt” has occurred since the last read of this register.

This bit-field will be set to “0” if the “DS1 Channel 26 Loop-back Request” interrupt has NOT occurred since the last read of this register.

Bit 5 - DS1 Channel 25 Loop-back Request Interrupt Status

This “Reset-upon-Read” bit-field indicates whether the “DS1 Channel 25 Loop-back Request” interrupt has occurred or not.

This bit-field will be set to “1” if the “DS1 Channel 25 Loop-back Request Interrupt” has occurred since the last read of this register.

This bit-field will be set to “0” if the “DS1 Channel 25 Loop-back Request” interrupt has NOT occurred since the last read of this register.

Bit 4 - DS1 Channel 24 Loop-back Request Interrupt Status

This “Reset-upon-Read” bit-field indicates whether the “DS1 Channel 24 Loop-back Request” interrupt has occurred or not.

This bit-field will be set to “1” if the “DS1 Channel 24 Loop-back Request Interrupt” has occurred since the last read of this register.

This bit-field will be set to “0” if the “DS1 Channel 24 Loop-back Request” interrupt has NOT occurred since the last read of this register.

Bit 3 - DS1 Channel 27 Loop-back Request Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS1 Channel 27 Loop-back Request” Interrupt.

Setting this bit to “0” disables this interrupt. Conversely, setting this bit to “1” enables this interrupt.

NOTE: *This bit-field is ignored if the XRT72L13 is configured to operate in the “ITU-T G.747 Mode”.*

Bit 2 - DS1 Channel 26 Loop-back Request Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS1 Channel 26 Loop-back Request” Interrupt.

Setting this bit to “0” disables this interrupt. Conversely, setting this bit to “1” enables this interrupt.

Bit 1 - DS1 Channel 25 Loop-back Request Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS1 Channel 25 Loop-back Request” Interrupt.

Setting this bit to “0” disables this interrupt. Conversely, setting this bit to “1” enables this interrupt.

Bit 0 - DS1 Channel 24 Loop-back Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS1 Channel 24 Loop-back Request” Interrupt.

Setting this bit to “0” disables this interrupt. Conversely, setting this bit to “1” enables this interrupt.

2.3.2.112 M12 DS2 # 7 Loopback Status Register

M12 DS2 # 1 LOOP-BACK STATUS REGISTER (ADDRESS = 0XA0)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				DS1 Channel # 27 Loopback Status	DS1 Channel # 26 Loopback Status	DS1 Channel # 25 Loopback Status	DS1 Channel # 24 Loopback Status
R/O	R/O	R/O	/RO	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

Bit 3 - DS1 Channel # 27 Loop-back Status

This “Read-Only” bit-field indicates whether or not a loop-back request has been detected for DS1 Channel # 27.

This bit-field will be set to “1” if a loop-back request has been detected for DS1 Channel # 27. Conversely, this bit-field will be set to “0” if a loop-back request has NOT been detected for DS1 Channel # 27.

NOTE: This bit-field is invalid if the XRT72L13 M13 device is operating in the “ITU-T G.747” Mode.

Bit 2 - DS1 Channel # 26 Loop-back Status

This “Read-Only” bit-field indicates whether or not a loop-back request has been detected for DS1 Channel # 26.

This bit-field will be set to “1” if a loop-back request has been detected for DS1 Channel # 26. Conversely, this bit-field will be set to “0” if a loop-back request has NOT been detected for DS1 Channel # 26.

Bit 1 - DS1 Channel # 25 Loop-back Status

This “Read-Only” bit-field indicates whether or not a loop-back request has been detected for DS1 Channel # 25.

This bit-field will be set to “1” if a loop-back request has been detected for DS1 Channel # 25. Conversely, this bit-field will be set to “0” if a loop-back request has NOT been detected for DS1 Channel # 25.

Bit 0 - DS1 Channel # 24 Loop-back Status

This “Read-Only” bit-field indicates whether or not a loop-back request has been detected for DS1 Channel # 24.

This bit-field will be set to “1” if a loop-back request has been detected for DS1 Channel # 24. Conversely, this bit-field will be set to “0” if a loop-back request has NOT been detected for DS1 Channel # 24.

2.3.2.113 DS2 # 1 Framer Interrupt Enable Register

DS2 # 1 FRAMER INTERRUPT ENABLE REGISTER (ADDRESS = 0XA1)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		DS2 COFA Interrupt Enable	DS2 OOF Interrupt Enable	DS2 FERF Interrupt Enable	DS2 RED Alarm Interrupt Enable	DS2 AIS Interrupt Enable	DS2 RESV Interrupt Enable
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit 5 - DS2 COFA (Change of Framing Alignment) Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS2 Change of Framing Alignment” Interrupt.

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Bit 4 - DS2 OOF (Out of Frame) Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS2 Out of Frame” interrupt.

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Bit 3 - DS2 FERF (Far-End-Receive Failure) Interrupt Enable.

This “Read/Write” bit-field permits the user to enable or disable the “DS2 Far-End Receive Failure” Interrupt.

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Bit 2 - DS2 RED Alarm Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS2 RED Alarm” Interrupt.

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Bit 1 - DS2 AIS Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS2 AIS” Interrupt.

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Bit 0 - DS2 RESV Interrupt Enable.

To be provided in the next update.

2.3.2.114 DS2 # 1 Framer Interrupt Register

DS2 # 1 FRAMER INTERRUPT REGISTER (ADDRESS = 0XA2)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		Change in DS2 COFA Interrupt Status	Change in DS2 OOF Interrupt Status	Change in DS2 FERF Interrupt Status	Change in DS2 RED Alarm Interrupt Status	Change in DS2 AIS Interrupt Status	Change in DS2 RESV Interrupt Status
R/O	R/O	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

Bit 5 - Change in DS2 COFA (Change of Framing Alignment) Interrupt Status

This “Reset-upon-Read” bit-field indicates whether or not a change in the “DS2 COFA State” has occurred since the last read of this register.

This bit-field will be set to “1” if a change in the DS2 COFA State has occurred since the last read of this register. Conversely, this bit-field will be set to “0” if a change in the DS2 COFA State has NOT occurred since the last read of this register.

Bit 4 - Change in DS2 OOF (Out-of-Frame) Interrupt Status

This “Reset-upon-Read” bit-field indicates whether or not a change in the “DS2 Out-of-Frame State” has occurred since the last read of this register.

This bit-field will be set to “1” if a change in the DS2 OOF State has occurred since the last read of this register. Conversely, this bit-field will be set to “0” if a change in the DS2 OOF State has NOT occurred since the last read of this register.

Bit 3 - Change in DS2 FERF (Far-End Receive Failure) Interrupt Status

This “Reset-upon-Read” bit-field indicates whether or not a change in the “DS2 FERF State” has occurred since the last read of this register.

This bit-field will be set to “1” if a change in the DS2 FERF State has occurred since the last read of this register. Conversely, this bit-field will be set to “0” if a change in the DS2 FERF State has NOT occurred since the last read of this register.

Bit 2 - Change in DS2 RED Alarm Interrupt Status

This “Reset-upon-Read” bit-field indicates whether or not a change in the “DS2 RED Alarm State” has occurred since the last read of this register.

This bit-field will be set to “1” if a change in the DS2 RED Alarm State has occurred since the last read of this register. Conversely, this bit-field will be set to “0” if a change in the DS2 RED Alarm State has NOT occurred since the last read of this register.

Bit 1 - Change in DS2 AIS Interrupt Status

This “Reset-upon-Read” bit-field indicates whether or not a change in the “DS2 AIS State” has occurred since the last read of this register.

This bit-field will be set to “1” if a change in the DS2 AIS State has occurred since the last read of this register. Conversely, this bit-field will be set to “0” if a change in the DS2 AIS State has NOT occurred since the last read of this register.

Bit 0 - Change in DS2 RESV Interrupt Status

To be provided in the next update.

2.3.2.115 DS2 # 1 Framer Status Register

DS2 # 1 FRAMER STATUS REGISTER (ADDRESS = 0XA3)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		DS2 COFA Status	DS2 OOF Status	DS2 FERF Status	DS2 RED Alarm Status	DS2 AIS Status	DS2 RESV Status
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit 5 - DS2 COFA (Change of Framing Alignment) Status

This “Read-Only” bit-field reflects the current “COFA” status of DS2 Channel # 1.

This bit-field will be set to “0” is there is no “Change of Framing Alignment” in DS2 Channel # 1. Conversely, this bit-field will be set to “1” is there is a “Change of Framing Alignment” in DS2 Channel # 1.

Bit 4 - DS2 OOF (Out-of-Frame) Status

This “Read-Only” bit-field reflects the current “OOF” status of DS2 Channel # 1.

This bit-field will be set to “0” if DS2 Channel # 1 is currently in the “In-Frame” condition. Conversely, this bit-field will be set to “1” if DS2 Channel # 1 is currently declaring an “Out-of-Frame” condtion.

Bit 3 - DS2 FERF (Far-End Receive Failure) Status

his “Read-Only” bit-field reflects the current “FERF” status of DS2 Channel # 1.

This bit-field will be set to “0” if DS2 Channel # 1 is currently not declaring the “FERF” condition. Conversely, this bit-field will be set to “1” if DS2 Channel # 1 is currently declaring a “FERF” condtion.

Bit 2 - DS2 RED Alarm Status

This “Read-Only” bit-field reflects the current “RED Alarm” status of DS2 Channel # 1.

This bit-field will be set to “0” if DS2 Channel # 1 is not currently declaring a “RED Alarm” condition. Conversely, this bit-field will be set to “1” if DS2 Channel # 1 is currently declaring a “RED Alarm” condition.

Bit 1 - DS2 AIS (Alarm Indication Signal) Status

This “Read-Only” bit-field reflects the current “AIS” status of DS2 Channel # 1.

This bit-field will be set to “0” if DS2 Channel # 1 is not currently declaring an “AIS” condition. Conversely, this bit-field will be set to “1” if DS2 Channel # 1 is currently declaring an “AIS” condition.

Bit 0 - DS2 RESV Status

To be provided in the next update.

2.3.2.116 DS2 # 2 Framer Interrupt Enable Register

DS2 # 2 FRAMER INTERRUPT ENABLE REGISTER (ADDRESS = 0XA4)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		DS2 COFA Interrupt Enable	DS2 OOF Interrupt Enable	DS2 FERF Interrupt Enable	DS2 RED Alarm Interrupt Enable	DS2 AIS Interrupt Enable	DS2 RESV Interrupt Enable
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit 5 - DS2 COFA (Change of Framing Alignment) Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS2 Change of Framing Alignment” Interrupt.

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Bit 4 - DS2 OOF (Out of Frame) Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS2 Out of Frame” interrupt.

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Bit 3 - DS2 FERF (Far-End-Receive Failure) Interrupt Enable.

This “Read/Write” bit-field permits the user to enable or disable the “DS2 Far-End Receive Failure” Interrupt.

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Bit 2 - DS2 RED Alarm Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS2 RED Alarm” Interrupt.

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Bit 1 - DS2 AIS Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS2 AIS” Interrupt.

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Bit 0 - DS2 RESV Interrupt Enable.

To be provided in the next update.

2.3.2.117 DS2 # 2 Framer Interrupt Register

DS2 # 2 FRAMER INTERRUPT REGISTER (ADDRESS = 0XA5)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		Change in DS2 COFA Interrupt Enable	Change in DS2 OOF Interrupt Enable	Change in DS2 FERF Interrupt Enable	Change in DS2 RED Alarm Interrupt Enable	Change in DS2 AIS Interrupt Enable	Change in DS2 RESV Interrupt Enable
R/O	R/O	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

Bit 5 - Change in DS2 COFA (Change of Framing Alignment) Interrupt Status

This “Reset-upon-Read” bit-field indicates whether or not a change in the “DS2 COFA State” has occurred since the last read of this register.

This bit-field will be set to “1” if a change in the DS2 COFA State has occurred since the last read of this register. Conversely, this bit-field will be set to “0” if a change in the DS2 COFA State has NOT occurred since the last read of this register.

Bit 4 - Change in DS2 OOF (Out-of-Frame) Interrupt Status

This “Reset-upon-Read” bit-field indicates whether or not a change in the “DS2 Out-of-Frame State” has occurred since the last read of this register.

This bit-field will be set to “1” if a change in the DS2 OOF State has occurred since the last read of this register. Conversely, this bit-field will be set to “0” if a change in the DS2 OOF State has NOT occurred since the last read of this register.

Bit 3 - Change in DS2 FERF (Far-End Receive Failure) Interrupt Status

This “Reset-upon-Read” bit-field indicates whether or not a change in the “DS2 FERF State” has occurred since the last read of this register.

This bit-field will be set to “1” if a change in the DS2 FERF State has occurred since the last read of this register. Conversely, this bit-field will be set to “0” if a change in the DS2 FERF State has NOT occurred since the last read of this register.

Bit 2 - Change in DS2 RED Alarm Interrupt Status

This “Reset-upon-Read” bit-field indicates whether or not a change in the “DS2 RED Alarm State” has occurred since the last read of this register.

This bit-field will be set to “1” if a change in the DS2 RED Alarm State has occurred since the last read of this register. Conversely, this bit-field will be set to “0” if a change in the DS2 RED Alarm State has NOT occurred since the last read of this register.

Bit 1 - Change in DS2 AIS Interrupt Status

This “Reset-upon-Read” bit-field indicates whether or not a change in the “DS2 AIS State” has occurred since the last read of this register.

This bit-field will be set to “1” if a change in the DS2 AIS State has occurred since the last read of this register. Conversely, this bit-field will be set to “0” if a change in the DS2 AIS State has NOT occurred since the last read of this register.

Bit 0 - Change in DS2 RESV Interrupt Status

To be provided in the next update.

2.3.2.118 DS2 # 2 Framer Status Register

DS2 # 2 FRAMER STATUS REGISTER (ADDRESS = 0XA6)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		DS2 COFA Status	DS2 OOF Status	DS2 FERF Status	DS2 RED Alarm Status	DS2 AIS Status	DS2 RESV Status
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit 5 - DS2 COFA (Change of Framing Alignment) Status

This “Read-Only” bit-field reflects the current “COFA” status of DS2 Channel # 2.

This bit-field will be set to “0” is there is no “Change of Framing Alignment” in DS2 Channel # 2. Conversely, this bit-field will be set to “1” is there is a “Change of Framing Alignment” in DS2 Channel # 2.

Bit 4 - DS2 OOF (Out-of-Frame) Status

This “Read-Only” bit-field reflects the current “OOF” status of DS2 Channel # 2.

This bit-field will be set to “0” if DS2 Channel # 2 is currently in the “In-Frame” condition. Conversely, this bit-field will be set to “1” if DS2 Channel # 2 is currently declaring an “Out-of-Frame” condtion.

Bit 3 - DS2 FERF (Far-End Receive Failure) Status

his “Read-Only” bit-field reflects the current “FERF” status of DS2 Channel # 2.

This bit-field will be set to “0” if DS2 Channel # 2 is currently not declaring the “FERF” condition. Conversely, this bit-field will be set to “1” if DS2 Channel # 2 is currently declaring a “FERF” condtion.

Bit 2 - DS2 RED Alarm Status

This “Read-Only” bit-field reflects the current “RED Alarm” status of DS2 Channel # 2.

This bit-field will be set to “0” if DS2 Channel # 2 is not currently declaring a “RED Alarm” condition. Conversely, this bit-field will be set to “1” if DS2 Channel # 1 is currently declaring a “RED Alarm” condition.

Bit 1 - DS2 AIS (Alarm Indication Signal) Status

This “Read-Only” bit-field reflects the current “AIS” status of DS2 Channel # 2.

This bit-field will be set to “0” if DS2 Channel # 2 is not currently declaring an “AIS” condition. Conversely, this bit-field will be set to “1” if DS2 Channel # 2 is currently declaring an “AIS” condition.

Bit 0 - DS2 RESV Status

To be provided in the next update.

2.3.2.119 DS2 # 3 Framer Interrupt Enable Register

DS2 # 3 FRAMER INTERRUPT ENABLE REGISTER (ADDRESS = 0XA7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		DS2 COFA Interrupt Enable	DS2 OOF Interrupt Enable	DS2 FERF Interrupt Enable	DS2 RED Alarm Interrupt Enable	DS2 AIS Interrupt Enable	DS2 RESV Interrupt Enable
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit 5 - DS2 COFA (Change of Framing Alignment) Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS2 Change of Framing Alignment” Interrupt.

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Bit 4 - DS2 OOF (Out of Frame) Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS2 Out of Frame” interrupt.

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Bit 3 - DS2 FERF (Far-End-Receive Failure) Interrupt Enable.

This “Read/Write” bit-field permits the user to enable or disable the “DS2 Far-End Receive Failure” Interrupt.

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Bit 2 - DS2 RED Alarm Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS2 RED Alarm” Interrupt.

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Bit 1 - DS2 AIS Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS2 AIS” Interrupt.

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Bit 0 - DS2 RESV Interrupt Enable.

To be provided in the next update.

2.3.2.120 DS2 # 3 Framer Interrupt Register

DS2 # 3 FRAMER INTERRUPT REGISTER (ADDRESS = 0XA8)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		Change in DS2 COFA Interrupt Enable	Change in DS2 OOF Interrupt Enable	Change in DS2 FERF Interrupt Enable	Change in DS2 RED Alarm Interrupt Enable	Change in DS2 AIS Interrupt Enable	Change in DS2 RESV Interrupt Enable
R/O	R/O	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

Bit 5 - Change in DS2 COFA (Change of Framing Alignment) Interrupt Status

This “Reset-upon-Read” bit-field indicates whether or not a change in the “DS2 COFA State” has occurred since the last read of this register.

This bit-field will be set to “1” if a change in the DS2 COFA State has occurred since the last read of this register. Conversely, this bit-field will be set to “0” if a change in the DS2 COFA State has NOT occurred since the last read of this register.

Bit 4 - Change in DS2 OOF (Out-of-Frame) Interrupt Status

This “Reset-upon-Read” bit-field indicates whether or not a change in the “DS2 Out-of-Frame State” has occurred since the last read of this register.

This bit-field will be set to “1” if a change in the DS2 OOF State has occurred since the last read of this register. Conversely, this bit-field will be set to “0” if a change in the DS2 OOF State has NOT occurred since the last read of this register.

Bit 3 - Change in DS2 FERF (Far-End Receive Failure) Interrupt Status

This “Reset-upon-Read” bit-field indicates whether or not a change in the “DS2 FERF State” has occurred since the last read of this register.

This bit-field will be set to “1” if a change in the DS2 FERF State has occurred since the last read of this register. Conversely, this bit-field will be set to “0” if a change in the DS2 FERF State has NOT occurred since the last read of this register.

Bit 2 - Change in DS2 RED Alarm Interrupt Status

This “Reset-upon-Read” bit-field indicates whether or not a change in the “DS2 RED Alarm State” has occurred since the last read of this register.

This bit-field will be set to “1” if a change in the DS2 RED Alarm State has occurred since the last read of this register. Conversely, this bit-field will be set to “0” if a change in the DS2 RED Alarm State has NOT occurred since the last read of this register.

Bit 1 - Change in DS2 AIS Interrupt Status

This “Reset-upon-Read” bit-field indicates whether or not a change in the “DS2 AIS State” has occurred since the last read of this register.

This bit-field will be set to “1” if a change in the DS2 AIS State has occurred since the last read of this register. Conversely, this bit-field will be set to “0” if a change in the DS2 AIS State has NOT occurred since the last read of this register.

Bit 0 - Change in DS2 RESV Interrupt Status

To be provided in the next update.

2.3.2.121 DS2 # 3 Framer Status Register

DS2 # 3 FRAMER STATUS REGISTER (ADDRESS = 0XA9)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		DS2 COFA Status	DS2 OOF Status	DS2 FERF Status	DS2 RED Alarm Status	DS2 AIS Status	DS2 RESV Status
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit 5 - DS2 COFA (Change of Framing Alignment) Status

This “Read-Only” bit-field reflects the current “COFA” status of DS2 Channel # 3.

This bit-field will be set to “0” is there is no “Change of Framing Alignment” in DS2 Channel # 3. Conversely, this bit-field will be set to “1” is there is a “Change of Framing Alignment” in DS2 Channel # 3.

Bit 4 - DS2 OOF (Out-of-Frame) Status

This “Read-Only” bit-field reflects the current “OOF” status of DS2 Channel # 3.

This bit-field will be set to “0” if DS2 Channel # 3 is currently in the “In-Frame” condition. Conversely, this bit-field will be set to “1” if DS2 Channel # 3 is currently declaring an “Out-of-Frame” condtion.

Bit 3 - DS2 FERF (Far-End Receive Failure) Status

his “Read-Only” bit-field reflects the current “FERF” status of DS2 Channel # 3.

This bit-field will be set to “0” if DS2 Channel # 3 is currently not declaring the “FERF” condition. Conversely, this bit-field will be set to “1” if DS2 Channel # 1 is currently declaring a “FERF” condtion.

Bit 2 - DS2 RED Alarm Status

This “Read-Only” bit-field reflects the current “RED Alarm” status of DS2 Channel # 3.

This bit-field will be set to “0” if DS2 Channel # 3 is not currently declaring a “RED Alarm” condition. Conversely, this bit-field will be set to “1” if DS2 Channel # 3 is currently declaring a “RED Alarm” condition.

Bit 1 - DS2 AIS (Alarm Indication Signal) Status

This “Read-Only” bit-field reflects the current “AIS” status of DS2 Channel # 3.

This bit-field will be set to “0” if DS2 Channel # 3 is not currently declaring an “AIS” condition. Conversely, this bit-field will be set to “1” if DS2 Channel # 3 is currently declaring an “AIS” condition.

Bit 0 - DS2 RESV Status

To be provided in the next update.

2.3.2.122 DS2 # 4 Framer Interrupt Enable Register

DS2 # 4 FRAMER INTERRUPT ENABLE REGISTER (ADDRESS = 0XAA)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		DS2 COFA Interrupt Enable	DS2 OOF Interrupt Enable	DS2 FERF Interrupt Enable	DS2 RED Alarm Interrupt Enable	DS2 AIS Interrupt Enable	DS2 RESV Interrupt Enable
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit 5 - DS2 COFA (Change of Framing Alignment) Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS2 Change of Framing Alignment” Interrupt.

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Bit 4 - DS2 OOF (Out of Frame) Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS2 Out of Frame” interrupt.

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Bit 3 - DS2 FERF (Far-End-Receive Failure) Interrupt Enable.

This “Read/Write” bit-field permits the user to enable or disable the “DS2 Far-End Receive Failure” Interrupt.

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Bit 2 - DS2 RED Alarm Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS2 RED Alarm” Interrupt.

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Bit 1 - DS2 AIS Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS2 AIS” Interrupt.

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Bit 0 - DS2 RESV Interrupt Enable.

To be provided in the next update.

2.3.2.123 DS2 # 4 Framer Interrupt Register

DS2 # 4 FRAMER INTERRUPT ENABLE REGISTER (ADDRESS = 0XAB)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		Change in DS2 COFA Interrupt Enable	Change in DS2 OOF Interrupt Enable	Change in DS2 FERF Interrupt Enable	Change in DS2 RED Alarm Interrupt Enable	Change in DS2 AIS Interrupt Enable	Change in DS2 RESV Interrupt Enable
R/O	R/O	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

Bit 5 - Change in DS2 COFA (Change of Framing Alignment) Interrupt Status

This “Reset-upon-Read” bit-field indicates whether or not a change in the “DS2 COFA State” has occurred since the last read of this register.

This bit-field will be set to “1” if a change in the DS2 COFA State has occurred since the last read of this register. Conversely, this bit-field will be set to “0” if a change in the DS2 COFA State has NOT occurred since the last read of this register.

Bit 4 - Change in DS2 OOF (Out-of-Frame) Interrupt Status

This “Reset-upon-Read” bit-field indicates whether or not a change in the “DS2 Out-of-Frame State” has occurred since the last read of this register.

This bit-field will be set to “1” if a change in the DS2 OOF State has occurred since the last read of this register. Conversely, this bit-field will be set to “0” if a change in the DS2 OOF State has NOT occurred since the last read of this register.

Bit 3 - Change in DS2 FERF (Far-End Receive Failure) Interrupt Status

This “Reset-upon-Read” bit-field indicates whether or not a change in the “DS2 FERF State” has occurred since the last read of this register.

This bit-field will be set to “1” if a change in the DS2 FERF State has occurred since the last read of this register. Conversely, this bit-field will be set to “0” if a change in the DS2 FERF State has NOT occurred since the last read of this register.

Bit 2 - Change in DS2 RED Alarm Interrupt Status

This “Reset-upon-Read” bit-field indicates whether or not a change in the “DS2 RED Alarm State” has occurred since the last read of this register.

This bit-field will be set to “1” if a change in the DS2 RED Alarm State has occurred since the last read of this register. Conversely, this bit-field will be set to “0” if a change in the DS2 RED Alarm State has NOT occurred since the last read of this register.

Bit 1 - Change in DS2 AIS Interrupt Status

This “Reset-upon-Read” bit-field indicates whether or not a change in the “DS2 AIS State” has occurred since the last read of this register.

This bit-field will be set to “1” if a change in the DS2 AIS State has occurred since the last read of this register. Conversely, this bit-field will be set to “0” if a change in the DS2 AIS State has NOT occurred since the last read of this register.

Bit 0 - Change in DS2 RESV Interrupt Status

To be provided in the next update.

2.3.2.124 DS2 # 4 Framer Status Register

DS2 # 4 FRAMER STATUS REGISTER (ADDRESS = 0XAC)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		DS2 COFA Status	DS2 OOF Status	DS2 FERF Status	DS2 RED Alarm Status	DS2 AIS Status	DS2 RESV Status
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit 5 - DS2 COFA (Change of Framing Alignment) Status

This “Read-Only” bit-field reflects the current “COFA” status of DS2 Channel # 4.

This bit-field will be set to “0” is there is no “Change of Framing Alignment” in DS2 Channel # 4. Conversely, this bit-field will be set to “1” is there is a “Change of Framing Alignment” in DS2 Channel # 4.

Bit 4 - DS2 OOF (Out-of-Frame) Status

This “Read-Only” bit-field reflects the current “OOF” status of DS2 Channel # 4.

This bit-field will be set to “0” if DS2 Channel # 4 is currently in the “In-Frame” condition. Conversely, this bit-field will be set to “1” if DS2 Channel # 4 is currently declaring an “Out-of-Frame” condtion.

Bit 3 - DS2 FERF (Far-End Receive Failure) Status

his “Read-Only” bit-field reflects the current “FERF” status of DS2 Channel # 4.

This bit-field will be set to “0” if DS2 Channel # 4 is currently not declaring the “FERF” condition. Conversely, this bit-field will be set to “1” if DS2 Channel # 4 is currently declaring a “FERF” condtion.

Bit 2 - DS2 RED Alarm Status

This “Read-Only” bit-field reflects the current “RED Alarm” status of DS2 Channel # 4.

This bit-field will be set to “0” if DS2 Channel # 4 is not currently declaring a “RED Alarm” condition. Conversely, this bit-field will be set to “1” if DS2 Channel # 4 is currently declaring a “RED Alarm” condition.

Bit 1 - DS2 AIS (Alarm Indication Signal) Status

This “Read-Only” bit-field reflects the current “AIS” status of DS2 Channel # 4.

This bit-field will be set to “0” if DS2 Channel # 4 is not currently declaring an “AIS” condition. Conversely, this bit-field will be set to “1” if DS2 Channel # 4 is currently declaring an “AIS” condition.

Bit 0 - DS2 RESV Status

To be provided in the next update.

2.3.2.125 DS2 # 5 Framer Interrupt Enable Register

DS2 # 5 FRAMER INTERRUPT ENABLE REGISTER (ADDRESS = 0XAD)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		DS2 COFA Interrupt Enable	DS2 OOF Interrupt Enable	DS2 FERF Interrupt Enable	DS2 RED Alarm Interrupt Enable	DS2 AIS Interrupt Enable	DS2 RESV Interrupt Enable
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit 5 - DS2 COFA (Change of Framing Alignment) Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS2 Change of Framing Alignment” Interrupt.

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Bit 4 - DS2 OOF (Out of Frame) Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS2 Out of Frame” interrupt.

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Bit 3 - DS2 FERF (Far-End-Receive Failure) Interrupt Enable.

This “Read/Write” bit-field permits the user to enable or disable the “DS2 Far-End Receive Failure” Interrupt.

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Bit 2 - DS2 RED Alarm Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS2 RED Alarm” Interrupt.

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Bit 1 - DS2 AIS Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS2 AIS” Interrupt.

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Bit 0 - DS2 RESV Interrupt Enable.

To be provided in the next update.

2.3.2.126 DS2 # 5 Framer Interrupt Register

DS2 # 5 FRAMER INTERRUPT ENABLE REGISTER (ADDRESS = 0XAF)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		Change in DS2 COFA Interrupt Enable	Change in DS2 OOF Interrupt Enable	Change in DS2 FERF Interrupt Enable	Change in DS2 RED Alarm Interrupt Enable	Change in DS2 AIS Interrupt Enable	Change in DS2 RESV Interrupt Enable
R/O	R/O	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

Bit 5 - Change in DS2 COFA (Change of Framing Alignment) Interrupt Status

This “Reset-upon-Read” bit-field indicates whether or not a change in the “DS2 COFA State” has occurred since the last read of this register.

This bit-field will be set to “1” if a change in the DS2 COFA State has occurred since the last read of this register. Conversely, this bit-field will be set to “0” if a change in the DS2 COFA State has NOT occurred since the last read of this register.

Bit 4 - Change in DS2 OOF (Out-of-Frame) Interrupt Status

This “Reset-upon-Read” bit-field indicates whether or not a change in the “DS2 Out-of-Frame State” has occurred since the last read of this register.

This bit-field will be set to “1” if a change in the DS2 OOF State has occurred since the last read of this register. Conversely, this bit-field will be set to “0” if a change in the DS2 OOF State has NOT occurred since the last read of this register.

Bit 3 - Change in DS2 FERF (Far-End Receive Failure) Interrupt Status

This “Reset-upon-Read” bit-field indicates whether or not a change in the “DS2 FERF State” has occurred since the last read of this register.

This bit-field will be set to “1” if a change in the DS2 FERF State has occurred since the last read of this register. Conversely, this bit-field will be set to “0” if a change in the DS2 FERF State has NOT occurred since the last read of this register.

Bit 2 - Change in DS2 RED Alarm Interrupt Status

This “Reset-upon-Read” bit-field indicates whether or not a change in the “DS2 RED Alarm State” has occurred since the last read of this register.

This bit-field will be set to “1” if a change in the DS2 RED Alarm State has occurred since the last read of this register. Conversely, this bit-field will be set to “0” if a change in the DS2 RED Alarm State has NOT occurred since the last read of this register.

Bit 1 - Change in DS2 AIS Interrupt Status

This “Reset-upon-Read” bit-field indicates whether or not a change in the “DS2 AIS State” has occurred since the last read of this register.

This bit-field will be set to “1” if a change in the DS2 AIS State has occurred since the last read of this register. Conversely, this bit-field will be set to “0” if a change in the DS2 AIS State has NOT occurred since the last read of this register.

Bit 0 - Change in DS2 RESV Interrupt Status

To be provided in the next update.

2.3.2.127 DS2 # 5 Framer Status Register

DS2 # 5 FRAMER STATUS REGISTER (ADDRESS = 0XAF)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		DS2 COFA Status	DS2 OOF Status	DS2 FERF Status	DS2 RED Alarm Status	DS2 AIS Status	DS2 RESV Status
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit 5 - DS2 COFA (Change of Framing Alignment) Status

This “Read-Only” bit-field reflects the current “COFA” status of DS2 Channel # 5.

This bit-field will be set to “0” is there is no “Change of Framing Alignment” in DS2 Channel # 5. Conversely, this bit-field will be set to “1” is there is a “Change of Framing Alignment” in DS2 Channel # 5.

Bit 4 - DS2 OOF (Out-of-Frame) Status

This “Read-Only” bit-field reflects the current “OOF” status of DS2 Channel # 5.

This bit-field will be set to “0” if DS2 Channel # 5 is currently in the “In-Frame” condition. Conversely, this bit-field will be set to “1” if DS2 Channel # 5 is currently declaring an “Out-of-Frame” condtion.

Bit 3 - DS2 FERF (Far-End Receive Failure) Status

his “Read-Only” bit-field reflects the current “FERF” status of DS2 Channel # 5.

This bit-field will be set to “0” if DS2 Channel # 5 is currently not declaring the “FERF” condition. Conversely, this bit-field will be set to “1” if DS2 Channel # 5 is currently declaring a “FERF” condtion.

Bit 2 - DS2 RED Alarm Status

This “Read-Only” bit-field reflects the current “RED Alarm” status of DS2 Channel # 5.

This bit-field will be set to “0” if DS2 Channel # 5 is not currently declaring a “RED Alarm” condition. Conversely, this bit-field will be set to “1” if DS2 Channel # 5 is currently declaring a “RED Alarm” condition.

Bit 1 - DS2 AIS (Alarm Indication Signal) Status

This “Read-Only” bit-field reflects the current “AIS” status of DS2 Channel # 5.

This bit-field will be set to “0” if DS2 Channel # 5 is not currently declaring an “AIS” condition. Conversely, this bit-field will be set to “1” if DS2 Channel # 5 is currently declaring an “AIS” condition.

Bit 0 - DS2 RESV Status

To be provided in the next update.

2.3.2.128 DS2 # 6 Framer Interrupt Enable Register

DS2 # 6 FRAMER INTERRUPT ENABLE REGISTER (ADDRESS = 0XB0)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		DS2 COFA Interrupt Enable	DS2 OOF Interrupt Enable	DS2 FERF Interrupt Enable	DS2 RED Alarm Interrupt Enable	DS2 AIS Interrupt Enable	DS2 RESV Interrupt Enable
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit 5 - DS2 COFA (Change of Framing Alignment) Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS2 Change of Framing Alignment” Interrupt.

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Bit 4 - DS2 OOF (Out of Frame) Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS2 Out of Frame” interrupt.

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Bit 3 - DS2 FERF (Far-End-Receive Failure) Interrupt Enable.

This “Read/Write” bit-field permits the user to enable or disable the “DS2 Far-End Receive Failure” Interrupt.

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Bit 2 - DS2 RED Alarm Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS2 RED Alarm” Interrupt.

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Bit 1 - DS2 AIS Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS2 AIS” Interrupt.

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Bit 0 - DS2 RESV Interrupt Enable.

To be provided in the next update.

2.3.2.129 DS2 # 6 Framer Interrupt Register

DS2 # 6 FRAMER INTERRUPT REGISTER (ADDRESS = 0XB2)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		Change in DS2 COFA Interrupt Enable	Change in DS2 OOF Interrupt Enable	Change in DS2 FERF Interrupt Enable	Change in DS2 RED Alarm Interrupt Enable	Change in DS2 AIS Interrupt Enable	Change in DS2 RESV Interrupt Enable
R/O	R/O	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

Bit 5 - Change in DS2 COFA (Change of Framing Alignment) Interrupt Status

This “Reset-upon-Read” bit-field indicates whether or not a change in the “DS2 COFA State” has occurred since the last read of this register.

This bit-field will be set to “1” if a change in the DS2 COFA State has occurred since the last read of this register. Conversely, this bit-field will be set to “0” if a change in the DS2 COFA State has NOT occurred since the last read of this register.

Bit 4 - Change in DS2 OOF (Out-of-Frame) Interrupt Status

This “Reset-upon-Read” bit-field indicates whether or not a change in the “DS2 Out-of-Frame State” has occurred since the last read of this register.

This bit-field will be set to “1” if a change in the DS2 OOF State has occurred since the last read of this register. Conversely, this bit-field will be set to “0” if a change in the DS2 OOF State has NOT occurred since the last read of this register.

Bit 3 - Change in DS2 FERF (Far-End Receive Failure) Interrupt Status

This “Reset-upon-Read” bit-field indicates whether or not a change in the “DS2 FERF State” has occurred since the last read of this register.

This bit-field will be set to “1” if a change in the DS2 FERF State has occurred since the last read of this register. Conversely, this bit-field will be set to “0” if a change in the DS2 FERF State has NOT occurred since the last read of this register.

Bit 2 - Change in DS2 RED Alarm Interrupt Status

This “Reset-upon-Read” bit-field indicates whether or not a change in the “DS2 RED Alarm State” has occurred since the last read of this register.

This bit-field will be set to “1” if a change in the DS2 RED Alarm State has occurred since the last read of this register. Conversely, this bit-field will be set to “0” if a change in the DS2 RED Alarm State has NOT occurred since the last read of this register.

Bit 1 - Change in DS2 AIS Interrupt Status

This “Reset-upon-Read” bit-field indicates whether or not a change in the “DS2 AIS State” has occurred since the last read of this register.

This bit-field will be set to “1” if a change in the DS2 AIS State has occurred since the last read of this register. Conversely, this bit-field will be set to “0” if a change in the DS2 AIS State has NOT occurred since the last read of this register.

Bit 0 - Change in DS2 RESV Interrupt Status

To be provided in the next update.

2.3.2.130 DS2 # 6 Framer Status Register

DS2 # 6 FRAMER STATUS REGISTER (ADDRESS = 0XB2)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		DS2 COFA Status	DS2 OOF Status	DS2 FERF Status	DS2 RED Alarm Status	DS2 AIS Status	DS2 RESV Status
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit 5 - DS2 COFA (Change of Framing Alignment) Status

This “Read-Only” bit-field reflects the current “COFA” status of DS2 Channel # 6.

This bit-field will be set to “0” is there is no “Change of Framing Alignment” in DS2 Channel # 6. Conversely, this bit-field will be set to “1” is there is a “Change of Framing Alignment” in DS2 Channel # 6.

Bit 4 - DS2 OOF (Out-of-Frame) Status

This “Read-Only” bit-field reflects the current “OOF” status of DS2 Channel # 6.

This bit-field will be set to “0” if DS2 Channel # 6 is currently in the “In-Frame” condition. Conversely, this bit-field will be set to “1” if DS2 Channel # 6 is currently declaring an “Out-of-Frame” condtion.

Bit 3 - DS2 FERF (Far-End Receive Failure) Status

his “Read-Only” bit-field reflects the current “FERF” status of DS2 Channel # 6.

This bit-field will be set to “0” if DS2 Channel # 6 is currently not declaring the “FERF” condition. Conversely, this bit-field will be set to “1” if DS2 Channel # 1 is currently declaring a “FERF” condtion.

Bit 2 - DS2 RED Alarm Status

This “Read-Only” bit-field reflects the current “RED Alarm” status of DS2 Channel # 6.

This bit-field will be set to “0” if DS2 Channel # 6 is not currently declaring a “RED Alarm” condition. Conversely, this bit-field will be set to “1” if DS2 Channel # 6 is currently declaring a “RED Alarm” condition.

Bit 1 - DS2 AIS (Alarm Indication Signal) Status

This “Read-Only” bit-field reflects the current “AIS” status of DS2 Channel # 6.

This bit-field will be set to “0” if DS2 Channel # 6 is not currently declaring an “AIS” condition. Conversely, this bit-field will be set to “1” if DS2 Channel # 6 is currently declaring an “AIS” condition.

Bit 0 - DS2 RESV Status

To be provided in the next update.

2.3.2.131 DS2 # 7 Framer Interrupt Enable Register

DS2 # 7 FRAMER INTERRUPT ENABLE REGISTER (ADDRESS = 0XB3)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		DS2 COFA Interrupt Enable	DS2 OOF Interrupt Enable	DS2 FERF Interrupt Enable	DS2 RED Alarm Interrupt Enable	DS2 AIS Interrupt Enable	DS2 RESV Interrupt Enable
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit 5 - DS2 COFA (Change of Framing Alignment) Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS2 Change of Framing Alignment” Interrupt.

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Bit 4 - DS2 OOF (Out of Frame) Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS2 Out of Frame” interrupt.

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Bit 3 - DS2 FERF (Far-End-Receive Failure) Interrupt Enable.

This “Read/Write” bit-field permits the user to enable or disable the “DS2 Far-End Receive Failure” Interrupt.

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Bit 2 - DS2 RED Alarm Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS2 RED Alarm” Interrupt.

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Bit 1 - DS2 AIS Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “DS2 AIS” Interrupt.

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Bit 0 - DS2 RESV Interrupt Enable.

To be provided in the next update.

2.3.2.132 DS2 # 7 Framer Interrupt Register

DS2 # 7 FRAMER INTERRUPT REGISTER (ADDRESS = 0XB5)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		Change in DS2 COFA Interrupt Enable	Change in DS2 OOF Interrupt Enable	Change in DS2 FERF Interrupt Enable	Change in DS2 RED Alarm Interrupt Enable	Change in DS2 AIS Interrupt Enable	Change in DS2 RESV Interrupt Enable
R/O	R/O	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

2.3.2.133 DS2 # 7 Framer Status Register

DS2 # 7 FRAMER STATUS REGISTER (ADDRESS = 0XB5)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		DS2 COFA Status	DS2 OOF Status	DS2 FERF Status	DS2 RED Alarm Status	DS2 AIS Status	DS2 RESV Status
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit 5 - DS2 COFA (Change of Framing Alignment) Status

This “Read-Only” bit-field reflects the current “COFA” status of DS2 Channel # 7.

This bit-field will be set to “0” is there is no “Change of Framing Alignment” in DS2 Channel # 7. Conversely, this bit-field will be set to “1” is there is a “Change of Framing Alignment” in DS2 Channel # 7.

Bit 4 - DS2 OOF (Out-of-Frame) Status

This “Read-Only” bit-field reflects the current “OOF” status of DS2 Channel # 7.

This bit-field will be set to “0” if DS2 Channel # 7 is currently in the “In-Frame” condition. Conversely, this bit-field will be set to “1” if DS2 Channel # 7 is currently declaring an “Out-of-Frame” condtion.

Bit 3 - DS2 FERF (Far-End Receive Failure) Status

his “Read-Only” bit-field reflects the current “FERF” status of DS2 Channel # 7.

This bit-field will be set to “0” if DS2 Channel # 7 is currently not declaring the “FERF” condition. Conversely, this bit-field will be set to “1” if DS2 Channel # 1 is currently declaring a “FERF” condtion.

Bit 2 - DS2 RED Alarm Status

This “Read-Only” bit-field reflects the current “RED Alarm” status of DS2 Channel # 7.

This bit-field will be set to “0” if DS2 Channel # 7 is not currently declaring a “RED Alarm” condition. Conversely, this bit-field will be set to “1” if DS2 Channel # 7 is currently declaring a “RED Alarm” condition.

Bit 1 - DS2 AIS (Alarm Indication Signal) Status

This “Read-Only” bit-field reflects the current “AIS” status of DS2 Channel # 1.

This bit-field will be set to “0” if DS2 Channel # 7 is not currently declaring an “AIS” condition. Conversely, this bit-field will be set to “1” if DS2 Channel # 7 is currently declaring an “AIS” condition.

Bit 0 - DS2 RESV Status

To be provided in the next update.

3.0 THE MICROPROCESSOR INTERFACE BLOCK

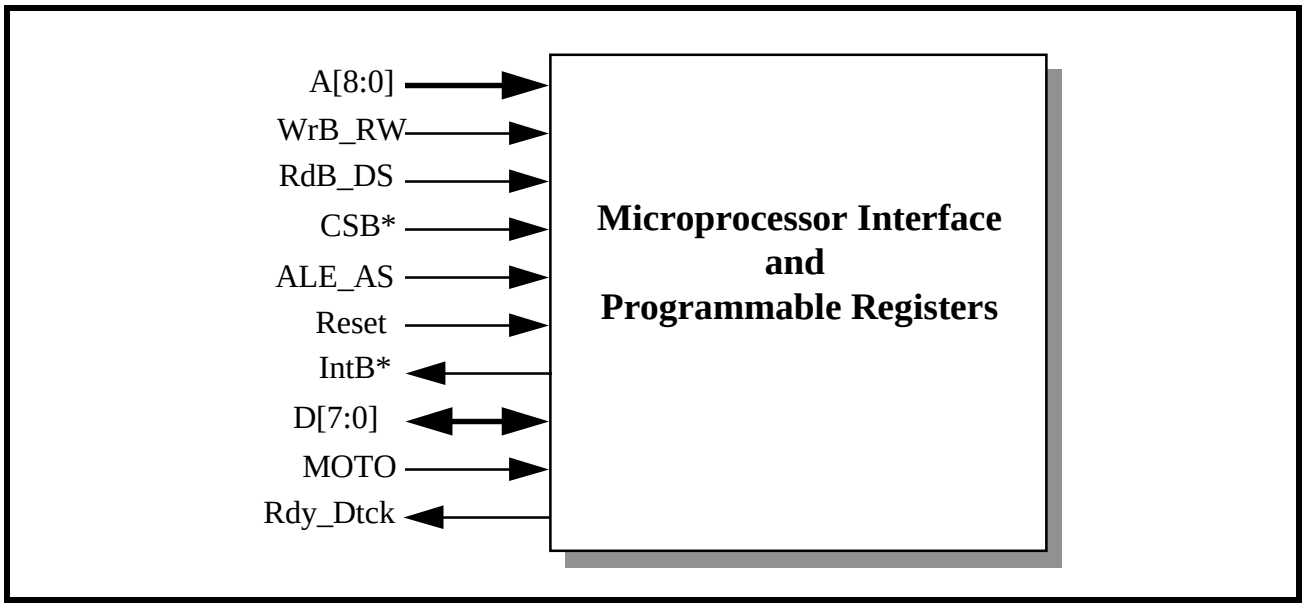
The Microprocessor Interface section supports communication between the "local" microprocessor (µP) and the Framer IC. In particular, the Microprocessor Interface section supports the following operations between the local microprocessor and the Framer.

- The writing of configuration data into the Framer on-chip (addressable) registers.
- The writing of an "outbound" PMDL µPath Maintenance Data Link) message into the "Transmit LAPD Message" buffer (within the Framer IC).
- The Framer IC's generation of an Interrupt Request to the µP.
- The µP's servicing of the interrupt request from the Framer IC.
- The monitoring of the system's "health" by periodically reading the on-chip Performance Monitor registers.
- The reading of an "inbound" PMDL Message from the "Receive LAPD" Message Buffer (within the Framer IC).

Each of these operations (between the local microprocessor and the Framer IC) will be discussed in some detail, throughout this data sheet.

Figure 46 presents a simple block diagram of the Microprosser Interface Block.

FIGURE 46. SIMPLE BLOCK DIAGRAM OF THE MICROPROCESSOR INTERFACE BLOCK, WITHIN THE FRAMER IC



3.1 THE MICROPROCESSOR INTERFACE BLOCK SIGNAL

The Framer IC may be configured into a wide variety of different operating modes and have its performance monitored by software through a standard (local "housekeeping") microprocessor, using data, address and control signals.

The local µP configures the Framer IC (into a desired operating mode) by writing data into specific addressable, on-chip "Read/Write" registers; or on-chip RAM. The microprocessor interface provides the signals which are required for a general purpose microprocessor to read or write data into these registers. The Microprocessor Interface also supports "polled" and interrupt driven environments. These interface signals are described below in Tables 1, 2, and 3. The microprocessor interface can be configured to operate in the "Motorola" Mode or in the "Intel" mode. When the Microprocessor Interface is operating in the "Motorola" mode, then some of the control signals function in a manner as required by the Motorola 68000 family of microprocessors. Likewise, when the Microprocessor Interface is operating in the "Intel" Mode, then some of these Control Signals function in a manner as required by the Intel 80xx family of microprocessors.

Table 6 lists and describes those Microprocessor Interface signals whose role is constant across the two modes. Table 7 describes the role of some of these signals when the Microprocessor Interface is operating in the Intel Mode. Likewise, Table 8 describes the role of these signals when the Microprocessor Interface is operating in the Motorola Mode.

TABLE 6: DESCRIPTION OF THE MICROPROCESSOR INTERFACE SIGNALS THAT EXHIBIT CONSTANT ROLES IN BOTH THE "INTEL" AND "MOTOROLA" MODES

PIN NAME	TYPE	DESCRIPTION
MOTO	I	Selection input for Intel/Motorola µP Interface. Setting this pin to a logic "high" configures the Microprocessor Interface to operate in the "Motorola" mode. Likewise, setting this pin to a logic "low" configures the Microprocessor Interface to operate in the "Intel" Mode.
D[7:0]	I/O	Bi-Directional Data Bus for register read or write operations
A[8:0]	I	Nine Bit Address Bus input: This nine bit Address Bus is provided to allow the user to select an on-chip register or on-chip RAM location.
$\overline{CS}$	I	Chip Select input. This "active low" signal selects the Microprocessor Interface of the UNI device and enables read/write operations with the on-chip registers/on-chip RAM.
$\overline{Int}$	O	Interrupt Request Output: This "open-drain/active-low" output signal will inform the local µP that the UNI has an interrupt condition that needs servicing.

TABLE 7: PIN DESCRIPTION OF MICROPROCESSOR INTERFACE SIGNALS - WHILE THE MICROPROCESSOR INTERFACE IS OPERATING IN THE INTEL MODE

PIN NAME	EQUIVALENT PIN IN INTEL ENVIRONMENT	TYPE	DESCRIPTION
ALE_AS	ALE	I	Address-Latch Enable: This "active-high" signal is used to latch the contents on the address bus, A[8:0]. The contents of the Address Bus are latched into the A[8:0] inputs on the falling edge of ALE_AS. Additionally, this signal can be used to indicate the start of a burst cycle.
$\overline{Rd}$_DS	$\overline{RD}$	I	Read Signal: This "active-low" input functions as the read signal from the local µP. When this signal goes "low", the UNI Microprocessor Interface will place the contents of the addressed register on the Data Bus pins (D[15:0]). The Data Bus will be "tri-stated" once this input signal returns "high".
$\overline{WR}$_RW	$\overline{WR}$	I	Write Signal: This "active-low" input functions as the write signal from the local µP. The contents of the Data Bus (D[15:0]) will be written into the addressed register (via A[8:0]), on the rising edge of this signal.
Rdy_Dtck	$\overline{READY}$	O	Ready Output: This "active-low" signal is provided by the UNI device, and indicates that the current read or write cycle is to be extended until this signal is asserted. The local µP will typically insert "WAIT" states until this signal is asserted. This output will toggle "low" when the device is ready for the next Read or Write cycle.

TABLE 8: PIN DESCRIPTION OF THE MICROPROCESSOR INTERFACE SIGNALS WHILE THE MICROPROCESSOR INTERFACE IS OPERATING IN THE MOTOROLA MODE

PIN NAME	EQUIVALENT PIN IN MOTOROLA ENVIRONMENT	TYPE	DESCRIPTION
ALE_AS	AS*	I	Address Strobe: This "active-low" signal is used to latch the contents on the address bus input pins: A[8:0] into the Microprocessor Interface circuitry. The contents of the Address Bus are latched into the UNI device on the rising edge of the ALE_AS signal. This signal can also be used to indicate the start of a burst cycle.
$\overline{Rd}$_DS	DS*	I	Data Strobe: This signal latches the contents of the bi-directional data bus pins into the Addressed Register (within the UNI) during a Write Cycle.
$\overline{WR}$_RW	R/W*	I	Read/Write* Input: When this pin is "high", it indicates a Read Cycle. When this pin is "low", it indicates a Write cycle.
Rdy_Dtck	DTACK*	O	Data Transfer Acknowledge: The UNI device asserts DTACK* in order to inform the CPU that the present READ or WRITE cycle is nearly complete. The 68000 family of CPUs requires this signal from its peripheral devices, in order to quickly and properly complete a READ or WRITE cycle.

3.2 INTERFACING THE XRT72L13 DS3 FRAMER TO THE LOCAL µC/µP OVER VIA THE MICROPROCESSOR INTERFACE BLOCK

The Microprocessor Interface block, within the Framer is very flexible and provides the following options to the user.

- To interface the Framer to a µC/µP over an 8-bit wide bi-directional data bus.
- To interface the Framer to an Intel-type or Motorola-type µC/µP.
- To transfer data (between the Framer IC and the µC/µP) via the Programmed I/O or Burst Mode

Each of the options are discussed in detail below. Section 3.2.1 will discussed the issues associated with interfacing the Framer to a µC/µP over an 8-bit bi-directional data bus. Afterwards, Section 3.2.2 will discuss Data Access (e.g., Programmed I/O and Burst) Mode when interfaced to both Motorola-type and Intel-type µC/µP.

3.2.1 Interfacing the XRT72L13 DS3 Framer to the Microprocessor over an 8 bit wide bi-directional Data Bus

The XRT72L13 DS3 Framer Microprocessor Interface permits the user to interface it to a µC/µP over an 8 wide bi-directional data bus.

3.2.1.1 Interfacing the Framer to the µC/µP over an 8-bit wide bi-directional data bus.

In general, interfacing the Framer to an "8-bit" µC/µP is quite straight-forward. This is because most of the registers, within the Framer, are 8-bits wide. Further, in this mode, the µC/µP can read or write data into both even and odd numbered addresses within the Framer address space.

Reading Performance Monitor (PMON) Registers

The only awkward issue that the user should be wary of (while operating in the "8-bit" mode) occurs whenever the µC/µP needs to read the contents of one of the PMON (Performance Monitor) registers.

The XRT72L13 DS3 Framer consists of the following PMON Registers.

- PMON LCV Event Count Register
- PMON Framing Error Event Count Register
- PMON Received FEBE Event Count Register
- PMON Parity Error Event Count Register
- PMON Received Single-Bit HEC Error Count Register
- PMON Received Multiple-Bit HEC Error Count Register
- PMON Received Idle Cell Count Register
- PMON Received Valid Cell Count Register
- PMON Discarded Cell Count Register
- PMON Transmitted Idle Cell Count Register
- PMON Transmitted Valid Cell Count Register.

Unlike most of the registers within the Framer, the PMON registers are "16-bit" registers (or 16-bits wide). Table 4 lists each of these PMON registers as consisting of two 8-bit registers. One of these "8-bit" register is labeled "MSB" (or Most Significant Byte")

and the other register is labeled "LSB" (or Least Significant Byte). When an "8-bit" PMON Register is concatenated with its "companion 8-bit" PMON Register, one obtains the "full 16-bit expression" within that PMON Register.

The consequence of having these 16-bit registers is that an "8-bit" µC/µP will have to perform two consecutive read operations in order to read in the full 16-bit expression contained within a given PMON register. To complicate matters, these PMON Registers are "Reset-Upon-Read" registers. More specifically, these PMON Register are "Reset-Upon-Read" in the sense that, the entire "16-bit" contents, within a given PMON Register is reset, as soon as an "8-bit" µC/µP reads in either "byte" of this "two-byte" (e.g., 16 bit) expression.

For example;

Consider that an "8-bit" µC/µP needs to read in the "PMON LCV Event Count" Register. In order to accomplish this task, the 8-bit µC/µP is going to have to read in the contents of "PMON LCV Event Count Register - MSB" (located at Address = 0x40) and the contents of the "PMON LCV Event Count Register - LSB (located at Address = 0x41). These two "eight-bit" registers, when concatenated together, make up the "PMON LCV Event Count" Register.

If the 8-bit µC/µP reads in the "PMON LCV Event Count-LSB" register first; then the entire "PMON LCV Event Count" register will be reset to 0x0000. As a consequence, if the 8-bit µC/µP attempts to read in the "PMON LCV Event Count-MSB" register in the very next read cycle, it will read in the value 0x00.

The PMON Holding Register

In order to "get-around" this "Reset-Upon-Read" problem, the XRT72L13 DS3 Framer includes a special register, which permits "8-bit" µC/µP to read in the full 16-bit contents of these PMON registers. This special register is called the "PMON Holding" Register; and is located at 0x56 within the Framer Address space.

The way the PMON Holding register works is as follows. Whenever an "8-bit" µC/µP reads in one of the bytes (of the "2-byte" PMON register); the contents of the "unread" (e.g., other) byte will be stored in the PMON Holding Register. Therefore, the "8-bit" µC/µP must then read in the contents of the PMON Holding Register in the very next read operation.

In Summary: Whenever an "8-bit" µC/µP needs to read a PMON Register, it must execute the following steps.

Step 1: Read in the contents of a given "8-bit" PMON Register (it does not matter whether the µC/µP reads in the "-MSB" or the "-LSB" register).

Step 2: Read in the contents of the "PMON Holding" Register (located at Address = 0x56). This register will contain the contents of the "other" byte.

3.2.2 Data Access Modes

As mentioned earlier, the Microprocessor Interface block supports data transfer between the Framer and the µC/µP (e.g., "Read" and "Write" operations) via two modes: the "Programmed I/O" and the "Burst" Modes. Each of these "Data Access" Modes are discussed in detail below.

3.2.2.1 Data Access using Programmed I/O

"Programmed I/O" is the conventional manner in which a microprocessor exchanges data with a peripheral device. However, it is also the slowest method of data exchange between the Framer and the µC/µP; as will be described in this text.

The next two sections present detailed information on Programmed I/O Access, when the XRT72L13 DS3 Framer is operating in the "Intel Mode" and in the "Motorola Mode".

3.2.2.1.1 Programmed I/O Access in the "Intel" Mode

If the XRT72L13 DS3 Framer is interfaced to an "Intel-type" µC/µP (e.g., the 80x86 family, etc.), then it should be configured to operate in the "Intel" mode (by tying the "MOTO" pin to ground). Intel-type "Read" and "Write" operations are described below.

3.2.2.1.1.1 The Intel Mode Read Cycle

Whenever an Intel-type µC/µP wishes to read the contents of a register or some location within the Receive LAPD Message buffer or the Receive OAM Cell Buffer, (within the Framer device), it should do the following.

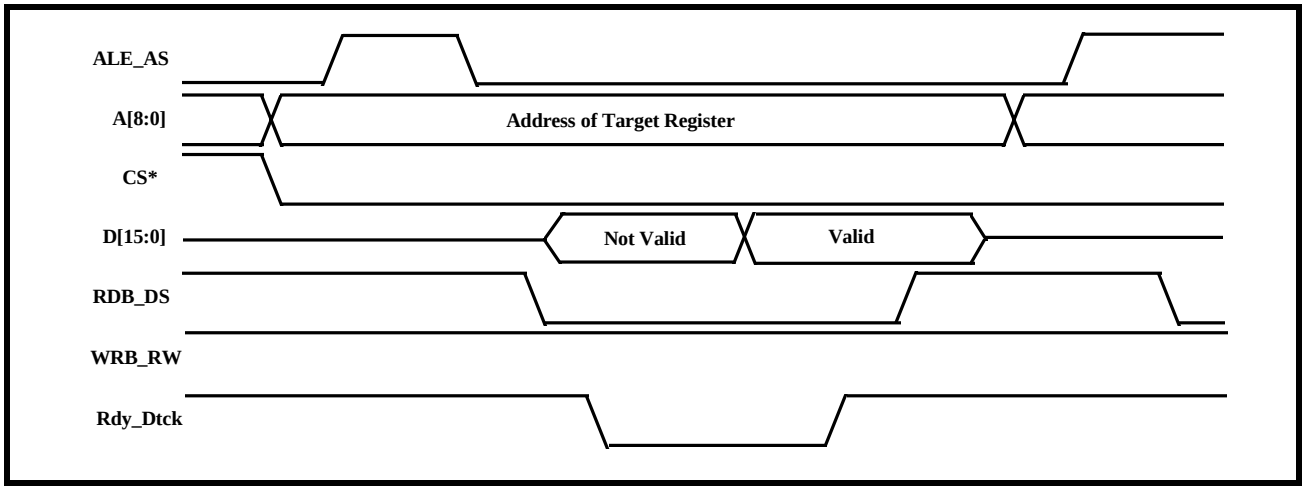
1. Place the address of the "target" register or buffer location (within the Framer) on the Address Bus input pins A[8:0].
2. While the µC/µP is placing this address value on the Address Bus, the Address Decoding circuitry (within the user's system) should assert the CS* (Chip Select) pin of the Framer, by toggling it "low". This action enables further communication between the µC/µP and the Framer Microprocessor Interface block.
3. Toggle the ALE_AS (Address Latch Enable) input pin "high". This step enables the "Address Bus" input drivers, within the Microprocessor Interface block of the Framer.
4. After allowing the data on the Address Bus pins to settle (by waiting the appropriate "Address"

Data Setup time"), the µC/µP should toggle the ALE_AS pin "low". This step causes the Framer device to "latch" the contents of the "Address Bus" into its internal circuitry. At this point, the address of the register or buffer locations (within the Framer), has now been selected.

5. Next, the µC/µP should indicates that this current bus cycle is a "Read" Operation by toggling the $\overline{Rd}$_DS (Read Strobe) input pin "low". This action also enables the bi-directional data bus output drivers of the Framer device. At this point, the "bi-directional" data bus output drivers will proceed to drive the contents of the "latched addressed" register (or buffer location) onto the bi-directional data bus, D[7:0].
6. Immediately after the µC/µP toggles the "Read Strobe" signal "low", the Framer device will toggle the Rdy_Dtck output pin "low". The Framer device does this in order to inform the µC/µP that the data (to be read from the data bus) is "NOT READY" to be "latched" into the µC/µP.
7. After some settling time, the data on the "bi-directional" data bus will stabilize and can be read by the µC/µP. The XRT72L13 DS3 Framer will indicate that this data can be read by toggling the Rdy_Dtck (READY) signal "high".
8. After the µC/µP detects the Rdy_Dtck signal (from the XRT72L13 DS3 Framer), it can then terminate the Read Cycle by toggling the $\overline{Rd}$_DS (Read Strobe) input pin "high".

Figure 47 presents a timing diagram which illustrates the behavior of the Microprocessor Interface signals, during an "Intel-type" Programmed I/O Read Operation.

FIGURE 47. BEHAVIOR OF MICROPROCESSOR INTERFACE SIGNALS DURING AN "INTEL-TYPE" PROGRAMMED I/O READ OPERATION



3.2.2.1.1.2 The Intel Mode Write Cycle

Whenever an Intel-type µC/µP wishes to write a byte or word of data into a register or buffer location, within the Framer, it should do the following.

1. Assert the ALE_AS (Address Latch Enable) input pin by toggling it "high". When the µC/µP asserts the ALE_AS input pin, it enables the "Address Bus Input Drivers" within the Framer chip.
2. Place the address of the "target" register or buffer location (within the Framer), on the Address Bus input pins, A[8:0].
3. While the µC/µP is placing this address value onto the Address Bus, the Address Decoding circuitry (within the user's system) should assert the CS* input pin of the Framer device by toggling it "low". This step enables further communication between the µC/µP and the Framer Microprocessor Interface block.
4. After allowing the data on the Address Bus pins to settle (by waiting the appropriate "Address Setup" time); the µC/µP should toggle the ALE_AS input pin "low". This step causes the Framer device to "latch" the contents of the "Address Bus" into its internal circuitry. At this point, the address of the register or buffer location (within the Framer), has now been selected.
5. Next, the µC/µP should indicate that this current bus cycle is a "Write" Operation; by toggling the $\overline{WR}$_RW (Write Strobe) input pin "low". This action also enables the "bi-directional" data bus input drivers of the Framer device.
6. The µC/µP should then place the byte or word that it intends to write into the "target" register, on the bi-directional data bus, D[7:0].
7. After waiting the appropriate amount of time, for the data (on the bi-directional data bus) to settle;

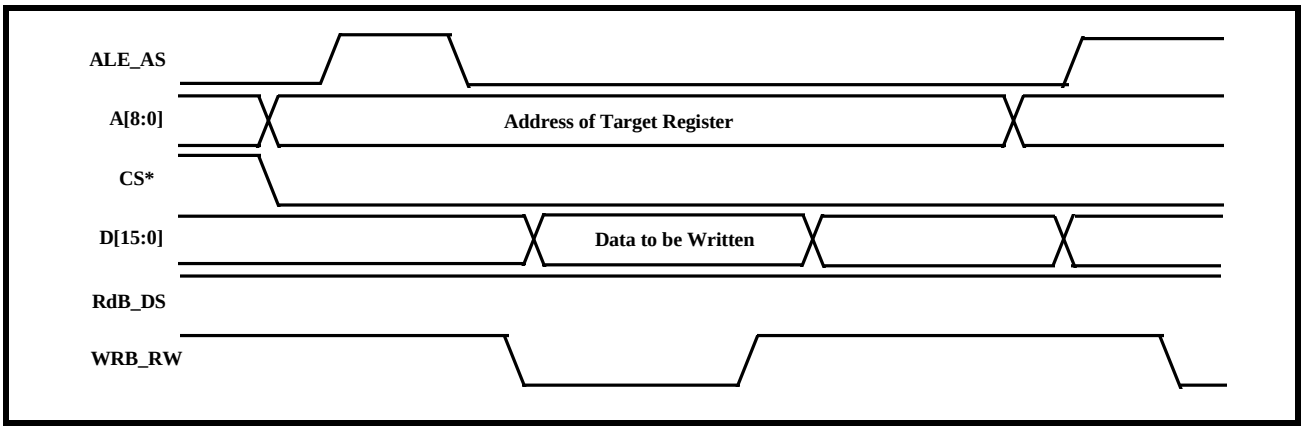
the µC/µP should toggle the WR_RW (Write Strobe) input pin "high". This action accomplishes two things:

a. It latches the contents of the bi-directional data bus into the XRT72L13 DS3 Framer Microprocessor Interface block.

b. It terminates the write cycle.

Figure 48 presents a timing diagram which illustrates the behavior of the Microprocessor Interface signals, during an "Intel-type" Programmed I/O Write Operation.

FIGURE 48. BEHAVIOR OF THE MICROPROCESSOR INTERFACE SIGNALS, DURING AN "INTEL-TYPE" PROGRAMMED I/O WRITE OPERATION



3.2.2.1.2 Programmed I/O Access in the Motorola Mode

If the XRT72L13 DS3 Framer is interfaced to a "Motorola-type" µC/µP (e.g., the MC680X0 family, etc.); it should be configured to operate in the "Motorola" mode (by tying the "MOTO" pin to Vcc). Motorola-type Programmed I/O "Read" and "Write" operations are described below.

3.2.2.1.2.1 The Motorola Mode Read Cycle

Whenever a "Motorola-type" µC/µP wishes to read the contents of a register or some location within the Receive LAPD Message or Receive OAM Cell Buffer, (within the Framer device) it should do the following.

1. Assert the ALE_AS (Address-Strobe) input pin by toggling it low. This step enables the Address Bus input drivers, within the Microprocessor Interface Block of the Framer IC.

2. Place the address of the "target" register (or buffer location) within the Framer, on the Address Bus input pins, A[8:0].

3. At the same time, the Address Decoding circuitry (within the user's system) should assert the CS* (Chip Select) input pin of the Framer device, by toggling it "low". This action enables further communication between the µC/µP and the Framer Microprocessor Interface block.

4. After allowing the data on the Address Bus pins to settle (by waiting the appropriate "Address Setup" time), the µC/µP should toggle the ALE_AS input pin "high". This step causes the Framer device to latch the contents of the "Address Bus" into its internal circuitry. At this point, the address of the register or buffer location (within the Framer) has now been selected.

5. Further, the µC/µP should indicate that this cycle is a "Read" cycle by setting the WR_RW (R/W*) input pin "high".

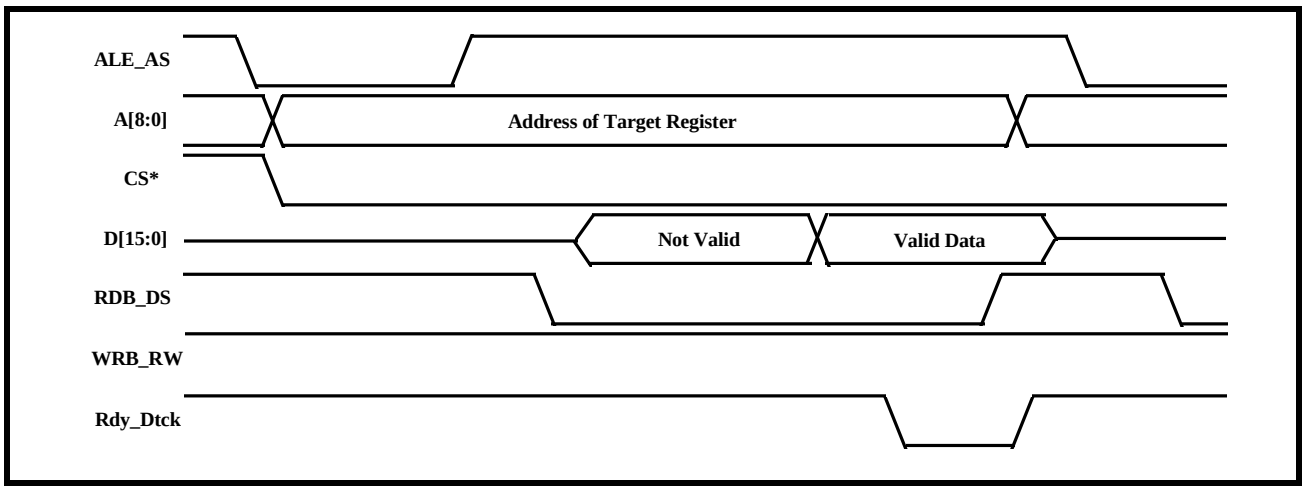
6. Next the µC/µP should initiate the current bus cycle by toggling the Rd_DS (Data Strobe) input pin "low". This step enables the bi-directional data bus output drivers, within the XRT72L13 DS3 Framer device. At this point, the bi-directional data bus output drivers will proceed to driver the contents of the "Address" register onto the bi-directional data bus, D[7:0].

7. After some settling time, the data on the "bi-directional" data bus will stabilize and can be read by the µC/µP. The XRT72L13 DS3 Framer will indicate that this data can be read by asserting the Rdy_Dtck (DTACK) signal.

8. After the µC/µP detects the Rdy_Dtck signal (from the XRT72L13 DS3 Framer) it will terminate the Read Cycle by toggling the "Rd_DS" (Data Strobe) input pin "high".

Figure 49 presents a timing diagram which illustrates the behavior of the Microprocessor Interface signals during a "Motorola-type" Programmed I/O Read Operation.

FIGURE 49. ILLUSTRATION OF THE BEHAVIOR OF MICROPROCESSOR INTERFACE SIGNALS, DURING A "MOTOROLA-TYPE" PROGRAMMED I/O READ OPERATION



3.2.2.1.2.2 The Motorola Mode Write Cycle

Whenever a Motorola-type µC/µP wishes to write a byte or word of data into a register or buffer location, within the Framer, it should do the following.

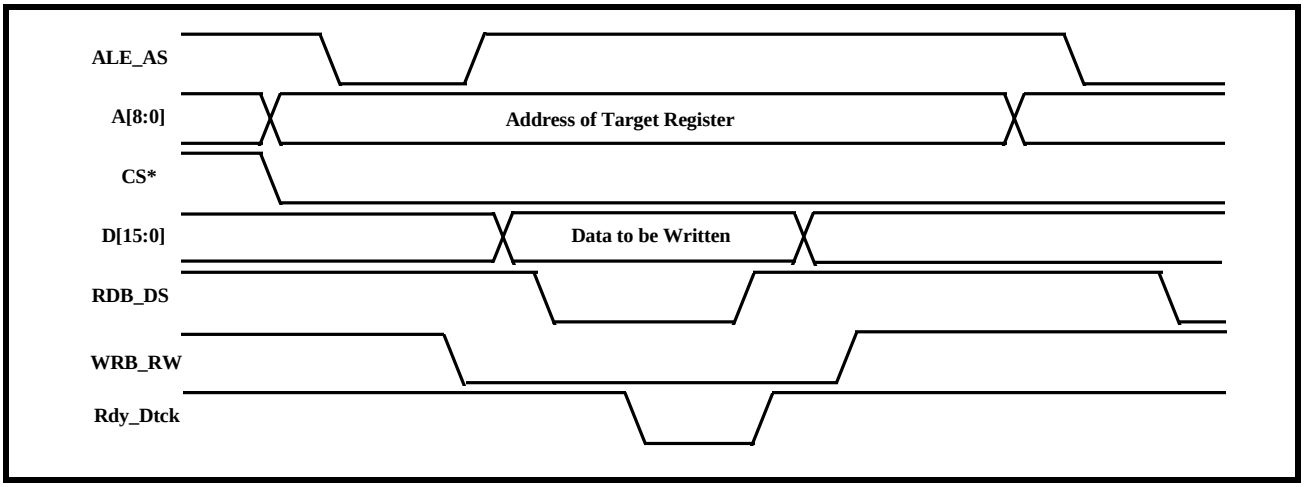
1. Assert the ALE_AS (Address Select) input pin by toggling it "low". This step enables the "Address Bus" input drivers (within the Framer chip).
2. Place the address of the "target" register or buffer location (within the Framer), on the Address Bus input pins, A[8:0].
3. While the µC/µP is placing this address value onto the Address Bus, the Address-Decoding circuitry (within the user's system) should assert the CS* (Chip Select) input pins of the Framer by toggling it "low". This step enables further communication between the µC/µP and the Framer Microprocessor Interface block.
4. After allowing the data on the Address Bus pins to settle (by waiting the appropriate "Address Setup" time), the µC/µP should toggle the ALE_AS input pin "high". This step causes the Framer device to "latch" the contents of the "Address Bus" into its own circuitry. At this point, the Address of the register or buffer location (within the Framer), has now been selected.
5. Further, the µC/µP should indicate that this current bus cycle is a "Write" operation by toggling the $\overline{WR}$_RW (R/W*) input pin "low".
6. The µC/µP should then place the byte or word that it intends to write into the "target" register, on the bi-directional data bus, D[7:0].
7. Next, the µC/µP should initiate the bus cycle by toggling the $\overline{Rd}$_DS (Data Strobe) input pin "low". When the XRT72L13 DS3 Framer senses that the $\overline{WR}$_RW (R/W*) input pin is "high" and that the $\overline{Rd}$_DS (Data Strobe) input pin has toggled "low", it will enable the "input drivers" of the bi-directional data bus, D[7:0].
8. After waiting the appropriate time, for this newly placed data to settle on the bi-directional data bus (e.g., the "Data Setup" time) the Framer will assert the Rdy_Dtck output signal.
9. After the µC/µP detects the Rdy_Dtck signal (from the Framer), the µC/µP should toggle the $\overline{Rd}$_DS input pin "high". This action accomplishes two things.

a. It latches the contents of the bi-directional data bus into the XRT72L13 DS3 Microprocessor Interface block.

b. It terminates the "Write" cycle.

Figure 50 presents a timing diagram which illustrates the behavior of the Microprocessor Interface signals, during a "Motorola-type" Programmed I/O Write Operation.

FIGURE 50. ILLUSTRATION OF THE BEHAVIOR OF THE MICROPROCESSOR INTERFACE SIGNAL, DURING A "MOTOROLA-TYPE" PROGRAMMED I/O WRITE OPERATION



3.2.2.2 Data Access using Burst Mode I/O

Burst Mode I/O access is a much faster way to transfer data between the µC/µP and the Microprocessor Interface (of the XRT72L13 DS3 Framer), than Programmed I/O. The reason why Burst Mode I/O is so much faster follows.

Data is placed upon the Address Bus input pins A[8:0]; only for the very first access, within a given burst access. The remaining read or write operations (within this burst access) do not require the placement of the Address Data on the Address Data Bus. As a consequence, the user does not have to wait through the "Address Setup" and "Hold" times; for each of these Read/Write operation, within the "Burst" Access.

It is important to note that there are some limitations associated with Burst Mode I/O Operations.

1. All cycles within the Burst Access, must be either "all Read" or "all Write" cycles. No "mixing of "Read" and "Write" cycles is permitted.
2. A Burst Access can only be used when "Read" or "Write" operations are to be employed over a contiguous range of address locations, within the Framer device.
3. The very first "Read" or "Write" cycle, within a burst access, must start at the "lowest" address value, of the range of addresses to be accessed. Subsequent operations will automatically be incremented to the very next higher address value.

Examples of Burst Mode I/O operations are presented below for read and write operations, with both "Intel-type" and "Motorola-type" µC/µP.

3.2.2.2.1 Burst I/O Access in the Intel Mode

If the XRT72L13 DS3 Framer is interfaced to an "Intel-type" µC/µP (e.g., the 80x86 family, etc.), then it should be configured to operate in the "Intel" mode (by tying the "MOTO" pin to ground). Intel-type "Read" and "Write" Burst I/O Access operations are described below.

3.2.2.2.1.1 The "Intel-Mode" Read Burst Access

Whenever an "Intel-type" µC/µP wishes to read the contents of numerous registers or buffer locations over a "contiguous" range of addresses; then it should do the following.

a. Perform the initial "read" operation of the burst access.

b. Perform the remaining "read" operations of the burst access.

c. Terminate the "burst access" operation.

Each of these "operations" within the burst access are described below.

3.2.2.2.1.1.1 The Initial Read Operation

The initial read operation of an "Intel-type" read burst access is accomplished by executing a "Programmed I/O" Read Cycle as summarized below.

A.0 Execute a Single Ordinary (Programmed I/O) Read Cycle, as described in steps A.1 through A.7 below.

A.1 Place the address of the "initial-target" register or buffer location (within the Framer) on the Address Bus input pins A[8:0].

A.2 While the µC/µP is placing this address value onto the Address Bus, the Address Decoding circuitry (within the user's system) should assert the CS* input pin of the Framer, by toggling it "low". This step enables further communication between the µC/µP and the Framer Microprocessor Interface block.

A.3 Assert the ALE_AS (Address Latch Enable) pin by toggling it "high". This step enables the "Address Bus" input drivers, within the Microprocessor Interface block of the Framer.

A.4 After allowing the data on the Address Bus pins to settle (by waiting the appropriate "Address" Data Setup time"), the µC/µP should then toggle the ALE_AS pin "low". This step latches the contents, on the Address Bus pins, A[8:0], into the XRT72L13 DS3 Framer Microprocessor Interface block. At this point, the "initial" address of the burst access has now been selected.

NOTE: *The ALE_AS input pin should remain "low" for the remainder of this "Burst Access" operation.*

A.5 Next, the µC/µP should indicate that this current bus cycle is a "Read" Operation by toggling the $\overline{\text{Rd}}$_DS (Read Strobe) input pin "low". This action also enables the "bi-directional" data bus output drivers of the Framer device. At this point, the bi-directional data bus output drivers will proceed to drive the contents of the "addressed" register onto the "bi-directional" data bus, D[7:0].

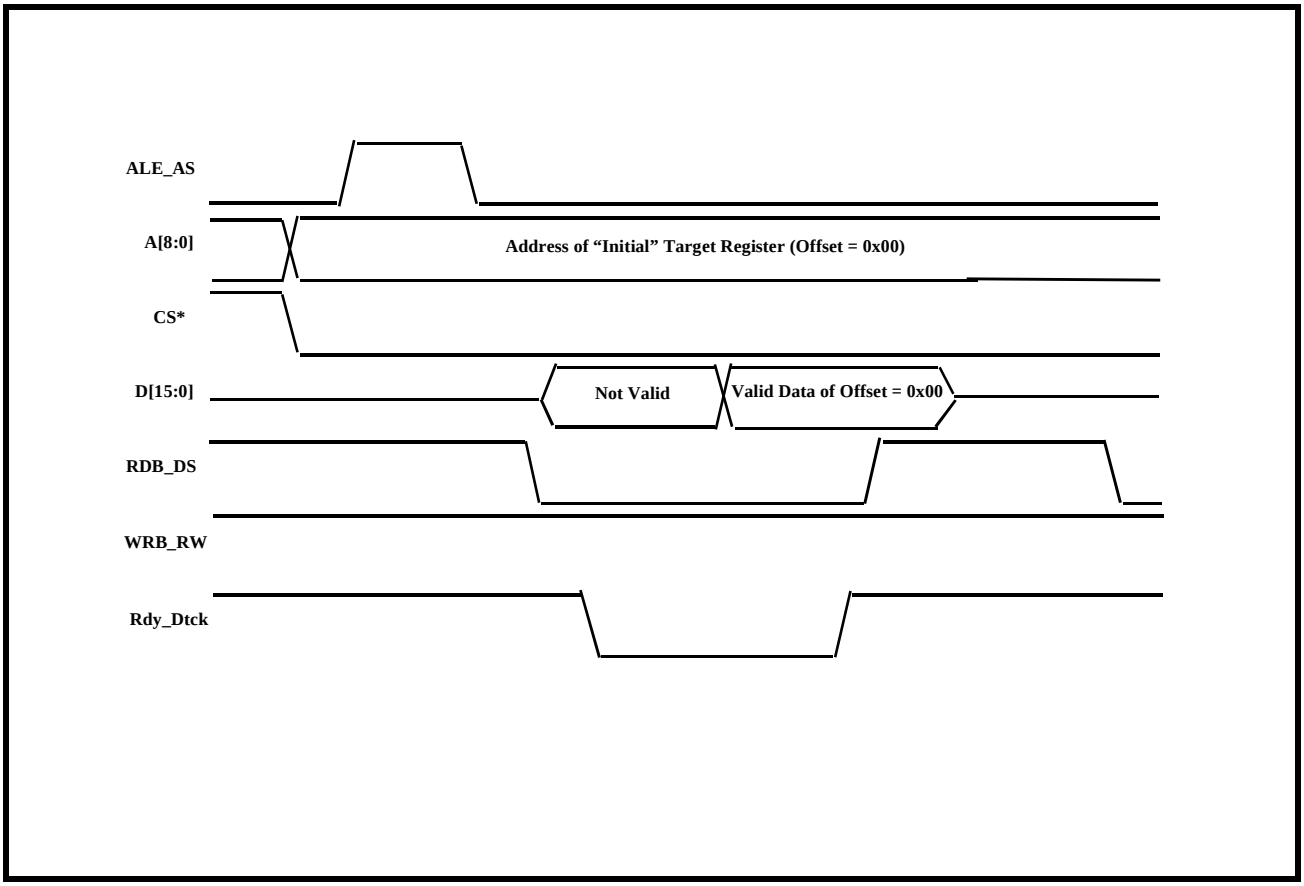
A.6 Immediately after the µC/µP toggles the "Read Strobe" signal "low", the Framer device will toggle the Rdy_Dtck (READY) output pin "low". The Framer device does this in order to inform the µC/µP that the data (to be read from the data bus) is "NOT READY" to be latched into the µC/µP.

A.7 After some settling time, the data on the "bi-directional" data bus will stabilize and can be read by the µC/µP. The XRT72L13 DS3 Framer will indicate that this data is ready to be read, by toggling the Rdy_Dtck (Ready) signal "high".

A.8 After the µC/µP detects the Rdy_Dtck signal (from the XRT72L13 DS3 Framer IC), it can then will terminate the "Read" cycle by toggling the $\overline{\text{Rd}}$_DS (Read Strobe) input pin "high".

Figure 51 presents an illustration of the behavior of the Microprocessor Interface Signals, during the "initial" Read Operation, within a Burst I/O Cycle; for an Intel-type µC/µP.

FIGURE 51. BEHAVIOR OF THE MICROPROCESSOR INTERFACE SIGNALS, DURING THE "INITIAL" READ OPERATION OF A BURST CYCLE (INTEL TYPE PROCESSOR)



At the completion of this initial read cycle, the µC/µP has read in the contents of the first register or buffer location (within the XRT72L13 DS3 Framer) for this particular burst I/O access operation. In order to illustrate how this "burst access operation" works, the byte (or word) of data, that is being read in Figure 51 , has been labeled "Valid Data at Offset = 0x00". This label indicates that the µC/µP is reading the very first register (or buffer location) in this burst access operation.

3.2.2.2.1.1.2 The Subsequent Read Operations

The procedure that the µC/µP must use to perform the remaining read cycles, within this Burst Access operation, is presented below.

B.0 Execute each subsequent Read Cycles, as described in steps 1 through 3 below.

B.1 Without toggling the ALE_AS input pin (e.g., keeping it "low"); toggle the $\overline{Rd}$_DS input pin "low". This step accomplishes the following.

a. The Framer will internally increments the "latched address" value (within the Microprocessor Interface circuitry).

b. The output drivers of the "bi-directional" data bus, D[7:0] are enabled. At some time later, the register or buffer location corresponding to the "incremented" latched address value will be driven onto the bi-directional data bus.

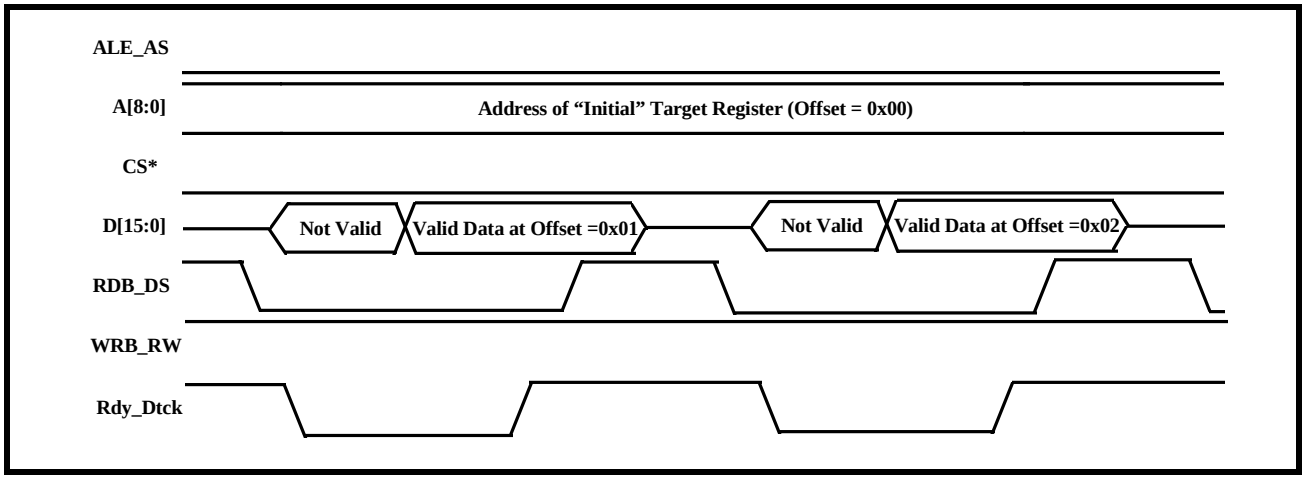
B.2 Immediately after the "Read Strobe" pin toggles "low" the Framer IC will toggle the Rdy_Dtck (READY) output pin "low" to indicate its "NOT READY" status.

B.3 After some settling time, the data on the bi-directional data bus will stabilize and can be read by the µC/µP. The XRT72L13 DS3 Framer will indicate that this data is ready to be read by toggling the Rdy_Dtck (READY) signal "high".

B.4 After the µC/µP detects the Rdy_Dtck signal (from the XRT72L13 DS3 Framer), it can then terminates the "Read" cycle by toggling the $\overline{Rd}$_DS (Read Strobe) input pin "high".

For subsequent read operations, within this burst cycle, the µC/µP simply repeats steps 1 through 3, as illustrated in Figure 52 .

FIGURE 52. BEHAVIOR OF THE MICROPROCESSOR INTERFACE SIGNALS, DURING SUBSEQUENT "READ" OPERATIONS WITHIN THE BURST I/O CYCLE



In addition to the behavior of the Microprocessor Interface signals, Figure 52 also illustrates other points regarding the "Burst Access Operation".

a. The Framer internally increments the address value, from the original "latched" value shown in Figure 51 . This is illustrated by the data, appearing on the data bus, (for the first read access) being labeled "Valid Data at Offset = 0x01"; and that for the second read access being labeled "Valid Data at Offset = 0x02.".

b. The Framer performs this "address incrementing" process even though there are no changes in the Address Bus Data, A[8:0].

3.2.2.2.1.1.3 Terminating the Burst Access Operation

The Burst Access Operation will be terminated upon the rising edge of the ALE_AS input signal. At this point the Framer will cease to internally increment the "latched" address value. Further, the µC/µP is now free to execute either a "Programmed I/O" access or to start another "Burst Access" Operation with the XRT72L13 DS3 Framer.

3.2.2.2.1.2 The "Intel-Mode" Write Burst Access

Whenever an "Intel-type" µC/µP wishes to write data into a "contiguous" range of addresses, then it should do the following.

a. Perform the initial "write" operation; of the burst access.

b. Perform the remaining "write" operations, of the burst access.

c. Terminate the burst access operation.

Each of these "operations" within the burst access are described below.

3.2.2.2.1.2.1 The Initial Write Operation

The initial write operation of an "Intel-type" Write Burst Access is accomplished by executing a "Programmed I/O" write cycle as summarized below.

A.0 Execute a Single Ordinary (Programmed I/O) Write cycle, as described in Steps A.1 through A.7 below.

A.1 Place the address of the "initial" target register (or buffer location) within the Framer, on the Address Bus pins, A[8:0].

A.2 A.2 At the same time, the "Address-Decoding" circuitry (within the user's system) should assert the CS* (Chip Select) input pin of the Framer, by toggling it "low". This step enables further communication between the µC/µP and the Framer Microprocessor Interface block.

A.3 Assert the ALE_AS (Address Latch Enable) input pin "high". This step enables the Address Bus input drivers, within the Microprocessor Interface Block of the Framer.

A.4 After allowing the data on the Address Bus pins to settle (by waiting the appropriate "Address Setup" time); the µC/µP should then toggle the ALE_AS input pin "low". This step latches the contents, on the Address Bus pins, A[8:0], into the XRT72L13 DS3 Framer Microprocessor Interface block. At this point, the "initial"

address of the "burst access" has now been selected.

NOTE: The ALE_AS input pin should remain "low" for the remainder of this "Burst I/O Access" operation.

A.5 Next, the µC/µP should indicate that this current bus cycle is a "Write" operation by keeping the $\overline{Rd}$_DS pin "high" and toggling the $\overline{WR}$_RW (Write Strobe) pin "low". This action also enables the "bi-directional" data bus input drivers of the Framer device.

A.6 The µC/µP places the byte (or word) that it intends to write into the "target" register on the "bi-directional data" bus, D[7:0].

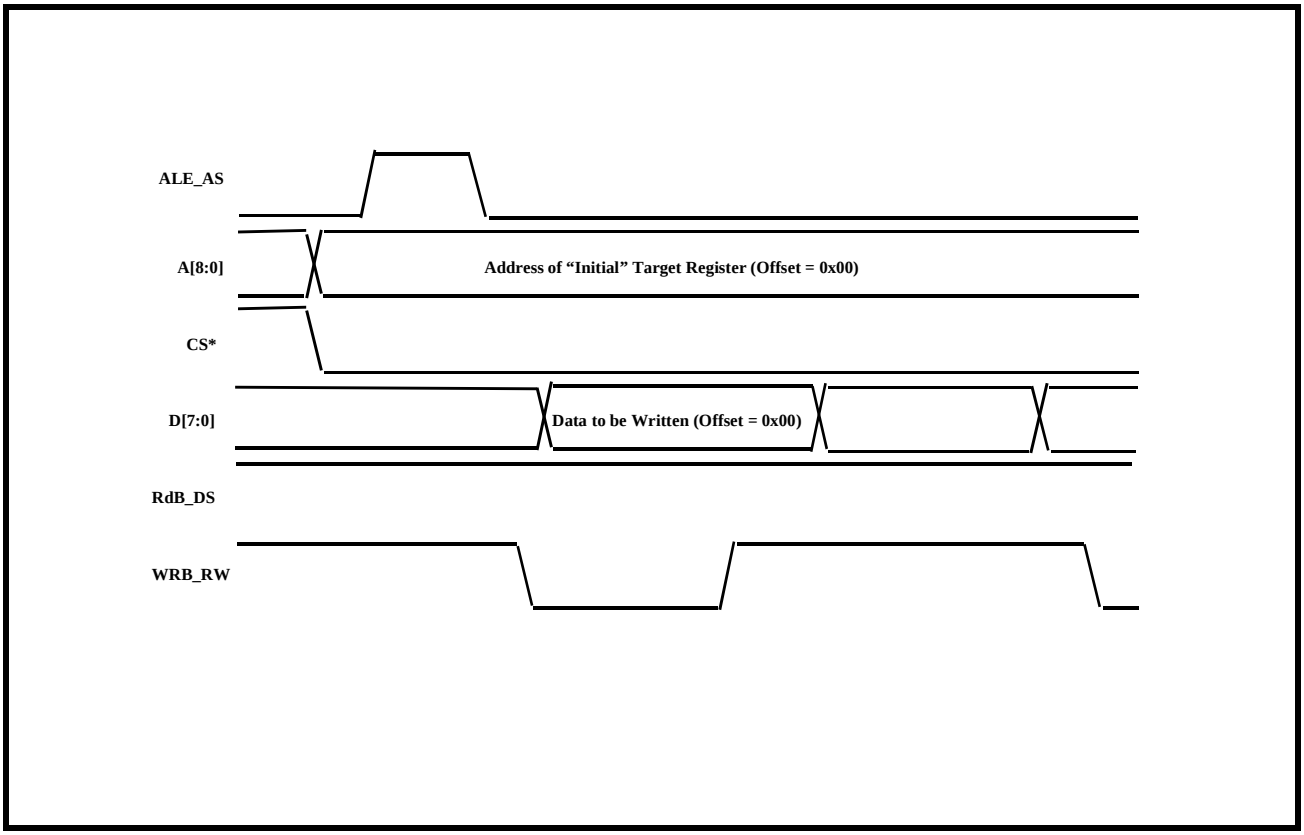
A.7 After waiting the appropriate amount of time, for the data (on the bi-directional data bus) to settle, the µC/µP should toggle the $\overline{WR}$_RW (Write Strobe) input pin "high". This action accomplishes two things.

a. It latches the contents of the bi-directional data bus into the XRT72L13 DS3 Framer Microprocessor Interface Block.

b. It terminates the write cycle.

Figure 53 presents a timing diagram which illustrates the behavior of the Microprocessor Interface signals, during the "initial" write operation within a Burst Access, for an "Intel-type" µC/µP.

FIGURE 53. BEHAVIOR OF THE MICROPROCESSOR INTERFACE SIGNALS, DURING THE "INITIAL" WRITE OPERATION OF A BURST CYCLE (INTEL-TYPE PROCESSOR)



At the completion of this initial write cycle, the µC/µP has written a byte or word into the first register or buffer location (within the XRT72L13 DS3 Framer) for this particular burst access operation. In order to illustrate this point, the byte (or word) of data, that is being written in Figure 53 has been labeled "Data to be Written (Offset = 0x00)".

3.2.2.2.1.2.2 The Subsequent Write Operations

The procedure that the µC/µP must use to perform the remaining write cycles, within this burst access operation, is presented below.

B.0 Execute each subsequent write cycle, as described in steps B.1 through B.3.

B.1 Without toggling the ALE_AS input pin (e.g., keeping it "low"); apply the value of the next byte or word (to be written into the Framer) to the bi-directional data bus pins, D[7:0].

B.2 Toggle the $\overline{WR}$_RW (Write Strobe) input pin "low". This step accomplishes two things.

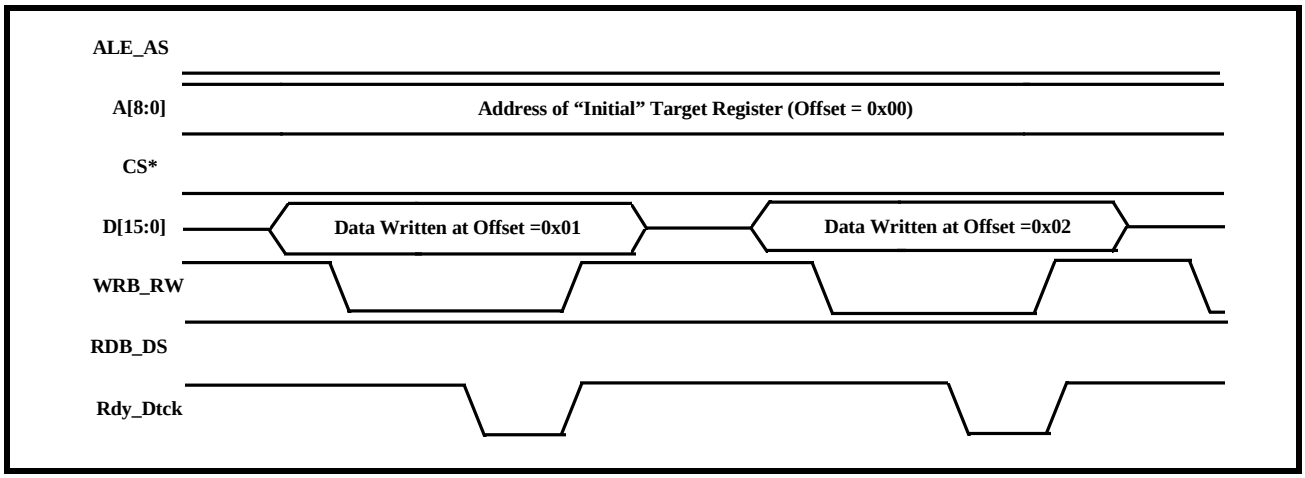
a. It enables the input drivers of the bi-directional data bus.

b. It causes the Framer to internally increment the value of the "latched" address.

B.3 After waiting the appropriate amount of settling time the data, in the internal data bus, will stabilize and is ready to be latched into the Framer Microprocessor Interface block. At this point, the µC/µP should latch the data into the Framer by toggling the $\overline{WR}$_RW input pin "high".

For subsequent write operations, within this burst I/O access, the µC/µP simply repeats steps B.1 through B.3, as illustrated in Figure 54 .

FIGURE 54. BEHAVIOR OF THE MICROPROCESSOR INTERFACE SIGNALS, DURING SUBSEQUENT "WRITE" OPERATIONS WITHIN THE BURST I/O CYCLE



3.2.2.2.1.2.3 Terminating the Burst I/O Access

Burst Access Operation will be terminated upon the rising edge of the ALE_AS input signal. At this point the Framer will cease to internally increment the "latched" address value. Further, the µC/µP is now free to execute either a "Programmed I/O" access or to start another "Burst Access Operation" with the XRT72L13 DS3 Framer.

3.2.2.2.2 Burst I/O Access in the Motorola Mode

If the XRT72L13 DS3 Framer is interfaced to a "Motorola-type" µC/µP (e.g., the MC680x0 family, etc.), then it should be configured to operate in the "Motorola" mode (by tying the "MOTO" pin to VCC). Motorola-type "Read" and "Write" Burst I/O Access operations are described below.

3.2.2.2.2.1 The "Motorola-Mode" Read Burst I/O Access Operation

Whenever a "Motorola-type" µC/µP wishes to read the contents of numerous registers or buffer locations over a "contiguous" range of addresses, then it should do the following.

a. Perform the initial "Read" operation of the burst access.

b. Perform the remaining "read" operations; in the burst access.

c. Terminate the "burst access" operation.

Each of these operations, within the Burst Access are discussed below.

3.2.2.2.2.1.1 The Initial Read Operation

The initial read operation of a "Motorola-type" read burst access is accomplished by executing a "Programmed I/O Read" cycle, as summarized below.

A.0 Execute a Single Ordinary (Programmed I/O) Read Cycle, as described in steps A.1 through A.8 below.

A.1 Assert the ALE_AS (AS*) input pin by toggling it "low". This step enables the "Address Bus" input drivers (within the XRT72L13 DS3 Framer) within the Framer Microprocessor Interface Block.

A.2 Place the address of the "initial" target register or buffer location (within the Framer), on the Address Bus input pins, A[8:0].

A.3 At the same time, the Address-Decoding circuitry (within the user's system) should assert the CS* (Chip Select) input pins of the Framer by toggling it "low". This action enables further

communication between the µC/µP and the Framer Microprocessor Interface block.

A.4 After allowing the data on the Address Bus pins to settle (by waiting the appropriate "Address Setup" time), the µC/µP should toggle the ALE_AS input pin "high". This step causes the Framer device to latch the contents of the Address Bus into its internal circuitry. At this point, the "initial" address of the burst access has now been selected.

A.5 Further, the µC/µP should indicate that this cycle is a "Read" cycle by setting the $\overline{WR}$_RW (R/W*) input pin "high".

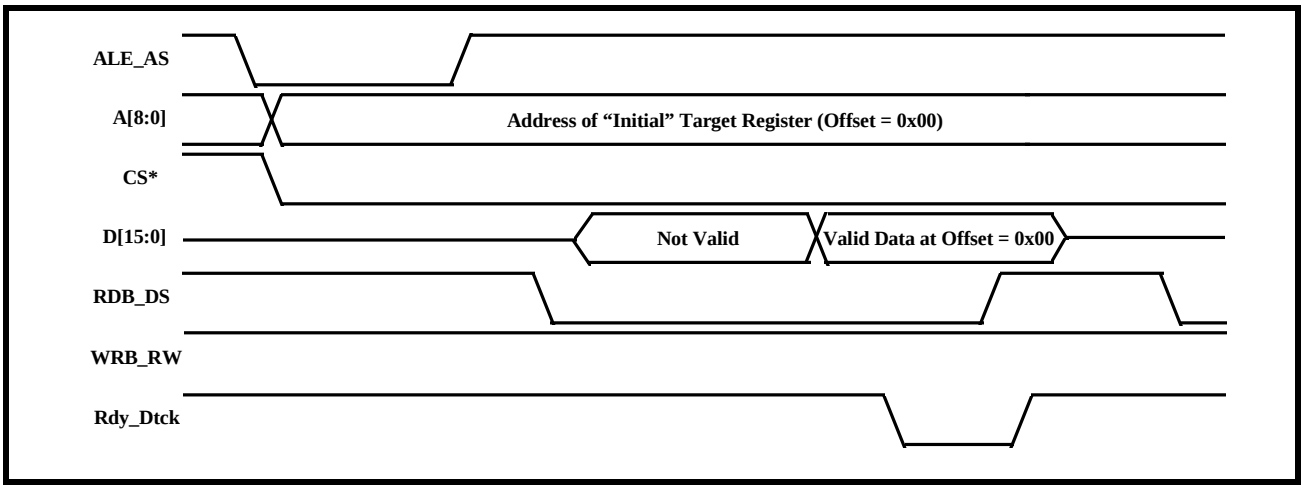
A.6 Next the µC/µP should initiate the current bus cycle by toggling the $\overline{Rd}$_DS (Data Strobe) input pin "low". This step will enable the bi-directional data bus output drivers, within the XRT72L13 DS3 Framer. At this point, the bi-directional data bus output drivers will proceed to driver the contents of the "Address" register onto the bi-directional data bus.

A.7 After some settling time, the data on the bi-directional data bus will stabilize and can be read by the µC/µP. The XRT72L13 DS3 Framer will indicate that this data can be read by asserting the Rdy_Dtck (DTACK) signal.

A.8 After the µC/µP detects the Rdy_Dtck signal (from the XRT72L13 DS3 Framer) it will terminate the Read Cycle by toggling the "$\overline{Rd}$_DS" (Data Strobe) input pin "high".

Figure 55 presents an illustration of the behavior of the Microprocessor Interface Signals during the "initial" Read Operation, within a Burst I/O Cycle; for a Motorola-type µC/µP.

FIGURE 55. BEHAVIOR OF THE MICROPROCESSOR INTERFACE SIGNALS, DURING THE "INITIAL" READ OPERATION OF A BURST CYCLE (MOTOROLA TYPE PROCESSOR)



At the completion of this initial read cycle, the µC/µP has read in the contents of the first register or buffer location (within the XRT72L13 DS3 Framer) for this particular burst access operation. In order to illustrate how this "burst I/O cycle" works, the byte (or word) of data, that is being read in Figure 55 has been labeled "Valid Data at Offset = 0x00". This indicates that the µC/µP is reading the very first register (or buffer location) in this burst access.

3.2.2.2.2.1.2 The Subsequent Read Operations

The procedure that the µC/µP must use to perform the remaining read cycles, within this Burst Access operation, is presented below.

B.0 Execute each subsequent Read Cycle, as described in steps B.1 through B.3, below.

B.1 Without toggling the ALE_AS input pin (e.g., keeping it "high"); toggle the $\overline{Rd}$_DS (Data Strobe) input pin "low". This step accomplishes the following.

a. The Framer internally increments the "latched address" value (within the Microprocessor Interface circuitry).

b. The output drivers of the "bi-directional" data bus (D[7:0]) are enabled. At some time later, the register or buffer location corresponding to the "incremented" latched address value will be driven onto the bi-directional data bus.

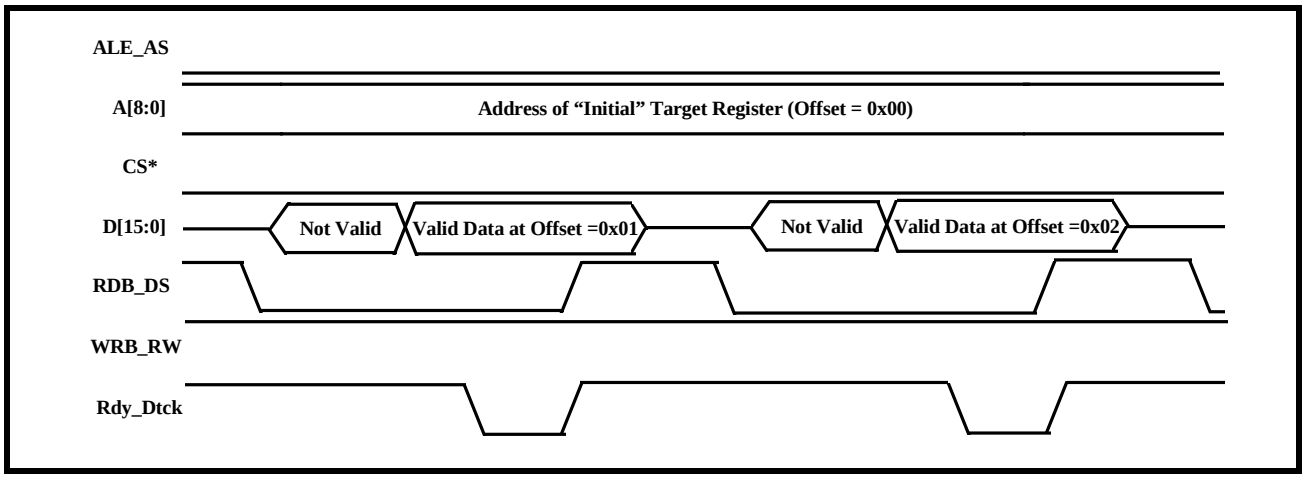
NOTE: *In order to insure that the XRT72L13 DS3 Framer will interpret this signal as being a "Read" signal, the* µC/µP *should keep the $\overline{WR}$_RW input pin "High".*

B.2 After some settling time, the data on the bi-directional data bus will stabilize and can be read by the µC/µP. The XRT72L13 DS3 Framer will indicate that this data is ready to be read by asserting the Rdy_Dtck (DTACK*) signal.

B.3 After the µC/µP detects the Rdy_Dtck signal (from the XRT72L13 DS3 Framer), it terminates the "Read" cycle by toggling the $\overline{Rd}$_DS (Data Strobe) input pin "high".

For subsequent read operations, within this burst cycle, the µC/µP simply repeats steps B.1 through B.3, as illustrated in Figure 56 .

FIGURE 56. BEHAVIOR THE MICROPROCESSOR INTERFACE SIGNALS, DURING SUBSEQUENT "READ" OPERATIONS WITHIN THE BURST I/O CYCLE (MOTOROLA-TYPE µC/µP)



3.2.2.2.2.1.3 Terminating the Burst Access Operation

The Burst I/O Access will be terminated upon the falling edge of the ALE_AS input signal. At this point the Framer will cease to internally increment the "latched" address value. Further, the µC/µP is now free to execute either a "Programmed I/O" access or to start another "Burst Access" Operation with the XRT72L13 DS3 Framer.

3.2.2.2.2 The "Motorola-Mode" Write Burst Access

Whenever a "Motorola-type" µC/µP wishes to write the contents of numerous registers or buffer locations over a "contiguous" range of addresses, then it should do the following.

a. Perform the initial "write" operation; of the burst access.

b. Perform the remaining "write" operations, of the burst access.

c. Terminate the burst access operation.

Each of these "operations" within the burst access are described below.

3.2.2.2.2.1 The Initial Write Operation

The initial write operation of a "Motorola-type" Write Burst Access is accomplished by executing a "Programmed I/O Write Cycle" as summarized below.

A.0 Execute a Single Ordinary (Programmed I/O) Write cycle, as described in Steps A.1 through A.7 below.

A.1 Assert the ALE_AS (Address Strobe) input pin by toggling it "low". This step enables the Address Bus input drivers (within the XRT72L13 DS3 Framer).

A.2 Place the address of the "initial" target register or buffer location (within the Framer), on the Address Bus input pins, A[8:0].

A.3 At the same time, the Address-Decoding circuitry (within the user's system) should assert the CS* input pin of the Framer by toggling it "low". This step enables further communication between the µC/µP and the Framer Microprocessor Interface block.

A.4 After allowing the data on the Address Bus pins to settle (by waiting the appropriate "Address Setup" time), the µC/µP should toggle the ALE_AS input pin "high". This step causes the Framer device to "latch" the contents of the "Address Bus" into its own circuitry. At this

point, the "initial" address of the burst access has now been selected.

A.5 Further, the µC/µP should indicate that this current bus cycle is a "Write" operation by toggling the $\overline{WR}$_RW (R/W*) input pin "low".

A.6 The µC/µP should then place the byte or word that it intends to write into the "target" register, on the bi-directional data bus, D[7:0].

A.7 Next, the µC/µP should initiate the bus cycle by toggling the $\overline{Rd}$_DS (Data Strobe) input pin "low". When the XRT72L13 DS3 Framer senses that the $\overline{WR}$_RW input pin is "low", and that the $\overline{Rd}$_DS input pin has toggled "low" it will enable the "input drivers" of the bi-directional data bus, D[7:0].

A.8 After waiting the appropriate amount of time, for this newly placed data to settle on the bi-directional data bus(e.g., the "Data Setup" time) the Framer will assert the Rdy_Dtck (DTACK) output signal.

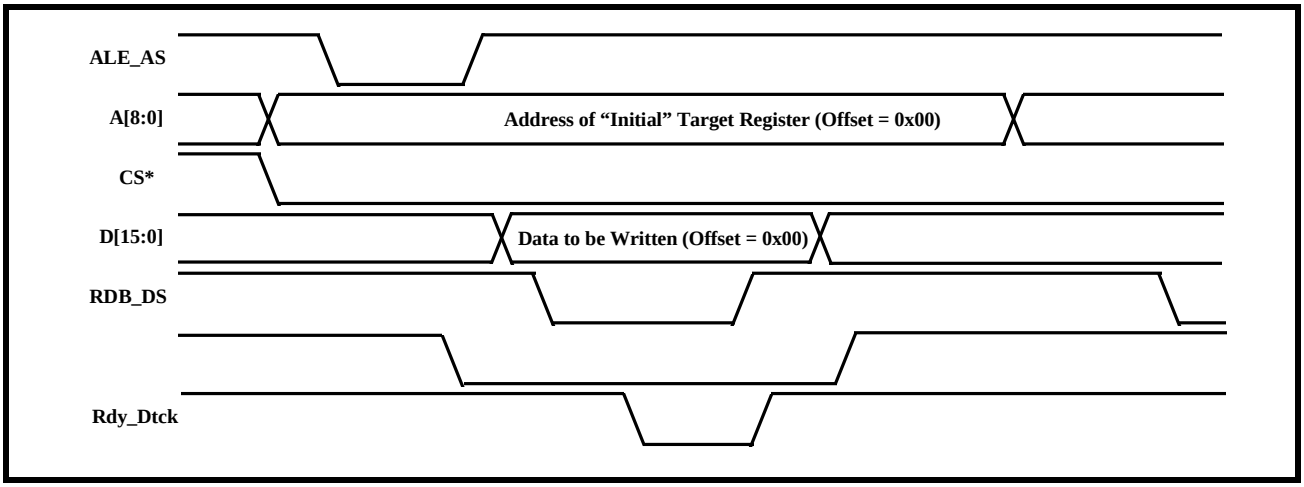
A.9 After the µP/µC detects the Rdy_Dtck signal (from the Framer) it should toggle the $\overline{Rd}$_DS input pin "high". This action accomplishes two things:

a. It latches the contents of the bi-directional data bus into the XRT72L13 DS3 Framer Microprocessor Interface block.

b. It terminates the "Write" cycle.

Figure 57 presents a timing diagram which illustrates the behavior of the Microprocessor Interface signals, during the "Initial" write operation within a Burst Access, for a "Motorola-type" µC/µP.

FIGURE 57. BEHAVIOR OF THE MICROPROCESSOR INTERFACE SIGNALS, DURING THE "INITIAL" WRITE OPERATION OF A BURST CYCLE (MOTOROLA-TYPE PROCESSOR)



At the completion of this initial write cycle, the µC/µP has written a byte or word into the first register or buffer location (within the XRT72L13 DS3 Framer) for this particular burst I/O access. In order to illustrate how this "burst I/O cycle" works, the byte (or word) of data, that is being written in Figure 57 has been labeled "Data to be Written (Offset = 0x00)."

3.2.2.2.2.2.2 The Subsequent Write Operations

The procedure that the µC/µP must use to perform the remaining write cycles, within this burst access operation, is presented below.

B.0 Execute each subsequent write cycle, as described in Steps B.1 through B.3

B.1 Without toggling the ALE_AS (Address Strobe) input pin (e.g., keeping it "high"); apply the value of the next byte or word (to be written into the Framer) to the bi-directional data bus pins, D[7:0].

B.2 Toggle the $\overline{Rd}$_DS (Data Strobe) input pin "low". This step accomplishes the following.

a. The Framer internally increments the "latched address" value (within the Microprocessor Interface).

b. The input drivers of the bi-directional data bus are enabled.

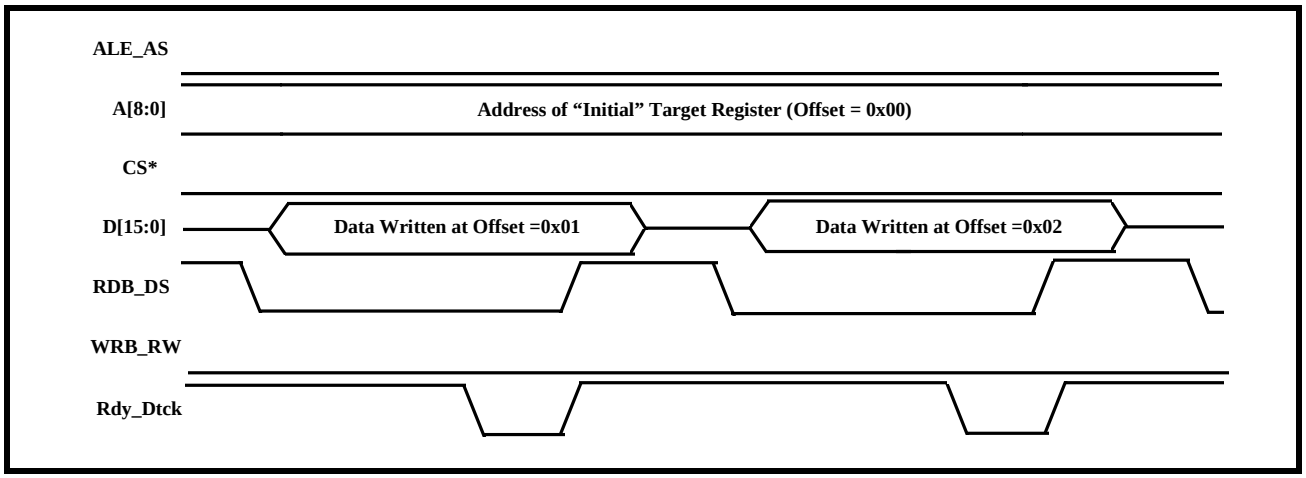
NOTE: *In order to insure that the XRT72L13 DS3 Framer will interpret this signal as being a "Write" signal, the* µC/µP *should keep the* $\overline{WR}$*_RW input pin "low".*

B.3 After some settling time, the data, in the internal data bus, will stabilize and is ready to be latched into the Framer Microprocessor Interface block. The Microprocessor Interface block

will indicate that this data is ready to be latched by asserting the Rdy_Dtck (DTACK) output signal. At this point, the µC/µP should latch the data into the Framer by toggling the $\overline{Rd}$_DS input pin "high".

For subsequent write operations, within this burst I/O access, the µC/µP simply repeats steps B.1 through B.3 as illustrated in Figure 58 .

FIGURE 58. BEHAVIOR OF THE MICROPROCESSOR INTERFACE SIGNALS, DURING SUBSEQUENT "WRITE" OPERATIONS WITH THE BURST I/O CYCLE (MOTOROLA-TYPE µC/µP)



3.2.2.2.2.3 Terminating the Burst I/O Access

The Burst I/O Access will be terminated upon the falling edge of the ALE_AS input signal. At this point the Framer will cease to internally increment the "latched" address value. Further, the µC/µP is now free to execute either a "Programmed I/O" access or to start another "Burst I/O Access" with the XRT72L13 DS3 Framer.

3.3 ON-CHIP REGISTER ORGANIZATION

The Microprocessor Interface section, within the Framer allows the user to do the following.

- Configure the Framer into a wide variety of operating modes.
- Employ various features of the Framer.
- Perform status monitoring
- Enable/Disable and service Interrupt Conditions

All of these things are accomplished by reading from and writing to the many on-chip registers within the Framer. Table 4 lists each of these registers and their corresponding address locations within the Framer Address space.

3.3.1 Framer Register Addressing

The array of on-chip registers consists of a variety of register types. These registers are denoted in Table 4, as follows.

R/O - Read Only Registers.

R/W - Read/Write Registers

RUR - Reset-upon-Read Registers

Additionally, some of these registers consists of both "R/O" and "R/W" bit-fields. These registers are denoted in Table 4 as "Combination of R/W and R/O".

The bit-format and definitions for each of these registers are presented in Section 3.3.2

3.3.2 M13 Mux/Framer Register Description

This section provides a function description of each bit-field within each of the on-chip Framer Register.

NOTE: *For all on-chip registers, a table containing the bit-format of the register is presented. Additionally, these tables also contain the default values for each of these register bits. Finally, the function description, associated with each register bit-field is presented, along with a reference to a Section Number, within this Data Sheet, that provides a more in-depth discussion of the functions associated with this register bit-field.*

3.3.2.1 Operating Mode Register

OPERATING MODE REGISTER (ADDRESS = 0X00)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Local Loop-back Mode	Line Loop-back Mode	Internal LOS Enable	RESET	Interrupt Enable RESET	Frame Format	TimRefSel[1]	TimRefSel[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	1	0	1	0	1	1

Bit 7 - Local Loop-back Mode

This bit-field permits the user to configure the XRT72L13 M13 device to operate in the “Local Loop-back” Mode.

Setting this bit-field to “1” configures the XRT72L13 M13 chip to operate in the “Local Loopback” Mode. Setting this bit-field to “0” configures the XRT72L13 M13 chip to not operate in the “Local Loopback” Mode.

Bit 6 - Line Loopback Mode

This bit-field permits the user to configure the XRT72L13 M13 device to operate in the “Line Loop-back” Mode.

Setting this bit-field to “1” configures the XRT72L13 M13 chip to operate in the “Line Loopback” Mode. Setting this bit-field to “0” configures the XRT72L13 M13 chip to not operate in the “Line Loopback” Mode.

Bit 5 - Internal LOS Enable

This “Read/Write” bit-field permits the user to configure the XRT72L13 M13 chip to either declare an LOS (Loss of Signal) condition, based upon the “Internal Circuit’s” criteria or not.

Setting this bit-field to “0” configures the XRT72L13 M13 chip to NOT declare an LOS condition, based upon its own internal criteria.

Setting this bit-field to “1” configures the XRT72L13 LOS condition, based upon its own internal criteria.

NOTES:

1. *The XRT72L13 M13 chip will declare an “LOS” condition anytime the RLOS input pin is set “high” independent of the setting of this bit-field.*
2. *For more information on the XRT72L13 M13 chip’s “internal criteria” for “Loss of Signal” please see Section _.*

Bit 4 - RESET

This “Read/Write” bit-field permits the user to command the XRT72L13 M13 chip into a software reset state. If the XRT72L13 M13 chip is commanded into the “RESET” state, all of its internal register bits will automatically be set to their default condition.

The user can configure the XRT72L13 to operate in the “RESET” state by inducing a “0” to “1” transition in this bit-field.

Bit 3 - Interrupt Enable RESET

This “Read/Write” bit-field permits the user to configure the XRT72L13 M13 chip to automatically disable all Interrupts that are activated.

Setting this bit-field to “0” configures the XRT72L13 M13 chip to NOT disable the Interrupt Enable Status” of any interrupt following their activation.

Setting this bit-field to “1” configures the XRT72L13 M13 to disable the Interrupt Enable Status” of any interrupt following their activation.

For more information on this feature, please see Section _.

Bit 2 - Frame Format Select

This “Read/Write” bit-field permits the user to select the Framing format that the XRT72L13 M13 device will be operating in.

Setting this bit-field to “0” configures the XRT72L13 M13 device to operate in the C-Bit Parity Framing Format.

Setting this bit-field to “1” configures the XRT72L13 M13 device to operate in the M13 Framing Format.

Bits 1 and 0 - TimRefSel[1:0] - Timing Reference Select

These two “Read/Write” bit-fields permits the user to select both a “Framing Reference” and a “Timing Reference” for the Transmit Section of the XRT72L1372L13. The following table relates the states of the two-fields to the selected “Framing” and “Timing” references.

TIMREFSEL[1:0]	FRAMING REFERENCE	TIMING REFERENCE
00	Asynchronous	RxLineClk Input signal
01	TxFrameRef	RxLineClk Input signal
10	Asynchronous	TxInClk Input signal
11	Asynchronous	TxInClk Input signal

NOTE: *For more information on Framing and Timing References, please see Section _.*

3.3.2.2 I/O Control Register

I/O CONTROL REGISTER (ADDRESS = 0X01)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Disable TxLOC	LOC	Disable RxLOC	AMI/B3ZS* Line Code	Single-Rail/ Dual-Rail*	TxClkInv	RxClkInv	Reframe]
R/W	RO	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	0	0	0	0

Bit 7 - Disable TxLOC

Bit 6 - LOC (Loss of Clock) Indicator

Bit 5 - Disable RxLOC

Bit 4 - AMI/B3ZS* Line Code Select

This “Read/Write” bit-field pemits the user to configure the XRT72L13 M13 device to transmit and receive data via the AMI (Alternate Mark Inversion) line code or via the B3ZS (Bipolar 3 Zero Substitution) line code.

Setting this bit-field to “0” configures the XRT72L13 M13 device to transmit and receive data (via the DS3 Framer block) via the B3ZS format. Setting this bit-field to “1” configures the XRT72L13 M13 device to transmit and receive data via the AMI line code.

Bit 3 - Single-Rail/Dual-Rail Select

This “Read/Write” bit-field permits the user to configure the XRT72L13 M13 device to operate in the “Single-Rail” or “Dual-Rail” format.

Setting this bit-field to “0” configures the XRT72L13 to operate in the “Dual-Rail” Mode. In this mode, the “Transmit Section” of the XRT72L13 M13 device will output data to the LIU via the “TxPOS” and “TxNEG” output pins. Additionally, the “Receive Section” of the device will receive data from the LIU via “RxPOS” and “RxNEG” input pins.

Setting this bit-field to “1” configures the XRT72L13 to operate in the “Single-Rail” Mode. In this mode, the “Transmit Section” of the XRT72L13 M13 device will output data to the LIU, in a binary data stream manner via the “TxPOS” output pin. Additionally, the “Receive Section” of the device will receive data from the LIU, in a binary data stream manner, via the RxPOS input pin.

Bit 2 - TxClkInv

This “Read/Write” bit-field permits the user to configure the XRT72L13 M13 device to output data, via the “TxPOS” and “TxNEG” output pins, upon the “rising” or “falling” edge of “TxLineClk”.

Setting this bit-field to “0” configures the XRT72L13 M13 device to output data via the “TxPOS” and “TxNEG” output pins, on the “rising” edge of “TxLineClk”.

Setting this bit-field to “1” configures the XRT72L13 M13 device to output data via the “TxPOS” and “TxNEG” output pins, on the “falling” edge of “TxLineClk”.

Bit 1 - RxClkInv

This “Read/Write” bit-field permits the user to configure the XRT72L13 M13 device to latch data on the “RxPOS” and “RxNEG” input pins input pins, into the XRT72L13 M13 device, on the “rising” or “falling” edge of “RxLineClk”.

Setting this bit-field to “0” configures the XRT72L13 M13 device to latch the data on the “RxPOS” and “RxNEG” input pins, into the device, on the “rising” edge of “RxLineClk”.

Setting this bit-field to “1” configures the XRT72L13 M13 device to latch the data on the “RxPOS” and “RxNEG” input pins, into the device, on the “falling” edge of “RxLineClk”.

Bit 0 - Reframe

This “Read/Write” bit-field permits the user to configure the “Receive Section” of the XRT72L13 M13 device to start a new frame search. A “0” to “1” transition in this bit-field will force the chip to start a new frame search.

3.3.2.3 Part Number Register

PART NUMBER REGISTER (ADDRESS = 0X02)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Part Number Value							
RO	RO	RO	RO	RO	RO	RO	RO
0	0	1	0	0	0	1	0

The Part Number Register (within the XRT72L13 M13 device) contains the fixed value of “0x22”. This part number value permits the user to read out the contents of this register and to uniquely identify this device as the “XRT72L13 M13” device.

3.3.2.4 Version Number Register

VERSION NUMBER REGISTER (ADDRESS = 0X03)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Version Number Value							
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	1

The “Version Number” register (within the XRT72L13 M13 device) contains a value which corresponds to the “Revision Number”. The very first Revision of the XRT72L13 (Revision A) will contain the fixed value “0x01”. The contents of the “Version Number” register will be incremented for subsequent version (if needed).

3.3.2.5 Block Interrupt Enable Register

BLOCK INTERRUPT ENABLE REGISTER (ADDRESS = 0X04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Rx DS3 Interrupt Enable	Not Used	Not Used	M13 Interrupt Enable	Not Used	Not Used	Tx DS3 Interrupt Enable]	One Second Interrupt Enable]
R/W	R/O	R/O	R/W	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

Bit 7 - Rx DS3 Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable all “Receive DS3 Framer” related interrupts (within the XRT72L13) at the “Block Level”.

Setting this bit-field to “0” disables all “Receive DS3 Framer” related interrupts within the XRT72L13 M13 device.

Setting this bit-field to “1” enables all “Receive DS3 Framer” related interrupts (within the XRT72L13 M13 device) at the “Block Level”.

NOTE: *Setting this bit-field to “1” does not enable all “Receive DS3 Framer” related interrupts. Each of these interrupts can still be disabled at the “Source” Level. However, setting this bit-field to “0” does disable all “Receive DS3 Framer” related interrupt.*

Bit 4 - M13 Interrupt Enable

This “Read/Write” bit-field permits the user to enable- or disable all “M13 Multiplexer” related interrupts (within the XRT72L13) at the “Block Level.

Setting this bit-field to “0” disables all “M13 Multiplexer” related interrupts within the XRT72L13 M13 device.

Setting this bit-field to “1” disables all “M13 Multiplexer” related interrupts (within the XRT72L13 M13 device) at the “Block Level”.

Bit 1 - Tx DS3 Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “Transmit DS3 Framer” related interrupts (within the XRT72L13) at the Block Level.

Setting this bit-field to “0” disables all “Transmit DS3 Framer” related interrupts within the XRT72L13 M13 device.

Setting this bit-field to “1” disables all “Transmit DS3 Framer” related interrupts (within the XRT72L13 M13 device) at the “Block Level”.

Bit 0 - One Second Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “One Second” Interrupt, within the XRT72L13. If this interrupt is enabled then the XRT72L13 will generate interrupts to the Microprocessor/Microcontroller at “one-second” intervals.

Setting this bit-field to “0” disables the “One Second” interrupt. Conversely, setting this bit-field to “1” enables the “One Second” interrupt.

3.3.2.6 Block Interrupt Status Register

BLOCK INTERRUPT STATUS REGISTER (ADDRESS = 0X05)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Rx DS3 Interrupt Status	Not Used	Not Used	M13 Interrupt Status	Not Used	Not Used	Tx DS3 Interrupt Status	One Second Interrupt Status
R/O	R/O	R/O	R/O	R/O	R/O	R/O	RUR
0	0	0	0	0	0	0	0

Bit 7 - Rx DS3 Interrupt Status

This “Read-Only” bit-field indicates whether or not a “Receive DS3 Framer” related Interrupt has been requested and is awaiting service.

If this bit-field is set to “0”, then there are no “Receive DS3 Framer” related interrupts awaiting service. Conversely, if this bit-field is set to “1”, then there is at least one “Receive DS3 Framer” related interrupt, awaiting service.

Bit 4 - M13 Multiplexer Interrupt Status

This “Read-Only” bit-field indicates whether or not an “M13 Multiplexer” related interrupt has been requested and is awaiting service.

If this bit-field is set to “0”, then there are no “M13 Multiplexer” related interrupts awaiting service. Conversely, if this bit-field is set to “1”, then there is at least one “M13 Multiplexer” related interrupt, awaiting service.

Bit 1 - Tx DS3 Interrupt Status

This “Read-Only” bit-field indicates whether or not a “Transmit DS3 Framer” related interrupt has been requested and is awaiting service.

If this bit-field is set to “0”, then there are no “Transmit DS3 Framer” related interrupts awaiting service. Conversely, if this bit-field is set to “1”, then there is at least one “Transmit DS3 Framer” related interrupt, awaiting service.

Bit 0 - One Second Interrupt Status

This “Reset-upon-Read” bit-field indicates whether or not a “One Second” interrupt has been requested and is awaiting service.

If this bit-field is set to “0”, then the “One Second” interrupt is not awaiting service. Conversely, if this bit-field is set to “1”, then the “One Second” interrupt is awaiting service.

NOTE: *This bit-field will be cleared immediately after the Microprocessor/Microcontroller has read this register.*

3.3.2.7 RxFIFO Control Register

RXFIFO CONTROL REGISTER (ADDRESS = 0X06)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	RxFIFO32	RxFIFO Enable
R/O	R/O	R/O	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

Bit 1 - RxFIFO32 - 32/64 Operating Depth Select

This “Read/Write” bit-field permits the user to configure the operating depth of the “de-jitter” FIFO to be either 32 or 64 bits.

Setting this bit-field to “0” configures the operating depth of the “De-Jitter” FIFO to be 64 bits.

Setting this bit-field to “1” configures the operating depth of the “De-Jitter” FIFO to be 32 bits.

NOTE: *This bit-field is ignored if the “De-Jitter FIFO” is disabled.*

Bit 0 - RxFIF0 Enable

This “Read/Write” bit-field permits the user to enable or disable the “De-Jitter” FIFO within the XRT72L13.

Setting this bit-field to “0” disables the “De-Jitter” FIFO.

Setting this bit-field to “1” enables the “De-Jitter” FIFO

3.3.2.8 M23 Configuration Register

M23 CONFIGURATION REGISTER (ADDRESS = 0X07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	Payload HDLC Controller Enable	RxDS1Clk Gapped (CRC-32)	M13 Disable	M13 Loopback/ (Remote Loopback)	Tributary Polarity	M23 Loopback Code[1]	M23 Loopback Code[0]
R/O	R/O	R/O	R/O	R/O	R/O	R/O	RUR
0	0	0	0	0	0	0	0

Bit 6 - Payload HDLC Controller Enable

This bit-field along with “M13 Disable” (bit 4) pemits the user to specify whether the XRT72L13 M13 device is to operate in either of the following modes.

- The “M13/Channelized” Mode
- The “DS3 Clear Channel Framer” Mode
- The “High Speed HDLC Controller” Mode.

The relationship between these two bit-fields and the resulting operating operating mode of the XRT72L13 M13 device is tabulated below.

PAYLOAD HDLC CONTROLLER ENABLE	M13 DISABLE	RESULTING OPERATING MODE
0	0	M13/ Channelized Mode
0	1	DS3 Clear Channel Framer Mode
1	0	M13/ Channelized Mode
1	1	High Speed HDLC Controller Mode

Bit 5 - RxDS1Clk Gapped (CRC-32) Select

The exact functionality of this bit-field depends upon whether the user is operating the XRT72L13 in the "M13-Channelized" or in the "High Speed HDLC Controller" Mode.

M13-Channelized Mode - RxDS1 Gapped Clock Select

In the "M13-Channelized" Mode, then this bit-field permits the user to either enable or disable the 28 Digital PLL blocks within the XRT72L13 M13 device.

Setting this bit-field to "0" enables all 28 of these Digital PLL blocks. In this mode, all 28 (or 21) of the RxDS1Clk and RxDS1Data output signals will be smoothed by an internal Digital PLL. This permits the user to interface the "Receive DS1/E1" Output interface to an external DS1 or E1 LIU IC.

Setting this bit-field to "1" disables all 28 of these Digital PLL blocks. In this mode, all 28 (or 21) of the RxDS1Clk and RxDS1Data output signals will NOT be smoothed by an internal Digital PLL, and will contain gaps.

HDLC Controller Mode - CRC16/32 Select

In the "High Speed HDLC Controller" Mode, this bit-field permits the user to configure the XRT72L13 to compute and verify a CRC-16 or CRC-32 value within the HDLC frame.

Setting this bit-field to "0" configures the XRT72L13 to compute and verify a CRC-16 value in each HDLC frame.

Setting this bit-field to "1" configures the XRT72L13 to compute and verify a CRC-32 value in each HDLC frame.

Bit 4 - M13 Disable

This bit-field along with "Payload HDLC Controller Enable" (bit 6) pemits the user to specify whether the XRT72L13 M13 device is to operate in either of the following modes.

- The "M13/Channelized" Mode
- The "DS3 Clear Channel Framer" Mode
- The "High Speed HDLC Controller" Mode.

The relationship between these two bit-fields and the resulting operating operating mode of the XRT72L13 M13 device is tabulated below.

PAYLOAD HDLC CONTROLLER ENABLE	M13 DISABLE	RESULTING OPERATING MODE
0	0	M13/ Channelized Mode
0	1	DS3 Clear Channel Framer Mode
1	0	M13/ Channelized Mode
1	1	High Speed HDLC Controller Mode

Bit 3 - M13Loopback/Remote Loopback

The exact functionality of this bit-field depends upon whether the user is operating the XRT72L13 in the "M13-Channelized" or in the "High Speed HDLC Controller" Mode.

M13-Channelized Mode - M13 Loopback Select

If the XRT72L13 is operating in the "M13 Channelized" Mode, then this bit-field functions as the "M13 Loopback" select bit-field.

Setting this bit-field to "0" disables the "M13 Loopback" Mode. In this mode, the Receive M13 Block will accept data from the Rx DS3 Framer block (Normal Operation).

Setting this bit-field to “1” enables the “M13 Loopback” Mode. In this mode, the Receive M13 Block accepts data from the “Transmit M13 Block” (the Transmit and Receive DS3 Framer blocks are bypassed).

High Speed HDLC Controller Mode - Remote Loopback Select

If the XRT72L13 is operating in the “High Speed HDLC Controller” Mode, then this bit-field functions as the “Remote Loopback” select bit-field.

Setting this bit-field to “0” disables the “Remote Loopback” Mode.

Setting this bit-field to “1” enables the “Remote Loopback” Mode.

Bit 2 - Tributary Polarity

This “Read/Write” bit-field permits the user to select the clock edge at which (a) the XRT72L13 M13 device will sample and latch the “Transmit DS1/E1” and Transmit HDLC data, and (b) the XRT72L13 will output the “Receive DS1/E1” and Receive HDLC data.

Setting this bit-field to “0” configures the XRT72L13 M13 device to (a) sample and latch the “Transmit DS1/E1” and “Transmit HDLC” data on the rising edge of the appropriate clock signal; and (b) to output the “Receive DS1/E1” and “Receive HDLC” data on the rising edge of the appropriate clock signal.

Setting this bit-field to “1” configures the XRT72L13 M13 device to (a) sample and latch the “Transmit DS1/E1” and “Transmit HDLC” data on the falling edge of the appropriate clock signal; and (b) to output the “Receive DS1/E1” and “Receive HDLC” data on the falling edge of the appropriate clock signal.

Bits 1 and 0 - M23LBCode[1, 0]

NOTES:*These two “Read/Write” bits permit the user to define which “C-bit” pattern (in the inbound DS3 data stream) will function as the loopback command. these register bits are only used if the XRT72L13 M13 device is operating in the “M13” Framing Format. These register bits are ignored if the XRT72L13 M13 device is operating in the “C-Bit Parity” Framing Format.*

The following table related the contents of these two bit-fields to the “M23 Loopback” code.

A more detailed description of these loopback codes will be presented in Section _.

TABLE 9:

M23LB CODE[1]	M23 LB CODE[0]	RESULTING “M23” LOOPBACK CODE
0	0	Cj1 = Cj2 = *Cj3
0	1	Cj1 = *Cj2 = Cj3
1	0	*Cj1 = Cj2 = Cj3
1	1	Cj1 = Cj2 = *Cj3

3.3.2.9 M23 DS3 AIS Register

M23 TX DS2 AIS REGISTER (ADDRESS = 0X08)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	TxDS2 AIS Channel 6	TxDS2 AIS Channel 5	TxDS2 AIS Channel 4	TxDS2 AIS Channel 3	TxDS2 AIS Channel 2	TxDS2 AIS Channel 1	TxDS2 AIS Channel 0
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bits 6 thru 0 - TxDS2 AIS Channel[6:0]

These seven (7) “Read/Write” bit-fields permits the user to specify which “outbound” DS2 channel will transmit an AIS (All Ones) pattern.

For example, setting “Bit 5” (within this register) to “1” configures the XRT72L13 M13 device to transmit an AIS pattern via the “outbound” (Transmit) DS2 Channel 5. In this mode, the content of the lower tributary

"TxDS1/E1" signals will be over-written by this AIS pattern.

Setting "Bit 5" to "0" configures the "Transmit" DS2 Channel 5 to carry normal traffic (as determined by the lower DS1 or E1 tributaries).

3.3.2.10 M23 Request Loopback Register

M23 REQUEST LOOPBACK REGISTER (ADDRESS = 0X09)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	DS2 Loopback Request Channel 6	DS2 Loopback Request Channel 5	DS2 Loopback Request Channel 4	DS2 Loopback Request Channel 3	DS2 Loopback Request Channel 2	DS2 Loopback Request Channel 1	DS2 Loopback Request Channel 0
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bits 6 thru 0 - DS2 Loopback Request Channel [6:0]

These seven (7) "Read/Write" bit-field permits the user to request that the Remote Terminal Equipment configure one of their DS2 channels to operate in the "Remote Loopback" Mode.

Setting any one of these bit-fields to "1" will cause the XRT72L13 M13 device to insert a "DS2 Remote Loopback Command Request" (for the corresponding DS2 channel) to be inserted into the "outbound" DS3 data stream. The "Remote Terminal Equipment" should respond by executing the appropriate loopback command.

For example, setting Bit 5 (within this register) will cause the XRT72L13 M13 device to insert the "Channel 5 DS2 Remote Loopback Command Register" into the "outbound" DS3 data stream. The Remote Terminal Equipment will be expected to respond by configuring DS2 Channel 5, into the "Remote Loopback" Mode.

NOTE: *This registert is only active if the XRT72L13 M13 device has been configured to operate in the "M13/Channelized" Mode.*

3.3.2.11 M23 Loopback Activation Register

M23 LOOPBACK ACTIVATION REGISTER (ADDRESS = 0X0A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	DS2 Loopback Activation Channel 6	DS2 Loopback Activation Channel 5	DS2 Loopback Activation Channel 4	DS2 Loopback Activation Channel 3	DS2 Loopback Activation Channel 2	DS2 Loopback Activation Channel 1	DS2 Loopback Activation Channel 0
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bits 6 thru 0 - DS2 Loopback Activation Channel [6:0]

These seven (7) "Read/Write" bit-fields permit the user to configure any of the seven DS2 channels into the "Remote Loopback" Mode.

Setting any one of these bit-fields to "1" will cause the corresponding DS2 channel to operate in the "Remote Loopback" Mode.

Setting any one of these bit-fields to "0" will cause the corresponding DS2 channel to terminate "Remote Loopback Mode" operation.

3.3.2.12 M23 RxAIS Register

M23 RX DS2 AIS REGISTER (ADDRESS = 0X0B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	RxDS2 AIS Channel 6	RxDS2 AIS Channel 5	RxDS2 AIS Channel 4	RxDS2 AIS Channel 3	RxDS2 AIS Channel 2	RxDS2 AIS Channel 1	RxDS2 AIS Channel 0
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bits 6 thru 0 - RxDS2 AIS Channel [6:0]

These seven (7) "Read/Write" bit-fields permits the user to specify which "inbound" DS2 channel (which is demultiplexed from the inbound DS3 channel) will carry an AIS (All Ones) pattern.

For example, setting "Bit 5" (within this register) to "1" configures the XRT72L13 M13 device to overwrite the contents of the de-multiplexed DS2 channel (corresponding to channel 5) with the AIS (All Ones) pattern.

Setting "Bit 5" to "0" configures the "Receive" DS2 Channel 5 to carry normal traffic (as de-multiplexed from the inbound DS3 data stream).

3.3.2.13 DS3 Test Register

DS3 TEST REGISTER (ADDRESS = 0X0C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	Rx Payload Clock Enable	Tx Payload Clock Enable	Rx PRBS Lock Indicator	Rx PRBS Enable	Tx PRBS Enable	Rx DS3 Bypass	Tx DS3 Bypass
R/O	R/W	R/W	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit 6 - Rx Payload Clock Enable

This "Read/Write" bit-field permits the user to configure the "Receive Payload Data Output Interface" (of the XRT72L13 M13 device) to generate either (a) a gapped-serial clock signal or (b) an ungapped-serial clock, along with an "RxOHInd" output signal.

Setting this bit-field to "0" configures the XRT72L13 to generate an ungapped (44.736MHz) clock sjgnal via the "RxClk" output pin, and to pulse the "RxOHInd" output pin, coincident with an Overhead bit being output via the "RxSer" output pin.

Setting this bit-field to "1" configures the XRT72L13 to generate a gapped clock signal (e.g., a clock edge for each payload bit) via the "RxOHInd" output pin.

NOTE: *This feature is only applicable if the XRT72L13 has been configured to operate in the "DS3 Clear Channel Framer" Mode.*

Bit 5 - Tx Payload Clock Enable

This "Read/Write" bit-field permits the user to configure the "Transmit Payload Data Input Interface" (or the XRT72L13 M13 device) to generate either (a) a gapped-serial clock signal or (b) an ungapped-serial clock, along with the "TxOHInd" output signal.

Setting this bit-field to "0" configurese the XRT72L13 to accept an ungapped clock (44.736MHz) signal via the "TxInClk" input pin (or to output an ungapped clock signal via the "RxOutClk" output pin). Further, in this mode, the XRT72L13 will pulse the "TxOHInd" output pin one bit period prior to the processing of an overhead bit.

Setting this bit-field to "1" configures the XRT72L13 to generate a gapped clock signal (e.g., a clock edge for each payload bit) via the "TxOHInd" output pin.

NOTE: *This feature is only applicable if the XRT72L13 has been configured to operate in the "DS3 Clear Channel Framer" Mode.*

Bit 4 - Rx PRBS Lock Indicator

This "Read-Only" bit-field indicates whether or not the "PRBS Checker/Receiver has acquired "PRBS Lock" with the payload portion of the "inbound" DS3 data stream.

If this bit-field is set to “0” then the “PRBS Checker/Receiver” has not acquired “PRBS Lock” with the payload portion of the “inbound” DS3 data stream.

Conversely, if this bit-field is set to “1”, then the “PRBS Checker/Receiver” has acquired “PRBS Lock” (or Pattern Sync) with the payload portion of the “inbound” DS3 data stream.

NOTE: *The contents of this bit-field are valid only if the “PRBS Checker/Receiver” is enabled.*

Bit 3 - Rx PRBS Enable

This “Read/Write” bit-field permits the user to enable the “PRBS Checker/Receiver” block within the XRT72L13 M13 device.

Setting this bit-field to “0” disables the “PRBS Checker/Receiver” block.

Setting this bit-field to “1” enables the “PRBS Checker/Receiver” block.

Bit 2 - Tx PRBS Enable

This “Read/Write” bit-field permits the user to enable or disable the “PRBS Generator/Transmitter” block within the XRT72L13 M13 device.

Setting this bit-field to “0” disables the “PRBS Generator/Transmitter” block.

Setting this bit-field to “1” enables the “PRBS Generator/Transmitter” block.

Bit 1 - RxDS3 Bypass

To be defined in the next revision

Bit 0 - TxDS3 Bypass

To be defined in the next revision

3.3.2.14 Rx DS3 Configuration and Status Regsiter

RX DS3 CONFIGURATION AND STATUS REGISTER (ADDRESS = 0X10)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Rx AIS	Rx LOS	Rx Idle	Rx OOF	Reserved	Framing On Parity	FSync Algo	MSync Algo
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit 7 - Rx AIS (Receive AIS Pattern) Indicator

This “Read-Only” bit-field indicates whether or not the “Receive DS3 Framer” block (within the XRT72L13 M13 device) is currently receiving an AIS pattern or not.

The XRT72L13 will set this bit-field to “0” if it is not currently detecting an AIS pattern in the incoming data stream. Conversely, the XRT72L13 will set this bit-field to “1” if it is currently receiving an AIS pattern in the incoming data stream.

NOTE: *For a detailed discussion on the AIS pattern please see Section _.*

Bit 6 - Rx LOS (Receive LOS Condition) Indicator

This “Read-Only” bit-field indicates whether or not the “Receive DS3 Framer” block (within the XRT72L13 M13 device) is currently declaring an LOS (Loss of Signal) condition of the incoming DS3 data stream.

If this bit-field is set to “0”, then the “Receive DS3 Framer” block (within the chip) is currently not declaring an LOS condition.

If this bit-field is set to “1”, then the “Receive DS3 Framer” block (within the chip) is currently declaring an LOS condition.

NOTE: *For more information on the “LOS Declaration” criteria, please see Section _.*

Bit 5 - Rx Idle (Receive Idle Pattern) Indicator

This “Read-Only” bit-field indicates whether or not the “Receive DS3 Framer” block (within the XRT72L13 M13 device) is currently detecting the “Idle Pattern” in the “incoming” DS3 data stream.

If this bit-field is set to “0”, then the Receive DS3 Framer block (within the chip) is currently not detecting the Idle pattern.

If this bit-field is set to “1”, then the Receive DS3 Framer block (within the chip) is currently detecting the Idle pattern.

NOTE: *For more information about the “Idle Pattern”, please see Section _.*

Bit 4 - Rx OOF (Receive Out-of-Frame) Indicator

This “Read-Only” bit-field indicates whether or not the “Receive DS3 Framer” block (within the XRT72L13

M13 device) is currently declaring an “OOF” (Out of Frame) condition.

If this bit-field is set to “0”, then the “Receive DS3 Framer” block (of the chip) is currently not declaring the “OOF” condition.

If this bit-field is set to “1”, then the “Receive DS3 Framer block is currently declaring the “OOF” condition.

NOTE: *For more information on the “OOF” and “In-Frame” Declaration Criteria (for DS3) please see Section _.*

Bit 2 - Framing On Parity ON/OFF Select

This “Read/Write” bit-field permits the user to require that the “Receive DS3 Framer” block include P-Bit Verification as a condition for declaring itself “In-Frame”, during “Frame Acquisition”.

This feature also imposes an additional “Frame Maintenance” requirement on the “Receive DS3 Framer” block. In particular, if this additional requirement is implemented, the “Receive DS3 Framer” block will perform a frame search if it detects P-bit errors in at least 2 out of 5 DS3 frames.

Setting this bit-field to “1” imposes this additional requirement.

Conversely, setting this bit-field to “0” configures the “Receive DS3 Framer” block to waive this requirement.

NOTE: *For more information on “Framing with Parity”, please see Section _.*

Bit 1 - FSync Algo(rithm) Select

This “Read/Write” bit-field, in conjunction with Bits 0 and 2 of this register, allows the user to completely define the “Frame Maintenance” criteria of the “Receive DS3 Framer” block (within the chip). This particular bit-field permits the user to define the “Frame Maintenance” criteria, as it applies to F-bits.

Setting this bit-field to “0” configures the “Receive DS3 Framer” block to declare an “OOF” (Out of Frame” condition) if it determines that 6 out of the last 16 F-bits are in error.

Setting this bit-field to “1” configures the “Receive DS3 Framer” block to declare an “OOF” (Out of Frame” condition) if it determines that 3 out of the last 16 F-bits are in error.

Bit 0 - MSync Algo(rithm) Select

This “Read/Write” bit-field, in conjunction with Bits 1 and 2 of this register, allows the user to completely define the “Frame Maintenance” criteria of the “Receive DS3 Framer” block (within the chip). This particular bit-field permits the user to define the “Frame Maintenance” criteria, as it applies to M-bits.

Setting this bit-field to “0” configures the “Receive DS3 Framer” block to ignore the occurrence of M-bit errors.

Setting this bit-field to “1” configures the “Receive DS3 Framer” block to declare an “OOF” condition if it determines that 3 out of 4 M-bits are in error.

3.3.2.15 RxDS3 Status Register

RX DS3 STATUS REGISTER (ADDRESS = 0X11)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	Not Used	Not Used	RxFERF	RxAIC	RxFEBE[2]	RxFEBE[1]	RxFEBE[0]
R/O	R/W	R/W	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

Bit 4 - RxFERF (Far-End Receive Failure) Indicator

This “Read-Only” bit-field indicates whether or not the “Receive DS3 Framer” block (within the XRT72L13 M13 device) is declaring a FERF (Far-End Receive Failure) condition.

If this bit-field is set to “0”, then the “Receive DS3 Framer” block (of the chip) is currently not declaring an LOS condition.

Conversely, if this bit-field is set to “1”, then the “Receive DS3 Framer” block is currently declaring an LOS condition.

NOTE: *For more information how the “Receive DS3 Framer” block declares a “FERF” condition, please see Section _.*

Bit 3 - RxAIC (Application Identification Channel) indicator

This “Read-Only” bit-field reflects the value of the AIC bit-field, within the incoming DS3 frames, as detected by the “Receive DS3 Framer” block.

This bit-field is set to “1” if the incoming DS3 data stream is determined to be in the “C-bit Parity” format (AIC bit = 1) for at least 63 consecutive frames.

This bit-field is set to “0” if the incoming DS3 data stream is determined to be in the “M13” format (AIC bit = 0).

Bits 2 thru 0 - RxFEBE[2:0]

These “Read-Only” bit-fields reflect the “FEBE” (Far-End Block Error) value, within the most recently received DS3 frame.

If these bit-fields are set to “111”, then it indicates that the “Remote” Receiving Terminal is receiving DS3 frames in an un-erred manner.

Conversely, if these bit-fields are set to any value other than “111”, then it indicates that the “Remote” Receiving Terminal has detected Framing or Parity bit errors in the DS3 frames that it is receiving.

NOTE: *For more information on FEBE (Far-End-Block Error), please see Section _.*

3.3.2.16 RxDS3 Interrupt Enable Register

RX DS3 INTERRUPT ENABLE REGISTER (ADDRESS = 0X12)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Detection of CP-Bit Error Interrupt Enable	Change in LOS Condition Interrupt Enable	Change in AIS Condition Interrupt Enable	Change in Idle Pattern Interrupt Enable	Change in FERF Condition Interrupt Enable	Change in AIC State Interrupt Enable	Change in OOF Condition Interrupt Enable	Detection of P-Bit Error Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit 7 - Detection of CP-Bit Error Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “Detection of CP-Bit Error” interrupt.

Setting this bit-field to “0” disables the “Detection of CP-Bit Error” Interrupt.

Setting this bit-field to “1” enables the “Detection of CP-Bit Error” Interrupt.

Bit 6 - Change in LOS Condition Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “Change in LOS Condition” Interrupt.

Setting this bit-field to “0” disables the “Change in LOS Condition” Interrupt.

Setting this bit-field to “1” enables the “Change in LOS Condition” Interrupt.

Bit 5 - Change in AIS Condition Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “Change in AIS Condition” Interrupt.

Setting this bit-field to “0” disables the “Change in AIS Condition” interrupt.

Setting this bit-field to “1” enables the “Change in AIS Condition” Interrupt.

Bit 4 - Change in Idle Pattern Condition Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “Change in Idle Pattern Condition” interrupt.

Setting this bit-field to “0” disables the “Change in Idle Pattern Condition” interrupt.

Setting this bit-field to “1” enables the “Change in Idle Pattern Condition” interrupt.

Bit 3 - Change in FERF Condition Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “Change in FERF Condition” Interrupt.

Setting this bit-field to “0” disables the “Change in FERF Condition” Interrupt.

Setting this bit-field to “1” enables the “Change in FERF Condition” Interrupt.

Bit 2 - Change in AIC State Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “Change in AIC State” Interrupt.

Setting this bit-field to “0” disables the “Change in AIC State” Interrupt.

Setting this bit-field to “1” enables the “Change in AIC State” Interrupt.

Bit 1 - Change in OOF Condition Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “Change in OOF Condition” Interrupt.

Setting this bit-field to “0” disables the “Change in OOF Condition” Interrupt.

Setting this bit-field to “1” enables the “Change in OOF Condition” Interrupt.

Bit 0 - Detection of P-Bit Error Interrupt Enable

This “Read/Write” bit-field permits the user to enable or disable the “Detection of P-Bit Error” Interrupt.

Setting this bit-field to “0” disables the “Detection of P-Bit Error” Interrupt.

Setting this bit-field to “1” enables the “Detection of P-Bit Error” Interrupt.

3.3.2.17 RxDS3 Interrupt Status Register

RX DS3 INTERRUPT STATUS REGISTER (ADDRESS = 0X13)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Detection of CP-Bit Error Interrupt Status	Change in LOS Condition Interrupt Status	Change in AIS Condition Interrupt Status	Change in Idle Pattern Condition Interrupt Status	Change in FERF Condition Interrupt Status	Change in AIC State Interrupt Status	Change in OOF Condition Interrupt Status	Detection of P-Bit Error Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

Bit 7 - Detection of CP-Bit Error Interrupt Status

This “Reset-upon-Read” bit-field indicates whether or not the “Receive DS3 Framer” block has detected a “CP-Bit Error” in the “inbound” DS3 data stream, since the last time this register was read.

This bit-field will be “0” if the “Detection of CP-Bit Error” interrupt has not occured since the last read of this register.

This bit-field will be “1” if the interrupt has occurred since the last read of this register.

Bit 6 - Change in LOS (Loss of Signal) Condition Interrupt Status

This “Reset-upon-Read” bit-field will be set to “1” if the “Receive DS3 Framer” block has detected a “Change in LOS” condition, since the last time this register was read. If the “Change in LOS Condition” interrupt is enabled, then this bit-field will be asserted under either of the following conditions.

a. When the Receive DS3 Framer block detects the occurrence of an LOS condition (e.g., the occurrence of 180 consecutive “spaces” in the incoming DS3 data stream), and

b. When the Receive DS3 Framer block detects the end of an LOS condition (e.g., when the “Receive DS3 Framer” block detects at least 60 mark pulses in the last 180 bit periods).

The Microprocessor/Microcontroller can determine the state of the LOS condition by reading bit 6, within the “Rx DS3 Configuration and Status” register (Address location = 0x10).

NOTE: *For more information about the “LOS Condition” please see Section _.*

Bit 5 - Change in AIS (Alarm Indication Signal) Condition Interrupt Status

This “Reset-upon-Read” bit-field will be set to “1” if the “Receive DS3 Framer” block has detected a “Change in AIS” condition, since the last time this register was read. If the “Change in AIS Condition” interrupt is enabled, then this bit-field will be asserted under either of the following conditions.

a. When the Receive DS3 Framer block first detects an AIS condition in the inbound DS3 data stream.

b. When the Receive DS3 Framer block has detected the end of an “AIS Condition”.

The Microprocessor/Microcontroller can determine the state of the AIS condition by reading bit 7, within the “Rx DS3 Configuration and Status” Register (Address location = 0x10).

NOTE: *For more information about the “AIS Condition” please see Section _.*

Bit 4 - Change in Idle Pattern Condition Interrupt Status

This “Reset-upon-Read” bit-field is set to “1” when the Receive DS3 Framer block detects a “Change in Idle Condition” in the incoming DS3 data stream. Specifi-

cally, the Receive DS3 Framer block will assert this bit-field under either of the following two conditions.

a. When the Receive DS3 Framer block initially detects the "Idle Pattern" in the "inbound" DS3 data stream.

b. When the Receive DS3 Framer block ceases to detect the "Idle Pattern" in the "inbound" DS3 data stream.

The Microprocessor/Microcontroller can determine the state of the "Idle Pattern Condition" by reading bit 5, within the "Rx DS3 Configuration and Status" register (Address location = 0x10).

NOTE: *For more information about the "Idle Pattern" please see Section _.*

Bit 3 - Change in FERF Condition Interrupt Status

This "Reset-upon-Read" bit-field is set to "1" if the "Receive DS3 Framer" block (within the XRT72L13 M13 device) has detected a "Change in the FERF" Condition, since the last time this register was read.

This bit-field will be asserted under either of the following conditions.

a. When the Receive DS3 Framer block first detects the occurrence of a "FERF" condition in the "inbound" DS3 data stream (e.g., all X-bits are set to "0").

b. When the Receive DS3 Framer block no longer detects the "FERF" condition in the "inbound" DS3 data stream (e.g., all X-bits are set to "1").

The Microprocessor/Microcontroller can determine the state of the of the "FERF" condition by reading bit 4 within the "Rx DS3 Status" register (Address location = 0x11).

NOTE: *For more information about the "FERF" condition, please see Section _.*

Bit 2 - Change in AIC State Interrupt Status

This "Reset-upon-Read" bit-field is set to "1" if the AIC bit-field, within the incoming DS3 data stream, has changed state since the last read of this register.

The Microprocessor/Microcontroller can determine the state of the "AIC" bit-field by reading bit 3, within the "Rx DS3 Status" Register (Address location = 0x11).

NOTE: *For more information on this interrupt condition, please see Section _.*

Bit 1 - Change in OOF Condition Interrupt Status

The "Reset-upon-Read" bit-field is set to "1" if the "Receive DS3 Framer" block (within the XRT72L13) has detected a "Change in the Out-of-Frame" (OOF) condition, since the last time this register was read.

This bit-field will be asserted under either of the following conditions.

a. When the "Receive DS3 Framer" block has detected the appropriate condition to declare an "OOF" condition.

b. When the "Receive DS3 Framer" block has transitioned from the "OOF" condition (Frame Acquisition Mode).

The Microprocessor/Microcontroller can detemine the state of the "OOF" condition by reading bit 4 within the "Rx DS3 Configuration and Status" Register (Address location = 0x10).

NOTE: *For more information about the "OOF" condition, please see Section _.*

Bit 0 - Detection of P-Bit Error Interrupt Status

This "Reset-upon-Read" bit-field indicates whether or not the "Detection of P-Bit Error" interrupt has occurred since the last read of this register.

This bit-field will be "0" if the "Receive DS3 Framer" block (within the XRT72L13 M13 device) has not detected a P-bit error since the last read of this register.

Conversely, this bit-field will be "1" if the "Receive DS3 Framer" block (within the XRT72L13 M13 device) has detected a P-Bit error since the last read of this register.

3.3.2.18 RxDS3 Sync Detect Register

RX DS3 SYNC DETECT REGISTER (ADDRESS = 0X14)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	Not Used	Not Used	Reserved	Reserved	Reserved	F Algorithm	One and Only One
R/O	R/O	R/O	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

Bit 1 - F Algorithm

Bit 0 - One and Only One

3.3.2.19 RxDS3 FEAC Register

RXDS3 FEAC REGISTER (ADDRESS = 0X16)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	RxFEAC[5:0]						Not Used
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	1	1	1	1	1	1	0

This "Read/Write" register contains the latest 6-bit FEAC code that has been "validated" by the Receive FEAC Processor. The contents of this register will be cleared if the previously "validated" code has been "removed" by the FEAC Processor.

3.3.2.20 RxDS3 FEAC Interrupt Enable/Status Register

RXDS3 FEAC INTERRUPT ENABLE/STATUS REGISTER (ADDRESS = 0X17)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			FEAC Valid	RxFEAC Remove Interrupt Enable	RxFEAC Remove Interrupt Status	RxFEAC Valid Interrupt Enable	RxFEAC Valid Interrupt Status
R/O	R/O	R/O	R/O	R/W	RUR	R/W	RUR
0	0	0	0	0	0	0	0

Bit 4 - FEAC Valid

This "Read Only" bit is set to "1" when an incoming FEAC Message Code has been validated by the Receive DS3 Framer. This bit is cleared to "0" when the FEAC code is removed.

NOTE: *For more information on the role of this bit-field and the Receive FEAC Processor, please see Section _.*

Bit 3 - RxFEAC Remove Interrupt Enable

This "Read/Write" bit-field allows the user to enable/disable the "RxFEAC Removal" interrupt. Writing a "1" to this bit enables this interrupt. Likewise, writing a "0" to this bit-field disables this interrupt.

NOTE: *For more information on the role of this bit-field and the Receive FEAC Processor, please see Section _.*

Bit 2 - RxFEAC Remove Interrupt Status

A "1" in this "Read Only" bit-field indicates that the last "validated" FEAC Message has now been removed by the Receive FEAC Processor. The Receive FEAC Processor will remove a validated FEAC message if 3 out of the last 10 received FEAC messages differ from the latest valid FEAC Message.

NOTE: *For more information on this bit-field and the Receive FEAC Processor, please see Section _.*

Bit 1 - RxFEAC Valid Interrupt Enable

This "Read/Write" bit-field allows the user to enable/disable the "Rx FEAC Valid" interrupt. Writing a "1" to this bit-field enables this interrupt. Whereas, writing a "0" disables this interrupt. The value of this bit-field is "0" following power up or reset.

NOTE: *For more information on this bit-field and the Receive FEAC Processor, please see Section _.*

Bit 0 - RxFEAC Valid Interrupt Status

A "1" in this "Read Only" bit-field indicates that a newly received FEAC Message has been validated by the Receive FEAC Processor.

NOTE: *For more information on this bit-field and the Receive FEAC Processor, please see Section _.*

3.3.2.21 RxDS3 LAPD Control Register

RXDS3 LAPD CONTROL REGISTER (ADDRESS = 0X18)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used				RxLAPD Any	RxLAPD Enable	RxLAPD Interrupt Enable	RxLAPD Interrupt Status
RO	RO	RO	RO	RO	R/W	R/W	RUR
0	0	0	0	0	0	0	0

Bit 3 RxLAPD Any

Bit 2 RxLAPD Enable

This "Read/Write" bit-field allows the user to enable or disable the LAPD Receiver. The LAPD Receiver MUST be enabled before it can begin to receive and process any LAPD Message frames from the incoming DS3 data stream.

Writing a "0" to this bit-field disables the LAPD Receiver (the default condition). Writing a "1" to this bit-field enables the LAPD Receiver.

Bit 1 RxLAPD (Message Frame Reception Complete) Interrupt Enable

This "Read/Write" bit-field allows the user to enable or disable the "LAPD Message Frame Reception Complete" interrupt. If this interrupt is enabled, then the UNI will generate this interrupt to the local µP, once the last bit of a LAPD Message frame has been received and the PMDL message has been extracted and written into the "Receive LAPD Message" buffer.

Writing a "0" to this bit-field disables this interrupt (the default condition). Writing a "1" to this bit-field enables this interrupt.

Bit 0 RxLAPD (Message Reception Complete) Interrupt Status

This "Read-Only" bit field indicates whether or not the "LAPD Message Reception Complete" interrupt has occurred since the last read of this register. The "LAPD Message Reception Complete" interrupt will occur once the LAPD Receiver has received the last bit of a complete LAPD Message frame, extracted the PMDL message from this LAPD Message frame and has written this (PMDL) message frame into the "Receive LAPD Message" buffer. The purpose of this interrupt is to notify the local µP that the "Receive LAPD Message" buffer contains a new PMDL message, that needs to be read and/or processed.

A "0" in this bit-field indicates that the "LAPD Message Reception Complete" interrupt has NOT occurred since the last read of this register. A "1" in this bit-field indicates that the "LAPD Message Reception Complete" interrupt has occurred since the last read of this register.

NOTE: *For more information on the LAPD Receiver, please see Section _.*

3.3.2.22 RxDS3 LAPD Status Register

RXDS3 LAPD STATUS REGISTER (ADDRESS = 0X19)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	RxAbort	RxLAPDType[1:0}		RxCR Type	RxFCS Error	End of Message	Flag Present
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

Bit 6 - RxAbort (Receive Abort Sequence)

This "Read-Only" bit-field indicates whether or not the LAPD Receiver has detected the occurrence of an "Abort Sequence" (e.g., a string of seven or more consecutive "1s") from the "far-end" LAPD Transmitter. A "0" in this bit-field indicates that no "Abort-Sequence" has been detected. A "1" in this bit-field indicates that the "Abort-Sequence" has been detected.

NOTE: *For more information on the LAPD Receiver, please see Section _.*

Bits, 5 and 4 - RxLAPDType[1, 0]

These two "Read Only" bit-fields combine to indicate the "type" of LAPD Message frame that has been received by the LAPD Receiver. The relationship between these two bit-fields and the LAPD Message Type follows:

BIT 5	BIT 4	MESSAGE TYPE	MESSAGE LENGTH
		Test Signal Identification	76 Bytes
0	1	Idle Signal Identification	76 Bytes
		CL Path Identification	76 Bytes
		ITU-T Path Identification	82 Bytes

Bit 3 - RxCR (Command/Response) Type

This "Read Only" bit field indicates the value of the C/R (Command/Response) bit-field of the latest received LAPD Message.

Bit 2 - Rx FCS (Frame Check Sequence) Error

This "Read-Only" bit-field indicates whether or not the LAPD Receiver has detected a "Frame Check Sequence" (FCS) error in the newly received LAPD Message Frame. A "0" in this bit-field indicates that the FCS for the latest received LAPD Message Frame is correct. A "1" in this bit-field indicates that the FCS for the latest received LAPD Message Frame is incorrect.

NOTE: *For more information on the LAPD Receiver, please see Section _.*

Bit 1 - End Of Message

This "Read-Only" bit-field indicates whether or not the LAPD Receiver has completed its reception of the latest incoming LAPD Message frame. The local µP can poll the progress of the LAPD Receiver by periodically reading this bit-field.

A "0" in this bit-field indicates that the LAPD Receiver is still receiving the latest message from the "far end" LAPD Transmitter. A "1" in this bit-field indicates that the LAPD Receiver has finished receiving the complete LAPD Message Frame.

Bit 0 - Flag Present

This "Read-Only" bit-field indicates whether or not the LAPD Receiver has detected the occurrence of the Flag Sequence byte (0x7E). A "0" in this bit-field indicates that the LAPD Receiver does not detect the occurrence of the Flag Sequence byte. A "1" in this bit-field indicates that the LAPD Receiver does detect the occurrence of the Flag Sequence byte.

NOTE: *For more information on the LAPD Receiver, please see Section _.*

3.3.2.23 M12 DS2 # 1 Configuration Register)

M12 DS2 # 1 CONFIGURATION REGISTER (ADDRESS = 0X1A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved 7	Reserved 6	M12 Bypass	M12 G.747	M12 G.747 Res	M12 FERF	M12LBCode[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	1	1	1

Bit 7 - Reserved

This bit-field must be set to “0”, in order for the XRT72L13 M13 device to function properly.

Bit 6 - Reserved

This bit-field must be set to “0” in order for the XRT72L13 M13 device to function properly.

Bit 5 - M12 Bypass

This “Read/Write” bit field permits the user to bypass M12 Multiplexer/De-Multiplexer # 1. By doing this the following will happen.

In the Transmit Direction

- The XRT72L13 M13 device will accept a DS2 clock signal (6.312MHz) via the TxDS1Clk3 input pin.
- The XRT72L13 M13 device will accept a DS2 signal via the TxDS1Data_3 input pin

In the Receive Direction

- The XRT72L13 M13 device will output a DS2 clock signal (6.312MHz) via the RxDS1Clk3 output pin.
- XRT72L13 M13 device will output the contents of DS2 Channel # 1 via the RxDS1Data3 output pin.

Setting this bit-field to “1” configures M12 MUX # 1 and M12 DEMUX # 1 to be bypassed.

Setting this bit-field to “0” enables M12 MUX # 1 and M12 DEMUX # 1.

Bit 4 - M12 G.747

This “Read/Write” bit-field permits the user to configure M12 MUX # 1 and DEMUX # 1 to support either a DS2 signal or an ITU-T G.747 signal.

Setting this bit-field to “0” configures M12 # 1 to support DS2. In this mode, the M12 MUX will accept four DS1 signals (via TxDS1Data0 thru TXDS1Data3) and will muitiplex these signals into a DS2 signal. Likewise, the M12 DEMUX will accept an incoming DS2 signal (from the M23 DEMUX) and will de-multiplex this signal into 4 DS1 signals. These four DS1 signals will be output via the “RxDS1Data0” thru “RxDS1Data3” output pins.

Setting this bit-field to “1” configures M12 # 1 to

support ITU-T G.747. In this mode, the M12 MUX will accept 3 E1 signals (via TxDS1Data0 thru TxDS1Data2) and will multiplex these signals into an ITU-T G.747 signal. Likewise, the M12 DEMUX will accept an incoming ITU-T G.747 signal (from the M23 DEMUX) and will de-multiplexe this signal into 3 E1 signals. These three E1 signals will output via the “RxDS1Data0” thru “RxDS1Data2” output pins.

Bit 3 - M12G.747 Reserved

Bit 2 - M12 FERF

This “Read/Write” bit-field permits the user to force M12 MUX # 1 to transmit a “FERF” (Far-End-Receive Failure) indicator to the M23 MUX (and in turn to the remote terminal equipment).

Setting this bit-field to “1” configures the M12 MUX to set the “X-bits” (within the “outbound” DS2 data stream) to “0”. This signaling will be interpreted (by the remote terminal equipment) as a FERF indicator.

Settiing this bit-field to “0” configures the M12 MUX to set the “X-bits” (within the “outbound” DS2 data stream) to “1”. This signaling will be interpreted (by the remote terminal equipment) as an indication of no FERF.

Bits 1 and 0 M12 LB Code[1:0]

3.3.2.24 M12 DS2 # 2 Configuration Register)

M12 DS2 # 2 CONFIGURATION REGISTER (ADDRESS = 0X1B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved 7	Reserved 6	M12 Bypass	M12 G.747	M12 G.747 Res	M12 FERF	M12LBCode[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	1	1	1

Bit 7 - Reserved

This bit-field must be set to “0”, in order for the XRT72L13 M13 device to function properly.

Bit 6 - Reserved

This bit-field must be set to “0” in order for the XRT72L13 M13 device to function properly.

Bit 5 - M12 Bypass

This “Read/Write” bit field permits the user to bypass M12 Multiplexer/De-Multiplexer # 1. By doing this the following will happen.

In the Transmit Direction

- The XRT72L13 M13 device will accept a DS2 clock signal (6.312MHz) via the TxDS1Clk7 input pin.
- The XRT72L13 M13 device will accept a DS2 signal via the TxDS1Data_7 input pin

In the Receive Direction

- The XRT72L13 M13 device will output a DS2 clock signal (6.312MHz) via the RxDS1Clk7 output pin.
- XRT72L13 M13 device will output the contents of DS2 Channel # 2 via the RxDS1Data7 output pin.

Setting this bit-field to “1” configures M12 MUX # 1 and M12 DEMUX # 2 to be bypassed.

Setting this bit-field to “0” enables M12 MUX # 1 and M12 DEMUX # 2.

Bit 4 - M12 G.747

This “Read/Write” bit-field permits the user to configure M12 MUX # 2 and DEMUX # 2 to support either a DS2 signal or an ITU-T G.747 signal.

Setting this bit-field to “0” configures M12 # 1 to support DS2. In this mode, the M12 MUX will accept four DS1 signals (via TxDS1Data0 thru TXDS1Data3) and will muitiplex these signals into a DS2 signal. Likewise, the M12 DEMUX will accept an incoming DS2 signal (from the M23 DEMUX) and will de-multiplex this signal into 4 DS1 signals. These four DS1 signals will be output via the “RxDS1Data0” thru “RxDS1Data3” output pins.

Setting this bit-field to “1” configures M12 # 2 to

support ITU-T G.747. In this mode, the M12 MUX will accept 3 E1 signals (via TxDS1Data4 thru TxDS1Data6) and will multiplex these signals into an ITU-T G.747 signal. Likewise, the M12 DEMUX will accept an incoming ITU-T G.747 signal (from the M23 DEMUX) and will de-multiplexe this signal into 3 E1 signals. These three E1 signals will output via the “RxDS1Data4” thru “RxDS1Data6” output pins.

Bit 3 - M12G.747 Reserved

Bit 2 - M12 FERF

This “Read/Write” bit-field permits the user to force M12 MUX # 2 to transmit a “FERF” (Far-End-Receive Failure) indicator to the M23 MUX (and in turn to the remote terminal equipment).

Setting this bit-field to “1” configures the M12 MUX to set the “X-bits” (within the “outbound” DS2 data stream) to “0”. This signaling will be interpreted (by the remote terminal equipment) as a FERF indicator.

Settiing this bit-field to “0” configures the M12 MUX to set the “X-bits” (within the “outbound” DS2 data stream) to “1”. This signaling will be interpreted (by the remote terminal equipment) as an indication of no FERF.

Bits 1 and 0 M12 LB Code[1:0]

3.3.2.25 M12 DS2 # 3 Configuration Register)

M12 DS2 # 3 CONFIGURATION REGISTER (ADDRESS = 0X1C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved 7	Reserved 6	M12 Bypass	M12 G.747	M12 G.747 Res	M12 FERF	M12LBCode[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	1	1	1

Bit 7 - Reserved

This bit-field must be set to “0”, in order for the XRT72L13 M13 device to function properly.

Bit 6 - Reserved

This bit-field must be set to “0” in order for the XRT72L13 M13 device to function properly.

Bit 5 - M12 Bypass

This “Read/Write” bit field permits the user to bypass M12 Multiplexer/De-Multiplexer # 3. By doing this the following will happen.

In the Transmit Direction

- The XRT72L13 M13 device will accept a DS2 clock signal (6.312MHz) via the TxDS1Clk11 input pin.
- The XRT72L13 M13 device will accept a DS2 signal via the TxDS1Data_11 input pin

In the Receive Direction

- The XRT72L13 M13 device will output a DS2 clock signal (6.312MHz) via the RxDS1Clk11 output pin.
- XRT72L13 M13 device will output the contents of DS2 Channel # 2 via the RxDS1Data11 output pin.

Setting this bit-field to “1” configures M12 MUX # 3 and M12 DEMUX # 3 to be bypassed.

Setting this bit-field to “0” enables M12 MUX # 3 and M12 DEMUX # 3.

Bit 4 - M12 G.747

This “Read/Write” bit-field permits the user to configure M12 MUX # 3 and DEMUX # 3 to support either a DS2 signal or an ITU-T G.747 signal.

Setting this bit-field to “0” configures M12 # 3 to support DS2. In this mode, the M12 MUX will accept four DS1 signals (via TxDS1Data8 thru TXDS1Data11) and will muitiplex these signals into a DS2 signal. Likewise, the M12 DEMUX will accept an incoming DS2 signal (from the M23 DEMUX) and will de-multiplex this signal into 4 DS1 signals. These four DS1 signals will be output via the “RxDS1Data8” thru “RxDS1Data11” output pins.

Setting this bit-field to “1” configures M12 # 3 to support ITU-T G.747. In this mode, the M12 MUX will accept 3 E1 signals (via TxDS1Data8 thru TxDS1Data10) and will multiplex these signals into an ITU-T G.747 signal. Likewise, the M12 DEMUX will accept an incoming ITU-T G.747 signal (from the M23 DEMUX) and will de-multiplexe this signal into 3 E1 signals. These three E1 signals will output via the “RxDS1Data8” thru “RxDS1Data10” output pins.

Bit 3 - M12G.747 Reserved

Bit 2 - M12 FERF

This “Read/Write” bit-field permits the user to force M12 MUX # 3 to transmit a “FERF” (Far-End-Receive

Failure) indicator to the M23 MUX (and in turn to the remote terminal equipment).

Setting this bit-field to “1” configures the M12 MUX to set the “X-bits” (within the “outbound” DS2 data stream) to “0”. This signaling will be interpreted (by the remote terminal equipment) as a FERF indicator.

Settiing this bit-field to “0” configures the M12 MUX to set the “X-bits” (within the “outbound” DS2 data stream) to “1”. This signaling will be interpreted (by the remote terminal equipment) as an indication of no FERF.

Bits 1 and 0 M12 LB Code[1:0]

3.3.2.26 M12 DS2 # 4 Configuration Register)

M12 DS2 # 4 CONFIGURATION REGISTER (ADDRESS = 0X1D)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved 7	Reserved 6	M12 Bypass	M12 G.747	M12 G.747 Res	M12 FERF	M12LBCode[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	1	1	1

Bit 7 - Reserved

This bit-field must be set to “0”, in order for the XRT72L13 M13 device to function properly.

Bit 6 - Reserved

This bit-field must be set to “0” in order for the XRT72L13 M13 device to function properly.

Bit 5 - M12 Bypass

This “Read/Write” bit field permits the user to bypass M12 Multiplexer/De-Multiplexer # 4. By doing this the following will happen.

In the Transmit Direction

- The XRT72L13 M13 device will accept a DS2 clock signal (6.312MHz) via the TxDS1Clk15 input pin.
- The XRT72L13 M13 device will accept a DS2 signal via the TxDS1Data_15 input pin

In the Receive Direction

- The XRT72L13 M13 device will output a DS2 clock signal (6.312MHz) via the RxDS1Clk15 output pin.
- XRT72L13 M13 device will output the contents of DS2 Channel # 4 via the RxDS1Data15 output pin.

Setting this bit-field to “1” configures M12 MUX # 4 and M12 DEMUX # 4 to be bypassed.

Setting this bit-field to “0” enables M12 MUX # 4 and M12 DEMUX # 4.

Bit 4 - M12 G.747

This “Read/Write” bit-field permits the user to configure M12 MUX # 4 and DEMUX # 4 to support either a DS2 signal or an ITU-T G.747 signal.

Setting this bit-field to “0” configures M12 # 4 to support DS2. In this mode, the M12 MUX will accept four DS1 signals (via TxDS1Data12 thru TXDS1Data15) and will muitiplex these signals into a DS2 signal. Likewise, the M12 DEMUX will accept an incoming DS2 signal (from the M23 DEMUX) and will de-multiplex this signal into 4 DS1 signals. These four DS1 signals will be output via the “RxDS1Data12” thru “RxDS1Data15” output pins.

Setting this bit-field to “1” configures M12 # 4 to support ITU-T G.747. In this mode, the M12 MUX will accept 3 E1 signals (via TxDS1Data12 thru TxDS1Data14) and will multiplex these signals into an ITU-T G.747 signal. Likewise, the M12 DEMUX will accept an incoming ITU-T G.747 signal (from the M23 DEMUX) and will de-multiplexe this signal into 3 E1 signals. These three E1 signals will output via the “RxDS1Data12” thru “RxDS1Data14” output pins.

Bit 3 - M12G.747 Reserved

Bit 2 - M12 FERF

This “Read/Write” bit-field permits the user to force M12 MUX # 4 to transmit a “FERF” (Far-End-Receive Failure) indicator to the M23 MUX (and in turn to the remote terminal equipment).

Setting this bit-field to “1” configures the M12 MUX to set the “X-bits” (within the “outbound” DS2 data stream) to “0”. This signaling will be interpreted (by the remote terminal equipment) as a FERF indicator.

Settiing this bit-field to “0” configures the M12 MUX to set the “X-bits” (within the “outbound” DS2 data stream) to “1”. This signaling will be interpreted (by the remote terminal equipment) as an indication of no FERF.

Bits 1 and 0 M12 LB Code[1:0]

3.3.2.27 M12 DS2 # 5 Configuration Register

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M12 DS2 # 5 CONFIGURATION REGISTER (ADDRESS = 0X1E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved 7	Reserved 6	M12 Bypass	M12 G.747	M12 G.747 Res	M12 FERF	M12LBCode[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	1	1	1

Bit 7 - Reserved

This bit-field must be set to “0”, in order for the XRT72L13 M13 device to function properly.

Bit 6 - Reserved

This bit-field must be set to “0” in order for the XRT72L13 M13 device to function properly.

Bit 5 - M12 Bypass

This “Read/Write” bit field permits the user to bypass M12 Multiplexer/De-Multiplexer # 5. By doing this the following will happen.

In the Transmit Direction

- The XRT72L13 M13 device will accept a DS2 clock signal (6.312MHz) via the TxDS1Clk19 input pin.
- The XRT72L13 M13 device will accept a DS2 signal via the TxDS1Data_19 input pin

In the Receive Direction

- The XRT72L13 M13 device will output a DS2 clock signal (6.312MHz) via the RxDS1Clk19 output pin.
- XRT72L13 M13 device will output the contents of DS2 Channel # 2 via the RxDS1Data19 output pin.

Setting this bit-field to “1” configures M12 MUX # 5 and M12 DEMUX # 5 to be bypassed.

Setting this bit-field to “0” enables M12 MUX # 5 and M12 DEMUX # 5.

Bit 4 - M12 G.747

This “Read/Write” bit-field permits the user to configure M12 MUX # 5 and DEMUX # 5 to support either a DS2 signal or an ITU-T G.747 signal.

Setting this bit-field to “0” configures M12 # 5 to support DS2. In this mode, the M12 MUX will accept four DS1 signals (via TxDS1Data16 thru TXDS1Data19) and will muitiplex these signals into a DS2 signal. Likewise, the M12 DEMUX will accept an incoming DS2 signal (from the M23 DEMUX) and will de-multiplex this signal into 4 DS1 signals. These four DS1 signals will be output via the “RxDS1Data16” thru “RxDS1Data19” output pins.

Setting this bit-field to “1” configures M12 # 5 to support ITU-T G.747. In this mode, the M12 MUX will accept 3 E1 signals (via TxDS1Data16 thru TxDS1Data18) and will multiplex these signals into an ITU-T G.747 signal. Likewise, the M12 DEMUX will accept an incoming ITU-T G.747 signal (from the M23 DEMUX) and will de-multiplexe this signal into 3 E1 signals. These three E1 signals will output via the “RxDS1Data16” thru “RxDS1Data18” output pins.

Bit 3 - M12G.747 Reserved

Bit 2 - M12 FERF

This “Read/Write” bit-field permits the user to force M12 MUX # 5 to transmit a “FERF” (Far-End-Receive Failure) indicator to the M23 MUX (and in turn to the remote terminal equipment).

Setting this bit-field to “1” configures the M12 MUX to set the “X-bits” (within the “outbound” DS2 data stream) to “0”. This signaling will be interpreted (by the remote terminal equipment) as a FERF indicator.

Settiing this bit-field to “0” configures the M12 MUX to set the “X-bits” (within the “outbound” DS2 data stream) to “1”. This signaling will be interpreted (by the remote terminal equipment) as an indication of no FERF.

Bits 1 and 0 M12 LB Code[1:0]

3.3.2.28 M12 DS2 # 6 Configuration Register

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M12 DS2 # 6 CONFIGURATION REGISTER (ADDRESS = 0X1F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved 7	Reserved 6	M12 Bypass	M12 G.747	M12 G.747 Res	M12 FERF	M12LBCode[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	1	1	1

Bit 7 - Reserved

This bit-field must be set to “0”, in order for the XRT72L13 M13 device to function properly.

Bit 6 - Reserved

This bit-field must be set to “0” in order for the XRT72L13 M13 device to function properly.

Bit 5 - M12 Bypass

This “Read/Write” bit field permits the user to bypass M12 Multiplexer/De-Multiplexer # 6. By doing this the following will happen.

In the Transmit Direction

- The XRT72L13 M13 device will accept a DS2 clock signal (6.312MHz) via the TxDS1Clk23 input pin.
- The XRT72L13 M13 device will accept a DS2 signal via the TxDS1Data_23 input pin

In the Receive Direction

- The XRT72L13 M13 device will output a DS2 clock signal (6.312MHz) via the RxDS1Clk23 output pin.
- XRT72L13 M13 device will output the contents of DS2 Channel # 6 via the RxDS1Data23 output pin.

Setting this bit-field to “1” configures M12 MUX # 6 and M12 DEMUX # 6 to be bypassed.

Setting this bit-field to “0” enables M12 MUX # 6 and M12 DEMUX # 6.

Bit 4 - M12 G.747

This “Read/Write” bit-field permits the user to configure M12 MUX # 6 and DEMUX # 6 to support either a DS2 signal or an ITU-T G.747 signal.

Setting this bit-field to “0” configures M12 # 6 to support DS2. In this mode, the M12 MUX will accept four DS1 signals (via TxDS1Data20 thru TXDS1Data23) and will muitiplex these signals into a DS2 signal. Likewise, the M12 DEMUX will accept an incoming DS2 signal (from the M23 DEMUX) and will de-multiplex this signal into 4 DS1 signals. These four DS1 signals will be output via the “RxDS1Data20” thru “RxDS1Data23” output pins.

Setting this bit-field to “1” configures M12 # 6 to support ITU-T G.747. In this mode, the M12 MUX will accept 3 E1 signals (via TxDS1Data20 thru TxDS1Data22) and will multiplex these signals into an ITU-T G.747 signal. Likewise, the M12 DEMUX will accept an incoming ITU-T G.747 signal (from the M23 DEMUX) and will de-multiplexe this signal into 3 E1 signals. These three E1 signals will output via the “RxDS1Data20” thru “RxDS1Data22” output pins.

Bit 3 - M12G.747 Reserved

Bit 2 - M12 FERF

This “Read/Write” bit-field permits the user to force M12 MUX # 6 to transmit a “FERF” (Far-End-Receive Failure) indicator to the M23 MUX (and in turn to the remote terminal equipment).

Setting this bit-field to “1” configures the M12 MUX to set the “X-bits” (within the “outbound” DS2 data stream) to “0”. This signaling will be interpreted (by the remote terminal equipment) as a FERF indicator.

Settiing this bit-field to “0” configures the M12 MUX to set the “X-bits” (within the “outbound” DS2 data stream) to “1”. This signaling will be interpreted (by the remote terminal equipment) as an indication of no FERF.

Bits 1 and 0 M12 LB Code[1:0]

3.3.2.29 M12 DS2 # 7 Configuration Register

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M12 DS2 # 7 CONFIGURATION REGISTER (ADDRESS = 0X20)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved 7	Reserved 6	M12 Bypass	M12 G.747	M12 G.747 Res	M12 FERF	M12LBCode[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	1	1	1

Bit 7 - Reserved

This bit-field must be set to “0”, in order for the XRT72L13 M13 device to function properly.

Bit 6 - Reserved

This bit-field must be set to “0” in order for the XRT72L13 M13 device to function properly.

Bit 5 - M12 Bypass

This “Read/Write” bit field permits the user to bypass M12 Multiplexer/De-Multiplexer # 6. By doing this the following will happen.

In the Transmit Direction

- The XRT72L13 M13 device will accept a DS2 clock signal (6.312MHz) via the TxDS1Clk23 input pin.
- The XRT72L13 M13 device will accept a DS2 signal via the TxDS1Data_23 input pin

In the Receive Direction

- The XRT72L13 M13 device will output a DS2 clock signal (6.312MHz) via the RxDS1Clk23 output pin.
- XRT72L13 M13 device will output the contents of DS2 Channel # 6 via the RxDS1Data23 output pin.

Setting this bit-field to “1” configures M12 MUX # 6 and M12 DEMUX # 6 to be bypassed.

Setting this bit-field to “0” enables M12 MUX # 6 and M12 DEMUX # 6.

Bit 4 - M12 G.747

This “Read/Write” bit-field permits the user to configure M12 MUX # 6 and DEMUX # 6 to support either a DS2 signal or an ITU-T G.747 signal.

Setting this bit-field to “0” configures M12 # 6 to support DS2. In this mode, the M12 MUX will accept four DS1 signals (via TxDS1Data20 thru TXDS1Data23) and will muitiplex these signals into a DS2 signal. Likewise, the M12 DEMUX will accept an incoming DS2 signal (from the M23 DEMUX) and will de-multiplex this signal into 4 DS1 signals. These four DS1 signals will be output via the “RxDS1Data20” thru “RxDS1Data23” output pins.

Setting this bit-field to “1” configures M12 # 6 to support ITU-T G.747. In this mode, the M12 MUX will accept 3 E1 signals (via TxDS1Data20 thru TxDS1Data22) and will multiplex these signals into an ITU-T G.747 signal. Likewise, the M12 DEMUX will accept an incoming ITU-T G.747 signal (from the M23 DEMUX) and will de-multiplexe this signal into 3 E1 signals. These three E1 signals will output via the “RxDS1Data20” thru “RxDS1Data22” output pins.

Bit 3 - M12G.747 Reserved

Bit 2 - M12 FERF

This “Read/Write” bit-field permits the user to force M12 MUX # 6 to transmit a “FERF” (Far-End-Receive Failure) indicator to the M23 MUX (and in turn to the remote terminal equipment).

Setting this bit-field to “1” configures the M12 MUX to set the “X-bits” (within the “outbound” DS2 data stream) to “0”. This signaling will be interpreted (by the remote terminal equipment) as a FERF indicator.

Settiing this bit-field to “0” configures the M12 MUX to set the “X-bits” (within the “outbound” DS2 data stream) to “1”. This signaling will be interpreted (by the remote terminal equipment) as an indication of no FERF.

Bits 1 and 0 M12 LB Code[1:0]

3.3.2.30 M12 DS2 # 1 AIS Register

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M12 DS2 # 1 AIS REGISTER (ADDRESS = 0X21)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Insert AIS Rx DS1 Channel 3	Insert AIS Rx DS1 Channel 2	Insert AIS Rx DS1 Channel 1	Insert AIS Rx DS1 Channel 0	Insert AIS Tx DS1 Channel 3	Insert AIS Tx DS1 Channel 2	Insert AIS Tx DS1 Channel 1	Insert AIS Tx DS1 Channel 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	1	1	1

Bit 7 - Insert AIS Rx DS1 Channel 3

This “Read/Write” bit-field permits the user to configure the contents of the “inbound” DS1 Channel 3 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits data to be output (via the RxDS1Data3 output pin, as demultiplexed via the inbound DS2 and DS3 data streams.

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 6 - Insert AIS Rx DS1 Channel 2

This “Read/Write” bit-field permits the user to configure the contents of the “inbound” DS1 Channel 2 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits data to be output (via the RxDS1Data2 output pin, as demultiplexed via the inbound DS2 and DS3 data streams.

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 5 - Insert AIS Rx DS1 Channel 1

This “Read/Write” bit-field permits the user to configure the contents of the “inbound” DS1 Channel 1 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits data to be output (via the RxDS1Data1 output pin, as demultiplexed via the inbound DS2 and DS3 data streams.

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 4 - Insert AIS Rx DS1 Channel 0

This “Read/Write” bit-field permits the user to configure the contents of the “inbound” DS1 Channel 0 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits data to be output (via the RxDS1Data0 output pin, as demultiplexed via the inbound DS2 and DS3 data streams.

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 3 - Insert AIS Tx DS1 Channel 3

This “Read/Write” bit-field permits the user to configure the contents of the “output” DS1 Channel 3 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits the contents of DS1 Channel 3 to be transmitted as received (via the TxDS1Data3 input pin).

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 2 - Insert AIS Tx DS1 Channel 2

This “Read/Write” bit-field permits the user to configure the contents of the “output” DS1 Channel 3 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits the contents of DS1 Channel 2 to be transmitted as received (via the TxDS1Data2 input pin).

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 1 - Insert AIS Tx DS1 Channel 1

This “Read/Write” bit-field permits the user to configure the contents of the “output” DS1 Channel 1 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits the contents of DS1 Channel 1 to be transmitted as received (via the TxDS1Data1 input pin).

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 0 - Insert AIS Tx DS1 Channel 0

This “Read/Write” bit-field permits the user to configure the contents of the “output” DS1 Channel 0 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits the contents of DS1 Channel 0 to be transmitted as received (via the TxDS1Data0 input pin).

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

3.3.2.31 M12 DS2 # 2 AIS Register

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M12 DS2 # 2 AIS REGISTER (ADDRESS = 0X21)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Insert AIS Rx DS1 Channel 7	Insert AIS Rx DS1 Channel 6	Insert AIS Rx DS1 Channel 5	Insert AIS Rx DS1 Channel 4	Insert AIS Tx DS1 Channel 7	Insert AIS Tx DS1 Channel 6	Insert AIS Tx DS1 Channel 5	Insert AIS Tx DS1 Channel 4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	1	1	1

Bit 7 - Insert AIS Rx DS1 Channel 7

This “Read/Write” bit-field permits the user to configure the contents of the “inbound” DS1 Channel 7 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits data to be output (via the RxDS1Data7 output pin, as demultiplexed via the inbound DS2 and DS3 data streams.

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 6 - Insert AIS Rx DS1 Channel 6

This “Read/Write” bit-field permits the user to configure the contents of the “inbound” DS1 Channel 6 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits data to be output (via the RxDS1Data6 output pin, as demultiplexed via the inbound DS2 and DS3 data streams.

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 5 - Insert AIS Rx DS1 Channel 5

This “Read/Write” bit-field permits the user to configure the contents of the “inbound” DS1 Channel 5 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits data to be output (via the RxDS1Data5 output pin, as demultiplexed via the inbound DS2 and DS3 data streams.

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 4 - Insert AIS Rx DS1 Channel 4

This “Read/Write” bit-field permits the user to configure the contents of the “inbound” DS1 Channel 4 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits data to be output (via the RxDS1Data4 output pin, as demultiplexed via the inbound DS2 and DS3 data streams.

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 3 - Insert AIS Tx DS1 Channel 7

This “Read/Write” bit-field permits the user to configure the contents of the “output” DS1 Channel 7 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits the contents of DS1 Channel 7 to be transmitted as received (via the TxDS1Data7 input pin).

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 2 - Insert AIS Tx DS1 Channel 6

This “Read/Write” bit-field permits the user to configure the contents of the “output” DS1 Channel 6 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits the contents of DS1 Channel 6 to be transmitted as received (via the TxDS1Data2 input pin).

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 1 - Insert AIS Tx DS1 Channel 5

This “Read/Write” bit-field permits the user to configure the contents of the “output” DS1 Channel 5 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits the contents of DS1 Channel 5 to be transmitted as received (via the TxDS1Data1 input pin).

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

Bit 0 - Insert AIS Tx DS1 Channel 4

This “Read/Write” bit-field permits the user to configure the contents of the “output” DS1 Channel 4 to be overwritten with an “All Ones” pattern.

Setting this bit-field to “0” permits the contents of DS1 Channel 4 to be transmitted as received (via the TxDS1Data0 input pin).

Setting this bit-field to “1” configures the XRT72L13 M13 device to overwrite this data with an AIS (all ones pattern).

3.3.2.32 M12 DS2 # 3 AIS Register

3.3.2.33 M12 DS2 # 4 AIS Register

3.3.2.34 M12 DS2 # 5 AIS Register

3.3.2.35 M12 DS2 # 6 AIS Register

3.3.2.36 M12 DS2 # 7 AIS Register

3.3.2.37 M12 DS2 # 1 Loopback Request Register

3.3.2.38 M12 DS2 # 2 Loopback Request Register

3.3.2.39 M12 DS2 # 3 Loopback Request Register

3.3.2.40 M12 DS2 # 4 Loopback Request Register

3.3.2.41 M12 DS2 # 5 Loopback Request Register

3.3.2.42 M12 DS2 # 6 Loopback Request Register

3.3.2.43 M12 DS2 # 7 Loopback Request Register

3.3.2.44 Tx DS3 Configuration Register)

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TX DS3 CONFIGURATION REGISTER (ADDRESS = 0X30)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Tx Yellow Alarm	Tx X Bits	Tx Idle	Tx AIS	Tx LOS	FERF on LOS	FERF on OOF	FERF on AIS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	1	1	1

Bit 7 - Tx Yellow Alarm

This "Read/Write" bit-field allows the local µP to command the Transmit DS3 Framer to transmit a "Yellow Alarm" (e.g., X bits are all "0") in the outgoing DS3 data stream.

Writing a "0" to this bit-field disables this feature (the default condition). In this condition, the X-bits in the out-bound DS3 frame, are internally generated (based upon receiver conditions).

Writing a "1" to this bit-field invokes this command. In this condition, the Transmit DS3 Framer will override the internally-generated X-bits and force all of the X-bits of each outbound DS3 frame to "0".

NOTE: *For more information in this feature, please see Section _.*

NOTE: *This bit-setting is ignored if Bits 3, 4 or 5 (within this register) are set to "1".*

Bit 6 - Tx X-Bit (Force X bits to "1")

This "Read/Write" bit-field allows the user to command the Transmit DS3 Framer to force all of the X-bits, in the outbound DS3 Frames, to "1".

Writing a "0" to this bit-field disables this feature (the default condition). In this case, the Transmit DS3

Framer will generate X-bits based upon the receive conditions.

Writing a "1" to this bit-field invokes this command. In this case, the Transmit DS3 Framer will overwrite the internally-generated X-bits and set them all to "1".

NOTE: *For more information on this feature, please see Section _.*

NOTE: *This bit-setting is ignored if Bits 3, 4, 5, or 7 (within this register) are set to "1".*

Bit 5 - Tx Idle (Pattern)

This "Read/Write" bit-field allows the user to command the Transmit DS3 Framer to transmit the "Idle Condition" pattern. If the user invokes this command, then the Transmit DS3 Framer will force the outbound DS3 Frames to have the following patterns.

- Valid M-bits, F-bits and P-bits
- The three CP-Bits (F-frame #3) are "0"
- The X-bits are set to "1"
- A repeating "1100..." pattern in written into the payload portion of the DS3 Frames.

Writing a "1" to this bit-field invokes this command. Writing a "0" allows the Transmit DS3 Framer to function normally (e.g., the Transmit DS3 Framer will transmit its payload and internally generated overhead bits).

NOTE: *For more information on this feature, please see Section _.*

NOTE: *This bit-setting is ignored if Bits 3 or 4 (within this register) are set to "1".*

Bit 4 - Tx AIS (Pattern)

This "Read/Write" bit-field allows the user to command the Transmit DS3 Framer to transmit an "AIS" pattern. If the user invokes this command, then the Transmit DS3 Framer will force the outbound DS3 frames to have the following patterns.

- Valid M-bits, F-bits, and P-bits
- All C-bits are set to '0'
- All X-bits are set to '1'
- A repeating '1010...' pattern is written into the payload of the DS3 Frames.

Writing a "1' to this bit-field invokes this command. Writing a "0" allows the Transmit DS3 Framer to function normally (e.g., the Transmit DS3 Framer will transmit its payload and internally generated overhead bits).

NOTE: *For more information on this feature, please see Section _.*

Bit 3 - Tx LOS (Loss of Signal)

This "Read/Write" bit-field allows the user to command the Transmit DS3 Framer to simulate an "LOS Condition". If the user invokes this command, then the Transmit DS3 Framer will stop sending "mark" pulses out on the line; and will transmit an all-zero pattern.

Writing a '0' to this bit-field disables (or shuts off) this feature, thereby allowing internally generated DS3 Frames to be generated and transmitted over the line.

Writing a '1' to this bit-field invokes this command, causing the Transmit DS3 Framing to generate an all '0' pattern.

NOTE: *For more information on this feature, please see Section _.*

Bit 2 - FERF on LOS

This "Read/Write" bit-field allows the user to configure the Transmit DS3 Framer to generate a "Yellow Alarm" if the Near-End Receive DS3 Framer detects a "LOS" (Loss of Signal) Condition.

Writing a "1" to this bit-field enables this feature. Writing a "0" to this bit-field disables this feature.

NOTE: *For more information on this feature, please see Section _.*

Bit 1 - FERF on OOF

This "Read/Write" bit-field allows the user to configure the Transmit DS3 Framer to generate a "Yellow Alarm" if the Near-End Receive DS3 Framer detects an "OOF (Out-of-Frame) Condition".

Writing a "1" to this bit-field enables this feature. Writing a "0" to this bit-field disables this feature.

NOTE: *For more information on this feature, please see Section _.*

Bit 0 - FERF on AIS

This "Read/Write" bit-field allows the user to configure the Transmit DS3 Framer to generate a "Yellow Alarm" if the Near-End Receive DS3 Framer detects an AIS (Alarm Indication Signal) Condition.

Writing a "1" to this bit-field enables this feature. Writing a "0" to this bit-field disables this feature.

NOTE: *For more information on this feature, please see Section _.*

3.3.2.45 TxDS3 FEAC Configuration and Status Register

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TRANSMIT DS3 CONFIGURATION & STATUS REGISTER (ADDRESS = 0X31)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			Tx FEAC Interrupt Enable	TxFEAC Interrupt Status	TxFEAC Enable	TxFEAC	TxFEAC Busy
RO	RO	RO	R/W	RUR	R/W	R/W	RO
0	0	0	0	0	0	0	0

Bit 4 - Tx FEAC Interrupt Enable

This “Read-Write” bit-field permits the user to enable or disable the “Transmit FEAC” Interrupt.

Setting this bit-field to “0” disables this interrupt.

Conversely, setting this bit-field to “1” enables this interrupt.

Bit 3 - TxFEAC Interrupt Status

This "Read-Only" bit-field indicates whether or not the "FEAC Message Transmission Complete" interrupt has occurred since the last read of this register. This interrupt will occur once the Transmit FEAC Processor has finished its 10th transmission of the 16 bit FEAC Message (6 bit FEAC Code word + 10 framing bits). The purpose of this interrupt is to let the local µP know that the Transmit FEAC Processor has completed its transmission of its latest FEAC Message and is now ready to transmit another FEAC Message.

If this bit-field is "0", then the "FEAC Message Transmission Complete" interrupt has NOT occurred since the last read of this register.

If this bit-field is "1", then the "FEAC Message Transmission Complete" interrupt has occurred since the last read of this register.

NOTE: *For more information on the Transmit FEAC Processor, please see Section _.*

Bit 2 - TxFEAC Enable

This "Read/Write" bit-field allows the user to enable or disable the Transmit FEAC Processor. The Transmit FEAC Processor will NOT function until it has been enabled.

Writing a "0" to this bit-field disables the Transmit FEAC Processor. Writing a "1" to this bit-field enables the Transmit FEAC Processor.

Bit 1 - TxFEAC Go

This bit-field allows the user to invoke the "Transmit FEAC Message" command. Once this command has been invoked, the Transmit FEAC Processor will do the following:

- Encapsulate the 6 bit FEAC code word, from the Tx DS3 FEAC Register (Address = 1Dh) into a 16 bit FEAC Message
- Serially transmit this 16-bit FEAC Message to the far-end receiver via the "outbound" DS3 datastream, 10 consecutive times.

NOTE: *For more information on the Transmit FEAC Processor, please see Section _.*

Bit 0 - TxFEAC Busy

This "Read-Only" bit-field allows the local µP to "poll" and determine if the Transmit FEAC Processor has completed its 10th transmission of the 16-bit FEAC Message. This bit-field will contain a "1", if the Transmit FEAC Processor is still transmitting the FEAC Message. This bit-field will toggle to "0", once the Transmit FEAC Processor has completed its 10th transmission of the FEAC Message.

NOTE: *For more information on the Transmit FEAC Processor, please see Section _.*

3.3.2.46 TxDS3 FEAC Register

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TX DS3 FEAC REGISER (ADDRESS = 0X32)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	TxFEAC[5:0]						Not Used
RO	R/W	R/W	R/W	R/W	R/W	R/W	RO
0	1	1	1	1	1	1	0

This register contains a six (6) bit "read/write" field that allows the user to write in the six-bit FEAC code word, that he/she wishes to transmit to the "Far End Receive FEAC Processor", via the outgoing DS3 data stream. The Transmit FEAC Processor will encapsulate this six-bit code into a 16-bit FEAC message, and will proceed to transmit this message to the "Far End Receiver" via the FEAC bit-field within each out-going DS3 frame.

NOTE: *For more information on the operation of the Transmit FEAC Processor, please see Section _.*

3.3.2.47 TxDS3 LAPD Configuration Register)

TXDS3 LAPD CONFIGURATION REGISTER (ADDRESS = 0X33)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used				Auto Retransmit	Not Used	TxLAPD Msg Length	TxLAPD Enable
RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	1	0	0	0

Bit 3 - Auto Retransmit

This "Read/Write" bit-field allows the user to configure the LAPD Transmitter to either transmit the LAPD Message frame only once; or repeatedly at one-second intervals.

Writing a "0" to this bit-field configures the LAPD Transmitter to transmit the LAPD Message frame once. Afterwards, the LAPD Transmitter will halt transmission, until it has commanded to transmit another LAPD Message frame.

Writing a "1" to this bit-field configures the LAPD Transmitter to transmit the LAPD Message frame repeatedly at one second intervals. In this configuration, the LAPD Transmitter will repeat its transmission of the LAPD Message frame until it has been disabled.

Bit 1 - TxLAPD Message Length Select

This "Read/Write" bit-field permits the user to select the length of the "outbound" LAPD Message frame. Setting this bit-field to "0" configures the "outbound" LAPD Message frame to be 76 bytes in length. Setting this bit-field to "1" configures the "outbound" LAPD Message frame to be 82 bytes in length.

Bit 0 - TxLAPD Enable

This "Read/Write" bit-field allows the user to enable or disable the LAPD Transmitter. The LAPD Transmitter must be enabled before it can be commanded to transmit a LAPD Message frame (containing a PMDL message) via the outbound DS3 frames, to the "Far-End" Terminal.

Writing a "0" disables the LAPD Transmitter (default condition). Writing a "1" enables the LAPD Transmitter.

NOTE: *For information on the LAPD Transmitter, please see Section _.*

3.3.2.48 TxDS3 LAPD Status/Interrupt Register)

TXDS3 LAPD STATUS AND INTERRUPT REGISTER (ADDRESS = 0X34)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used				TxDL Start	TxDL Busy	TxLAPD Interrupt Enable	TxLAPD Interrupt Status
RO	RO	RO	RO	R/W	RO	R/W	RUR
0	0	0	0	0	0	0	0

Bit 3 - TxDL Start

This "Read/Write" bit-field allows the user to invoke the "Transmit LAPD Message" command. Once the user invokes this command, the LAPD Transmitter will do the following:

- Read in the PMDL Message from the "Transmit LAPD Message" Buffer.
- Encapsulate the PMDL Message into a complete LAPD Message frame by including the necessary

header and trailer bytes (e.g., flag sequence bytes, SAPI, CR, EA values, etc.).

- Compute the frame check sequence word (16 bit value)
- Insert the Frame Check Sequence value into the 2 octet slot after the payload section of the Message.
- Proceed to transmit the LAPD Message Frame to the "far end" terminal via the outgoing DS3 frames.

Writing a "1" to this bit-field start the transmission of the LAPD Message Frame, via the LAPD Transmitter.

NOTE: *For more information on the LAPD Transmitter, please see Section _.*

Bit 2 - TxDL Busy

This "Read-Only" bit-field allows the local µP to "poll" and determine if the LAPD Transmitter has completed its transmission of the LAPD Message frame. This bit-field will contain a "1", if the LAPD Transmitter is still transmitting the LAPD Message frame to the "far-end" terminal. This bit-field will toggle to "0", once the LAPD Transmitter has completed its transmission of the LAPD Message frame.

NOTE: *For more information on the LAPD Transmitter, please see Section _.*

Bit 1 - TxLAPD Interrupt Enable

This "Read/Write" bit-field allows the user to enable or disable the "LAPD Message Frame Transmission Complete" interrupt.

Writing a "0" to this bit-field disables this interrupt. Writing a "1" to this bit-field enables this interrupt.

Bit 0 - TxLAPD Interrupt Status

This "Reset Upon Read" bit-field indicates whether or not the "LAPD Message frame Transmission Complete" interrupt has occurred since the last read of this register. The purpose of this interrupt is to let the local µP know that the LAPD Transmitter has completed its transmission of the LAPD Message frame (containing the latest PMDL message); and is now ready to transmit another LAPD Message frame.

A "0" in this bit-field indicates that the "LAPD Message frame Transmission Complete" interrupt has not occurred since the read of this register. A "1" in this bit-field indicates that this interrupt has occurred since the last read of this register.

NOTE: *For more information on the LAPD Transmitter, please see Section _.*

3.3.2.49 TxDS3 M-Bit Mask Register

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TXDS3 M-BIT MASK REGISTER (ADDRESS = 0X35)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxFEBEDat[2:0]			FEBE Reg Enable	Tx Error P-Bit	MBit Mask[2]	MBit Mask[1]	MBit Mask[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit 7 - 5: TxFEBEDat[2:0]

These three (3) "read/write" bit-fields, along with Bit 4 of this register, allows the user to configure and transmit his/her choice for FEBE bits in each outgoing DS3 Frame. The user will write his/her value for the FEBE bits into these bit-fields. The Transmit DS3 Framer will insert these values into the FEBE bit-fields of each outgoing DS3 Frame, once the user has written a "1" to Bit 4 (FEBE Register Enable).

NOTE: *For more information on this feature, please see Section _.*

Bit 4 - FEBE Register Enable

This "Read/Write" bit-field allows the user to configure the Transmit DS3 Framer to insert the contents of TxFEBEDat[2:0] into the FEBE bit-fields each outgoing DS3 Frame.

Writing a "0" to this bit-field disables this feature (e.g., the Transmit DS3 Framer will transmit the internally generated FEBE bits). Writing a "1" to this bit-field enables this features (e.g., the internally generated FEBE bits are overwritten by the contents of the TxFEBEDat[2:0] bit-field).

NOTE: *For more information on this feature, please see Section _.*

Bit 3 - Transmit Erred P-Bit

This "Read/Write bit-field allows the user to insert errors into the P-bits of the outgoing DS3 frames (via the Transmit DS3 Framer block). If the user enables this feature, then the Transmit DS3 Framer will proceed to invert each and every P-bit, from its computed value, prior to transmission to the "Far-end" Terminal.

Writing a "0" to this bit-field (the default condition) disables this feature (e.g., the correct P-bits are sent).

Writing a "1" to this bit-field enables this feature (e.g., the incorrect P-bits are sent).

NOTE: For more information on this feature, please see Section _.

Bit 2 - 0 M-Bit Mask[2:0]

These "Read/Write" bit-fields allow the user to insert errors in the M-bits for Test and Diagnostic purposes. The Transmit DS3 Framer automatically performs an XOR operation on the actual contents of the M-bit fields to these register bit-fields. Therefore, for every '1' that exists in these bit-fields, will result in a change of state of the corresponding M-bit, prior to being transmitted to the Far End Receive DS3 Framer.

If the user wishes to operate the Transmit DS3 Framer in the normal mode (e.g., when no errors are being injected into the M-bit fields of the outbound DS3 Frame), then he/she must ensure that these bit-fields are all '0'.

3.3.2.50 Tx DS3 F-Bit Mask1 Register

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TX DS3 F-BIT MASK REGISTER - 1 (ADDRESS = 0X36)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used				FBit Mask[27]	FBit Mask[26]	FBit Mask[25]	FBit Mask[24]
RO	RO	RO	RO	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bits 3 - 0 F-Bit Mask[27:24]

These "Read/Write" bit-fields allow the user to insert errors into the first four F-bits of a DS3 M-frame, for test and diagnostic purposes. The Transmit DS3 Framer block (within the chip) automatically performs an XOR operation on the actual contents of these F-bit fields to these register bit-fields. Therefore, for every "1" that exists in these bit-fields, this will result in a change of state for the corresponding F-bit, prior to being transmitted to the Far-End Receive DS3 Framer.

If the user wishes to operate the Transmit DS3 Framer block in the normal mode (e.g., when no errors are being injected into these F-bit fields of the outbound DS3 frames), then he/she must ensure that all of these bit-fields are "0s".

3.3.2.51 TxDS3 F-Bit Mask2 Register

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TXDS3 F-BIT MASK REGISTER - 2 (ADDRESS = 0X37)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FBit Mask[23]	FBit Mask[22]	FBit Mask[21]	FBit Mask[20]	FBit Mask[19]	FBit Mask[18]	FBit Mask[17]	FBit Mask[16]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bits 7 - 0 F-Bit Mask[23:16]

These "Read/Write" bit-fields allow the user to insert errors into the fifth through twelfth F-bits of a DS3 M-frame, for test and diagnostic purposes. The Transmit DS3 Framer block automatically performs an XOR operation on the actual contents of these F-bit fields to these register bit-fields. Therefore, for every "1" that exists in these bit-fields, this will result in a change of state for the corresponding F-bit, prior to being transmitted to the Remote Receive DS3 Framer.

If the user wishes to operate the Transmit DS3 Framer block in the normal mode (e.g., when no errors are being injected into these F-bit fields of the outbound DS3 frames), then he/she must ensure that all of these bit-fields are "0s".

3.3.2.52 TxDS3 F-Bit Mask3 Register

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TX DS3 F-BIT MASK REGISTER - 3 (ADDRESS = 0X38)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FBit Mask[15]	FBit Mask[14]	FBit Mask[13]	FBit Mask[12]	FBit Mask[11]	FBit Mask[10]	FBit Mask[9]	FBit Mask[8]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bits 7 - 0 F-Bit Mask[15:8]

These "Read/Write" bit-fields allow the user to insert errors into the thirteenth through twentieth F-bits of a DS3 M-frame, for test and diagnostic purposes. The Transmit DS3 Framer automatically performs an XOR operation on the actual contents of these F-bit fields to these register bit-fields. Therefore, for every "1" that exists in these bit-fields, this will result in a change of state for the corresponding F-bit, prior to being transmitted to the Far-End Receive DS3 Framer.

If the user wishes to operate the Transmit DS3 Framer in the normal mode (e.g., when no errors are being injected into these F-bit fields of the outbound DS3 frames), then he/she must ensure that all of these bit-fields are "0s".

3.3.2.53 TxDS3 F-Bit Mask4 Register

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TXDS3 F-BIT MASK REGISTER - 4 (ADDRESS = 0X39)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FBit Mask[7]	FBit Mask[6]	FBit Mask[5]	FBit Mask[4]	FBit Mask[3]	FBit Mask[2]	FBit Mask[1]	FBit Mask[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bits 7 - 0 F-Bit Mask[7:0]

These "Read/Write" bit-fields allow the user to insert errors into the last eight F-bits of a DS3 M-frame, for test and diagnostic purposes. The Transmit DS3 Framer automatically performs an XOR operation on the actual contents of these F-bit fields to these register bit-fields. Therefore, for every "1" that exists in these bit-fields, this will result in a change of state for the corresponding F-bit, prior to being transmitted to the Far-End Receive DS3 Framer.

If the user wishes to operate the Transmit DS3 Framer in the normal mode (e.g., when no errors are being injected into these F-bit fields of the outbound DS3

3.3.2.54 M12 DS2 # 1 Framer Configuration Register

3.3.2.55 M12 DS2 # 2 Framer Configuration Register

3.3.2.56 M12 DS2 # 3 Framer Configuration Register

3.3.2.57 M12 DS2 # 4 Framer Configuration Register

3.3.2.58 M12 DS2 # 5 Framer Configuration Register

3.3.2.59 M12 DS2 # 6 Framer Configuration Register

3.3.2.60 M12 DS2 # 7 Framer Configuration Register

3.3.2.61 PMON LCV Event Count Register - MSB

PMON LCV EVENT COUNT REGISTER - MSB (ADDRESS = 0X50)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LCV Count - High Byte							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

This "Reset-upon-Read" register, along with the "PMON LCV Event Count Register - LSB" (Address = 0x51) contains a 16-bit representation of the number of "Line Code Violations" that have been detected by the Receive DS3 Framer block (within the chip), since the last read of these registers. This register contains the MSB (or Upper-Byte) value of this 16 bit expression.

3.3.2.62 PMON LCV Event Count Register - LSB

PMON LCV EVENT COUNT REGISTER - LSB (ADDRESS = 0X51)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LCV Count - Low Byte							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

This "Reset-upon-Read" register, along with the "PMON LCV Event Count Register - LSB" (Address = 0x50) contains a 16-bit representation of the number of "Line Code Violations" that have been detected by the Receive DS3 Framer block (within the chip), since the last read of these registers. This register contains the LSB (or Lower-Byte) value of this 16 bit expression.

3.3.2.63 PMON Framing Bit Error Event Count Register - MSB

PMON FRAMING BIT ERROR COUNT REGISTER - MSB (ADDRESS = 0X52)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Framing Bit Error Count - High Byte							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

This "Reset-upon-Read" register, along with the "PMON Framing Bit Error Count Register - LSB" (Address = 0x53) contains a 16-bit representation of the number of "Framing Bit Errors" that have been detected by the Receive DS3 Framer block (within the chip), since the last read of these registers. This register contains the MSB (or Upper-Byte) value of this 16 bit expression.

3.3.2.64 PMON Framing Bit Error Event Count Register - LSB

PMON FRAMING BIT ERROR COUNT REGISTER - LSB (ADDRESS = 0X53)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Framing Bit Error Count - Low Byte							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

This "Reset-upon-Read" register, along with the "PMON Framing Bit Error Count Register - MSB" (Address = 0x52) contains a 16-bit representation of the number of "Framing Bit Errors" that have been detected by the Receive DS3 Framer block (within the chip), since the last read of these registers. This register contains the LSB (or Lower-Byte) value of this 16 bit expression.

3.3.2.65 PMON P-Bit Error Event Count Register - MSB

PMON P-BIT ERROR COUNT REGISTER - MSB (ADDRESS = 0X54)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P-Bit Error Count - High Byte							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

This "Reset-upon-Read" register, along with the "PMON P-Bit Error Count Register - LSB" (Address = 0x55) contains a 16-bit representation of the number of "P-bit Errors that have been detected by the Receive DS3 Framer block (within the chip), since the last read of these registers. This register contains the MSB (or Upper-Byte) value of this 16 bit expression.

3.3.2.66 PMON P-Bit Error Event Count Register - LSB

PMON P-BIT ERROR COUNT REGISTER - LSB (ADDRESS = 0X55)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P-Bit Error Count - Low Byte							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

This "Reset-upon-Read" register, along with the "PMON P-Bit Error Count Register - MSB" (Address = 0x54) contains a 16-bit representation of the number of "P-bit Errors that have been detected by the Receive DS3 Framer block (within the chip), since the last read of these registers. This register contains the LSB (or Lower-Byte) value of this 16 bit expression.

3.3.2.67 PMON FEBE Event Count Register - MSB

PMON FEBE EVENT COUNT REGISTER - MSB (ADDRESS = 0X56)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FEBE Event Count - High Byte							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

This "Reset-upon-Read" register, along with the "PMON FEBE Event Count Register - LSB" (Address = 0x57) contains a 16-bit representation of the number of "FEBE Events that have been detected by the Receive DS3 Framer block (within the chip), since the last read of these registers. This register contains the MSB (or Upper-Byte) value of this 16 bit expression.

3.3.2.68 PMON FEBE Event Count Register - LSB

PMON FEBE EVENT COUNT REGISTER - LSB (ADDRESS = 0X57)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FEBE Event Count - Low Byte							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

This "Reset-upon-Read" register, along with the "PMON FEBE Event Count Register - MSB" (Address = 0x56) contains a 16-bit representation of the number of "FEBE Events that have been detected by the Receive DS3 Framer block (within the chip), since the last read of these registers. This register contains the LSB (or Lower-Byte) value of this 16 bit expression.

3.3.2.69 PMON CP-Bit Error Event Count Register - MSB

PMON CP-BIT ERROR COUNT REGISTER - MSB (ADDRESS = 0X58)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CP-Bit Error Count - High Byte							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

This "Reset-upon-Read" register, along with the "PMON CP-Bit Error Count Register - LSB" (Address = 0x59) contains a 16-bit representation of the number of "CP-bit Errors that have been detected by the Receive DS3 Framer block (within the chip), since the last read of these registers. This register contains the MSB (or Upper-Byte) value of this 16 bit expression.

3.3.2.70 PMON CP-Bit Error Event Count Register - LSB

PMON CP-BIT ERROR COUNT REGISTER - LSB (ADDRESS = 0X59)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CP-Bit Error Count - Low Byte							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

This "Reset-upon-Read" register, along with the "PMON CP-Bit Error Count Register - MSB" (Address = 0x58) contains a 16-bit representation of the number of "CP-bit Errors that have been detected by the Receive DS3 Framer block (within the chip), since the last read of these registers. This register contains the MSB (or Upper-Byte) value of this 16 bit expression.

3.3.2.71 PMON DS2 # 1 Framing Bit Error Counter

3.3.2.72 PMON DS2 # 2 Framing Bit Error Counter

3.3.2.73 PMON DS2 # 3 Framing Bit Error Counter

3.3.2.74 PMON DS2 # 4 Framing Bit Error Counter

3.3.2.75 PMON DS2 # 5 Framing Bit Error Counter

3.3.2.76 PMON DS2 # 6 Framing Bit Error Counter

3.3.2.77 PMON DS2 # 7 Framing Bit Error Counter

3.3.2.78 PMON ITU-T G.747 # 1 Parity Bit Error Counter

3.3.2.79 PMON ITU-T G.747 # 2 Parity Bit Error Counter

3.3.2.80 PMON ITU-T G.747 # 3 Parity Bit Error Counter

3.3.2.81 PMON ITU-T G.747 # 4 Parity Bit Error Counter

3.3.2.82 PMON ITU-T G.747 # 5 Parity Bit Error Counter

3.3.2.83 PMON ITU-T G.747 # 6 Parity Bit Error Counter

3.3.2.84 PMON ITU-T G.747 # 7 Parity Bit Error Counter

3.3.2.85 PMON Holding Register

PMON HOLDING REGISTER (ADDRESS = 0X6C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON Holding Value							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

Each of the PMON registers are 16 bit "Reset-upon-Read" registers. More specifically, whenever the Microprocessor intends to read a PMON register, there are two things to bear in mind.

1. This Microprocessor is going to require two read accesses in order read out the full 16-bit expression of these PMON registers.
2. The entire 16-bit expression (of a given PMON register) is going to be reset, immediately after

the Microprocessor has completed its first read access to the PMON register.

Hence, the contents of the other byte (of the partially read PMON register) will reside within the PMON Holding register.

3.3.2.86 One Second Error Status Register

3.3.2.87 LCV One Second Accumulator Register - MSB

3.3.2.88 LCV One Second Accumulator Register - LSB

3.3.2.89 P-Bit Error One Second Accumulator Register - MSB

3.3.2.90 P-Bit Error One Second Accumulator Register - LSB

3.3.2.91 CP-Bit Error One Second Accumulator Register - MSB

3.3.2.92 CP-Bit Error One Second Accumulator Register - LSB

3.3.2.93 Line Interface Drive Register

3.3.2.94 Line Interface Scan Register

4.0 CLEAR CHANNEL FRAMER OPERATION OF THE XRT72L13

The XRT72L13 M13/Framer IC can be configured to operate in any of the following modes:

- Clear-Channel Framer Mode
- Channelized (M13) Mode
- High-Speed HDLC Controller Mode.

As a consequence, the discussion of the XRT72L13 will be organized as follows:

Section 4.0 - Clear Channel Framer Mode Operation of the XRT72L13.

Section 5.0 - Channelized (M13) Mode Operation of the XRT72L13.

Section 5.0 - High-Speed HDLC Controller (e.g., Frame-Relay over DS3) Mode.

Section 6.0 - Diagnostic Features of the XRT72L13.

This section will discuss Clear-Channel Framer Mode operation of the XRT72L13, in detail.

Configuring the XRT72L13 to Operate in the Clear-Channel Framer Mode

The XRT72L13 can be configured to operate in the "Clear-Channel Framer" Mode by writing a "0" into bit-field 6 (Payload HDLC Controller Enable) and bit 4 (M13 Disable) within the “M23 Configuration" register; as illustrated below.

M23 CONFIGURATION REGISTER (ADDRESS = 0X07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Unused	Payload HDLC Controller Enable	RxDS1Clk Gapped (CRC-32)	M13 Disable	M13 Loop-back (Remote Loop-back)	Tributary Polarity	M23 Loop-back Code[1:0]	
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	0	x	1	x	x	x	x

The XRT72L13 can be configured to support either the “DS3 M13” or the “DS3 C-Bit Parity” framing formats. Prior to describing the functional blocks within the Transmit and Receive Sections of the XRT72L13; it is important to describe these following two framing formats.

- M13
- C-Bit Parity

4.1 DESCRIPTION OF THE DS3 FRAMES AND ASSOCIATED OVERHEAD BITS

The role of the various overhead bits are best described by discussing the DS3 Frame Format as a whole. The DS3 Frame contains 4760 bits, of which 56 bits are overhead and the remaining 4704 bits are "payload" bits. The "payload" data is formatted into packets of 84 bits and the overhead (OH) bits are inserted between these payload packets. The XRT72L13 Framer device supports the following two DS3 framing formats:

- C-bit Parity
- M13

Figures 59 and 60 present the DS3 Frame Format for C-bit Parity and M13, respectively.

FIGURE 59. DS3 FRAME FORMAT FOR C-BIT PARITY

X	I	F1	I	AIC	I	F0	I	NA	I	F0	I	FEAC	I	F1	I
								I							
X	I	F1	I	UDL	I	F0	I	NA	I	F0	I	FEAC	I	F1	I
P	I	F1	I	CP	I	F0	I	CP	I	F0	I	CP	I	F1	I
P	I	F1	I	FEBE	I	F0	I	FEBE	I	F0	I	FEBE	I	F1	I
M0	I	F1	I	DL	I	F0	I	DL	I	F0	I	DL	I	F1	I
M1	I	F1	I	UDL	I	F0	I	UDL	I	F0	I	UDL	I	F1	I
M0	I	F1	I	UDL	I	F0	I	UDL	I	F0	I	UDL	I	F1	I

X = Signaling bit for network control

I = Payload Information (84 bit packets)

Fi = Frame synchronization bit with logic value i

P = Parity bit

Mi = Multiframe synchronization bit with logic value i

AIC = Application Identification Channel

NA = reserved for network application

FEAC = Far End Alarm and Control

DL = Data Link

CP = CP (Path)-bit parity

FEBE = Far End Block Error

UDL = User Data Link

FIGURE 60. DS3 FRAME FORMAT FOR M13

X	I	F1	I	C11	I	F0	I	C12	I	F0	I	C13	I	F1	I
								I							
X	I	F1	I	C21	I	F0	I	C22	I	F0	I	C23	I	F1	I
P	I	F1	I	C31	I	F0	I	C32	I	F0	I	C33	I	F1	I
P	I	F1	I	C41	I	F0	I	C42	I	F0	I	C43	I	F1	I
M0	I	F1	I	C51	I	F0	I	C52	I	F0	I	C53	I	F1	I
M1	I	F1	I	C61	I	F0	I	C62	I	F0	I	C63	I	F1	I
M0	I	F1	I	C71	I	F0	I	C72	I	F0	I	C73	I	F1	I

X = Signaling bit for network control

I = Payload Information (84 bit packets)

Fi = Frame synchronization bit with logic value i

Cij = jth stuff code bit of ith channel

P = Parity bit

Mi = multiframe synchronization bit with logic values i

The user can choose between these two framing formats, by writing the appropriate data to bit 2 of the "Operating Mode" Register (Address = 0x00), as depicted below.

OPERATING MODE REGISTER (ADDRESS = 0X00)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Local Loop-back Mode	Line Loop-back Mode	Internal LOS Enable	RESET	Interrupt Enable Reset	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
x	1	x	0	x	x	x	x

Table 10 lists the relationship between the value of the this bit-field and the resulting DS3 Frame Format.

TABLE 10: THE RELATIONSHIP BETWEEN THE CONTENT OF BIT 2, (C-BIT PARITY*/M13) WITHIN THE "FRAMER OPERATING MODE" REGISTER AND THE RESULTING DS3 FRAMING FORMAT

BIT 2	DS3 FRAME FORMAT
0	C-Bit Parity
1	M13

NOTE: *This bit setting also configures the frame format for both the Transmit and Receive Section of the XRT72L13.*

Each of the two DS3 Frame Formats, as presented in Figure 59 and Figure 60 , constitute an M-frame (or a full DS3 Frame). Each M-frame consists of 7 - 680 bit F-frames (sometimes referred to as, subframes). In Figure 59 and 60 , each F-frame is represented by the individual rows of payload and overhead bits. Each F-frame can be further divided into 8 blocks of 85 bits, with 84 of the 85 bits available for payload information and the remaining one bit used for frame overhead.

Differences Between the M13 and C-Bit Parity Frame Formats

The frame formats for M13 and C-bit Parity are very similar. However, the main difference between these two framing formats is in the use of the C-bits.

M13 Framing Format

In the M13 Format, the C-bits typically reflect the status of stuff-opportunities that either were or were not used while multiplexing the 7 DS2 signals into this DS3 signal. If two of the three stuff bits, within a F-frame, are "1", then the associated stuff bit, Si (not shown in Figure 60), is interpreted as being a stuff bit.

NOTES:

1. *For "Clear-Channel Framing" applications, each of these 21 C-bits will automatically set to "0".*
2. *For "Channelized" applications, then these C-bits will reflect the "stuff-bit" status of the composite DS2/ITU-T G.747 signals, wiithin the DS3 signal.*

C-Bit Parity Framing Format

In the C-bit Parity framing format, the "C" bits take on different roles, as presented in Table 11 .

TABLE 11: C-BIT FUNCTIONS FOR THE C-BIT PARITY DS3 FRAME FORMAT

C - BIT	FUNCTION OF C-BITS WHILE IN THE C-BIT PARITY FRAMING FORMAT
C11	AIC (C-Bit Parity Mode)
C12	NA (Reserved for Network Application)
C13	FEAC (Far End Alarm & Control)
C21, C22, C23	User Data Link (undefined for DS3 Frame)
C31,C32, C33	C-bit Parity bits
C41, C42, C43	FEBE (Far End Block Error) Indicators
C51, C52, C53	Path Maintenance Data Link
C61, C62, C63, C71, C72, C73	User Data Link (undefined for DS3 Frame)

Definition of the DS3 Frame Overhead Bits

In general, the DS3 Frame Overhead Bits serve the following three purposes:

1. Support Frame Synchronization between the Local and Remote DS3 Terminals
2. Provide parity bits in order to facilitate performance monitoring and error detection.
3. Support the transmission of Alarms, Status, and Data Link information to the Remote DS3 Terminal.

The Overhead bits supporting each of these purposes are further defined below.

4.1.1 Frame Synchronization Bits (Applies to both M13 and C-bit Parity Framing Formats)

Each DS3 Frame (M-frame) contains a total of 31 bits that support frame synchronization. Each DS3 M-frame contains three M-bits. According to Figure 59 and Figure 60 , these M-bits are the first bits in F-frames 5, 6 and 7. These three bits appear in each M-frame with the repeating pattern of "010". This fact is also presented in Figure 59 and Figure 60 , which contains bit-fields that are designated as: M0, M1, and M0 (where M0 = "0", and M1 = "1").

Each F-frame contains four F-bits; which also aid in synchronization between the Local and the "remote" DS3 terminals. Therefore, each DS3 "M-frame" consists of a total of 28 F-bits. These F-bits exhibit a repeating pattern of "1001" within each F-frame. This fact is also presented in Figure 59 and Figure 60 , which contains bit-fields that are designated as: F1, F0, F0, and F1 (where F0 = "0", and F1 = "1").

Each of these bit-fields will be used by the Receive DS3 Framer block, within the remote terminal equipment, to perform Frame Acquisition and Frame Maintenance functions.

NOTE: *For more information on how the Receive DS3 Framer uses these bit-fields, please see Section 3.3.2.*

4.1.2 Performance Monitoring/Error Detection Bits (Parity)

The DS3 Frame uses numerous bit fields to support performance monitoring of the transmission link between the "Local" Transmitting Terminal and the "Remote" Receiving Terminal. The DS3 frame can contain two types of parity bits, depending upon the framing format chosen. P-bits are available in both the M13 and C-bit Parity Formats. However, the C-bit Parity format also includes additional "CP-Parity" bits.

P-Bits (Applies to M13 and C-Bit Parity Frame Formats)

Each DS3 "M-frame" consists of two (2) P-bits. These two P-bits carry the parity information of the previous DS3 frame for performance monitoring. These two P-bits must be identical, within a given DS3 frame. The Transmit Section will compute the even parity over all 4704 payload bits within a given DS3 frame, and insert the resulting parity information in the P-bit fields of the very next DS3 frame. The two P-bits are set to "1" if the payload of the previous DS3 frame consists of an odd number of "ones" in the frame. Conversely, the two P-bits are set to zero if an even number of "ones" is found in the payload of the previous DS3 frame. For information on how the Receive DS3 Framer handles P-bits, please see Section 3.3.2.6.1.

4.1.3 Alarm and Signaling-Related Overhead Bits

The Alarm Indication Signal (AIS) Pattern (C-Bit Parity Framing Format only)

The Alarm Indication Signal (AIS) pattern is an alarm signal that is inserted into the "outbound" DS3 stream when a failure is detected by the “Local" Terminal. The Transmit DS3 Framer will generate the AIS pattern as defined in ANSI.T1.107a-1990, which is described as follows.

VALID M-BITS, F-BITS, AND P-BITS

- All C-bits are zeros
- All X-bits are set to "1"
- A repeating "1010..." pattern is written into the payload of the DS3 frames.

Consequently, no user (or "payload") data will be transmitted while the Transmit Section of the chip is transmitting the AIS pattern.

The IDLE Condition Signal

The IDLE Condition signal is used to indicate that the DS3 channel is functionally sound, but has not yet been assigned any traffic. The Transmit Section will transmit the IDLE Condition signal as defined in ANSI T1.107a-1990, which is described as follows.

- Valid M-bits, F-bits, and P-bits
- The three CP-bits (F-frame #3) are zeros
- The X-bits are set to "1"
- A repeating "1100.." pattern is written into the payload of the DS3 frames.

FEAC - Far End Alarm & Control (Only available for the C-bit Parity Frame Format)

The third C-bit (C13 or FEAC) in the first F-frame is used as the "Far End Alarm and Control" (FEAC) channel between the "Near-End" DS3 terminal and the "Remote" DS3 terminal. The FEAC channel carries:

- Alarm and Status Information

- Loopback commands to initiate and deactivate DS3 and DS1 loopbacks at the distant terminals.

The FEAC message consists of a six (6) bit code word of the form [d5, d4, d3, d2, d1 d0]. This message is encapsulated with 10 framing bits to form a 16 bit "FEAC Message"; as illustrated below. The FEAC signals are encoded into repeating 16 bit message of the form:

0	d5	d4	d3	d2	d1	d0	0	1	1	1	1	1	1	1	1

Since each DS3 frame carries only one FEAC bit, 16 DS3 frames are required to deliver 1 complete FEAC message. The six bits labeled "dx" can represent up-to 64 distinct messages, of which 43 have been defined in the standards. For a more detailed discussion on the transmission of FEAC Messages, please see Section 3.2.3.1.

FEBE - Far End Block Error (Only available for the C-bit Parity Frame Format)

F-Frame # 4 consists of 3 bit fields for the FEBE (Far-End Block Error) channel. If the (Local) Receive Section (within the Framer IC) detects P-bit parity errors, CP-bit errors or a framing error on the incoming (received) DS3 stream it will inform the Transmit Section of this fact. The Transmit Section will, in turn, set the three FEBE bits (within an outgoing DS3 Frame) to any pattern other than "111" to indicate an error. The Transmit Section will then transmit this information out to the "Remote" Terminal (e.g., the source of the errored-data). The FEBE bits, in the outbound DS3 frames, are set to "111" only if both of the following conditions are true:

- The Receive DS3 Framer has detected no M-bit or F-bit framing errors, and
- No P-Bit parity errors have been detected.
- No CP-Bit errors have been detected.

NOTE: *A more detailed discussion on the Transmit Section's handling of the "FEBE" bit-fields can be found in Section 3.2.4.2.1.9.*

The Yellow Alarm or FERF (Far-End Receive Failure) Indicator

The X-bits are used for sending "Yellow Alarms" or the FERF (Far-End Receive Failure) indication. When the Receive Section (of the XRT72L13), within the "Remote" Receiving terminal equipment, cannot identify valid framing, or detects an AIS pattern in the incoming DS3 data-stream, the Framer IC can be configured such that the Transmit Section will send a "Yellow Alarm" or a FERF (Far-End Receive Failure) indication to the "Remote" Terminal by setting both of the X-bits to zero in the outbound (returning) DS3 path. The X-bits are set to "1" during non-alarm conditions.

4.1.4 The "Data Link" Related Overhead Bits

UDL: User Data Link (C-bit Parity Frame Format Only)

These bit-fields are not used by the framer and are set to "1" by default. However, these bits may be used for the transmission of data via a proprietary data link. The user can access these bit-fields via the Transmit Overhead Data Input Interface and the Receive Overhead Data Output Interface blocks.

DL: Path Maintenance Data Link (C-bit Parity Frame Format Only)

The LAPD transceiver block uses these bit-fields for the transmission and reception of path maintenance data link (PMDL) messages via ITU-T Q.921 (LAP-D) Message frames. Please see Sections 3.2.3.2 and 3.3.3.2 for more information on the operation and function of the LAPD Transmitter.

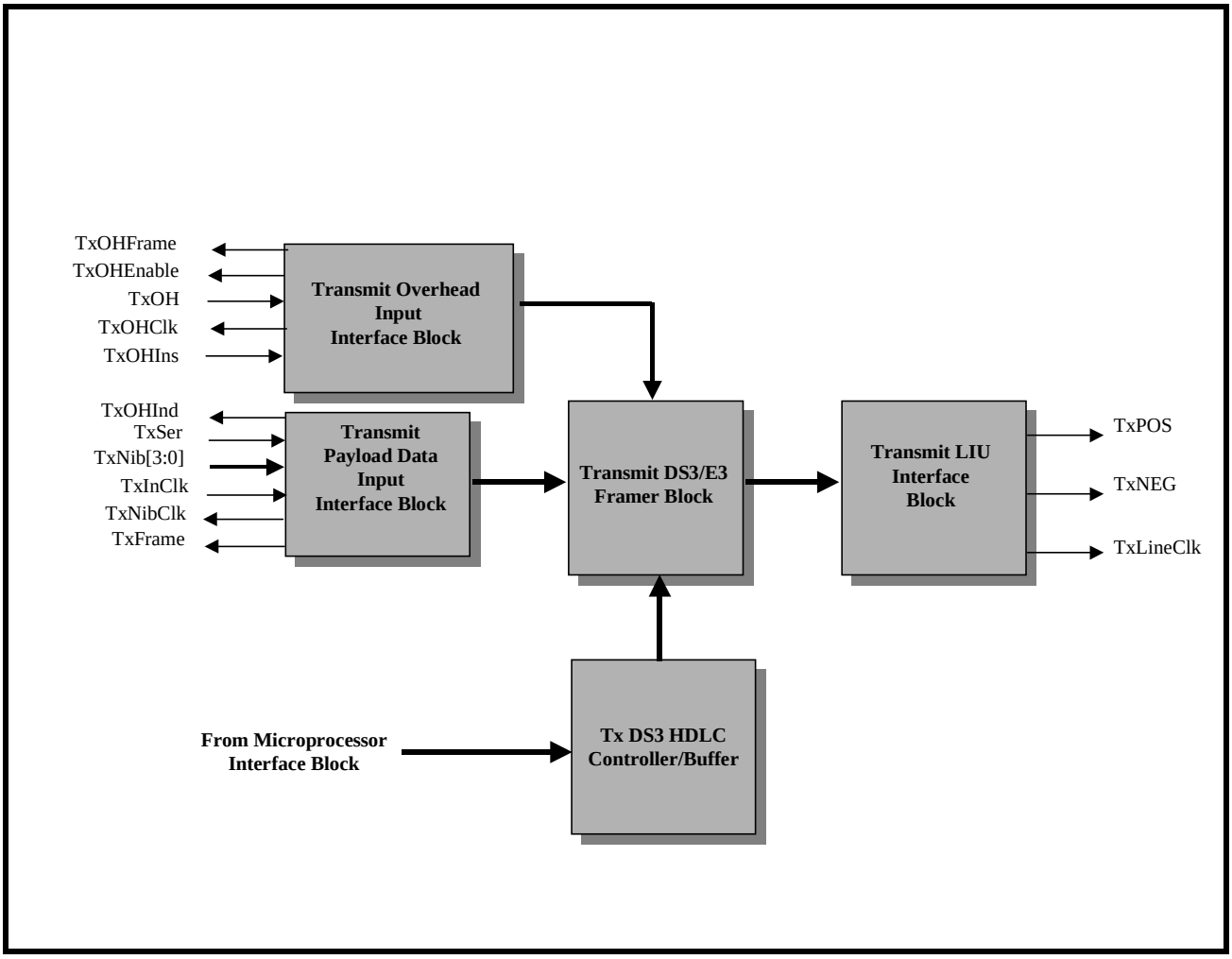
4.2 THE TRANSMIT SECTION OF THE XRT72L13 (CLEAR-CHANNEL FRAMER MODE OPERATION)

When the XRT72L13 has been configured to operate in the Clear-Channel Framer Mode, the Transmit Section of the XRT72L13 consists of the following functional blocks.

- Transmit Payload Data Input Interface block
- Transmit Overhead Data Input Interface block
- Transmit DS3 Framer block
- Transmit DS3 HDLC Controller block
- Transmit LIU Interface block

Figure 61 presents a simple illustration of the Transmit Section of the XRT72L13 Framer IC.

FIGURE 61. A SIMPLE ILLUSTRATION OF THE TRANSMIT SECTION, WITHIN THE XRT72L13; WHEN IT HAS BEEN CONFIGURED TO OPERATE IN THE CLEAR-CHANNEL FRAMER MODE

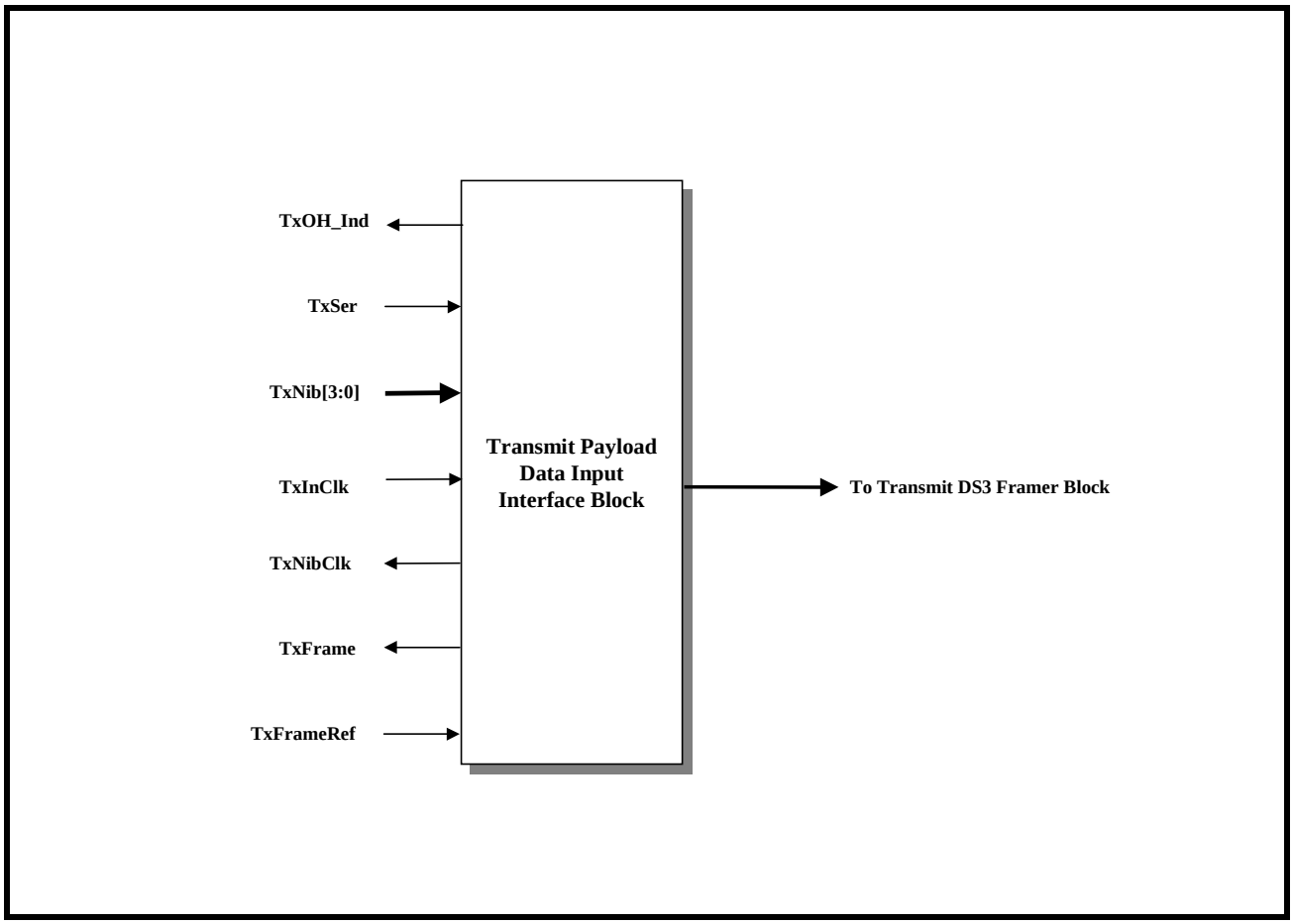


Each of these functional blocks will be discussed in detail in this document.

4.2.1 The "Transmit Payload Data Input Interface" Block

Figure 62 presents a simple illustration of the "Transmit Payload Data Input Interface" block.

FIGURE 62. A SIMPLE ILLUSTRATION OF THE TRANSMIT PAYLOAD DATA INPUT INTERFACE BLOCK



Each of the input and output pins of the "Transmit Payload Data Input Interface" are listed in Table 12 and described below. The exact role that each of these inputs and output pins assume, for a variety of operating scenarios, are described throughout this section.

TABLE 12: LISTING AND DESCRIPTION OF THE PINS ASSOCIATED WITH THE "TRANSMIT PAYLOAD DATA INPUT INTERFACE

SIGNAL NAME	TYPE	DESCRIPTION
TxSer	Input	**Transmit Serial Payload Data Input Pin:** If the user opts to operate the XRT72L13 in the "Serial" mode, then the Terminal Equipment is expected to apply the payload data (that is to be transported via the "outbound" DS3 data stream) to this input pin. The XRT72L13 will sample the data that is at this input pin; upon the rising edge either the "RxOutClk" or the "TxInClk" signal (whichever is appropriate). ***NOTE:*** *This signal is only active if the "NibInt" input pin is pulled "low".*
TxNib[3:0]	Input	**Transmit Nibble-Parallel Payload Data Input pins:** If the user opts to operate the XRT72L13 in the "Nibble-Parallel" mode, then the Terminal Equipment is expected to apply the payload data (that is to be transported via the "outbound" DS3 data stream) to these input pins. The XRT72L13 will sample the data that is at these input pins; upon the rising edge of the "TxNibClk" signal. ***NOTE:*** *These pins are only active if the "NibInt" input pin is pulled "high".*
TxInClk	Input	**Transmit Section Timing Reference Clock Input pin:** The Transmit Section of the XRT72L13 can be configured to use this clock signal as the "Timing Reference". If the user has made this configuration selection, then the XRT72L13 will use this clock signal to sample the data on the TxSer input pin. ***NOTE:*** *If the user has made this configuration selection; then he/she must insure that a 44.736 MHz clock signal is applied to this input pin.*
TxNibClk	Output	**Transmit Nibble Mode Output** If the user opts to operate the XRT72L13 in the "Nibble-Parallel" mode, then the XRT72L13 will derive this clock signal from the selected "Timing Reference" for the Transmit Section of the chip (e.g., either the TxInClk or the RxLineClk signals). The XRT72L13 will use this signal to sample the data on the "TxNib[3:0]" input pins.
TxOHInd	Output	**Transmit Overhead Bit Indicator Output:** This output pin will pulse "high" one-bit period prior to the time that the Transmit Section of the XRT72L13 will be processing an Overhead bit. The purpose of this output pin is to warn the Terminal Equipment that, during the very next bit-period, the XRT72L13 is going to be processing an "Overhead" bit and will be ignoring any data that is applied to the "TxSer" input pin. For DS3 applications, this output pin is only active if the XRT72L13 is operating in the "Serial" Mode. This output pin will be pulled "low" if the device is operating in the "Nibble-Parallel" Mode.
TxFrame	Output	**Transmit "End of Frame" Output Indicator:** The Transmit Section of the XRT72L13 will pulse this output pin "high" (for one bit-period), when the Transmit Payload Data Input Interface is processing the last bit of a given DS3 frame. The purpose of this output pin is to alert the Terminal Equipment that it needs to begin transmission of a new DS3 frame to the XRT72L13 (e.g., to permit the XRT72L13 to maintain Transmit DS3 framing alignment control over the Terminal Equipment).
TxFrameRef	Input	**Transmit Frame Reference Input:** The XRT72L13 permits the user to configure the Transmit Section to use this input pin as a "frame reference". If the user makes this configuration selection, then the Transmit Section will initiate its transmission of a new DS3 frame, upon the rising edge of this signal. The purpose of this input pin is to permit the Terminal Equipment to maintain Transmit DS3 Framing alignment control over the XRT72L13.

TABLE 12: LISTING AND DESCRIPTION OF THE PINS ASSOCIATED WITH THE "TRANSMIT PAYLOAD DATA INPUT INTERFACE

SIGNAL NAME	TYPE	DESCRIPTION
RxOutClk	Output	**Loop-Timed Timing Reference Clock Output pin:** The Transmit Section of the XRT72L13 can be configured to use the "RxLineClk" signal as the "Timing Reference" (e.g., loop-timing). If the user has made this configuration selection, then the XRT72L13 will: • Output a 44.736 MHz clock signal via this pin, to the Terminal Equipment. • Sample the data on the "TxSer" input pin, upon the rising edge of this clock signal.

Operation of the "Transmit Payload Data Input Interface"

The Transmit Payload Data Input Interface is extremely flexible, in that it permits the user to make the following configuration options.

- The "Serial" or the "Nibble-Parallel" Interface Mode
- The "Loop-Timing" or the "TxInClk" (Local Timing) Mode

Further, if the XRT72L13 has been configured to operate in the "TxInClk" (Local Timing) mode, then the user has two additional options.

- The XRT72L13 functions as the "Frame Master" (e.g., it dictates when the Terminal Equipment will initiate the transmission of data within a new DS3 frame).
- The XRT72L13 functions as the "Frame Slave" (e.g., the Terminal Equipment will dictate when the XRT72L13 initiates the transmission of a new DS3 frame).

Given these three set of options, the Transmit Terminal Input Interface can be configured to operate in one of the six (6) following modes.

- Mode 1 - "Serial/Loop-Timed" Mode
- Mode 2 - "Serial/Local-Timed/Frame Slave" Mode
- Mode 3 - "Serial/Local-Timed/Frame Master" Mode
- Mode 4 - "Nibble/Loop-Timed" Mode
- Mode 5 - "Nibble/Local-Timed/Frame Slave" Mode
- Mode 6 - "Nibble/Local-Timed/Frame Master" Mode

Each of these modes are described, in detail, below.

4.2.1.1 Mode 1 - The "Serial/Loop-Timing" Mode

The Behavior of the XRT72L13

If the XRT72L13 has been configured to operate in this mode, then the XRT72L13 will behave as follows.

A. Loop-Timing (Uses the "RxLineClk" signal as the Timing Reference)

Since the XRT72L13 is configured to operate in the "loop-timed" mode, the Transmit Section (of the XRT72L13) will use the "RxLineClk" input clock signal (e.g., the Recovered Clock signal, from the LIU) as its timing source. When the XRT72L13 is operating in this mode it will do the following.

1. It will ignore any signal at the "TxInClk" input pin.
2. The XRT72L13 will output a 44.736MHz clock signal via the "RxOutClk" output pin. This clock signal functions as the "Transmit Payload Data Input Interface" block clock signal.
3. The XRT72L13 will use the rising edge of the "RxOutClk" signal to latch in the data residing on the TxSer input pin.

B. Serial Mode

The XRT72L13 will accept the "DS3" payload data from the Terminal Equipment, in a serial-manner, via the "TxSer" input pin The "Transmit Payload Data Input Interface" block will latch this data into its circuitry, on the rising edge of the "RxOutClk" output clock signal.

C. Delineation of "outbound" DS3 frames

The XRT72L13 will pulse the "TxFrame" output pin "high" for one bit-period; coincident with the XRT72L13 processing the last bit of a given DS3 frame.

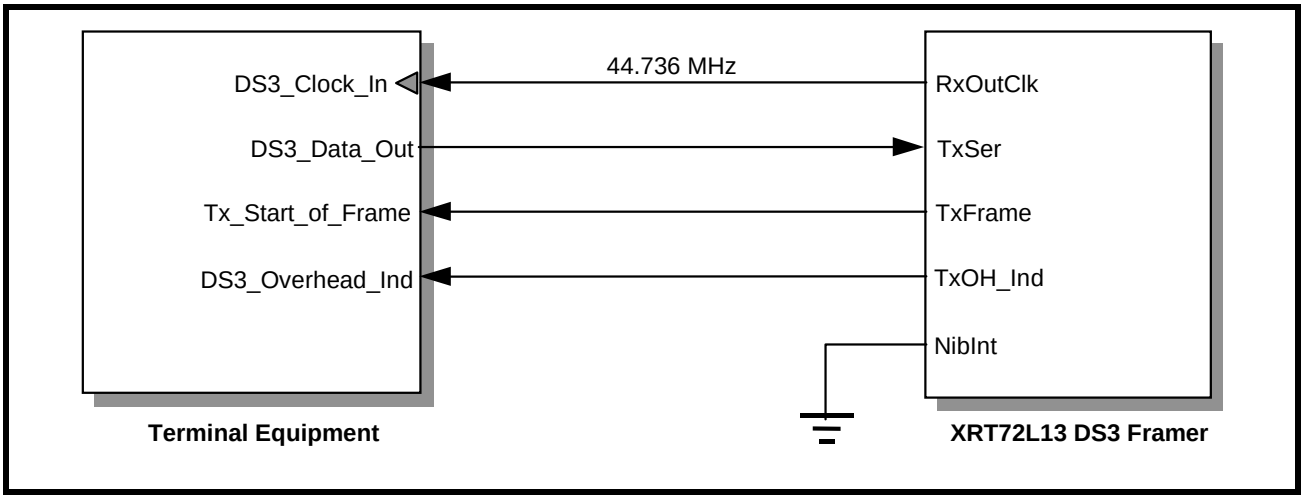
D. Sampling of Payload Data, from the Terminal Equipment

In Mode 1, the XRT72L13 will sample the data at the "TxSer" input, on the rising edge of "RxOutClk".

Interfacing the "Transmit Payload Data Input Interface" block (of the XRT72L13) to the Terminal Equipment for Mode 1 Operation

Figure 63 presents an illustration of the "Transmit Payload Data Input Interface" block (within the XRT72L13) being interfaced to the Terminal Equipment, for "Mode 1" operation.

FIGURE 63. ILLUSTRATION OF THE "TERMINAL EQUIPMENT" BEING INTERFACED TO THE "TRANSMIT PAYLOAD DATA INPUT INTERFACE" BLOCK (OF THE XRT72L13) FOR MODE 1(SERIAL/LOOP-TIMING) OPERATION



Mode 1, Operation of the Terminal Equipment

When the XRT72L13 is operating in this mode; it will function as the source of the 44.736MHz clock signal (via the “RxOutClk” signal). This clock signal will be used as the "Terminal Equipment Interface" clock by both the XRT72L13 IC and the Terminal Equipment.

The Terminal Equipment will serially output the "payload data" of the "outbound" DS3 data stream via its "DS3_Data_Out" pin. The Terminal Equipment will update the data on the "DS3_Data_Out" pin upon the rising edge of the 44.736 MHz clock signal, at its "DS3_Clock_In" input pin (as depicted in Figure 63 and Figure 64).

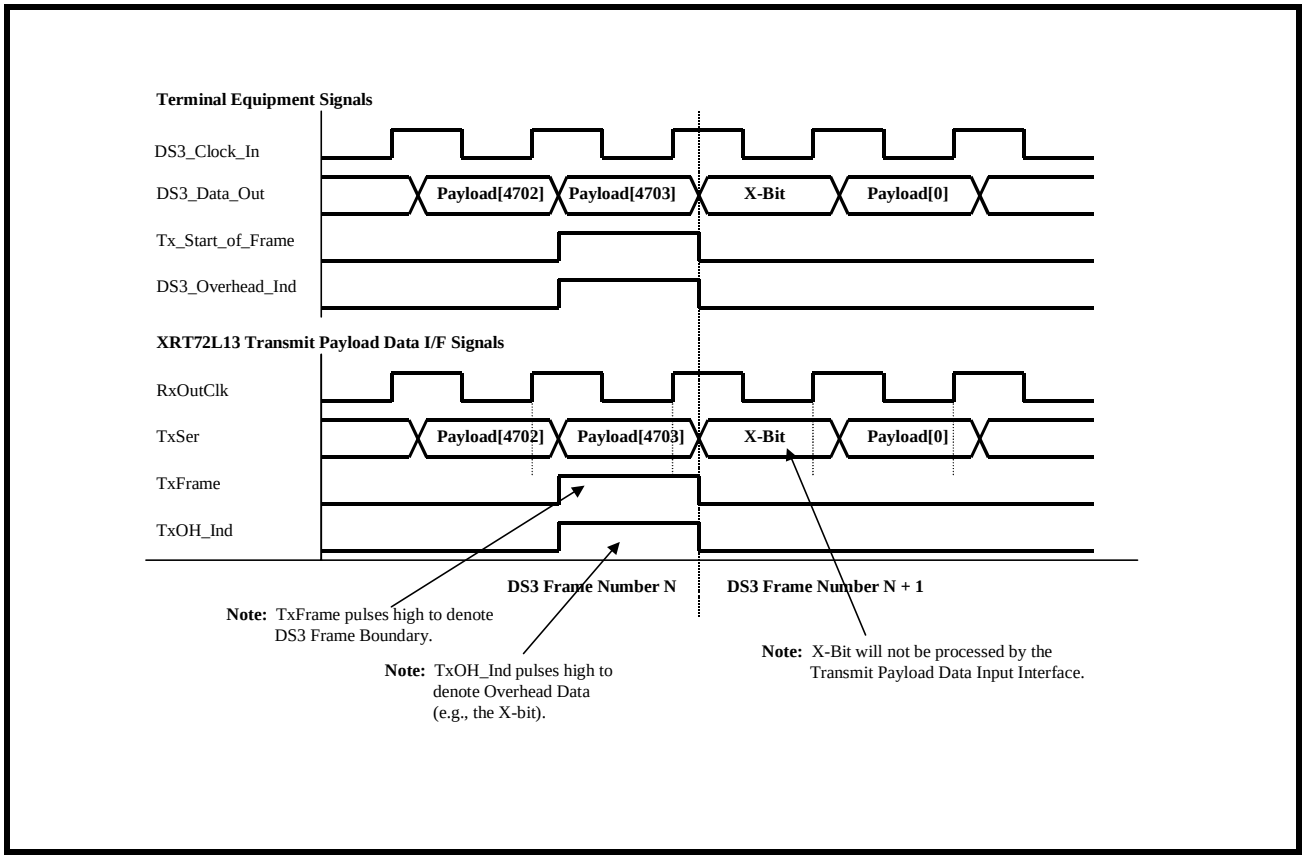
The XRT72L13 will latch the "outbound" DS3 data stream (from the Terminal Equipment) on the rising edge of the "RxOutClk" signal.

The XRT72L13 will indicate that it is processing the last bit, within a given "outbound" DS3 frame, by pulsing its "TxFrame" output pin "high" for one bit-period. When the Terminal Equipment detects this pulse at its "Tx_Start_of_Frame" input, it is expected to begin transmission of the very next outbound DS3 frame to the XRT72L13 via the "DS3_Data_Out" (or "TxSer" pin).

Finally, the XRT72L13 will indicate that it is about to process an overhead bit by pulsing the "TxOH_Ind" output pin "high" one bit period prior to its processing of an OH (Overhead) bit. In Figure 63 , the "TxOH_Ind" output pin is connected to the "DS3_Overhead_Ind" input pin; of the Terminal Equipment. Whenever the "DS3_Overhead_Ind" pin is pulsed "high" the Terminal Equipment is expected to not transmit a DS3 payload bit upon the very next clock edge. Instead, the Terminal Equipment is expected to delay its transmission of the very next payload bit, by one clock cycle.

The behavior of the signals, between the XRT72L13 and the Terminal Equipment, for DS3 Mode 1 operation is illustrated in Figure 64 .

FIGURE 64. BEHAVIOR OF THE "TERMINAL INTERFACE" SIGNALS BETWEEN THE "TRANSMIT PAYLOAD DATA INPUT INTERFACE" BLOCK (OF THE XRT72L13) AND THE TERMINAL EQUIPMENT (FOR MODE 1 OPERATION)



How to configure the XRT72L13 into the "Serial/ Loop-Timed/Non-Overhead Interface" Mode

1. Set the "NibIntf" input pin "low".
2. Set the "TimRefSel[1:0]" bit fields (within the "Framer Operating Mode Register") to "00"; as illustrated below.

OPERATING MODE REGISTER (ADDRESS = 0X00)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Local Loop-back Mode	Line Loop-back Mode	Internal LOS Enable	RESET	Interrupt Enable Reset	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	1	0	1	0	0	0

3. Interface the XRT72L13, to the Terminal Equipment, as illustrated in Figure 63 .

NOTE: *The XRT72L13 Framer IC cannot support the "Framer Local Loop-back" Mode of operation, when operating in the "Loop-Timing" Mode. The user must configure the XRT72L13 Framer IC into any of the following modes, prior to configuring the "Framer Local Loop-back" Mode.*

- Mode 2 - Serial/Local-Timed/Frame-Slave Mode.
- Mode 3 - Serial/Local-Timed/Frame-Master Mode.
- Mode 5 - Nibble-Parallel/Local-Timed/Frame-Slave Mode.
- Mode 6 - Nibble-Parallel/Local-Timed/Frame-Master Mode.

For more detailed information on "Framer Local Loop-back" Mode of operation, please see Section 6.0.

4.2.1.2 Mode 2 - The "Serial/Local-Timed/ Frame-Slave" Mode

Behavior of the XRT72L13

If the XRT72L13 has been configured to operate in this mode, then the XRT72L13 will function as follows.

A. Local-Timing - Uses the "TxInClk" signal as the Timing Reference

In this mode, the Transmit Section of the XRT72L13 will use the TxInClk signal as its timing reference.

B. Serial Mode

The XRT72L13 will receive the DS3 payload data, in a serial manner, via the "TxSer" input pin. The "Transmit Payload Data Input Interface" (within the XRT72L13) will latch this data into its circuitry, on the rising edge of the "TxInClk" input clock signal.

C. Delineation of "outbound" DS3 frames (Frame Slave Mode)

The Transmit Section (of the XRT72L13) will use the "TxInClk" input as its timing reference, and will use the "TxFrameRef" input signal as its "framing reference". In other words, the Transmit Section of the XRT72L13 will initiate frame generation upon the rising edge of the "TxFrameRef" input signal).

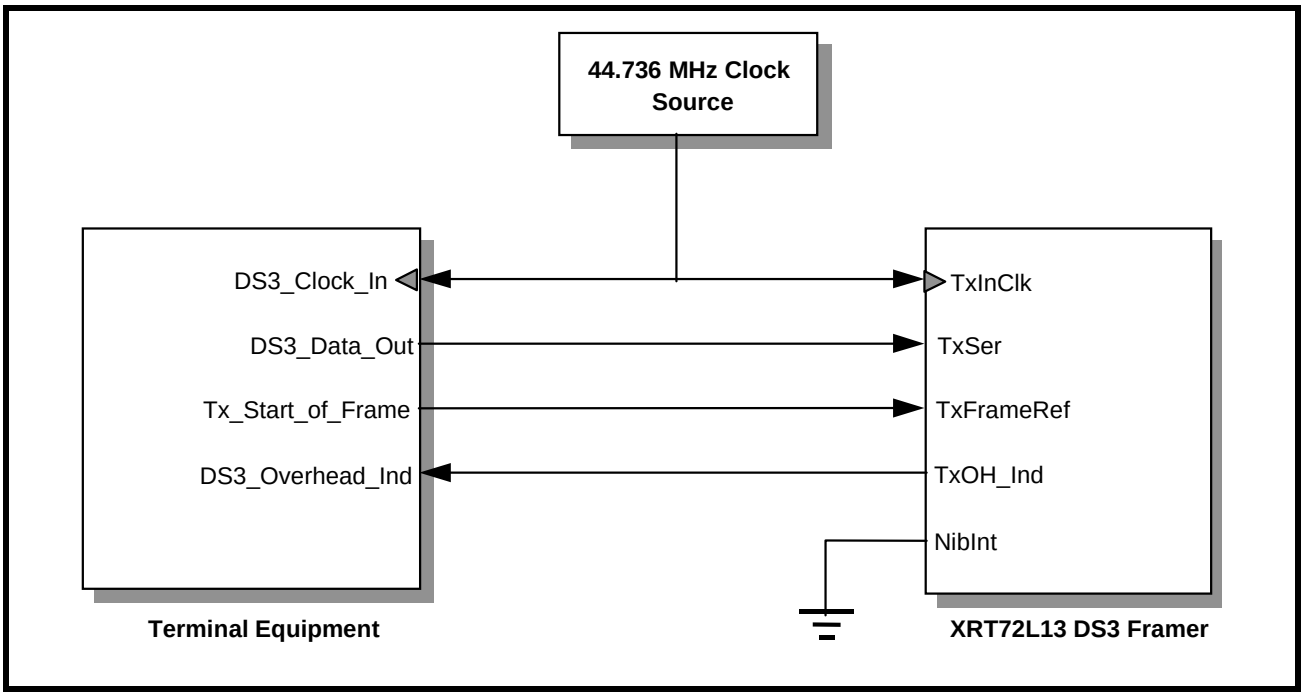
D. Sampling of payload data, from the Terminal Equipment

In Mode 2, the XRT72L13 will sample the data, at the "TxSer" input pin, on the rising edge of "TxInClk".

Interfacing the "Transmit Payload Data Input Interface" block (of the XRT72L13) to the Terminal Equipment for Mode 2 Operation

Figure 65 presents an illustration of the "Transmit Payload Data Input Interface" block (within the XRT72L13) being interfaced to the Terminal Equipment, for "Mode 2" operation.

FIGURE 65. ILLUSTRATION OF THE "TERMINAL EQUIPMENT" BEING INTERFACED TO THE "TRANSMIT PAYLOAD DATA INPUT INTERFACE" BLOCK (OF THE XRT72L13) FOR MODE 2 (SERIAL/LOCAL-TIMED/FRAME-SLAVE) OPERATION



Mode 2, Operation of the Terminal Equipment

As shown in Figure 65 , both the Terminal Equipment and the XRT72L13 will be driven by an external 44.736MHz clock signal. The Terminal Equipment will receive the 44.736MHz clock signal via its "DS3_Clock_In" input pin, and the XRT72L13 Framer IC will receive the 44.736MHz clock signal via the "TxInClk" input pin.

The Terminal Equipment will serially output the "payload data" of the "outbound" DS3 data stream, via the "DS3_Data_Out" output pin, upon the rising edge of the signal at the "DS3_Clock_In" input pin. (Note: The "DS3_Data_Out" output pin of the Terminal Equipment is electrically connected to the "TxSer" input pin). The XRT72L13 Framer IC will latch the data, residing on the "TxSer" input line, on the rising edge of the "TxInClk" signal.

In this case, the Terminal Equipment has the responsibility of providing the "framing reference" signal by pulsing its "Tx_Start_of_Frame" output signal (and in

turn, the "TxFrameRef" input pin of the XRT72L13), "high" for one-bit period, coincident with the first bit of a new DS3 frame. Once the XRT72L13 detects the rising edge of the input at its "TxFrameRef" input pin; it will begin generation of a new DS3 frame.

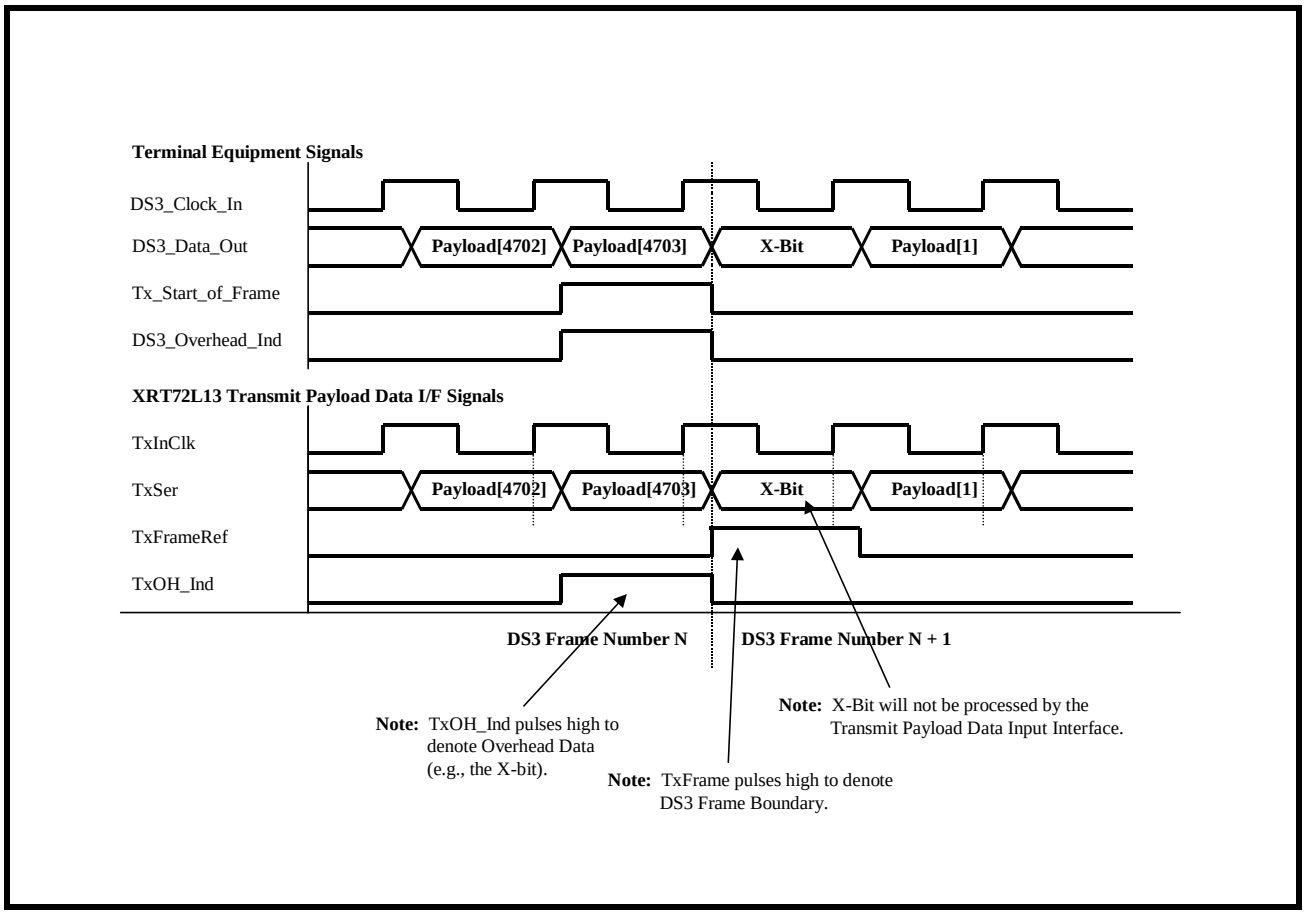
NOTES:

1. *In this case, the Terminal Equipment is controlling the "start" of Frame Generation, and is therefore referred to as the "Frame Master". Conversely, since the XRT72L13 does not control the generation of a new DS3 frame, but is rather driven by the "Terminal Equipment". Hence, the XRT72L13 is referred to as the "Frame Slave".*
2. *If the user opts to configure the XRT72L13 to operate in Mode 2, it is imperative that the "Tx_Start_of_Frame" (or "TxFrameRef") signal is synchronized to the "TxInClk" input clock signal.*

Finally, the XRT72L13 will pulse its "TxOH_Ind" output pin, one bit-period prior to it processing a given "overhead" bit, within the "outbound" DS3 frame. Since the "TxOH_Ind" output pin (of the XRT72L13) is electrically connected to the "DS3_Overhead_Ind"; whenever the XRT72L13 pulses the "TxOH_Ind" output pin "high", it will also be driving the "DS3_Overhead_Ind" input pin (of the Terminal Equipment) "high". Whenever the Terminal Equipment detects this pin toggling "high", it should delay transmission of the very next "DS3 frame" payload bit by one clock cycle.

The behavior of the signals between the XRT72L13 and the Terminal Equipment for DS3 Mode 2 Operation is illustrated in Figure 66 .

FIGURE 66. BEHAVIOR OF THE "TERMINAL INTERFACE" SIGNALS BETWEEN THE XRT72L13 AND THE TERMINAL EQUIPMENT (MODE 2 OPERATION)



How to configure the XRT72L13 to operate in this mode.

1. Set the "NibIntf" input pin "low".
2. Set the "TimRefSel[1:0] bit-fields (within the "Framer Operating Mode Register") to "01" as depicted below.

OPERATING MODE REGISTER (ADDRESS = 0X00)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Local Loop-back Mode	Line Loop-back Mode	Internal LOS Enable	RESET	Interrupt Enable Reset	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	1	0	1	0	0	1

3. Interface the XRT72L13, to the Terminal Equipment, as illustrated in Figure 65 .

4.2.1.3 Mode 3 - The "Serial/Local-Timed/ Frame-Master" Mode

Behavior of the XRT72L13

If the XRT72L13 has been configured to operate in this mode, then the XRT72L13 will function as follows.

A. Local Timing - (Uses the "TxInClk" signal as the Timing Reference)

In this mode, the Transmit Section of the XRT72L13 will use the "TxInClk" signal as its timing reference.

B. Serial Mode

The XRT72L13 will receive the DS3 payload data, in a serial manner, via the "TxSer" input pin. The "Transmit Payload Data Input Interface" (within the XRT72L13) will latch this data into its circuitry, on the rising edge of the "TxInClk" input clock signal.

C. Delineation of "outbound" DS3 frames (Frame Master Mode)

The Transmit Section of the XRT72L13 will use the "TxInClk" signal as its timing reference, and will initiate DS3 frame generation, asynchronously with respect to any externally applied signal. The XRT72L13 will pulse its "TxFrame" output pin "high" whenever its it processing the very last bit-field within a given DS3 frame.

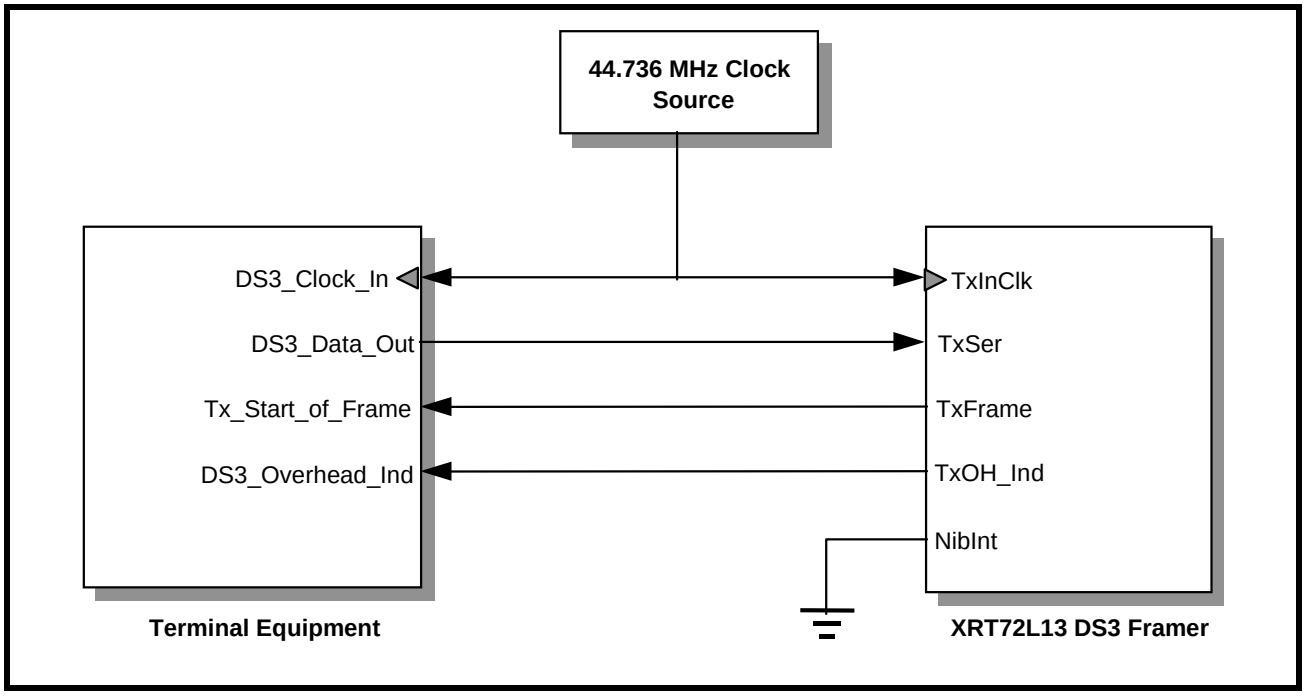
D. Sampling of payload data, from the Terminal Equipment

In Mode 3, the XRT72L13 will sample the data, at the "TxSer" input pin, on the rising edge of "TxInClk".

Interfacing the "Transmit Payload Data Input Interface" block (of the XRT72L13) to the Terminal Equipment for Mode 3 Operation

Figure 67 presents an illustration of the "Transmit Payload Data Input Interface" block (within the XRT72L13) being interfaced to the Terminal Equipment, for "Mode 3" operation.

FIGURE 67. ILLUSTRATION OF THE "TERMINAL EQUIPMENT" BEING INTERFACED TO THE "TRANSMIT PAYLOAD DATA INPUT INTERFACE" BLOCK (OF THE XRT72L13) FOR MODE 3 (SERIAL/LOCAL-TIMED/FRAME-MASTER) OPERATION



Mode 3 Operation of the Terminal Equipment

In Figure 67 , both the Terminal Equipment and the XRT72L13 are driven by an external 44.736MHz clock signal. This clock signal is connected to the "DS3_Clock_In" input of the Terminal Equipment; and the "TxInClk" input pin of the XRT72L13.

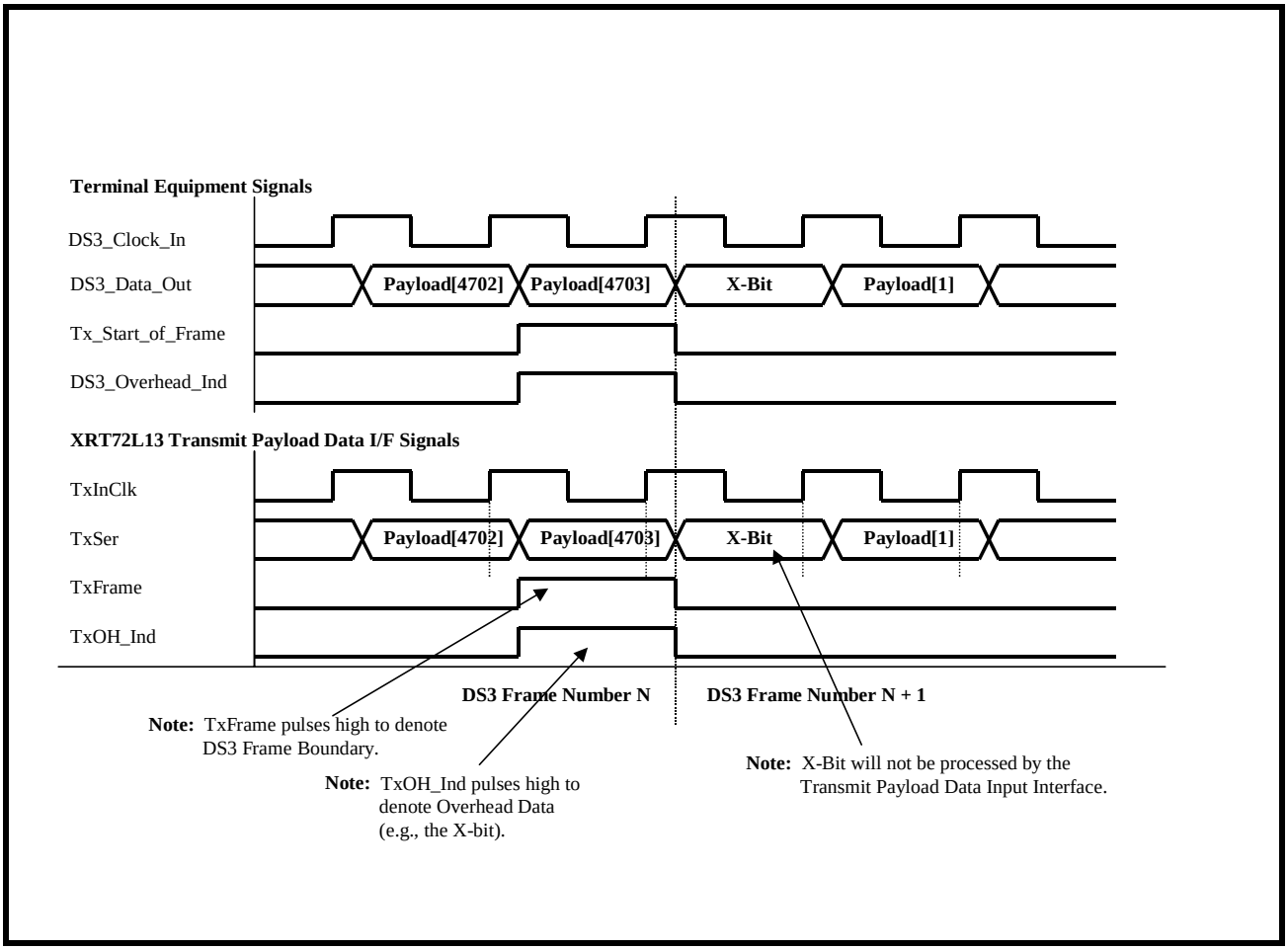
The Terminal Equipment will serially output the payload data on its "DS3_Data_Out" output pin, upon the rising edge of the signal at the "DS3_Clock_In" input pin. Similarly, the XRT72L13 will latch the data, residing on the "TxSer" input pin, on the rising edge of "TxInClk".

The XRT72L13 will pulse the "TxFrame" output pin "high" for one bit-period, coincident while it is processing the last bit-field within a given "outbound" DS3 frame. The Terminal Equipment is expected to monitor the "TxFrame" signal (from the XRT72L13) and to place the first bit, within the very next "outbound" DS3 frame on the "TxSer" input pin. (Note: In this case, the XRT72L13 dictates exactly when the very next DS3 frame will be generated. The Terminal Equipment is expected to respond appropriately by providing the XRT72L13 with the first bit of the new DS3 frame, upon demand. Hence, in this mode, the XRT72L13 is referred to as the "Frame Master" and the "Terminal Equipment" is referred to as the "Frame Slave".

Finally, the XRT72L13 will pulse its "TxOH_Ind" output pin, one bit-period prior to it processing a given "overhead" bit, within the "outbound" DS3 frame. Since the "TxOH_Ind" output pin (of the XRT72L13) is electrically connected to the "DS3_Overhead_Ind"; whenever the XRT72L13 pulses the "TxOH_Ind" output pin "high", it will also be driving the "DS3_Overhead_Ind" input pin (of the Terminal Equipment) "high". Whenever the Terminal Equipment detects this pin toggling "high", it should delay transmission of the very next "DS3 frame" payload bit by one clock cycle.

The behavior of the signal between the XRT72L13 and the Terminal Equipment for DS3 Mode 3 Operation is illustrated in Figure 68 .

FIGURE 68. BEHAVIOR OF THE TERMINAL INTERFACE SIGNALS BETWEEN THE XRT72L13 AND THE TERMINAL EQUIPMENT (DS3 MODE 3 OPERATION)



How to configure the XRT72L13 to operate in this mode.

1. Set the "NibIntf" input pin "low".

2. Set the "TimRefSel[1:0] bit-fields (within the "Framer Operating Mode Register") to "10" or "11" as depicted below.

OPERATING MODE REGISTER (ADDRESS = 0X00)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Local Loop-back Mode	Line Loop-back Mode	Internal LOS Enable	RESET	Interrupt Enable Reset	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	1	0	1	0	1	X

3. Interface the XRT72L13, to the Terminal Equipment, as illustrated in Figure 67 .

4.2.1.4 Mode 4 - The "Nibble-Parallel/Loop-Timed" Mode

Behavior of the XRT72L13

If the XRT72L13 has been configured to operate in this mode, then the XRT72L13 devide will behave as follows.

A. Looped Timing (Uses the RxLineClk as the Timing Reference)

In this mode, the Transmit Section of the XRT72L13 will use the "RxLineClk" signal as its timing reference. When the XRT72L13 is operating in the "Nibble-Mode", it will "internally" divide the RxLineClk signal, by a factor of four (4) and will output this signal via the "TxNibClk" output pin.

B. Nibble-Parallel Mode

The XRT72L13 will accept the "DS3" payload data, from the Terminal Equipment in a "nibble-parallel" manner, via the TxNib[3:0] input pins. The "Transmit Terminal Equipment Input Interface" block will latch this data into its circuitry, on the rising edge of the TxNibClk output signal.

C. Delineation of the "outbound" DS3 frames

The XRT72L13 will pulse the "TxNibFrame" output pin "high" for one bit-period; coincident with the XRT72L13 processing the last nibble of a given DS3 frame.

D. Sampling of payload data, from the Terminal Equipment

In Mode 4, the XRT72L13 will sample the data, at the TxNib[3:0] input pins, on the third rising edge of the "RxOutClk" clock signal, following a pulse in the "TxNibClk" signal (see Figure 70).

NOTE: *The "TxNibClk" signal, from the XRT72L13; operates nominally at 11.184 MHz (e.g., 44.736 MHz divided by 4). However, for reasons described below, "TxNibClk" effectively operates at a lower clock frequency. The Transmit Payload Data Input Interface is only used to accept the payload data, which is intended to be carried by "outbound" DS3 frames. The Transmit Payload Data Input Interface is not designed to accommodate the entire DS3 data stream.*

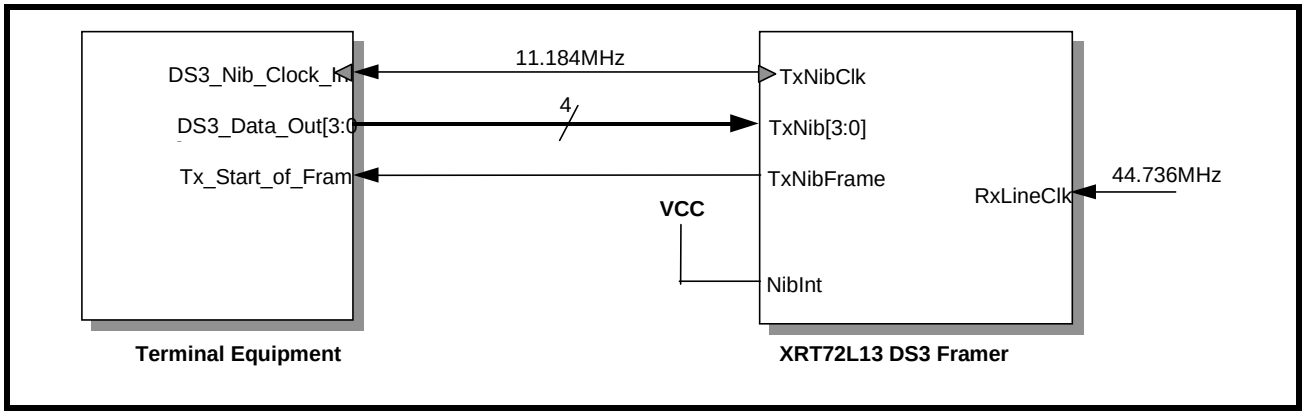
The DS3 Frame consists of 4704 payload bits or 1176 nibbles. Therefore, the XRT72L13 will supply 1176 "TxNibClk" pulses between the rising edges of two consecutive "TxNibFrame" pulses. The DS3 Frame repetition rate is 9.398kHz. Hence, 1176 "TxNibClk" pulses for each DS3 frame period amounts to "TxNibClk" running at approximately 11.052 MHz. The method by which the 1176 "TxNibClk" pulses are distributed throughout the DS3 frame period is presented below.

Nominally, the "Transmit Section" within the XRT72L13 will generate a "TxNibClk" pulse for every 4 "RxOutClk" (or "TxInClk") periods. However, in 14 cases (within a DS3 frame period), the Transmit Payload Data Input Interface will allow 5 "TxInClk" periods to occur between two consecutive "TxNibClk" pulses.

Interfacing the "Transmit Payload Data Input Interface" block (of the XRT72L13) to the Terminal Equipment for Mode 4 Operation

Figure 69 presents an illustration of the "Transmit Payload Data Input Interface" block (within the XRT72L13) being interfaced to the Terminal Equipment, for "Mode 4" Operation.

FIGURE 69. ILLUSTRATION OF THE "TERMINAL EQUIPMENT" BEING INTERFACED TO THE "TRANSMIT PAYLOAD DATA INPUT INTERFACE" BLOCK (OF THE XRT72L13) FOR MODE 4 (NIBBLE-PARALLEL/LOOP-TIMED) OPERATION



Mode 4 Operation of the Terminal Equipment

When the XRT72L13 is operating in this mode, it will function as the source of the 11.184MHz (e.g., the 44.736MHz clock signal divided by "4") clock signal; that will be used as the "Terminal Equipment" Interface clock by both the XRT72L13 and the Terminal Equipment.

The Terminal Equipment will output the payload data of the "outbound" DS3 data stream via its "DS3_Data_Out[3:0]" pins on the rising edge of the "11.184MHz clock signal at the "DS3_Nib_Clock_In" input pin.

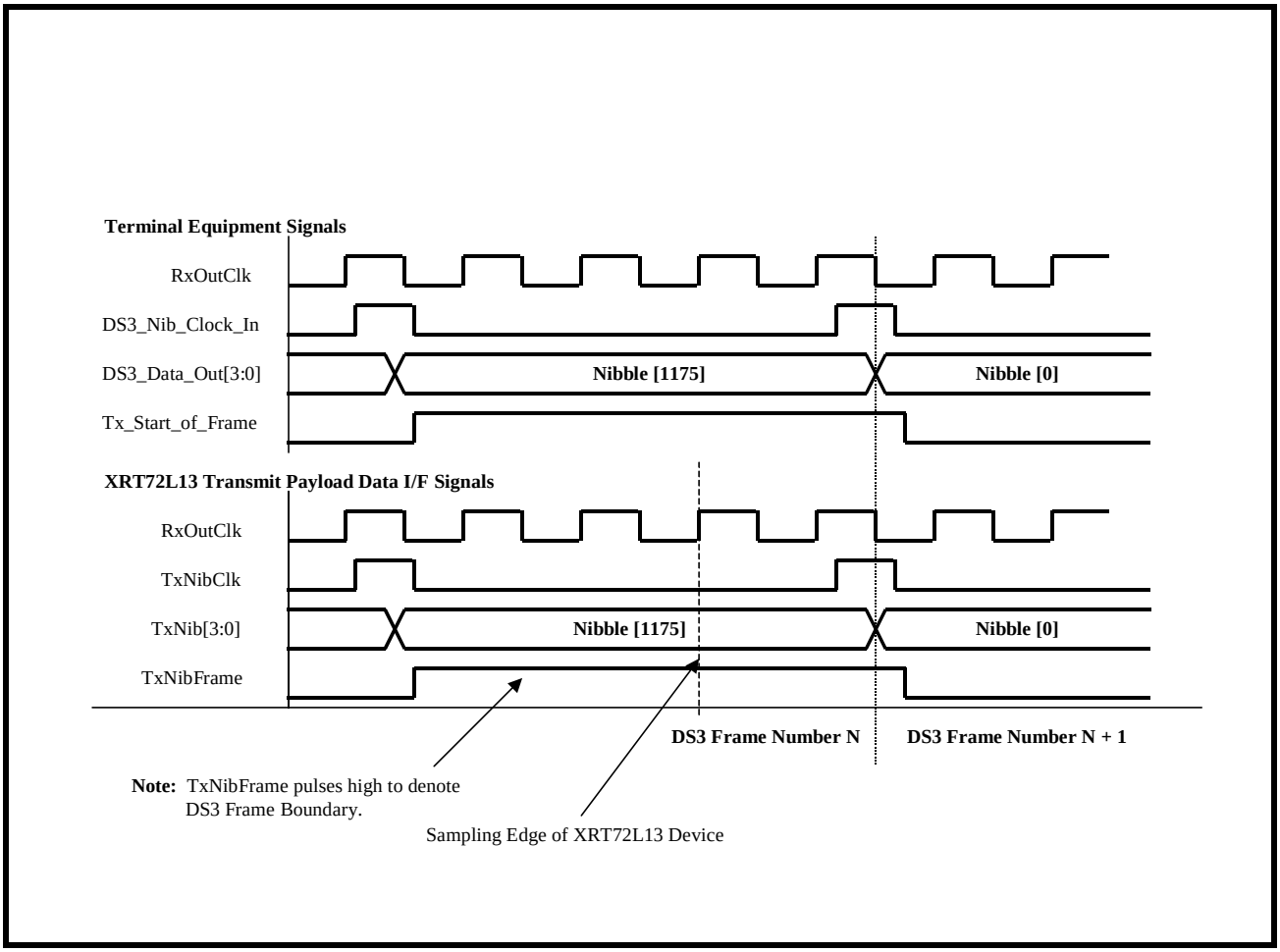
The XRT72L13 will latch the "outbound" DS3 data stream (from the Terminal Equipment) on the rising edge of the "TxNibClk" output clock signal. The

XRT72L13 will indicate that it is processing the last nibble, within a given DS3 frame, by pulsing its "TxNibFrame" output pin "high" for one "TxNibClk" clock period. When the Terminal Equipment detects a pulse at its "Tx_Start_of_Frame" input pin, it is expected to transmit the first nibble, of the very next "outbound" DS3 frame" to the XRT72L13 via the "DS3_Data_Out[3:0]" (or "TxNib[3:0]" pins).

Finally, for the "Nibble-Parallel" Mode operation, the XRT72L13 will continuously pull the "TxOHInd" output pin "low".

The behavior of the signals between the XRT72L13 and the Terminal Equipment for "DS3 Mode 4" Operation is illustrated in Figure 70 .

FIGURE 70. BEHAVIOR OF THE TERMINAL INTERFACE SIGNALS BETWEEN THE XRT72L13 AND THE TERMINAL EQUIPMENT (MODE 4 OPERATION)



How to configure the XRT72L13 into Mode 4

1. Set the "NibIntf" input pin "high".
2. Set the TimRefSel[1:0] bit-fields (within the "Framer Operating Mode" Register) to "00" as illustrated below.

OPERATING MODE REGISTER (ADDRESS = 0X00)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Local Loop-back Mode	Line Loop-back Mode	Internal LOS Enable	RESET	Interrupt Enable Reset	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	1	0	1	0	0	0

3. Interface the XRT72L13, to the Terminal Equipment, as illustrated in Figure 69 .

NOTE: *The XRT72L13 Framer IC cannot support the "Framer Local Loop-back" Mode of operation. The user must configure the XRT72L13 Framer IC into any of the following modes, prior to configuring the "Framer Local-Loop-back" Mode operation.*

- Mode 2 - Serial/Local-Timed/Frame-Slave Mode.
- Mode 3 - Serial/Local-Timed/Frame-Master Mode.
- Mode 5 - Nibble-Parallel/Local-Timed/Frame-Slave Mode.
- Mode 6 - Nibble-Parallel/Local-Timed/Frame-Master Mode.

For more detailed information on the "Framer Local Loop-back Mode" Operation, please see Section 6.0.

4.2.1.5 Mode 5 - The "Nibble-Parallel/Local-Timed/Frame-Slave" Interface Mode

Behavior of the XRT72L13

If the XRT72L13 has been configured to operate in this mode, then the XRT72L13 will function as follows:

A. Local-Timed (Uses the "TxInClk" signal as the Timing Reference)

In this mode, the Transmit Section of the XRT72L13 will use the TxInClk signal at its timing reference. Further, the chip will internally divide the "TxInClk" clock signal by a factor of "4" and will output this divided clock signal via the "TxNibClk" output pin. The "Transmit Terminal Equipment Input Interface" block (within the XRT72L13) will use the rising edge of the "TxNibClk" signal, to latch the data, residing on the "TxNib[3:0] into its circuitry.

B. Nibble-Parallel Mode

The XRT72L13 will accept the "DS3 payload" data, from the Terminal Equipment, in a parallel manner, via the "TxNib[3:0]" input pins. The "Transmit Terminal Equipment Input Interface" will latch this data into its circuitry, on the rising edge of the "TxNibClk" output signal.

C. Delineation of "outbound" DS3 Frames

The Transmit Section will use the "TxInClk" input signal as its timing reference; and will use the "TxFrameRef" input signal as its "Framing Reference" (e.g., the Transmit Section of the XRT72L13 initiates frame generation upon the rising edge of the "TxFrameRef" signal).

NOTE: *In this case, the Terminal Equipment should pulse the "TxFrameRef" input signal (of the XRT72L13 Framer IC) coincident with it applying the first payload nibble, within a given "outbound" DS3 frame. Hence, the duration of this pulse should be one "nibble-period" of the DS3 signal (see Figure 33).*

D. Sampling of payload data, from the Terminal Equipment

In Mode 5, the XRT72L13 will sample the data, at the "TxNib[3:0]" input pins, on the third rising edge of the "TxInClk" clock signal, following a pulse in the "TxNibClk" signal (see Figure 72).

NOTE: *The "TxNibClk" signal, from the XRT72L13; operates nominally at 11.184 MHz (e.g., 44.736 MHz divided by 4). However, for reasons described below, "TxNibClk" effectively operates at a lower clock frequency. The Transmit Payload Data Input Interface is only used to accept the payload data, which is intended to be carried by "outbound" DS3 frames. The Transmit Payload Data Input Interface is not designed to accommodate the entire DS3 data stream.*

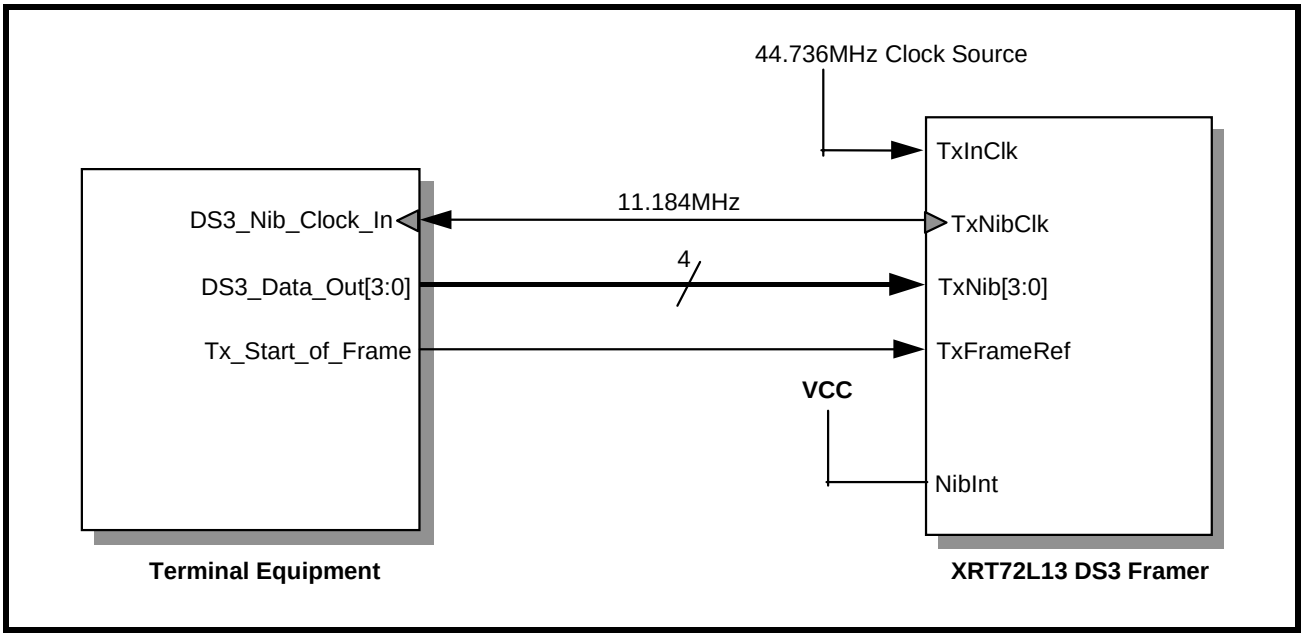
The DS3 Frame consists of 4704 payload bits or 1176 nibbles. Therefore, the XRT72L13 will supply 1176 "TxNibClk" pulses between the rising edges of two consecutive "TxNibFrame" pulses. The DS3 Frame repetition rate is 9.398kHz. Hence, 1176 "TxNibClk" pulses for each DS3 frame period amounts to "TxNibClk" running at approximately 11.052 MHz. The method by which the 1176 "TxNibClk" pulses are distributed throughout the DS3 frame period is presented below.

Nominally, the "Transmit Section" within the XRT72L13 will generate a "TxNibClk" pulse for every 4 "RxOutClk" (or "TxInClk") periods. However, in 14 cases (within a DS3 frame period), the Transmit Payload Data Input Interface will allow 5 "TxInClk" periods to occur between two consecutive "TxNibClk" pulses.

Interfacing the "Transmit Payload Data Input Interface" block (of the XRT72L13) to the Terminal Equipment for Mode 5 Operation

Figure 71 presents an illustration of the "Transmit Payload Data Input Interface" block (within the XRT72L13) being interfaced to the Terminal Equipment, for "Mode 5" Operation.

FIGURE 71. ILLUSTRATION OF THE "TERMINAL EQUIPMENT" BEING INTERFACED TO THE "TRANSMIT PAYLOAD DATA INPUT INTERFACE" BLOCK (OF THE XRT72L13) FOR MODE 5 (NIBBLE-PARALLEL/LOCAL-TIMED/FRAME-SLAVE) OPERATION



Mode 5 Operation of the Terminal Equipment

In Figure 71 both the Terminal Equipment and the XRT72L13 will be driven by an external 11.184MHz clock signal. The Terminal Equipment will receive the 11.184MHz clock signal via the "DS3_Nib_Clock_In" input pin. The XRT72L13 will output the 11.184MHz clock signal via the "TxNibClk" output pin.

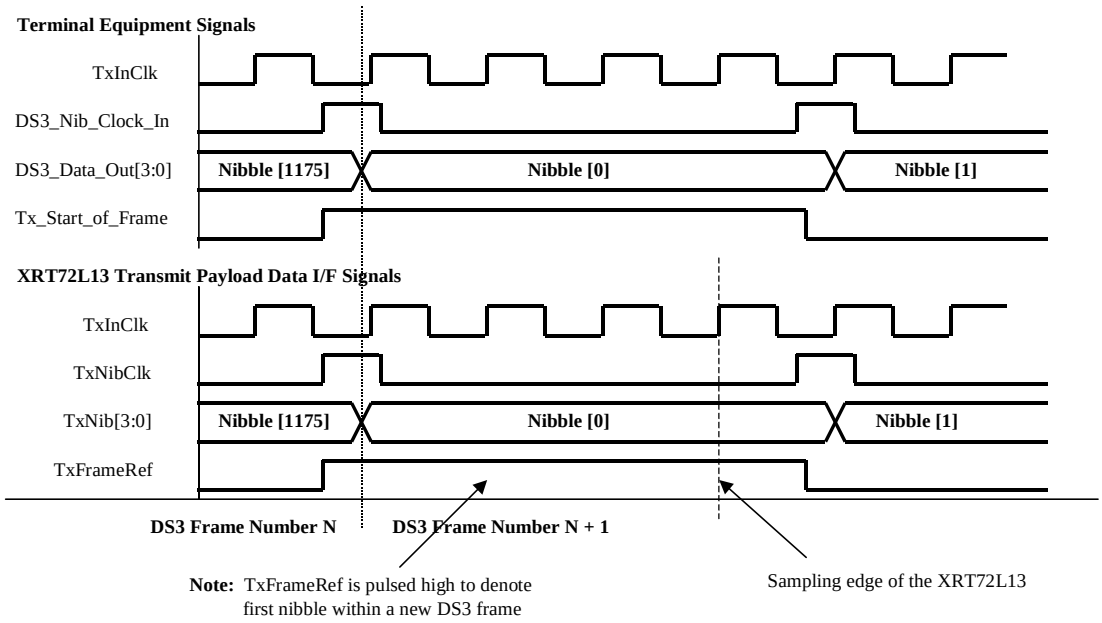
The Terminal Equipment will serially output the data on the "DS3_Data_Out[3:0]" pins, upon the rising edge of the signal at the "DS3_Clock_In" input pin. (Note: The "DS3_Data_Out[3:0]" output pins of the Terminal Equipment is electrically connected to the "TxNib[3:0] input pins.). The XRT72L13 will latch the data, residing on the "TxNib[3:0] input pins, on the rising edge of the "TxNibClk" signal.

In this case, the Terminal Equipment has the responsibility of providing the "framing reference" signal by pulsing the "Tx_Start_of_Frame" output pin (and in turn, the "TxFrameRef" input pin of the XRT72L13) "high" for one bit-period, coincident with the first nibble of a new DS3 frame. Once the XRT72L13 detects the rising edge of the input at its "TxFrameRef" input pin; it will begin generation of a new DS3 frame.

Finally, the XRT72L13 will always internally generate the "Overhead" bits, when it is operating in both the "DS3" and "Nibble-parallel" modes. The XRT72L13 will pull the "TxOHInd" input pin "low".

The behavior of the signals between the XRT72L13 and the Terminal Equipment for DS3 Mode 5 Operation is illustrated in Figure 72 .

FIGURE 72. BEHAVIOR OF THE "TERMINAL INTERFACE" SIGNALS BETWEEN THE XRT72L13 AND THE TERMINAL EQUIPMENT (DS3 MODE 5 OPERATION)



How to configure the XRT72L13 into Mode 5

1. Set the "NibIntf" input pin "high".
2. Set the TimRefSel[1:0] bit-fields (within the "Framer Operating Mode" Register) to "01" as illustrated below.

OPERATING MODE REGISTER (ADDRESS = 0X00)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Local Loop-back Mode	Line Loop-back Mode	Internal LOS Enable	RESET	Interrupt Enable Reset	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	1	0	1	0	0	1

3. Interface the XRT72L13, to the Terminal Equipment, as illustrated in Figure 71 .

4.2.1.6 Mode 6 - The "Nibble-Parallel/TxInClk/ Frame-Master" Interface" Mode

Behavior of the XRT72L13

If the XRT72L13 has been configured to operate in this mode, then the XRT72L13 will function as follows:

A. Local-Timed (Uses the "TxInClk" signal as the Timing Reference)

In this mode, the Transmit Section of the XRT72L13 will use the TxInClk signal at its timing reference.

Further, the chip will internally divide the "TxInClk" clock signal by a factor of "4" and will output this divided clock signal via the "TxNibClk" output pin. The "Transmit Terminal Equipment Input Interface" block (within the XRT72L13) will use the rising edge of the "TxNibClk" signal, to latch the data, residing on the "TxNib[3:0] into its circuitry.

B. Nibble-Parallel Mode

The XRT72L13 will accept the "DS3 payload" data, from the Terminal Equipment, in a parallel manner, via the "TxNib[3:0]" input pins. The "Transmit Terminal Equipment Input Interface" will latch this data into its circuitry, on the rising edge of the "TxNibClk" output signal.

C. Delineation of "outbound" DS3 Frames

The Transmit Section will use the "TxInClk" input signal as its timing reference; and will initiate the generation of DS3 frames, asynchronous with respect to any external signal. The XRT72L13 will pulse the "TxFrame" output pin "high" whenever it is processing the last nibble, within a given "outbound" DS3 frame.

D. Sampling of payload data, from the Terminal Equipment

In Mode 6, the XRT72L13 will sample the data, at the "TxNib[3:0]" input pins, on the third rising edge of the "TxInClk" clock signal, following a pulse in the "TxNibClk" signal (see Figure 74).

NOTE: *The "TxNibClk" signal, from the XRT72L13; operates nominally at 11.184 MHz (e.g., 44.736 MHz divided by 4). However, for reasons described below, "TxNibClk" effectively operates at a lower clock frequency. The Transmit Payload Data Input Interface is only used to accept the payload data, which is intended to be carried by "outbound" DS3 frames. The Transmit Payload Data Input Interface is not designed to accommodate the entire DS3 data stream.*

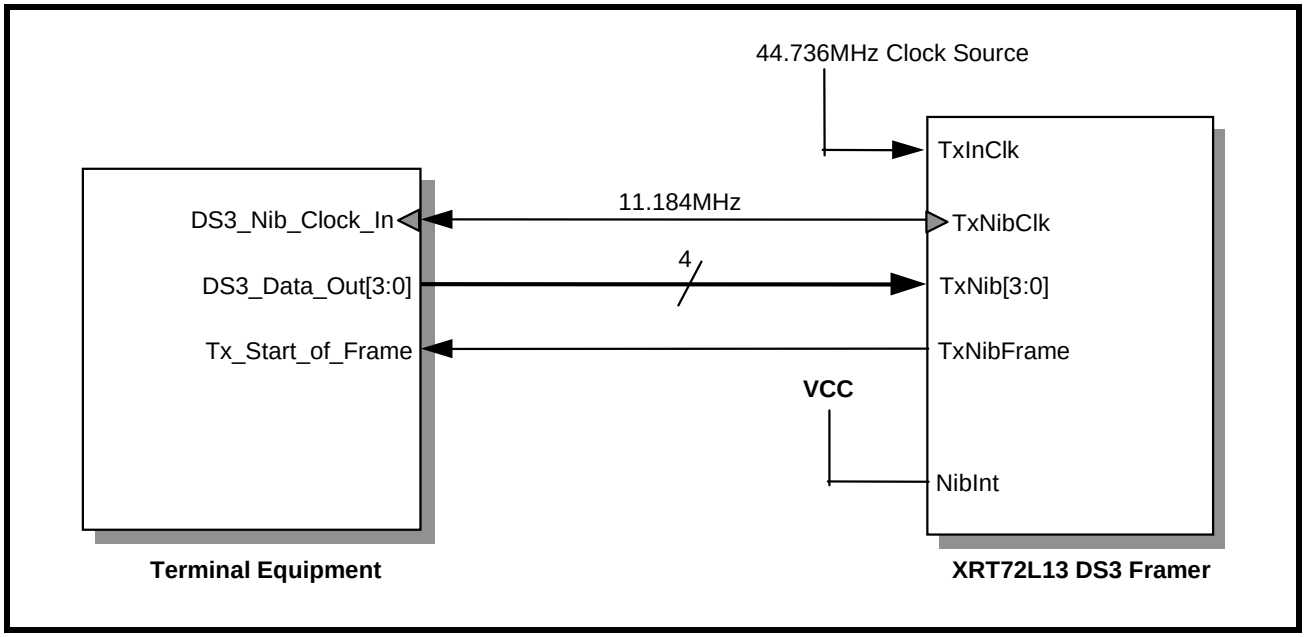
The DS3 Frame consists of 4704 payload bits or 1176 nibbles. Therefore, the XRT72L13 will supply 1176 "TxNibClk" pulses between the rising edges of two consecutive "TxNibFrame" pulses. The DS3 Frame repetition rate is 9.398kHz. Hence, 1176 "TxNibClk" pulses for each DS3 frame period amounts to "TxNibClk" running at approximately 11.052 MHz. The method by which the 1176 "TxNibClk" pulses are distributed throughout the DS3 frame period is presented below.

Nominally, the "Transmit Section" within the XRT72L13 will generate a "TxNibClk" pulse for every 4 "RxOutClk" (or "TxInClk") periods. However, in 14 cases (within a DS3 frame period), the Transmit Payload Data Input Interface will allow 5 "TxInClk" periods to occur between two consecutive "TxNibClk" pulses.

Interfacing the "Transmit Payload Data Input Interface" block (of the XRT72L13) to the Terminal Equipment for Mode 6 Operation

Figure 73 presents an illustration of the "Transmit Payload Data Input Interface" block (within the XRT72L13) being interfaced to the Terminal Equipment, for "Mode 6" Operation.

FIGURE 73. ILLUSTRATION OF THE "TERMINAL EQUIPMENT" BEING INTERFACED TO THE "TRANSMIT PAYLOAD DATA INPUT INTERFACE" BLOCK (OF THE XRT72L13) FOR MODE 6 (NIBBLE-PARALLEL/LOCAL-TIMED/FRAME-MASTER) OPERATION



Mode 6, Operation of the Terminal Equipment

In Figure 73 both the Terminal Equipment and the XRT72L13 will be driven by an external 11.184MHz clock signal. The Teriminal Equipment will receive the 11.184MHz clock signal via the "DS3_Nib_Clock_In" input pin. The XRT72L13 will output the 11.184MHz clock signal via the "TxNibClk" output pin.

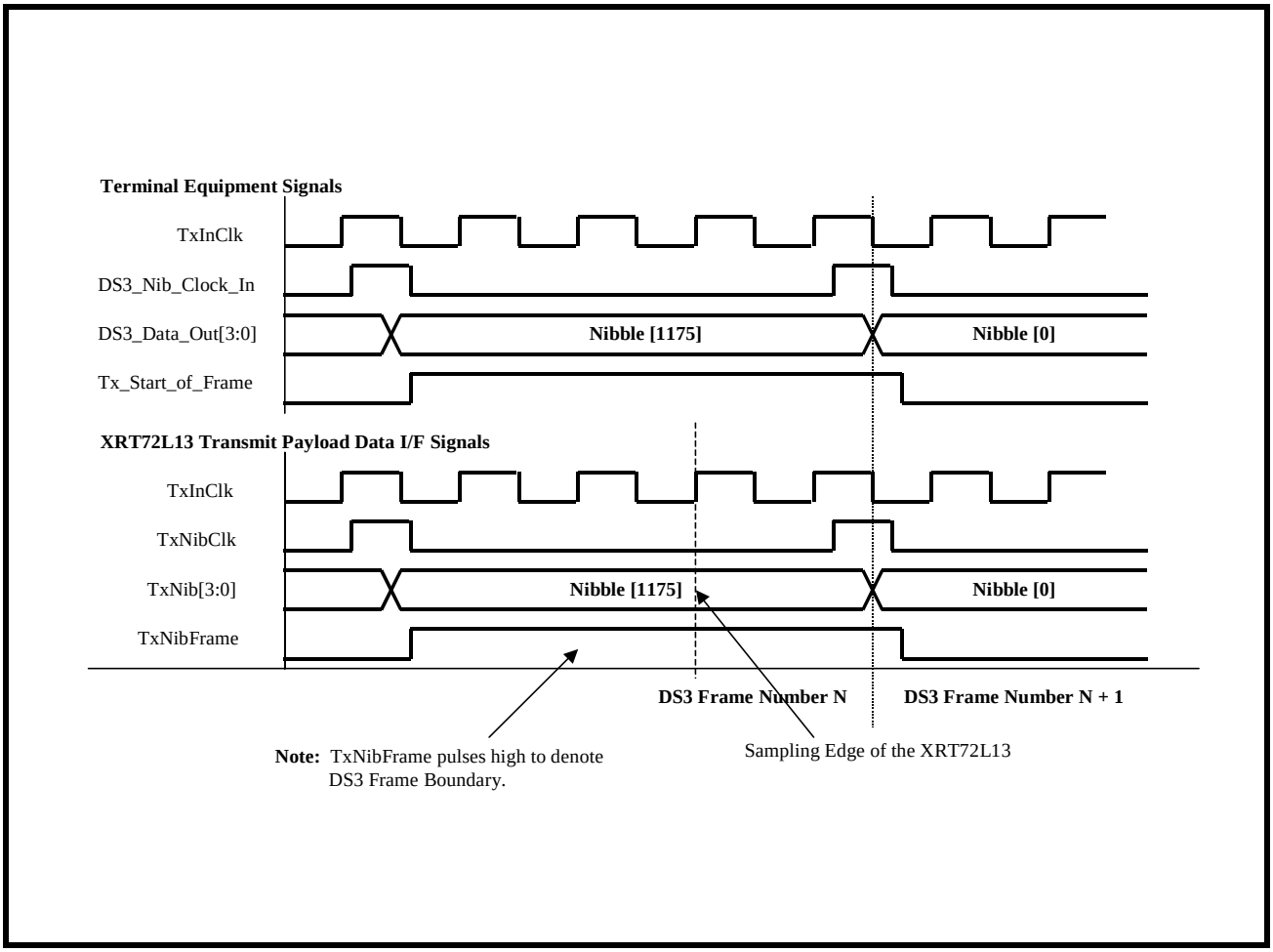
The Terminal Equipment will serially output the data on the "DS3_Data_Out[3:0]" pins upon the rising edge of the signal at the "DS3_Clock_In" input pin. The XRT72L13 will latch the data, residing on the "TxNib[3:0] input pins, on the rising edge of the "TxNibClk" signal.

In this case the XRT72L13 has the responsibility of providing the "framing reference" signal by pulsing the "TxFrame" output pin (and in turn the "Tx_Start_of_Frame" input pin of the Terminal Equipment) "high" for one bit-period, coincident with the last bit within a given DS3 frame.

Finally, the XRT72L13 will always internally generate the "Overhead" bits, when it is operating in both the "DS3" and "Nibble-parallel" modes. The XRT72L13 will pull the "TxOHInd" input pin "low".

The behavior of the signals between the XRT72L13 and the Terminal Equipment for "DS3 Mode 6" Operation is illustrated in Figure 74 .

FIGURE 74. BEHAVIOR OF THE "TERMINAL INTERFACE" SIGNALS BETWEEN THE XRT72L13 AND THE TERMINAL EQUIPMENT (DS3 MODE 6 OPERATION)



How to configure the XRT72L13 into Mode 6

1. Set the "NibInt" input pin "high".

2. Set the "TimRefSel[1:0] bit-fields (within the "Framer Operating Mode" Register) to "1X" as illustrated below.

OPERATING MODE REGISTER (ADDRESS = 0X00)

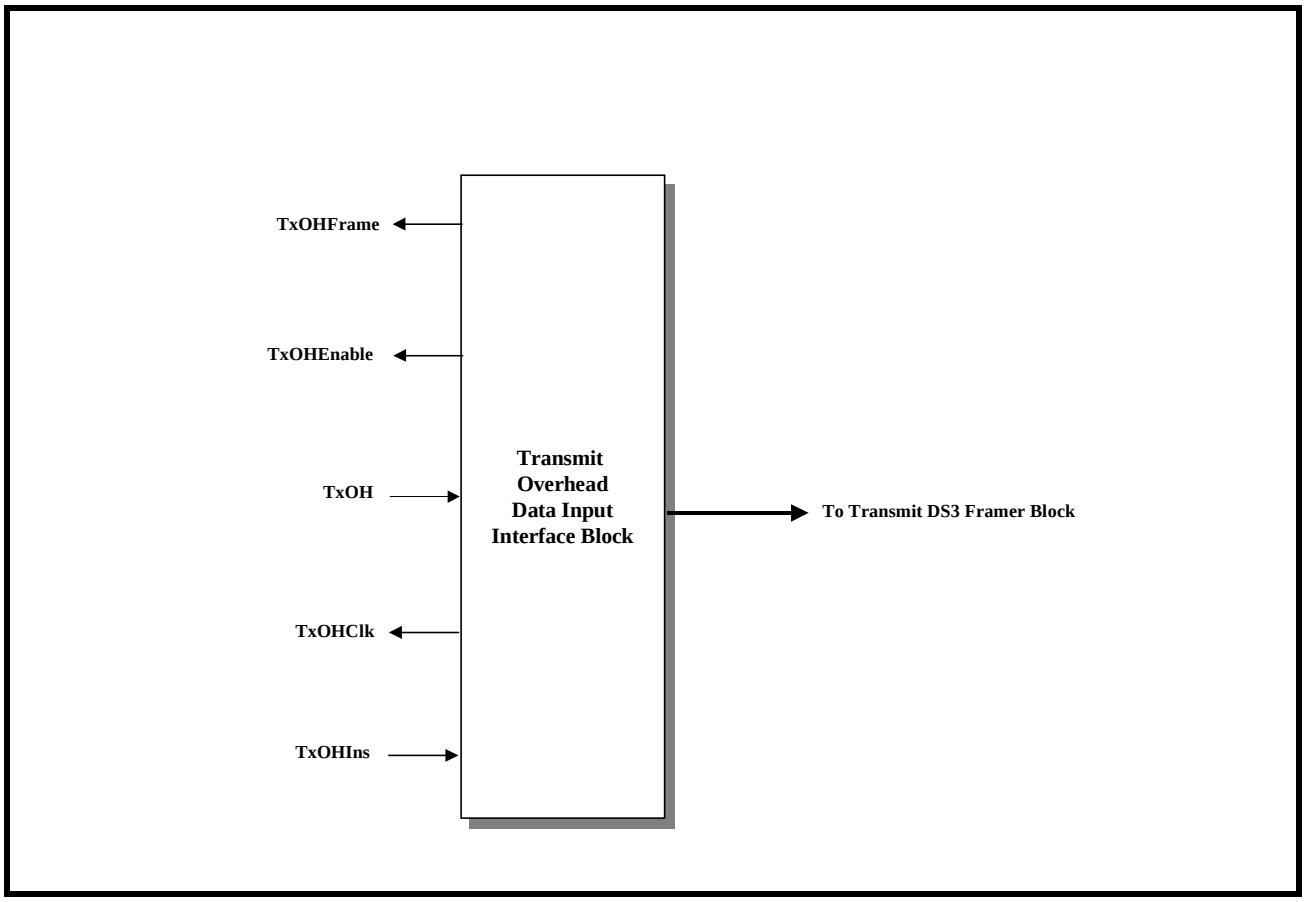
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Local Loop-back Mode	Line Loop-back Mode	Internal LOS Enable	RESET	Interrupt Enable Reset	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	1	0	1	0	1	x

3. Interface the XRT72L13, to the Terminal Equipment, as illustrated in Figure 73 .

4.2.2 The Transmit Overhead Data Input Interface

Figure 75 presents a simple illustration of the "Transmit Overhead Data Input Interface" block within the XRT72L13.

FIGURE 75. SIMPLE ILLUSTRATION OF THE "TRANSMIT OVERHEAD DATA INPUT INTERFACE" BLOCK



The DS3 Frame consists of 4760 bits. Of these bits, 4704 bits are "payload" bits and the remaining 56 bits are "overhead" bits. The XRT72L13 has been designed to handle and process both the "payload" type and "overhead" type bits for each DS3 frame. Within the "Transmit Section" within the XRT72L13, the "Transmit Payload Data Input Interface" has been designed to handle the "payload" data. Likewise, the "Transmit Overhead Data Input Interface" has been designed to handle and process the overhead bits.

The Transmit Section of the XRT72L13 generates or processes the various overhead bits within the DS3 frame, in the following manner.

The Frame Synchronization Overhead Bits (e.g., the "F" and "M" bits)

The "F" and "M" bits are always internally generated by the "Transmit Section" of the XRT72L13. These overhead bits are used (by the Remote Terminal Equipment) for Frame Synchronization purposes. Hence, the user cannot insert his/her value for the "F" and "M" bits into the "outbound" DS3 data stream, via the "Transmit Overhead Data Input Interface". Any attempt to externally insert values for the “F” and “M” bits, will be ignored by the “Transmit Overhead Data Input Interface” block.

The "Performance Monitoring" Overhead Bits (P and CP Bits)

The P-bits are always internally generated by the Transmit Section of the XRT72L13. The “P” bits are used by the “Remote Terminal Equipment” to perform error-checking/detection of a DS3 data stream, as it is transmitted from one Terminal Equipment to adjacent Terminal Equipment (e.g., point-to-point checking). Hence, the user cannot insert his/her value for the "P-bits" into the "outbound" DS3 data stream, via the "Transmit Overhead Data Input Interface".

In contrast to “P” bits, “CP” bits are used perform error-checking/detection of a DS3 data stream from the “Source” Terminal Equipment to the “Sink” Terminal Equipment. In applications where a given DS3 data stream is received via one port, and is output via another port; it is necessary that the “CP” bit-values remain constant. The only way to insure this to (1) extract out the “CP” bit values, via the “Receiving Line Card” and (2) insert these CP-bit values into the “outbound” DS3 data stream, via the “Transmit Overhead

Data Input Interface" block. Hence, the "Transmit Overhead Data Input Interface" block will permit the user to externally insert the "CP" bits into the "outbound" DS3 data stream.

The "Alarm" and signaling related Overhead bits

Bits that are used to transport the "alarm" conditions can be either internally generated by the Transmit Section within the XRT72L13, or can be externally generated and inserted into the "outbound" DS3 data stream, via the Transmit Overhead Data Input Interface. The DS3 frame overhead bits that fall into this category are:

- The "X" bits
- The "FEAC" bits
- The "FEBE" bits.

The Data Link Related Overhead Bits

The DS3 frame structure also contains bits which can be used to transport "User Data Link" information and "Path Maintenance Data Link" information. The "UDL" (User Data Link) bits are only accessible via the "Transmit Overhead Data Input Interface. The Path Maintenance Data Link (PMDL) bits can either be sourced from the "Transmit LAPD Controller/Buffer" or via the "Transmit Overhead Data Input Interface".

Table 13 lists the "Overhead Bits" within the DS3 frame. Additionally, this table also indicates whether or not these overhead bits can be sourced by the "Transmit Overhead Data Input Interface" or not.

TABLE 13: A LISTING OF THE OVERHEAD BITS WITHIN THE DS3 FRAME, AND THEIR POTENTIAL SOURCES, WITHIN THE XRT72L13

OVERHEAD BIT	INTERNALLY GENERATED	ACCESSIBLE VIA THE "TRANSMIT OVERHEAD DATA INPUT INTERFACE"	BUFFER/REGISTER ACCESSIBLE
P	Yes	No	Yes*
X	Yes	Yes	Yes
F	Yes	No	Yes*
M	Yes	No	Yes*
FEAC	No	Yes	Yes
FEBE	Yes	Yes	Yes
DL	No	Yes	Yes+
UDL	No	Yes	No
CP	No	Yes	No

NOTES:

* The XRT72L13 contains "mask register bits" that permit the user to alter the state of the internally generated value for these bits.

+ The Transmit LAPD Controller/Buffer can be configured to be the source of the DL bits, within the "outbound" DS3 data stream.

In all, the "Transmit Overhead Data Input Interface" permits the user to insert "overhead data" into the "outbound" DS3 frames via the following two different methods.

- Method 1 - Using the "TxOHClk" clock signal
- Method 2 - Using the "TxInClk" and the "TxOHEnable" signals.

Each of these methods are described below.

4.2.2.1 4.2.2.1 Method 1 - Using the TxOHClk Clock Signal

The "Transmit Overhead Data Input Interface" consists of the five signals. Of these five (5) signals, the following four (4) signals are to be used when implementing "Method 1".

- TxOH
- TxOHClk
- TxOHFrame
- TxOHIns

Each of these signals are listed and described below.

Table 14 .

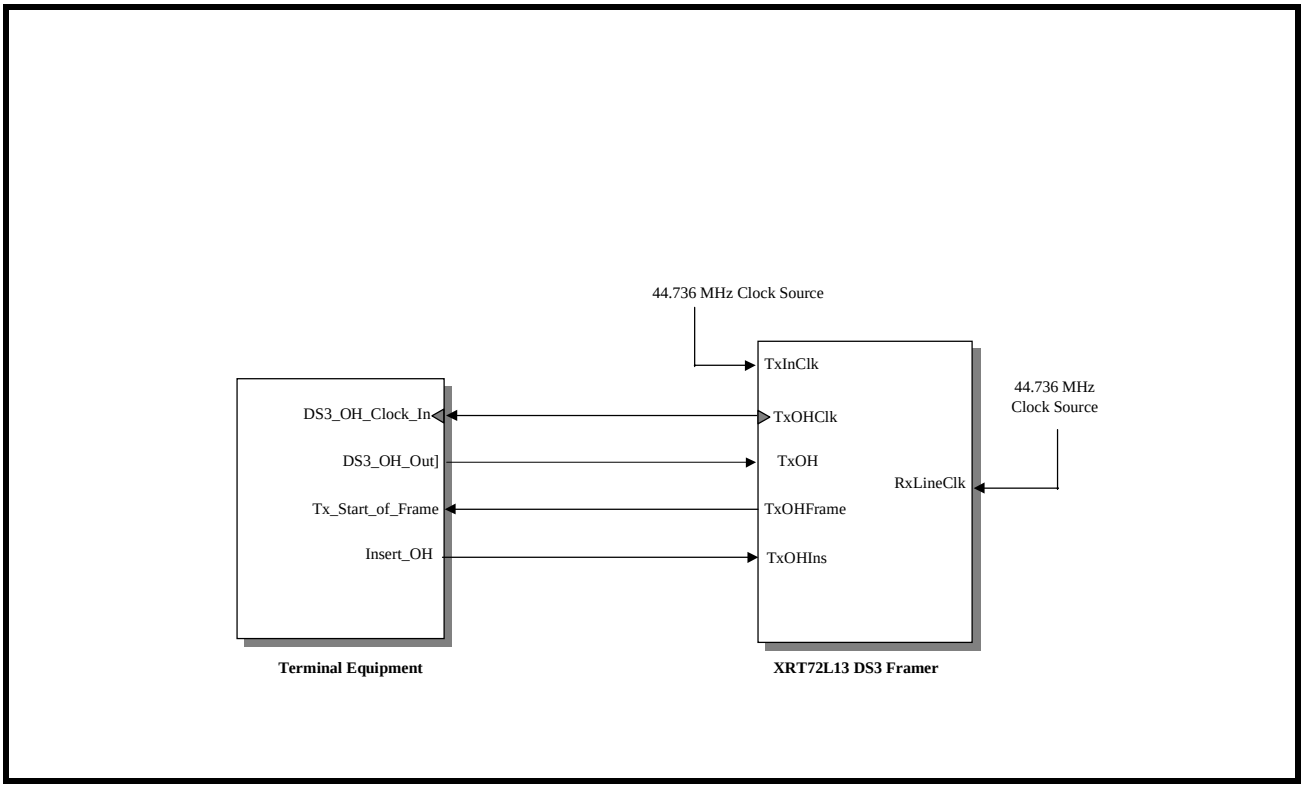
TABLE 14: DESCRIPTION OF "METHOD 1" TRANSMIT OVERHEAD INPUT INTERFACE SIGNALS

NAME	TYPE	DESCRIPTION
TxOHIns	Input	**Transmit Overhead Data Insert Enable input pin.** Asserting this input signal (e.g., setting it "high") enables the Transmit Overhead Data Input Interface to accept "overhead" data from the Terminal Equipment. In other words, while this input pin is "high", the Transmit Overhead Data Input Interface will sample the data at the "TxOH" input pin, on the falling edge of the "TxOHClk" output signal. Conversely, setting this pin "low" configures the "Transmit Overhead Data Input Interface" to NOT sample (e.g., ignore) the data at the "TxOH" input pin, on the falling edge of the "TxOHClk" output signal. ***NOTE:*** *If the Terminal Equipment attempts to insert an overhead bit that cannot be accepted by the "Transmit Overhead Data Input Interface" (e.g., if the Terminal Equipment asserts the "TxOHIns" signal, at a time when one of these "non-insertable" overhead bits are being processed); that particular insertion effort will be ignored.*
TxOH	Input	**Transmit Overhead Data Input pin:** The Transmit Overhead Data Input Interface accepts the overhead data via this input pin, and inserts into the "overhead" bit position within the very next "outbound" DS3 frame. If the "TxOHIns" pin is pulled "high", the Transmit Overhead Data Input Interface will sample the data at this input pin (TxOH), on the falling edge of the "TxOHClk" output pin. Conversely, if the "TxOHIns" pin is pulled "low", then the Transmit Overhead Data Input Interface will NOT sample the data at this input pin (TxOH). Consequently, this data will be ignored.
TxOHClk	Output	**Transmit Overhead Input Interface Clock Output signal:** This output signal serves two purposes: 1. The Transmit Overhead Data Input Interface will provide a rising clock edge on this signal, one bit-period prior to the instant that the "Transmit Overhead Data Input Interface" is processing an overhead bit. 2. The Transmit Overhead Data Input Interface will sample the data at the TxOH input, on the falling edge of this clock signal (provided that the TxOHIns input pin is "high"). ***NOTE:*** *The Transmit Overhead Data Input Interface will supply a clock edge for all overhead bits within the DS3 frame (via the "TxOHClk" output signal). This includes those overhead bits that the "Transmit Overhead Data Input Interface" will not accept from the Terminal Equipment.*
TxOHFrame	Output	**Transmit Overhead Input Interface Frame Boundary Indicator Output:** This output signal pulses "high" when the XRT72L13 is processing the last bit within a given DS3 frame. The purpose of this output signal is to alert the Terminal Equipment that the Transmit Overhead Data Input Interface" block is about to begin processing the overhead bits for a new DS3 frame.

Interfacing the "Transmit Overhead Data Input Interface" to the Terminal Equipment.

Figure 76 illustrates how one should interface the "Transmit Overhead Data Input Interface" to the Terminal Equipment, when using "Method 1".

FIGURE 76. ILLUSTRATION OF THE "TERMINAL EQUIPMENT" BEING INTERFACED TO THE "TRANSMIT OVERHEAD DATA INPUT INTERFACE" (METHOD 1)



Method 1 Operation of the Terminal Equipment

If the Terminal Equipment intends to insert any overhead data into the "outbound" DS3 data stream, (via the Transmit Overhead Data Input Interface), then it is expected to do the following.

1. To sample the state of the "TxOHFrame" signal (e.g., the "Tx_Start_of_Frame" input signal) on the rising edge of the "TxOHClk" (e.g., the "DS3_OH_Clock_In" signal).
2. To keep track of the number of rising clock edges that have occurred, via the "TxOHClk" (e.g., the "DS3_OH_Clock_In" signal) since the last time the "TxOHFrame" signal was sampled "high". By doing this the Terminal Equipment will be able to keep track of which overhead bit is being processed by the “Transmit Overhead Data Input Interface” block at any given time. When the Terminal Equipment “knows” which overhead bit is being processed, at a given “TxOHClk” period, it will know when to insert a desired overhead bit value into the “outbound” DS3 data stream. From this, the Terminal Equipment will know when it should assert the “TxOHIns” input pin and place the appropriate value on the “TxOH” input pin (of the XRT72L13).

Table 15 relates the number of rising clock edges (in the "TxOHClk" signal, since "TxOHFrame" was sampled "high") to the DS3 Overhead Bit, that is being processed.

TABLE 15: THE RELATIONSHIP BETWEEN THE NUMBER OF RISING CLOCK EDGES IN TXOHCLK, (SINCE "TXOHFRAME" WAS LAST SAMPLED "HIGH") TO THE DS3 OVERHEAD BIT, THAT IS BEING PROCESSED

NUMBER OF RISING CLOCK EDGES IN TXOHCLK	THE OVERHEAD BIT EXPECTED BY THE "XRT72L13"	CAN THIS OVERHEAD BIT BE ACCEPTED BY THE XRT72L13?
0 (Clock edge is coincident with TxOHFrame being detected “high”)	X	Yes
1	F1	No
2	AIC	Yes
3	F0	No
4	NA	Yes
5	F0	No
6	FEAC	Yes
7	F1	No
8	X	Yes
9	F1	No
10	UDL	Yes
11	F0	No
12	UDL	Yes
13	F0	No
14	UDL	Yes
15	F1	No
16	P	No
17	F1	No
18	CP	Yes
19	F0	No
20	CP	Yes
21	F0	No
22	CP	Yes
23	F1	No
24	P	No
25	F1	No
26	FEBE	Yes
27	F0	No
28	FEBE	Yes
29	F0	No

TABLE 15: THE RELATIONSHIP BETWEEN THE NUMBER OF RISING CLOCK EDGES IN TXOHCLK, (SINCE "TXOHFRAME" WAS LAST SAMPLED "HIGH") TO THE DS3 OVERHEAD BIT, THAT IS BEING PROCESSED

NUMBER OF RISING CLOCK EDGES IN TXOHCLK	THE OVERHEAD BIT EXPECTED BY THE "XRT72L13"	CAN THIS OVERHEAD BIT BE ACCEPTED BY THE XRT72L13?
30	FEBE	Yes
31	F1	No
32	M0	No
33	F1	No
34	DL	Yes
35	F0	No
36	DL	Yes
37	F0	No
38	DL	Yes
39	F1	No
40	M1	No
41	F1	No
42	UDL	Yes
43	FO	No
44	UDL	Yes
45	FO	No
46	UDL	Yes
47	F1	No
48	M0	No
49	F1	No
50	UDL	Yes
51	F0	No
52	UDL	Yes
53	F0	No
54	UDL	Yes
55	F1	No

3. After the Terminal Equipment has waited the appropriate number of clock edges (from the "TxOHFrame" signal being sampled "high"), it should assert the "TxOHIns" input signal. Concurrently, the Terminal Equipment should also place the appropriate value (of the inserted overhead bit) onto the "TxOH" signal.
4. The Terminal Equipment should hold both the "TxOHIns" input pin "high" and the value of the "TxOH" signal, stable until the next rising edge of "TxOHClk" is detected.

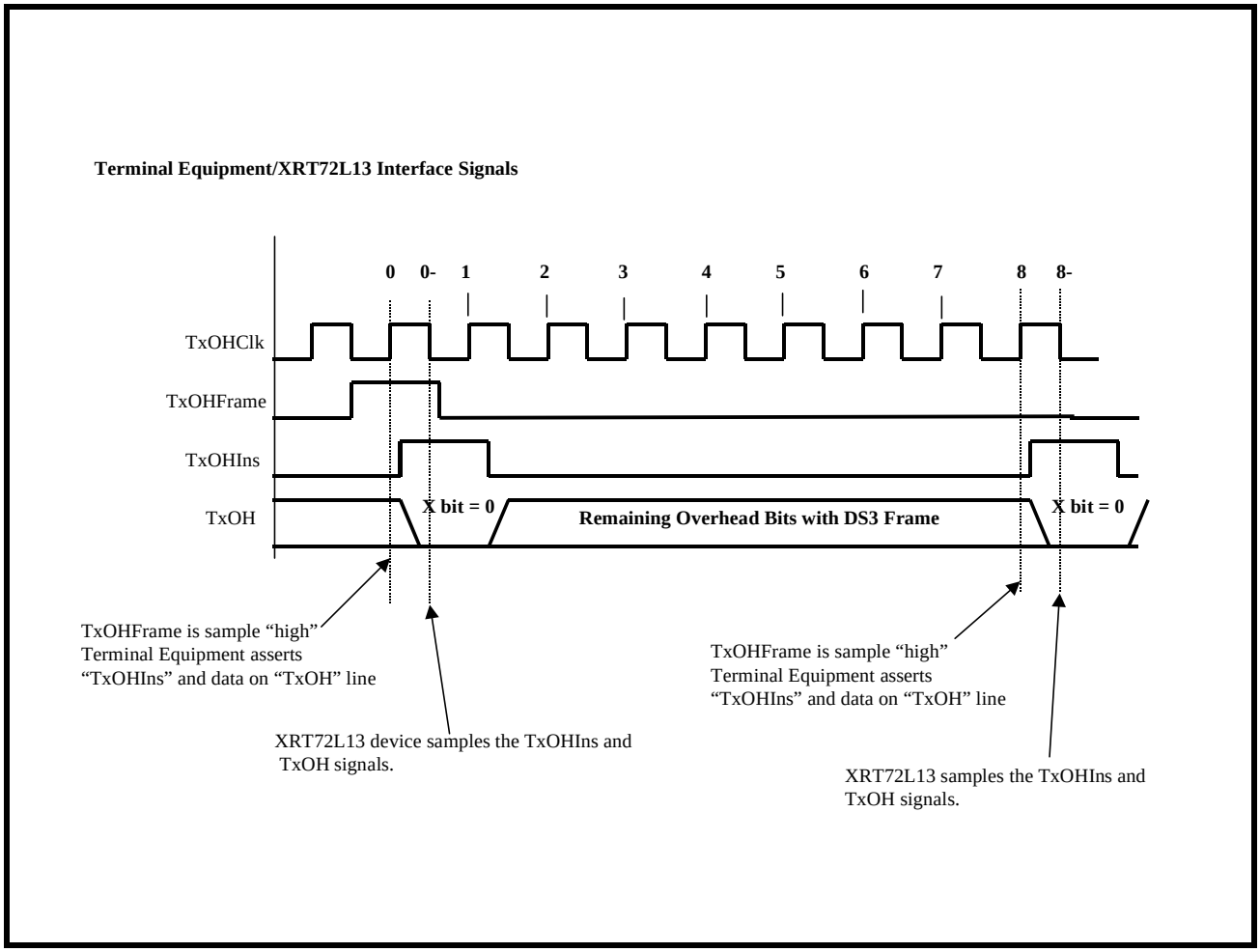
Case Study: The Terminal Equipment intends to insert the appropriate overhead bits into the "Transmit Overhead Data Input Interface" (using

Method 1) in order to transmit a "Yellow Alarm" to the remote terminal equipment.

In this example, the Terminal Equipment intends to insert the appropriate overhead bits, into the "Transmit Overhead Data Input Interface", such that the XRT72L13 will transmit a "Yellow Alarm" to the remote terminal equipment. Recall that, for DS3 Applications, a "Yellow Alarm" is transmitted by setting both of the "X" bits (within each “outbound” DS3 frame) to "0".

If one assumes that the connection between the Terminal Equipment and the XRT72L13 are as illustrated in Figure 76 then Figure 77 presents an illustration of the signaling that must go on between the Terminal Equipment and the XRT72L13.

FIGURE 77. ILLUSTRATION OF THE SIGNAL THAT MUST OCCUR BETWEEN THE TERMINAL EQUIPMENT AND THE XRT72L13, IN ORDER TO CONFIGURE THE XRT72L13 TO TRANSMIT A "YELLOW ALARM" TO THE "REMOTE TERMINAL EQUIPMENT"



In Figure 77 the Terminal Equipment samples the "TxOHFrame" signal being "high" at "rising clock edge # 0". At this point, the Terminal Equipment knows that the XRT72L13 is just about to process the very first overhead bit within a given "outbound" DS3 frame. Additionally, according to Table 15 , the very first overhead bit to be processed is the first "X" bit. In order to facilitate the transmission of the "Yellow Alarm", the Terminal Equipment must set this "X" bit to "0". Hence, the Terminal Equipments starts this data, it will then insert a "0" into the first "X" bit position, in the "outbound" DS3 frame.

process by implementing the following steps concurrently.

a. Assert the "TxOHIns" input pin by setting it "high".

b. Set the "TxOH" input pin to "0".

After the Terminal Equipment has applied these signals, the XRT72L13 will sample the data on both the "TxOHIns" and "TxOH" signals upon the very next falling edge of "TxOHClk" (designated at "0-" in Figure 77 . Once the XRT72L13 has sampled this

Upon detection of the very next rising edge of the "TxOHClk" clock signal (designated as "clock edge 1" in Figure 77), the Terminal Equipment will negate the "TxOHIns" signal (e.g., toggles it "low") and will cease inserting data into the "Transmit Overhead Data Input Interface", until "rising clock edge # 8" (of the "TxOHClk" signal). According to Table 15 , "rising clock edge # 8" indicates that the XRT72L13 is just about ready to process the second "X" bit within the "outbound" DS3 frame. Once again, in order to facilitate the transmission of the "Yellow Alarm" this "X-Bit" must also be set to "0". Hence, the Terminal Equipment will (once again) implement the following steps, concurrently.

a. Assert the "TxOHIns" input pin by setting it "high".

b. Set the "TxOH" input to "0".

Once again, after the Terminal Equipment has applied these signals these signals; the XRT72L13 will sample the data on both the "TxOHIns" and "TxOH" signal upon the very next falling edge of "TxOHClk" (designated as "8-" in Figure 77). Once the XRT72L13 has sampled this data, it will then insert a "0" into the second "X" bit position, in the "outbound" DS3 frame.

4.2.2.2 Method 2 - Using the TxInClk and TxOHEnable Signals

Method 1 requires the use of an additional clock signal, "TxOHClk". However, there may be a situation in which the user does not wish to accommodate and process this extra clock signal to their design, in order to use the "Transmit Overhead Data Input Interface". Hence, Method 2 is available. When using "Method 2", either the "TxInClk" or "RxOutClk" signal is used to sample the "overhead" bits and signals which are input to the "Transmit Overhead Data Input Interface. Method 2 involves the use of the following signals:

- TxOH
- TxInClk
- TxOHFrame
- TxOHEnable

Each of these signals are listed and described in Table 16 .

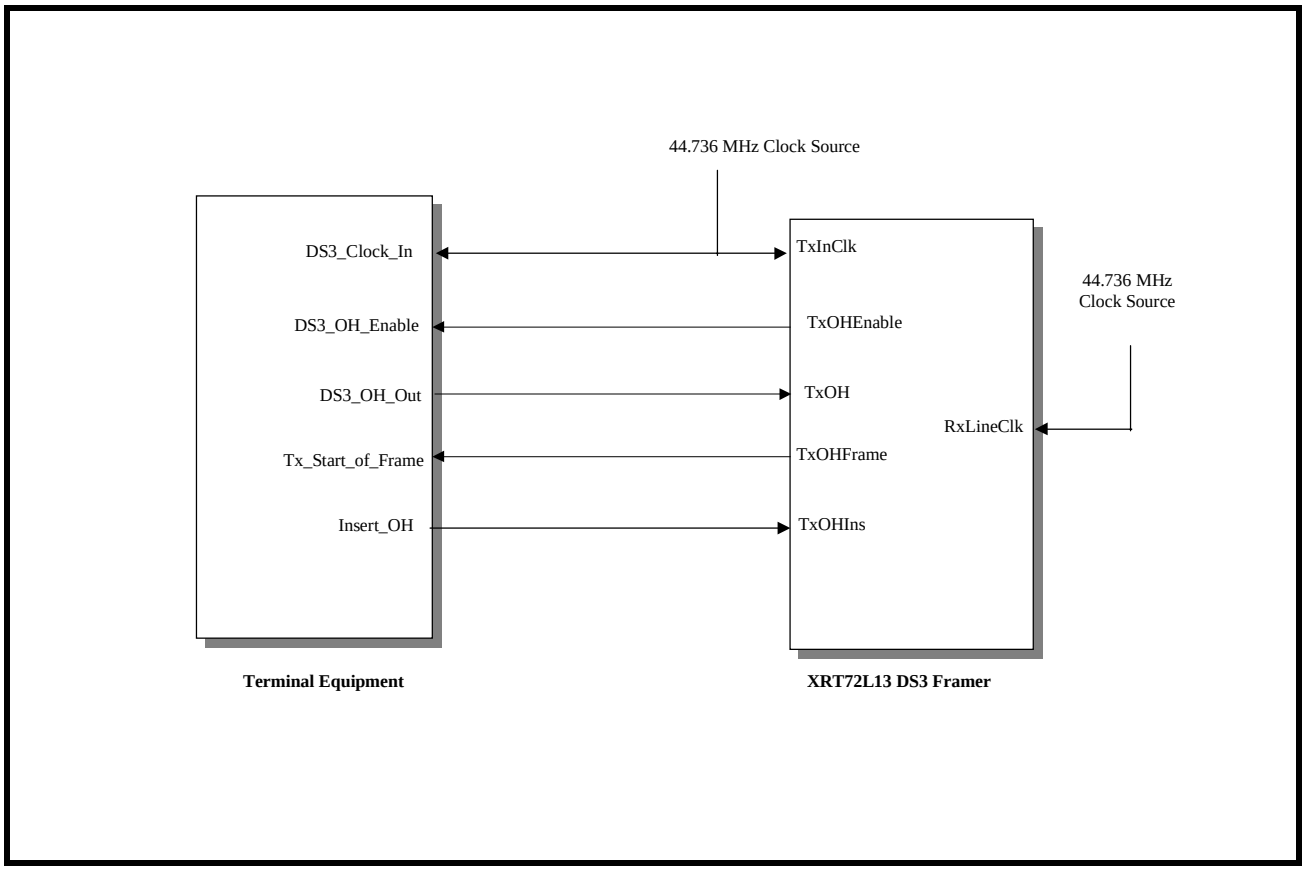
TABLE 16: DESCRIPTION OF "METHOD 2" TRANSMIT OVERHEAD INPUT INTERFACE SIGNALS

NAME	TYPE	DESCRIPTION
TxOHEnable	Output	**Transmit Overhead Data Enable Output pin** The XRT72L13 will assert this signal, for one TxInClk period, just prior to the instant that the "Transmit Overhead Data Input Interface" is processing an overhead bit.
TxOHFrame	Output	**Transmit Overhead Input Interface Frame Boundary Indicator Output:** This output signal pulses "high" when the XRT72L13 is processing the last bit within a given DS3 frame.
TxOHIns	Input	**Transmit Overhead Data Insert Enable input pin.** Asserting this input signal (e.g., setting it "high") enables the Transmit Overhead Data Input Interface to accept "overhead" data from the Terminal Equipment. In other words, while this input pin is "high", the Transmit Overhead Data Input Interface will sample the data at the "TxOH" input pin, on the falling edge of the "TxInClk" output signal. Conversely, setting this pin "low" configures the "Transmit Overhead Data Input Interface" to NOT sample (e.g., ignore) the data at the "TxOH" input pin, on the falling edge of the "TxOHClk" output signal. ***NOTE:*** *If the Terminal Equipment attempts to insert an overhead bit that cannot be accepted by the "Transmit Overhead Data Input Interface" (e.g., if the Terminal Equipment asserts the "TxOHIns" signal, at a time when one of these "non-insertable" overhead bits are being processed); that particular insertion effort will be ignored.*
TxOH	Input	**Transmit Overhead Data Input pin:** The Transmit Overhead Data Input Interface accepts the overhead data via this input pin, and inserts into the "overhead" bit position within the very next "outbound" DS3 frame. If the "TxOHIns" pin is pulled "high", the Transmit Overhead Data Input Interface will sample the data at this input pin (TxOH), on the falling edge of the "TxOHClk" output pin. Conversely, if the "TxOHIns" pin is pulled "low", then the Transmit Overhead Data Input Interface will NOT sample the data at this input pin (TxOH). Consequently, this data will be ignored.

Interfacing the "Transmit Overhead Data Input Interface to the Terminal Equipment

Figure 78 illustrates how one should interface the "Transmit Overhead Data Input Interface" to the Terminal Equipment when using Method 2.

FIGURE 78. ILLUSTRATION OF THE "TERMINAL EQUIPMENT" BEING INTERFACED TO THE "TRANSMIT OVERHEAD DATA INPUT INTERFACE" (METHOD 2)



Method 2 Operation of the Terminal Equipment

If the Terminal Equipment intends to insert any overhead data into the "outbound" DS3 data stream (via the Transmit Overhead Data Input Interface), then it is expected to do the following.

1. To sample the state of both the "TxOHFrame" and the "TxOHEnable" input signals, via the "DS3_Clock_In" (e.g., either the TxInClk or the RxOutClk signal of the XRT72L13) signal. If the Terminal Equipment samples the "TxOHEnable" signal "high"; then it knows that the XRT72L13 is about to process an overhead bit. Further, if the Terminal Equipment samples both the "TxOHFrame" and the "TxOHEnable" pins "high" (at the same time) then the Terminal Equipment knows that the XRT72L13 is about to process the first overhead bit, within a new DS3 frame.
2. To keep track of the number of times that the "TxOHEnable" signal has been sampled "high" since the last time both the "TxOHFrame" and the "TxOHEnable" signals were sampled "high". By doing this, the Terminal Equipment will be able to keep track of which overhead bit the "Transmit Overhead Data Input Interface" is about ready to process. From this, the Terminal Equipment will know when it should assert the "TxOHIns" input pin and place the appropriate value on the "TxOH" input pins (of the XRT72L13).

Table 17 also relates the number of "TxOHEnable" output pulses (that have occurred since both the "TxOHFrame" and "TxOHEnable" pins were sampled "high") to the DS3 overhead bit, that is being processed.

TABLE 17: THE RELATIONSHIP BETWEEN THE NUMBER OF "TXOHENABLE" PULSES (SINCE THE LAST OCCURRENCE OF THE "TXOHFRAME" PULSE) TO THE DS3 OVERHEAD BIT, THAT IS BEING PROCESSED BY THE XRT72L13

NUMBER OF "TXOHENABLE" PULSES	THE OVERHEAD BIT EXPECTED BY THE "XRT72L13"	CAN THIS OVERHEAD BIT BE ACCEPTED BY THE XRT72L13?
0 (The "TxOHEnable" and "TxOHFrame" signals are both sampled "High")	X	Yes
1	F1	No
2	AIC	Yes
3	F0	No
4	NA	Yes
5	F0	No
6	FEAC	Yes
7	F1	No
8	X	Yes
9	F1	No
10	UDL	Yes
11	F0	No
12	UDL	Yes
13	F0	No
14	UDL	Yes
15	F1	No
16	P	No
17	F1	No
18	CP	Yes
19	F0	No
20	CP	Yes
21	F0	No
22	CP	Yes
23	F1	No
24	P	No
25	F1	No
26	FEBE	Yes
27	F0	No
28	FEBE	Yes

TABLE 17: THE RELATIONSHIP BETWEEN THE NUMBER OF "TXOHENABLE" PULSES (SINCE THE LAST OCCURRENCE OF THE "TXOHFRAME" PULSE) TO THE DS3 OVERHEAD BIT, THAT IS BEING PROCESSED BY THE XRT72L13

NUMBER OF "TXOHENABLE" PULSES	THE OVERHEAD BIT EXPECTED BY THE "XRT72L13"	CAN THIS OVERHEAD BIT BE ACCEPTED BY THE XRT72L13?
29	F0	No
30	FEBE	Yes
31	F1	No
32	M0	No
33	F1	No
34	DL	Yes
35	F0	No
36	DL	Yes
37	F0	No
38	DL	Yes
39	F1	No
40	M1	No
41	F1	No
42	UDL	Yes
43	FO	No
44	UDL	Yes
45	FO	No
46	UDL	Yes
47	F1	No
48	M0	No
49	F1	No
50	UDL	Yes
51	F0	No
52	UDL	Yes
53	F0	No
54	UDL	Yes
55	F1	No

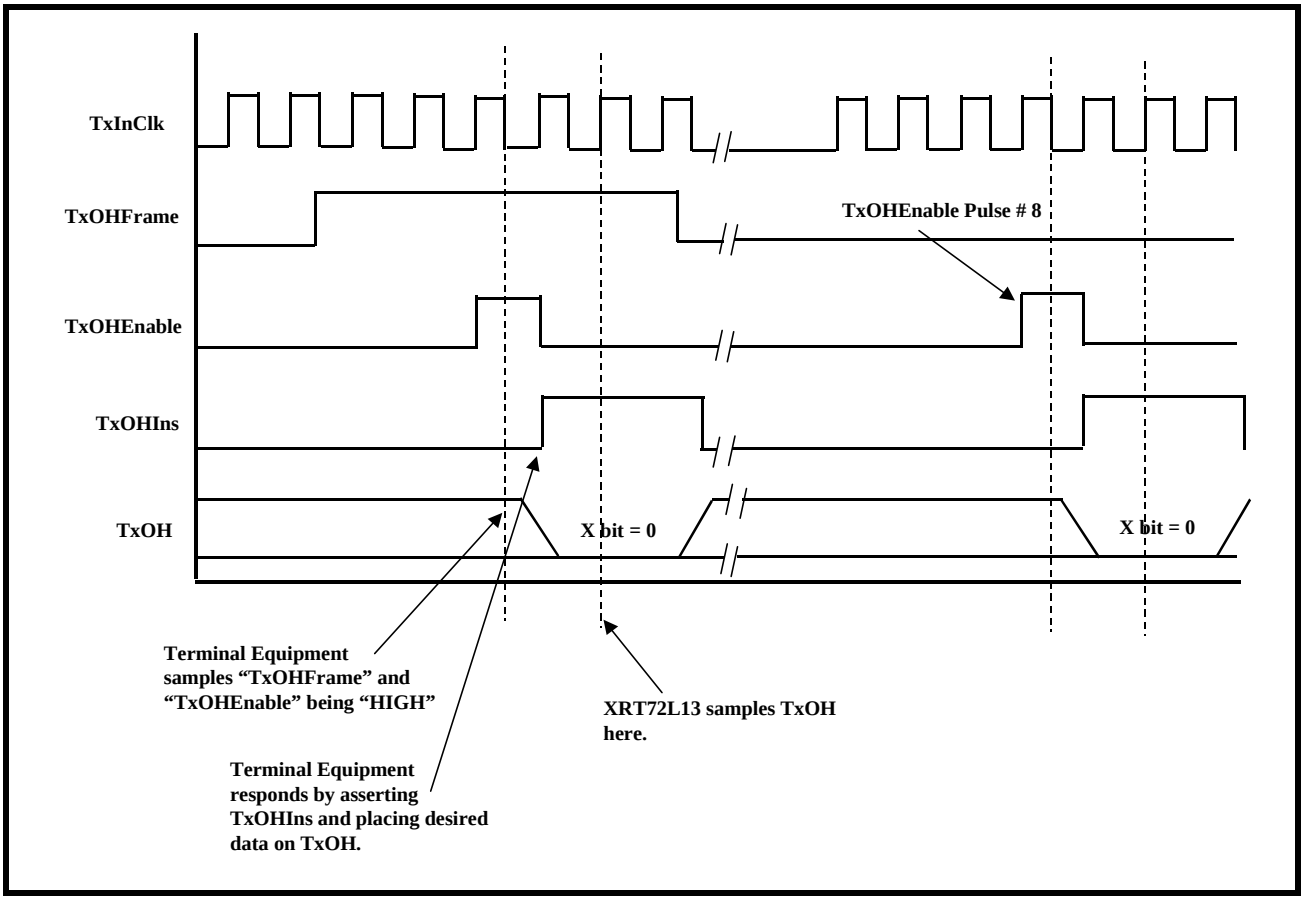
3. After the Terminal Equipment has waited through the appropriate number of pulses via the "TxOHEnable" pin, it should then assert the "TxOHIns" input signal. Concurrently, the Terminal Equipment should also place the appropriate value (of the inserted overhead bit) onto the "TxOH" signal.
4. The Terminal Equipment should hold both the "TxOHIns" input pin "high" and the value of the "TxOH" signal stable, until the next "TxOHEnable" pulse is detected.

Case Study: The Terminal Equipment intends to insert the appropriate overhead bits into the "Transmit Overhead Data Input Interface" (using Method 2) in order to transmit a "Yellow Alarm" to the remote terminal equipment.

In this case, the Terminal Equipment intends to insert the appropriate overhead bits, into the "Transmit Overhead Data Input Interface" such that the XRT72L13 will transmit a "Yellow Alarm" to the remote terminal equipment. Recall that, for DS3 applications, a "Yellow Alarm" is transmitted by setting all of the "X" bits to "0".

If one assumes that the connection between the Terminal Equipment and the XRT72L13s are as illustrated in Figure 78 then, Figure 79 presents an illustration of the signaling that must go on between the Terminal Equipment and the XRT72L13.

FIGURE 79. BEHAVIOR OF "TRANSMIT OVERHEAD DATA INPUT INTERFACE" SIGNALS BETWEEN THE XRT72L13 AND THE TERMINAL EQUIPMENT (FOR METHOD 2)



4.2.3 The Transmit DS3 HDLC Controller

The Transmit DS3 HDLC Controller block can be used to transport either "Bit-Oriented Signaling (BOS) or "Message-Oriented Signaling" (MOS) type messages or both types of messages to the remote terminal equipment. Both BOS and MOS types of HDLC message processing are discussed in detail below.

4.2.3.1 Bit-Oriented Signaling (or FEAC Message) processing via the "Transmit DS3 HDLC Controller".

The "Transmit DS3 HDLC Controller" block consists of two major blocks:

- The "Transmit FEAC Processor.
- The "LAPD Transmitter".

This section describes how to operate the "Transmit FEAC Processor". If the Transmit DS3 Framer is operating in the "C-bit Parity" Framing Format then the FEAC (Far-End Alarm & Control) bit-field of the DS3 Frame can be used to transmit the FEAC messages (See Figure 42). The FEAC code word is a 6-bit value which is encapsulated by 10 framing bits, forming a 16-bit FEAC message of the form:

0	d5	d4	d3	d2	d1	d0	0	1	1	1	1	1	1	1	1

where '[d5, d4, d3, d2, d1, d0]' is the FEAC code word. The rightmost bit (e.g., a "1") of the FEAC Message, is transmitted first. Since each DS3 frame contains only 1 FEAC bit, 16 DS3 Frames are required to transmit the 16 bit FEAC Code Message.

The XRT72L13 contains the following two registers that support FEAC Message Transmission.

- Tx DS3 FEAC Register (Address = 0x32)
- Tx DS3 FEAC Configuration and Status Register (Address = 0x33)

Operating the Transmit FEAC Processor

In order to transmit a FEAC message to the "remote terminal", the user must execute the following steps.

1. Write the 6-bit FEAC code (to be sent) into the "Tx DS3 FEAC" Register.
2. Enable the Transmit FEAC Processor.
3. Initiate the Transmission of the FEAC Message.

Each of these steps will be described in detail below.

STEP 1 - Writing in the six bit FEAC Codeword (to be sent)

In this step, the µP/µC writes the six bit FEAC code word into the "Tx DS3 FEAC" Register. The bit format of this register is presented below.

TX DS3 FEAC REGISTER (ADDRESS = 0X32)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Not Used	TxFEAC[5]	TxFEAC[4]	TxFEAC[3]	TxFEAC[2]	TxFEAC[1]	TxFEAC[0]	Not Used
RO	R/W	R/W	R/W	R/W	R/W	R/W	R0
0	d5	d4	d3	d2	d1	d0	0

STEP 2 - Enabling the Transmit FEAC Processor

In order to enable the Transmit FEAC Processor (within the Transmit DS3 HDLC Controller block) the user must write a "1" into bit 2 (Tx FEAC Enable) within the "Tx DS3 FEAC Configuration and Status" Register, as depicted below.

TRANSMIT DS3 FEAC CONFIGURATION AND STATUS REGISTER (ADDRESS = 0X31)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Not Used			TxFEAC Interrupt Enable	TxFEAC Interrupt Status	TxFEAC Enable	TxFEAC Go	TxFEAC Busy
RO	RO	RO	R/W	RO	R/W	R/W	R0
x	x	x	x	x	1	X	X

At this point, the "Transmit FEAC Processor" can be commanded to begin transmission (See STEP 3).

STEP 3 - Initiate the Transmission of the FEAC Message

The user can initiate the transmission of the FEAC code word (residing in the "Tx DS3 FEAC" register) by writing a "1" to bit 1 (Tx FEAC Go) within the "Tx DS3 FEAC Configuration and Status" register, as depicted below.

TRANSMIT DS3 FEAC CONFIGURATION AND STATUS REGISTER (ADDRESS = 0X31)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Not Used	Not Used	Not Used	TxFEAC Interrupt Enable	TxFEAC Interrupt Status	TxFEAC Enable	TxFEAC Go	TxFEAC Busy
RO	RO	RO	R/W	RO	R/W	R/W	R0
x	x	x	x	x	1	1	X

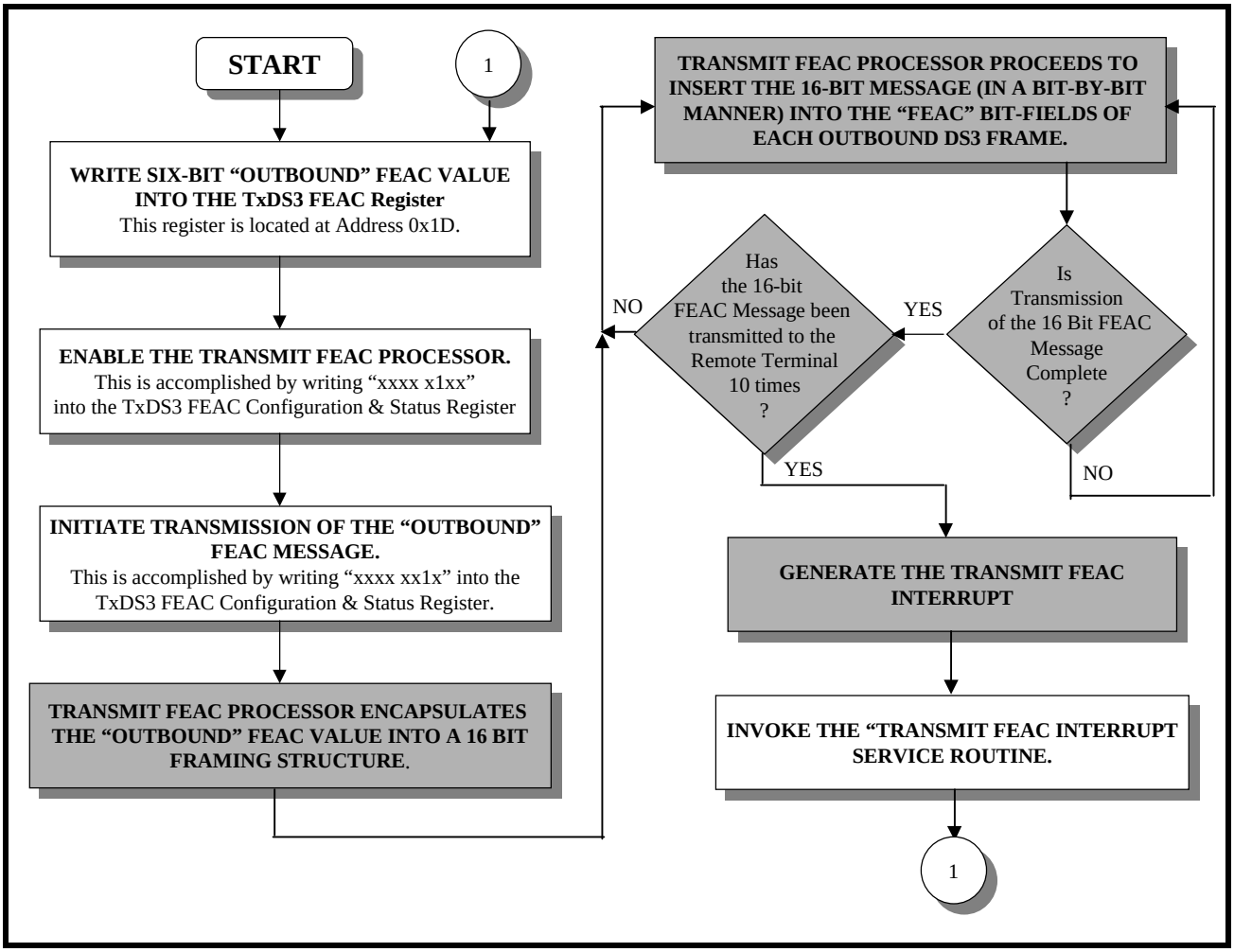
NOTE: *While executing this particular write operation, the user should write the binary value "000xx110b" into the "Tx DS3 FEAC Configuration and Status" Register. By doing this the user insures that a "1" is also being written to Bit 2*

(Tx FEAC Enable) of the register, in order to keep the "Transmit FEAC Processor" enabled.

Once this step has been completed, the Transmit FEAC Processor will proceed to transmit the 16 bit FEAC code via the outbound DS3 frames. This 16 bit FEAC message will be transmitted repeatedly 10 consecutive times. Hence, this process will require a total of 160 DS3 Frames. During this process the "Tx FEAC Busy" bit (Bit 0, within the "Transmit DS3 FEAC Configuration and Status" register) will be asserted, indicating that the Tx FEAC Processor is currently transmitting the FEAC Message to the "remote" Terminal. This bit-field will toggle to "0" upon completion of the 10th transmission of the FEAC Code Message. The Transmit FEAC Processor will generate an interrupt (if enabled) to the local µP/µC, upon completion of the 10th transmission of the FEAC Message. The purpose of having the Framer IC generating this interrupt is to let the local µP/µC know that the Transmit FEAC Processor is now available and ready to transmit a new FEAC message. Finally, once the Transmit FEAC Processor has completed its 10th transmission of a FEAC Code Message it will then begin sending all "1s" in the FEAC bit-field of each DS3 Frame. The Receive FEAC Processor (at the remote terminal equipment) will interpret this "all 1s" message as an "Idle" FEAC Message. The Transmit FEAC Processor will continue sending all "1"s in the FEAC bit field, for an indefinite period of time, until the local µP/µC commands it to transmit a new FEAC message.

Figure 80 presents a flow chart depicting how to use the Transmit FEAC Processor.

FIGURE 80. A FLOW CHART DEPICTING HOW TO TRANSMIT A FEAC MESSAGE VIA THE FEAC TRANSMITTER



For a detailed description of the Receive FEAC Processor (within the Receive DS3 HDLC Controller block), please see Section 3.3.3.1.

4.2.3.2 Message-Oriented Signaling (e.g., LAP-D) processing via the "Transmit DS3 HDLC Controller"

The LAPD Transmitter (within the Transmit DS3 HDLC Controller Block) allows the user to transmit path maintenance data link (PMDL) messages to the remote terminal via the "outbound" DS3 Frames. In this case the message bits are inserted into and carried by the 3 "DL" bit fields of F-Frame #5 within each DS3 M-frame. The on-chip LAPD transmitter supports both the 76 byte and 82 byte length message formats, and the Framer IC allocates 88 bytes of on-chip RAM (e.g., the "Transmit LAPD Message" buffer) to store the message to be transmitted. The message format complies with ITU-T Q.921 (LAP-D) protocol with different addresses and is presented below in Figure 81 .

FIGURE 81. LAPD MESSAGE FRAME FORMAT

Flag Sequence (8 bits)		
SAPI (6-bits)	C/R	EA
TEI (7 bits)		EA
Control (8-bits)		
76 or 82 Bytes of Information (Payload)		
FCS - MSB		
FCS - LSB		
Flag Sequence (8-bits)		

Where: Flag Sequence = 0x7E

SAPI + CR + EA = 0x3C or 0x3E

TEI + EA = 0x01

Control = 0x03

The following sections defines each of these bit/byte-fields within the LAPD Message Frame Format.

Flag Sequence Byte

The Flag Sequence byte is of the value 0x7E, and is used to for two purposes

1. To denote the boundaries of the LAPD Message Frame, and
2. To function as the “Idle Pattern” (e.g., Transmit HDLC Controller block transmits a continuous stream of flag sequence octets; whenever no LAPD Message is being transmitted).

SAPI - Service Access Point Identifier

The SAPI bit-fields are assigned the value of "001111b" or 15 (decimal).

TEI - Terminal Endpoint Identifier

The TEI bit-fields are assigned the value of 0x00. The TEI field is used in N-ISDN systems to identify a terminal out of multiple possible terminal. However, since the Framer IC transmits data in a point-to-point manner, the TEI value is unimportant.

Control

The Control identifies the type of frame being transmitted. There are three general types of frame formats: Information, Supervisory, and Unnumbered. The Framer assigned the Control byte the value 0x03. Hence, the Framer will be transmitting and receiving Unnumbered LAPD Message frames.

Information Payload

The "Information Payload" is the 76 bytes or 82 bytes of data (e.g., the PMDL Message) that the user has written into the on-chip "Transmit LAPD Message" buffer (which is located at addresses 0x86 through 0xDD).

It is important to note that the user must write in a specific octet value into the first byte position within the Transmit LAPD Message buffer (located at Address = 0x86, within the Framer). The value of this octet depends upon the type of LAPD Message frame/PMDL Message that the user wishes to transmit. Table 18 presents a list of the various types of LAPD Message frames/PMDL Messages that are supported by the XRT72L13 Framer device; and the corresponding octet value that the user must write into the first octet position within the "Transmit LAPD Message buffer.

TABLE 18: THE LAPD MESSAGE TYPE AND THE CORRESPONDING VALUE OF THE FIRST BYTE, WITHIN THE INFORMATION PAYLOAD

LAPD MESSAGE TYPE	VALUE OF FIRST BYTE, WITHIN INFORMATION PAYLOAD OF MESSAGE	MESSAGE SIZE
CL Path Identification	0x38	76 bytes
IDLE Signal Identification	0x34	76 bytes
Test Signal Identification	0x32	76 bytes
ITU-T Path Identification	0x3F	82 bytes

Frame Check Sequence Bytes

The 16 bit FCS (Frame Check Sequence) is calculated over the LAPD Message Header and Information Payload bytes, by using the CRC-16 polynomial, $x^{16} + x^{12} + x^5 + 1$.

Operation of the LAPD Transmitter

If the user wishes to transmit a message via the LAPD Transmitter, he/she must write the information portion (or the body) of the message into the Transmit LAPD Message Buffer, which is located at 0x86 through 0xDD in on-chip RAM via the Microprocessor Interface. Afterwards, the user must do three things:

1. Specify the length of LAPD message to be transmitted.
2. Enable the LAPD Transmitter.
3. Initiate the Transmission of the PMDL Message.

Each of these steps will be discussed in detail.

STEP 1 - Specifying the Length of the LAPD Message

The user can transmit one of two different sizes of LAPD Messages. He/she can accomplish this by writing the appropriate data to bit 1 within the "Tx DS3 LAPD Configuration" Register. The bit-format of this register is presented below.

TRANSMIT DS3 LAPD CONFIGURATION REGISTER (ADDRESS = 0X33)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Not Used				Auto Retransmit	Not Used	TxLAPD Msg Length	TxLAPD Enable
R/O	R/O	R/O	R/O	R/W	R/O	R/W	R/W
0	0	0	0	X	0	X	X

The relationship between the contents of bit-fields 1 and the LAPD Message size is given in Table 19 .

TABLE 19: RELATIONSHIP BETWEEN TXLAPD MSG LENGTH AND THE LAPD MESSAGE SIZE

TXLAPD MSG LENGTH	LAPD MESSAGE LENGTH
0	LAPD Message size is 76 bytes
1	LAPD Message size is 82 bytes

NOTE: *The Message Type selected must correspond with the contents of the first byte of the Information (Payload) portion, as presented in Table 18 .*

STEP 2 - Enabling the LAPD Transmitter

Prior to the transmission of any data via the LAPD Transmitter, the user must enable the LAPD Transmitter. He/she can accomplish this by writing a "1" to bit 0 of the Tx DS3 LAPD Configuration Register, as depicted below.

TRANSMIT DS3 LAPD CONFIGURATION REGISTER (ADDRESS = 0X33)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Not Used				Auto Retransmit	Not Used	TxLAPD Msg Length	TxLAPD Enable
R/O	R/O	R/O	R/O	R/W	R/O	R/W	R/W

TRANSMIT DS3 LAPD CONFIGURATION REGISTER (ADDRESS = 0X33)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
0	0	0	0	X	0	X	1

Bit 0 - TxLAPD Enable

This bit-field allow the user to enable or disable the LAPD Transmitter in accordance with Table 20 .

TABLE 20: RELATIONSHIP BETWEEN TXLAPD MSG LENGTH AND THE LAPD MESSAGE SIZE

TXLAPD ENABLE	RESULTING ACTION OF THE LAPD TRANSMITTER
0	The LAPD Transmitter is disabled and the DL bits, in the DS3 frame, are transmitted as all "1"s.
1	The LAPD Transmitter is enabled and is transmitting a continuous stream of Flag Sequence octets (0x7E).

Prior to executing step 2 (Enabling the LAPD Transmitter), the LAPD Transmitter will be disabled and the Transmit DS3 Framer block will be setting each of the "DL" bits (within the "outbound" DS3 data stream) to "1". After the user executes this step, the LAPD Transmitter will begin transmitting the "flag sequence" octet (0x7E) via the "DL" bits.

NOTE: *Upon power up or reset, the LAPD Transmitter is disabled. Therefore, the user must set this bit to "1" in order to enable the LAPD Transmitter.*

STEP 3 - Initiate the Transmission

At this point, the LAPD Transmitter is ready to begin transmission. The user has written the "information portion" of the PMDL message into the on-chip Transmit LAPD Message buffer. Further, the user has specified the type of LAPD message that he/she wishes to transmit, and has enabled the LAPD Transmitter. The only thing remaining to do is to initiate the transmission of this message. The user initiates this process by writing a "1" to Bit 3 of the Tx DS3 LAPD Status/Interrupt Register (TxDL Start). The bit format of this register is presented below.

TRANSMIT DS3 LAPD STATUS/INTERRUPT REGISTER (ADDRESS = 0X34)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Not Used				Tx DL Start	Tx DL Busy	TxLAPD Interrupt Enable	TxLAPD Interrupt Status
R/O	R/O	R/O	R/O	R/W	RO	R/W	RUR
0	0	0	0	1	X	X	X

A "0" to "1" transition of Bit 3 (TxDL Start) in this register, initiates the transmission of the data link message. While the LAPD transmitter is transmitting the message, the 'TxDL Busy' (bit 2) bit will be set to "1". This bit-field allows the user to "poll" the status of the LAPD Transmitter. Once the message transfer is completed, this bit-field will toggle back to '0'.

The user can configure the LAPD Transmitter to interrupt the µC/µP upon completion of transmission of the LAPD Message, by setting bit-field 1 (TxLAPD Interrupt Enable) of the "Tx DS3 LAPD Status/Interrupt" register to "1". The purpose of this interrupt is to let the local µC/µP know that the LAPD Transmitter is available and ready to transmit a new message. Bit 0 will reflect the interrupt status for the LAPD Transmitter.

NOTE: *This bit-field will be reset on reading this register.*

Details Associated with the Transmission of a PMDL Message

Once the user has invoked the "TxDL Start" command, the LAPD Transmitter will do the following.

- Generate the four octets of LAPD frame header (e.g., Flag Sequence, SAPI, TEI, Control, etc.) and insert it into the LAPD Message, prior to the user's information (see the LAPD Message Frame Format in Figure 81).

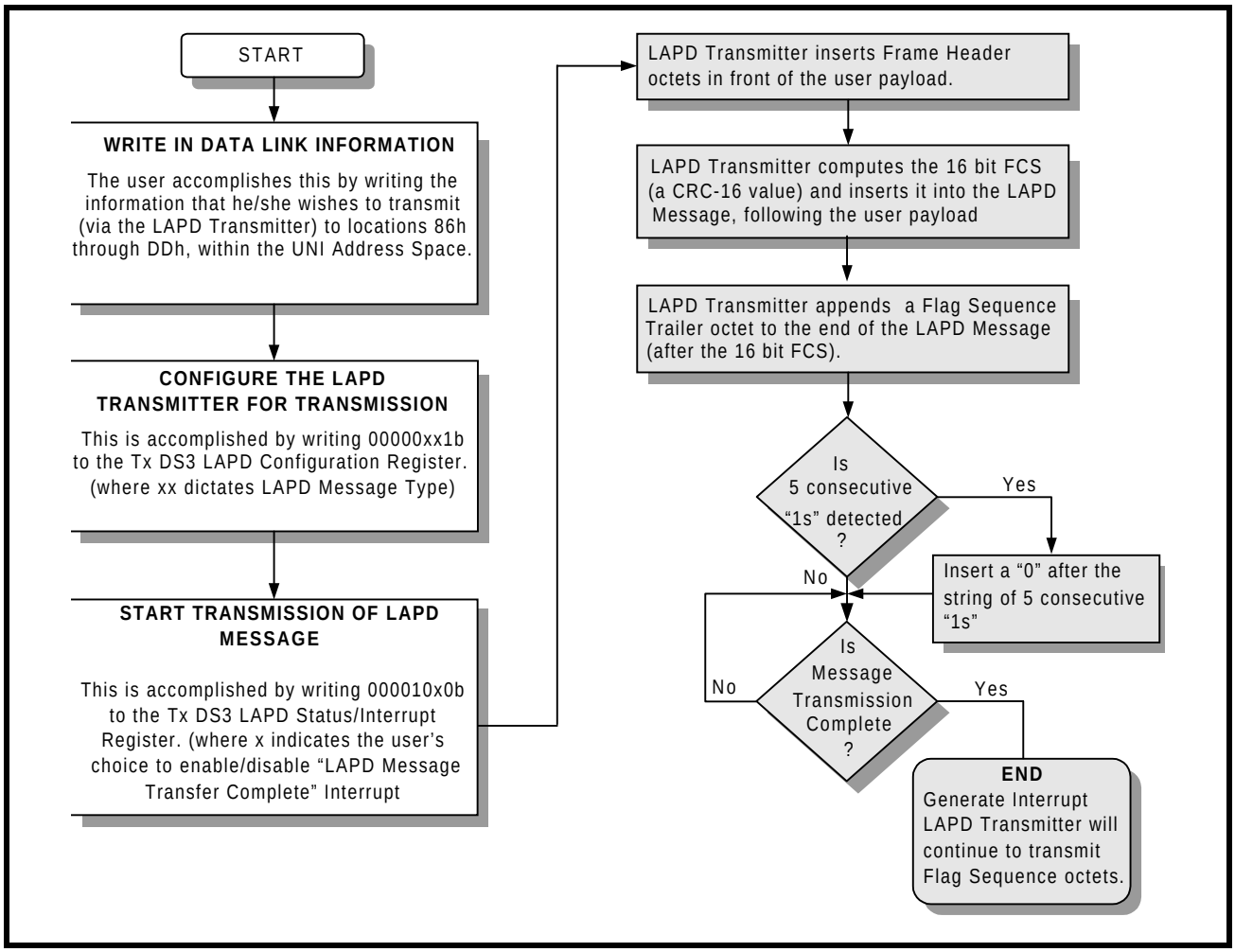
- Compute the 16 bit "Frame Check Sum" (FCS) of the LAPD Message Frame (e.g., of the LAPD Message header and information payload) and append this value to the LAPD Message.
- Append a "trailer" Flag Sequence octet to the end of the message LAPD (following the 16 bit FCS value).
- Serialize the composite LAPD message and begin inserting the LAPD message into the "DL" bit fields of each outgoing DS3 Frame.
- Complete the transmission of the frame overhead, payload, FCS value, and trailer Flag Sequence octet via the Transmit DS3 Framer.

Once the LAPD Transmitter has completed its transmission of the LAPD Message, the Framer will generate an interrupt to the local µC/µP (if enabled). Afterwards, the LAPD Transmitter will proceed to retransmit the LAPD Message, repeatedly at one second intervals. During "Idle" periods (e.g., in between these transmission of the LAPD Message), the LAPD Transmitter will be sending a continuous stream of "Flag Sequence Bytes". The LAPD Transmitter will continue this behavior until the user has disabled the LAPD Transmitter by writing a "0" to bit 0 (TxLAPD Enable) within the Tx DS3 LAPD Configuration Register. If the LAPD Transmitter is idle, then it will continuously send the Flag Sequence octets (via the "DL" bits of each outbound DS3 Frame) to the remote terminal equipment.

NOTE: *In order to prevent the user's data (e.g., the payload portion of the LAPD Message Frame) from mimicking the "Flag Sequence" byte, the LAPD Transmitter will insert a "0" into the LAPD data stream immediately following the detection of five (5) consecutive "1s" (this "stuffing" occurs only while the information payload is being transmitted). The 'remote' LAPD Receiver (see Section 4.3.3.2) will have the responsibility of "detecting the 5 consecutive "1s" and removing the subsequent "0" from the payload portion of the incoming LAPD message.*

Figure 82 presents a flow chart depicting the procedure (in 'white boxes') that the user should use in order to transmit a LAPD message. This figure also indicates (via the "shaded" boxes) what the LAPD Transmitter circuitry will do before and during message transmission.

FIGURE 82. FLOW CHART DEPICT HOW TO USE THE LAPD TRANSMITTER



The Mechanics of Transmitting a New LAPD Message

As mentioned above, after the LAPD Transmitter has been enabled, and commanded to transmit the message, residing in the "Transmit LAPD Message" buffer; it will continue to transmit this message at one-second intervals. If the user wishes to transmit another (e.g., different) PMDL message to the "Remote" LAPD Receiver, he/she will have to write this "new" message into the "Transmit LAPD Message" buffer, via the Microprocessor Interface section of the Framer. However, the user must be careful when writing in this new message. If he/she writes this message into the "Transmit LAPD Message" buffer at the "wrong time" (with respect to these "one-second" transmissions), the user's action could interfere with these transmissions; thereby causing the LAPD Transmitter to transmit a "corrupted" message to the "Remote" LAPD Receiver. In order to avoid this problem, while writing the new message into the "Transmit LAPD Message" buffer, the user should do the following:

1. Configure the Framer to automatically reset activated interrupts

The user can do this by writing a "1" into Bit 3 of the Framer Operating Mode Register, as depicted below.

OPERATING MODE REGISTER (ADDRESS = 0X00)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Local Loop-back Mode	Line Loop-back Mode	Internal LOS Enable	RESET	Interrupt Enable Reset	Frame Format	TimRefSel[1:0]	

OPERATING MODE REGISTER (ADDRESS = 0X00)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	1	1	0	1	X	X	X

This action will prevent the LAPD Transmitter from generating its own "one-second" interrupts.

This can be done by writing a "1" into Bit 0 of the Block Interrupt Enable Register, as depicted below.

2. Enable the "One-Second" Interrupt

BLOCK INTERRUPT ENABLE REGISTER (ADDRESS = 0X04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
RxDS3/E3 Interrupt Enable	Not Used		M13 Interrupt Status	Not Used		TxDS3/E3 Interrupt Enable	One Second Interrupt Enable
R/W	RO	RO	RO	RO	RO	R/W	R/W
0	0	0	0	0	0	0	X

3. Write the new message into the "Transmit LAPD Message" buffer immediately after the occurrence of the "One-Second" interrupt.

By timing the writes to the "Transmit LAPD Message" buffer to occur immediately after the occurrence of the "One-Second" interrupt, the user avoids conflicting with the "one-second" transmissions of the LAPD Message, and will transmit the correct messages to the "remote" LAPD Receiver.

4.2.4 The Transmit DS3 Framer Block

4.2.4.1 Brief Description of the Transmit DS3 Framer

The Transmit DS3 Framer block accepts data from any of the following three sources, and uses it to form the DS3 data stream.

- The Transmit Payload Data Input block
- The Transmit Overhead Data Input block
- The Transmit HDLC Controller block
- The Internal Overhead Data Generator

The manner in how the Transmit DS3 Framer block handles data from each of these sources is described below.

Handling of data from the "Transmit Payload Data Input Interface

For DS3 applications, all data that is input to the "Transmit Payload Data Input" Interface will be inserted into the payload bit positions within the "outbound" DS3 frames.

Handling of data from the "Internal Overhead Bit" Generator

By default, the Transmit DS3 Framer block will internally generate the overhead bits. However, if the Terminal Equipment inserts its own values for the overhead bits (via the "Transmit Overhead Data Input Interface); or if the user enables and employs the "Transmit DS3 HDLC Controller" block, then these "internally generated" overhead bits will be overwritten.

Handling of data from the "Transmit Overhead Data Input Interface

For DS3 applications, the Transmit DS3 Framer block automatically generates and inserts the framing alignment bits (e.g., the "F" and "M" bits) into the "outbound" DS3 frames. Further, the Transmit DS3 Framer block will automatically compute and insert the P-bits into the "outbound" DS3 frames. Hence, the Transmit DS3 Framer block will not accept data from the "Transmit OH Data Input Interface" block for the "F", "M" and "P" bits.

However, the Transmit DS3 Framer block will accept (and insert) data from the "Transmit Overhead Data Input" Interface for the following bit-fields.

- X-bits
- FEBE bits
- FEAC bits
- DL bits
- UDL bits
- CP bits

If the user's local "Data Link" Equipment activates the "Transmit Overhead Data Input Interface" block and writes data into this interface for these bits, then the

Transmit DS3 Framer block will insert this data into the appropriate overhead bit-fields, within the "outbound" DS3 frames.

Handling of Data from the Transmit HDLC Controller block

The exact manner in how the Transmit DS3 Framer handles data from the "Transmit HDLC Controller" block depends upon whether the "Transmit HDLC Controller" is transmitting "BOS" (Bit Oriented Signaling) or "MOS" (Message Oriented Signaling) data.

If the Transmit DS3 HDLC Controller block is not activated, then the “Transmit DS3 Framer” block will insert a “1” into each “FEAC” and “DL” bit-field, within each outbound DS3 frame.

If the “Transmit DS3 HDLC Controller” block is activated, and is configured to transmit either a “BOS” or “MOS” type message; then data will be inserted into the “FEAC” and “DL” bit-fields as described in Section 3.2.3.

4.2.4.2 Detailed Functional Description of the Transmit DS3 Framer Block

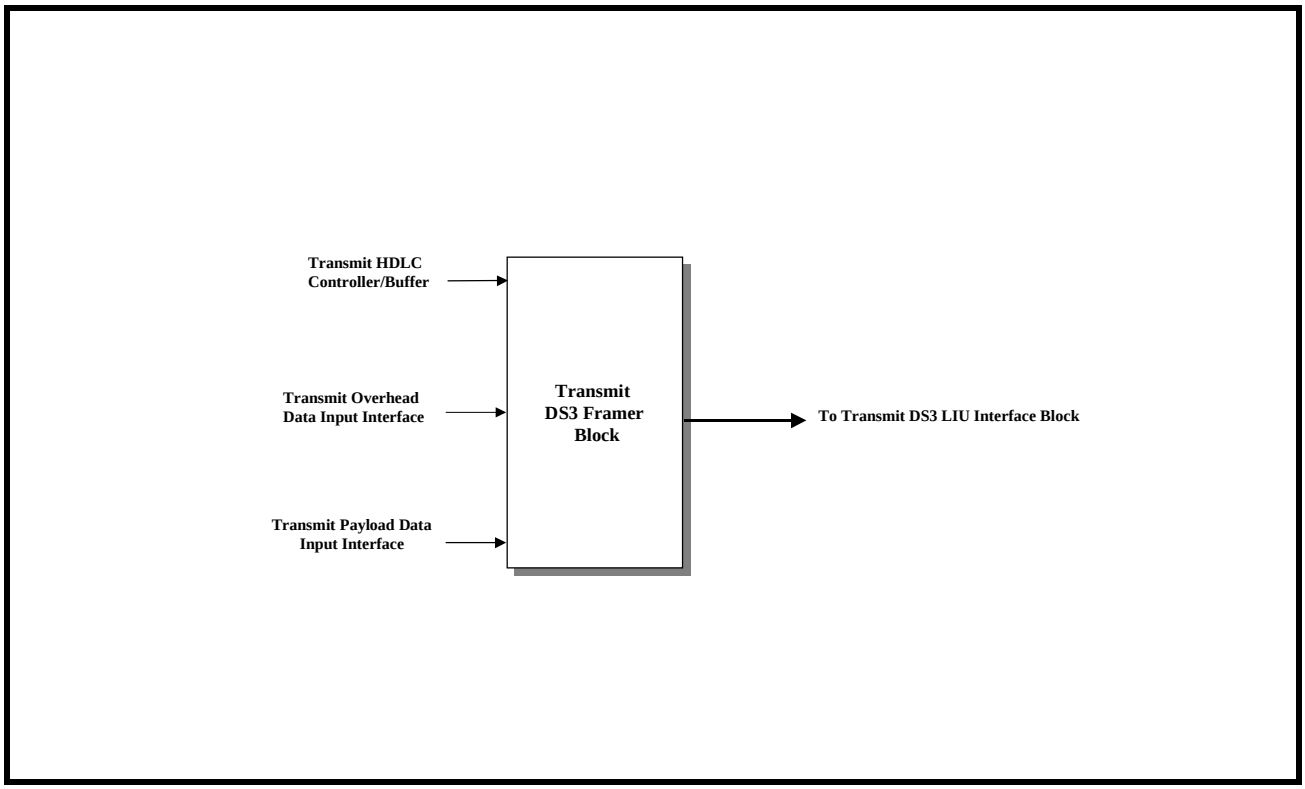
The Transmit DS3 Framer receives data from the following three sources and combines them together to form a DS3 data stream.

- The Transmit Payload Data Input Interface block.
- The Transmit Overhead Data Input Interface block
- The Transmit HDLC Controller block.

Afterwards, this DS3 data stream will be routed to the "Transmit DS3 LIU Interface" block, for further processing.

Figure 83 presents a simple illustration of the Transmit DS3 Framer block, along with the associated paths to the other functional blocks within the chip.

FIGURE 83. A SIMPLE ILLUSTRATION OF THE TRANSMIT DS3 FRAMER BLOCK AND THE ASSOCIATED PATHS TO OTHER FUNCTIONAL BLOCKS



In addition to taking data from multiple sources and multiplexing them, in appropriate manner, to create the "outbound" DS3 frames, the Transmit DS3 Framer block has the following roles.

- Generating Alarm Conditions
- Generating Errored Frames (for testing purposes)
- Routing "outbound" DS3 frames to the "Transmit DS3 LIU Interface" block

Each of these additional roles are discussed below.

4.2.4.2.1 Generating Alarm Conditions

The Transmit DS3 Framer block permits the user to, by writing the appropriate data into the on-chip registers, to override the data that is being written into the

"Transmit Payload Data" and "Overhead Data Input Interfaces" and transmit the following alarm conditions.

- Generate the Yellow Alarms (or "FERF" indicators)
- Manipulate the X-bit (set them to "1")
- Generate the AIS Pattern
- Generate the IDLE pattern
- Generate the LOS pattern
- Generate FERF (Yellow) Alarms, in response to detection of a "Red Alarm" condition (via the Receive Section of the XRT72L13).
- Generate and transmit a desired value for FEBE (Far-End-Block Error).

The procedure and results of generating any of these alarm conditions is presented below.

The user can exercise each of these options by writing the appropriate data to the Tx DS3 Configuration Register (Address = 0x30). The bit format of this register is presented below.

TX DS3 CONFIGURATION REGISTER (ADDRESS = 0X30)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Tx Yellow Alarm	Tx X-Bit	Tx IDLE Pattern	Tx AIS Pattern	Tx LOS Pattern	FERF on LOS	FERF on OOF	FERF on AIS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	1	0	1	0	1	1

The role/function of each of these bit-fields within the register, are discussed below.

4.2.4.2.1.1 Transmit Yellow Alarm - Bit 7

This "read/write" bit field permits the user to force the transmission of a "Yellow Alarm" to the "remote terminal equipment" via software control. If the user opts to transmit a "Yellow Alarm" then both of the X-bits, within the "outbound" DS3 frames will be set to '0'. Table 21 relates the content of this bit field to the Transmit DS3 Framer block's action.

TABLE 21: THE RELATIONSHIP BETWEEN THE CONTENTS OF BIT 7 (TX YELLOW ALARM) WITHIN THE TX DS3 CONFIGURATION REGISTER, AND THE RESULTING TRANSMIT DS3 FRAMER BLOCK'S ACTION

BIT 7	TRANSMIT DS3 FRAMER'S ACTION
0	**Normal Operation:** The X-bits are generated by the Transmit DS3 Framer block based upon "Near End" Receiving Conditions" (as detected by the Receive Section of the chip)
1	**Transmit Yellow Alarm:** The Transmit DS3 Framer block will overwrite the X-bits by setting them all to "0". The payload information is not modified and is transmitted as normal.

NOTE: *This bit is ignored when either the "TxIDLE", "TxAIS", or the "TxLOS" bit-fields are set.*

4.2.4.2.1.2 Transmit X-bit - Bit 6

This bit field functions as the logical complement to Bit 7 (e.g., "Tx Yellow Alarm). This "read/write" bit field permits the user to force all of the X-bits, in the "outbound" DS3 frames, to "1" and transmit them to the "remote terminal equipment". Table 22 relates the content of this bit field to the Transmit DS3 Framer Block's action.

TABLE 22: THE RELATIONSHIP BETWEEN THE CONTENTS OF BIT 6 (TX X-BITS) WITHIN THE TX DS3 CONFIGURATION REGISTER, AND THE RESULTING TRANSMIT DS3 FRAMER BLOCK'S ACTION

BIT 6	TRANSMIT DS3 FRAMER'S ACTION
0	**Normal Operation:** The X-bits are generated by the Transmit DS3 Framer block based upon "Receiving Conditions" (as detected by the Receive Section of the Framer chip).
1	**Set X-bits to "1":** The Transmit DS3 Framer will overwrite the X-bits by setting them to "1". Payload information is not modified and is transmitted as normal.

NOTE: *This bit is ignored when either the Transmit Yellow Alarm, Tx AIS, Tx IDLE, or TxLOS bit is set.*

4.2.4.2.1.3 Transmit Idle Pattern - Bit 5

This "read/write" bit field permits the user to transmit an "Idle pattern" to the "remote terminal equipment" upon software control. Table 23 relates the contents of this bit field to the Transmit DS3 Framer's action.

TABLE 23: THE RELATIONSHIP BETWEEN THE CONTENTS OF BIT 5 (TX IDLE) WITHIN THE TX DS3 CONFIGURATION REGISTER, AND THE RESULTING TRANSMIT DS3 FRAMER ACTION

BIT 5	TRANSMIT DS3 FRAMER'S ACTION
0	**Normal Operation:** The Overhead bits are either internally generated, or they are inserted via the "Transmit Overhead Data Input Interface" or the "Transmit HDLC Controller" blocks. The Payload bits are received from the "Transmit Payload Data Input Interface".
1	**Transmit Idle Condition Pattern:** When this command is invoked, the Transmit DS3 Framer will do the following: • Set the X-bits to "1" • Set the CP-Bits (F-Frame #3) to "0" • Generate Valid M, F, and P bits Overwrite the data in the DS3 payload with a repeating "1100..." pattern.

NOTE: *This bit is ignored when either the "Tx AIS" or the "Tx LOS" bit is set.*

4.2.4.2.1.4 Transmit AIS Pattern - Bit 4

This "read/write" bit field allows the user to transmit an AIS pattern to the "remote terminal equipment", upon software control. Table 24 relates the contents of this bit field to the Transmit DS3 Framer block's action.

TABLE 24: THE RELATIONSHIP BETWEEN THE CONTENTS OF BIT 4 (TX AIS PATTERN) WITHIN THE TX DS3 CONFIGURATION REGISTER, AND THE RESULTING TRANSMIT DS3 FRAMER BLOCK'S ACTION

BIT 4	TRANSMIT DS3 FRAMER'S ACTION
0	**Normal Operation:** The Overhead bits are either internally generated, or they are inserted via the "Transmit Overhead Data Input Interface" or the "Transmit HDLC Controller" blocks. The Payload bits are received from the "Transmit Payload Data Input Interface".
1	**Transmit AIS Pattern:** When this command is invoked, the Transmit DS3 Framer block will do the following. • Set the X-bits to "1" • Set all the C-bits to "0" • Generate valid M, F, and P bits Overwrite the data in the DS3 payload with a repeating "1010..." pattern

NOTE: This bit is ignored when the TxLOS bit is set.

4.2.4.2.1.5 Transmit LOS Pattern - Bit 3

This "read/write" bit field allows the user to transmit an LOS (Loss of Signal) pattern to the "remote terminal", upon software control. Table 25 relates the contents of this bit field to the Transmit DS3 Framer block's action.

TABLE 25: THE RELATIONSHIP BETWEEN THE CONTENTS OF BIT 3 (TX LOS) WITHIN THE TX DS3 CONFIGURATION REGISTER, AND THE RESULTING TRANSMIT DS3 FRAMER BLOCK'S ACTION

BIT 3	TRANSMIT DS3 FRAMER'S ACTION
0	**Normal Operation:** The Overhead bits are either internally generated, or they are inserted via the "Transmit Overhead Data Input Interface" or the "Transmit HDLC Controller" blocks. The Payload bits are received from the "Transmit Payload Data Input Interface".
1	**Transmit LOS Pattern:** When this command is invoked the Transmit DS3 Framer will do the following. • Set all of the overhead bits to "0" (including the M, F, and P bits) Overwrite the DS3 payload bits with an "all zeros" pattern.

NOTE: When this bit is set, it overrides all of the other bits in this register.

4.2.4.2.1.6 FERF (Far-End Receive Failure) on LOS - Bit 2

This "Read/Write" bit-field allows the user to configure the Transmit DS3 Framer block to automatically generate a "Yellow Alarm" if the Near-End Receive Section (of the XRT72L13) detects a "LOS" (Loss of Signal) Condition.

Writing a "1" to this bit-field enables this feature. Writing a "0" to this bit-field disables this feature.

4.2.4.2.1.7 FERF (Far-End Receive Failure) on OOF - Bit 1

This "Read/Write" bit-field allows the user to configure the Transmit DS3 Framer block to automatically generate a "Yellow Alarm" if the Near-End Receive Section (of the XRT72L13) detects an "OOF (Out-of-Frame) Condition".

Writing a "1" to this bit-field enables this feature. Writing a "0" to this bit-field disables this feature.

4.2.4.2.1.8 FERF (Far-End Receive Failure) on AIS - Bit 0

This "Read/Write" bit-field allows the user to configure the Transmit DS3 Framer block to automatically generate a "Yellow Alarm" if the Near-End Receive Section (of the XRT72L13) detects an AIS (Alarm Indication Signal) pattern.

Writing a "1" to this bit-field enables this feature. Writing a "0" to this bit-field disables this feature.

4.2.4.2.1.9 Transmitting FEBE (Far-End Block Error) Values

By default, the Transmit DS3 Framer block will set the three (3) FEBE bit-fields to [1, 1, 1] if all of the following conditions are true.

- The “Local” Receive DS3 Framer block detects no P-Bit Errors.
- The “Local” Receive DS3 Framer block detects no CP-Bit Errors

Conversely, the Transmit DS3 Framer block will set the three (3) FEBE bit-fields to a value other than [1, 1, 1] if any one of the following conditions are true.

- The “Local” Receive DS3 Framer block detects a P-bit Error in the most recently received DS3 frame.
- The “Local” Receive DS3 Framer block detects a “CP” bit Error in the most recently received DS3 frame.

4.2.4.2.2 Generating Errored DS3 Frames

The Transmit DS3 Framer block permits the user to insert errors into the framing and error detection overhead bits (e.g., the P, M and F-bits) of the "outbound" DS3 data stream in order to support "Far-End" Equipment testing. The user can exercise this option by writing data to any of the numerous Transmit DS3 Mask Registers. These "Mask Registers" and their comprising bit-fields are defined below.

TX DS3 M-BIT MASK REGISTER, ADDRESS = 0X35

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
TxFEBE DAT[2]	TxFEBE DAT[1]	TxFEBE DAT[0]	FEBE Reg Enable	TxErr PBit	MBit Mask(2)	MBit Mask(1)	MBit Mask(0)
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
X	X	X	X	X	X	X	X

The bit-fields of the Tx DS3 M-bit Mask Register, that are relevant to error-insertion are shaded. The remaining bit-fields pertain to the FEBE bit-fields, and are discussed in Section 4.2.4.2.1.9.

The Tx DS3 M-Bit Mask Register serves two purposes

1. It allows the user to transmit his/her own value for FEBE (3 bits) - please see Section 4.2.4.2.1.9.
2. It allows the user to transmit errored P-bits.
3. It allows the user to insert errors into the M-bit (framing bits) in order to support equipment testing.

Each of these bit-fields are discussed below.

Bit 3 - Tx Err (Transmit Errored) P-Bit

This bit-field allows the user to insert errors into the P-bits, of each outbound DS3 Frame, for equipment testing purposes. If this bit-field is "0", then the P-Bits are transmitted as calculated from the payload of the previous DS3 frames. However, if this bit-field is "1", then the P-bits are inverted (from their calculated value) prior to transmission.

Bits 2 - 0: M-Bit Mask[2:0]

The Transmit DS3 Framer will automatically perform an XOR operation with the M-bits (in the DS3 datastream) and the contents of the corresponding bit-field, within this register. The results of this operation will be written back into the M-bit positions within the "outbound" DS3 Frames. Therefore, if the user does not wish to insert errors into the M-bits, he/she must make sure that the contents of these bit-fields: M-Bit Mask[2:0] are "0".

F-Bit Error Insertion

The remaining mask registers (Tx DS3 F-Bit Mask1 through Mask4 registers) contain bit-fields which correspond to each of the 28 F-bits, within the DS3 frame. Prior to transmission, these bit-fields are automatically XORed with the contents of the corresponding bit fields within these Mask Registers. The result of this XOR operation is written back into the corresponding bit-field, within the outgoing DS3 frame, and is transmitted on the line. Therefore, if the user does not wish to modify any of these bits, then he/she must insure that these registers contain all "0s" (the default value).

TX DS3 F-BIT MASK1 REGISTER, ADDRESS = 0X36

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Unused	Unused	Unused	Unused	FBit Mask(27)	FBit Mask(26)	FBit Mask(25)	FBit Mask(24)
RO	RO	RO	RO	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

TX DS3 F-BIT MASK2 REGISTER, ADDRESS = 0X37

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
FBit Mask(23)	FBit Mask(22)	FBit Mask(21)	FBit Mask(20)	FBit Mask(19)	FBit Mask(18)	FBit Mask(17)	FBit Mask(16)
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

TX DS3 F-BIT MASK3 REGISTER, ADDRESS = 0X38

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
FBit Mask(15)	FBit Mask(14)	FBit Mask(13)	FBit Mask(12)	FBit Mask(11)	FBit Mask(10)	FBit Mask(9)	FBit Mask(8)
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

TX DS3 F-BIT MASK4 REGISTER, ADDRESS = 0X39

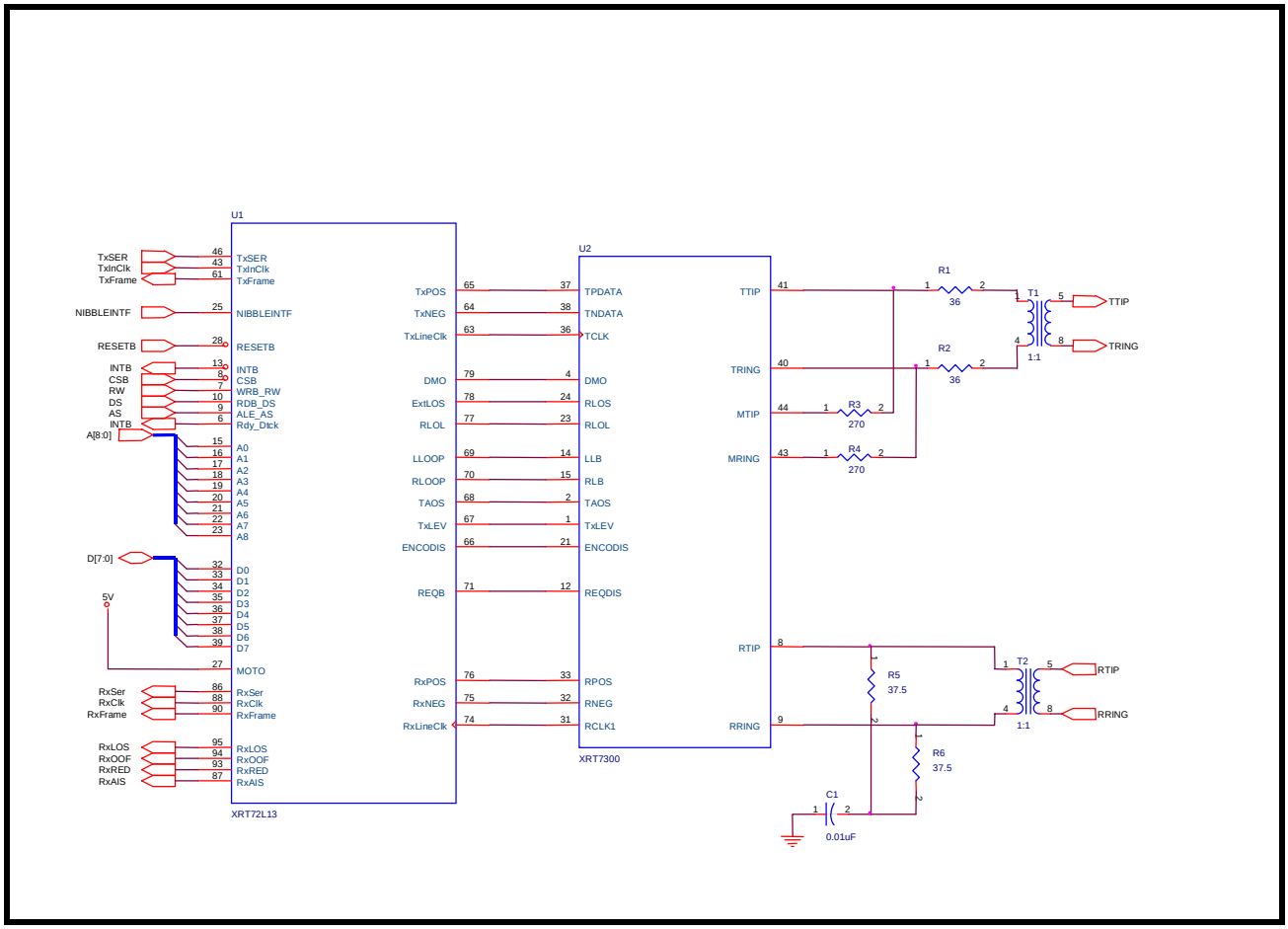
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
FBit Mask(7)	FBit Mask(6)	FBit Mask(5)	FBit Mask(4)	FBit Mask(3)	FBit Mask(2)	FBit Mask(1)	FBit Mask(0)
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

4.2.5 The Transmit DS3 Line Interface Block

The XRT72L13 Framer IC is a digital device that takes DS3 payload and overhead bit information from some terminal equipment, processes this data and ultimately, multiplexes this information into a series of "outbound" DS3 frames. However, for DS3 coaxial cable applications, the XRT72L13 Framer IC lacks the current drive capability to be able to directly transmit this DS3 data stream through some transformer-coupled coax cable with enough signal strength for it to comply with the Isolated Pulse Template requirements and be received by the remote receiver.

Therefore, in order to get around this problem, the Framer IC requires the use of an LIU (Line Interface Unit) IC. An LIU is a device that has sufficient drive capability, along with the necessary pulse-shaping circuitry to be able to transmit a signal through the transmission medium in a manner that it can (1) comply with the DSX-3 Isolated Pulse Template requirements and (2) be reliably received by the Remote Terminal Equipment. Figure 84 presents a circuit drawing depicting the Framer IC interfacing to an LIU (XRT7300 DS3/E3/STS-1 Transmit LIU).

FIGURE 84. APPROACH TO INTERFACING THE XRT72L13 FRAMER IC DEVICE TO THE XRT7300 DS3/E3/STS-1 TRANSMITTER LIU

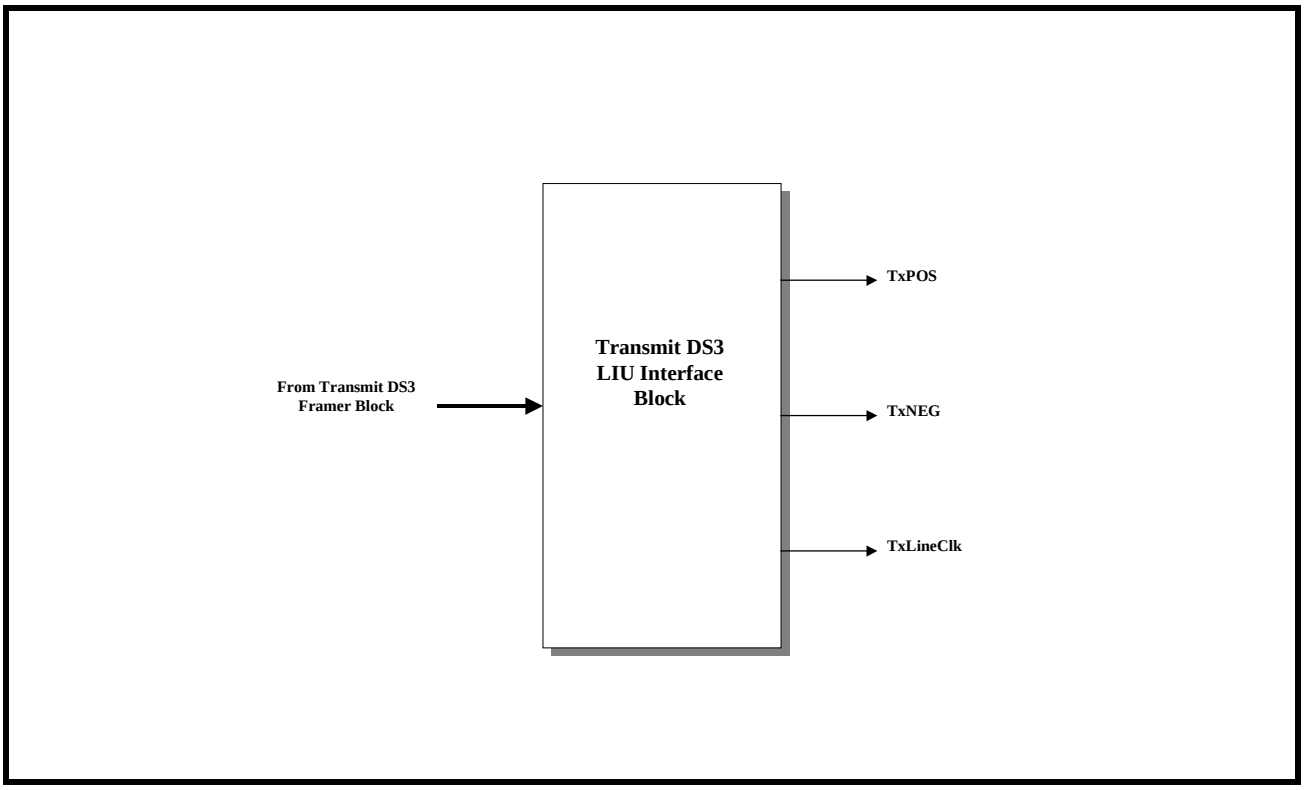


The "Transmit Section" of the XRT72L13 contains a block which is known as the "Transmit DS3 LIU Interface" block. The purpose of the "Transmit DS3 LIU Interface" block is to take the "outbound" DS3 data stream, from the "Transmit DS3 Framer" block, and to do the following:

1. Encode this data into one of the following line codes
   a. Unipolar (e.g., Single-Rail)
   b. AMI (Alternate Mark Inversion)
   c. B3ZS (Bipolar 3 Zero Substitution)
2. And to transmit this data to the LIU IC.

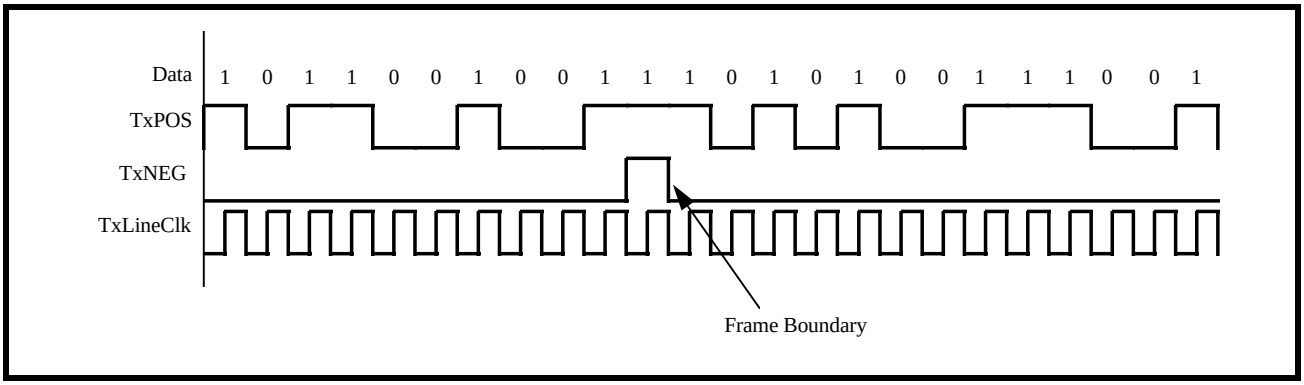
Figure 85 presents a simple illustration of the "Transmit DS3 LIU Interface" block.

FIGURE 85. A SIMPLE ILLUSTRATION OF THE "TRANSMIT DS3 LIU INTERFACE" BLOCK



The "Transmit DS3 LIU Interface" block can transmit data to the LIU IC or other external circuitry via two different output modes: Unipolar or Bipolar. If the user selects Unipolar (or Single Rail) mode, then the contents of the DS3 Frame is output, in a binary (NRZ manner) data stream via the TxPOS pin to the LIU IC. The TxNEG pin will only be used to denote the frame boundaries. TxNEG will pulse "high" for one bit period, at the start of each new DS3 frame, and will remain "low" for the remainder of the frame. Figure 86 presents an illustration of the TxPOS and TxNEG signals during data transmission while the "Transmit DS3 LIU Interface" block is operating in the "Unipolar" mode. This mode is sometimes referred to as "Single Rail" mode because the data pulses only exist in one polarity: positive.

FIGURE 86. THE BEHAVIOR OF TXPOS AND TXNEG SIGNALS DURING DATA TRANSMISSION WHILE THE TRANSMIT DS3 LIU INTERFACE IS OPERATING IN THE UNIPOLAR MODE



When the "Transmit DS3 LIU Interface" block is operating in the "Bipolar" (or "Dual Rail") mode, then the contents of the DS3 Frame is output via both the “TxPOS” and “TxNEG” pins. If the user chooses the Bipolar mode, then he/she can transmit the DS3 data to the LIU via one of two different line codes: Alternate

Mark Inversion (AMI) or Binary - 3 Zero Substitution (B3ZS). Each one of these line codes will be discussed below. Bipolar mode is sometimes referred to as "Dual Rail" because the data pulses occur in two polarities: positive and negative. The role of the TxPOS, TxNEG and TxLineClk output pins, for this mode are discussed below.

TxPOS - Transmit Positive Polarity Pulse: The Transmit DS3 LIU Interface block will assert this output to the LIU IC when it desires for the LIU to generate and transmit a "positive polarity" pulse to the remote terminal equipment.

TxNEG - Transmit Negative Polarity Pulse: The Transmit DS3 LIU Interface block will assert this output to the LIU IC when it desires for the LIU to generate and transmit a "negative polarity" pulse to the remote terminal equipment.

TxLineClk - Transmit Line Clock: The LIU IC uses this signal from the "Transmit DS3 LIU Interface" block to sample the state of its TxPOS and TxNEG inputs. The results of this sampling dictates the type of pulse (positive polarity, zero, or negative polarity) that it will generate and transmit to the remote Receive DS3 Framer.

4.2.5.1 Selecting the various Line Codes

The user can select either the "Unipolar" Mode or "Bipolar" Mode by writing the appropriate value to Bit 3 of the I/O Control Register (Address = 0x01), as shown below.

I/O CONTROL REGISTER (ADDRESS = 0X01)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit2	Bit 1	Bit 0
Disable TxLOC	LOC	Disable RxLOC	AMI/ZeroSup*	Unipolar/ Bipolar*	TxLine CLK Invert	RxLine CLK Invert	Reframe
R/W	RO	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	0	0	0	0

Table 26 relates the value of this bit field to the "Transmit DS3 LIU Interface Output" Mode.

TABLE 26: THE RELATIONSHIP BETWEEN THE CONTENT OF BIT 3 (UNIPOLAR/BIPOLAR*) WITHIN THE UNI I/O CONTROL REGISTER AND THE TRANSMIT DS3 FRAMER LINE INTERFACE OUTPUT MODE

Bit 3	Transmit DS3 Framer LIU Interface Output Mode
0	**Bipolar Mode:** AMI or B3ZS Line Codes are Transmitted and Received
1	**Unipolar (Single Rail) Mode** of transmission and reception of DS3 data is selected.

NOTES:

1. *The default condition is the Bipolar Mode.*
2. *This selection also effects the operation of the Receive DS3 LIU Interface block*

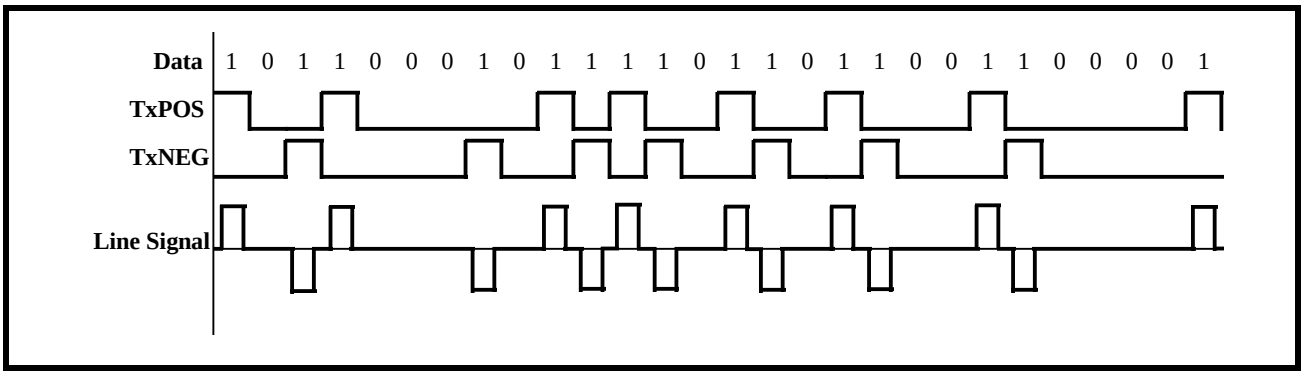
4.2.5.1.1 The Bipolar Mode Line Codes

If the user chooses to operate the Framer in the Bipolar Mode, then he/she can choose to transmit the DS3 data-stream via the AMI (Alternate Mark Inversion) or the B3ZS Line Codes. The definition of AMI and B3ZS line codes follow.

4.2.5.1.1.1 The AMI Line Code

AMI or Alternate Mark Inversion, means that consecutive "one's" pulses (or marks) will be of opposite polarity with respect to each other. The line code involves the use of three different amplitude levels: +1, 0, and -1. +1 and -1 amplitude signals are used to represent one's (or mark) pulses and the "0" amplitude pulses (or the absence of a pulse) are used to represent zeros (or space) pulses. The general rule for AMI is: if a given "mark" pulse is of positive polarity, then the very next "mark" pulse will be of negative polarity and vice versa. This alternating-polarity relationship exists between two consecutive mark pulses, independent of the number of 'zeros' that may exist between these two pulses. Figure 87 presents an illustration of the AMI Line Code as would appear at the TxPOS and TxNEG pins of the Framer, as well as the output signal on the line.

FIGURE 87. ILLUSTRATION OF AMI LINE CODE



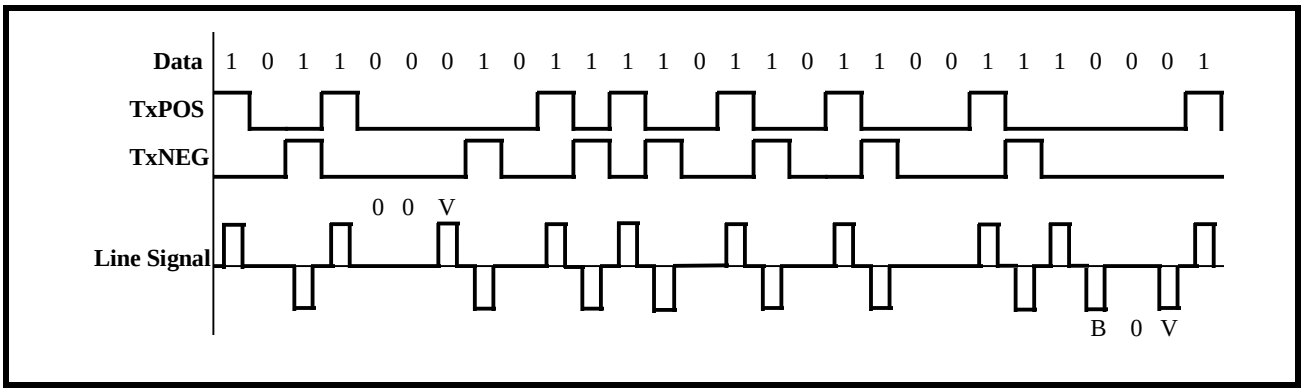
NOTE: One of the main reasons that the AMI Line Code has been chosen for driving transformer-coupled media is that this line code introduces no dc component; thereby minimizing dc distortion in the line.

4.2.5.1.1.2 The B3ZS Line Code

The Transmit DS3 Framer and the associated LIU IC combine the data and timing information (originating from the TxLineClk signal) into the line signal that is transmitted to the far-end receiver. The far-end receiver has the task of recovering this data and timing information from the incoming DS3 data stream. Many clock and data recovery schemes rely on the use of Phase Locked Loop technology. Phase-Locked-Loop (PLL) technology for clock recovery relies on transitions in the line signal, in order to maintain "lock" with the incoming DS3 data stream. However, PLL-based clock recovery scheme, are vulnerable to the occurrence of a long stream of consecutive zeros (e.g., the absence of transitions). This scenario can cause the PLL to lose "lock" with the incoming DS3 data, thereby causing the "clock" and data recovery process of the receiver to fail. Therefore, some approach is needed to insure that such a long string of consecutive zeros can never happen. One such technique is B3ZS encoding. B3ZS (or Bipolar 3 Zero Substitution) is a form of AMI line coding that implements the following rule.

In general the B3ZS line code behaves just like AMI; with the exception of the case when a long string of consecutive zeros occur on the line. Any string of 3 consecutive zeros will be replaced with either a "00V" or a "B0V" where "B" refers to a Bipolar pulse (e.g., a pulse with a polarity that is compliant with the AMI coding rule). And "V" refers to a Bipolar Violation pulse (e.g., a pulse with a polarity that violates the alternating polarity scheme of AMI.) The decision between inserting an "00V" or a "B0V" is made to insure that an odd number of Bipolar (B) pulses exist between any two Bipolar Violation (V) pulses. Figure 88 presents a timing diagram that illustrates examples of B3ZS encoding.

FIGURE 88. ILLUSTRATION OF TWO EXAMPLES OF B3ZS ENCODING



The user chooses between AMI or B3ZS line coding by writing to bit 4 of the "I/O Control" Register (Address = 0x01), as shown below.

I/O CONTROL REGISTER (ADDRESS = 0X01)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Disable TxLOC	LOC	Disable RxLOC	AMI/ZeroSup*	Unipolar/ Bipolar*	TxLine CLK Invert	RxLine CLK Invert	Reframe
R/W	RO	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	0	0	0	0

Table 27 relates the content of this bit-field to the Bipolar Line Code that DS3 Data will be transmitted and received at.

TABLE 27: THE RELATIONSHIP BETWEEN BIT 4 (AMI/B3ZS*) WITHIN THE "I/O CONTROL" REGISTER AND THE BIPOLAR LINE CODE THAT IS OUTPUT BY THE TRANSMIT DS3 LIU INTERFACE BLOCK

BIT 4	BIPOLAR LINE CODE
0	B3ZS
1	AMI

NOTES:

1. *This bit is ignored if the "Unipolar" mode is selected.*
2. *This selection also effects the operation of the "Receive DS3 LIU Interface" block*

4.2.5.2 TxLineClk Clock Edge Selection

The Framer also allows the user to specify whether the DS3 output data (via TxPOS and/or TxNEG output pins) is to be updated on the rising or falling edges of the TxLineClk signal. The purpose of this feature is to insure that the Framer will alway be able to output data to the LIU IC, in such a way that the LIU set-up and hold time requirements can always be met. This selection is made by writing to bit 2 of the "I/O Control" Register, as depicted below.

II/O CONTROL REGISTER (ADDRESS = 0X01)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Disable TxLOC	LOC	Disable RxLOC	AMI/ZeroSup*	Unipolar/ Bipolar*	TxLine CLK Invert	RxLine CLK Invert	Reframe
R/W	RO	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	0	X	X	0

Table 28 relates the contents of this bit field to the clock edge of TxClk that DS3 Data is output on the TxPOS and/or TxNEG output pins.

TABLE 28: THE RELATIONSHIP BETWEEN THE CONTENTS OF BIT 2 (TXLINECLK INV) WITHIN THE "I/O CONTROL" REGISTER AND THE TXLINECLK CLOCK EDGE THAT TXPOS AND TXNEG ARE UPDATED ON

BIT 2	RESULT
0	**Rising Edge:** Outputs on TxPOS and/or TxNEG are updated on the rising edge of TxLineClk. See Figure 89 for timing relationship between TxLineClk, TxPOS and TxNEG signals, for this selection.
1	**Falling Edge:** Outputs on TxPOS and/or TxNEG are updated on the falling edge of TxLineClk. See Figure 90 for timing relationship between TxLineClk, TxPOS and TxNEG signals, for this selection.

NOTE: The user will typically make the selection based upon the "set-up" and "hold" time requirements of the "Transmit LIU" IC.

FIGURE 89. WAVEFORM/TIMING RELATIONSHIP BETWEEN TXLINECLK, TXPOS AND TXNEG - TXPOS AND TXNEG ARE CONFIGURED TO BE UPDATED ON THE RISING EDGE OF TXLINECLK

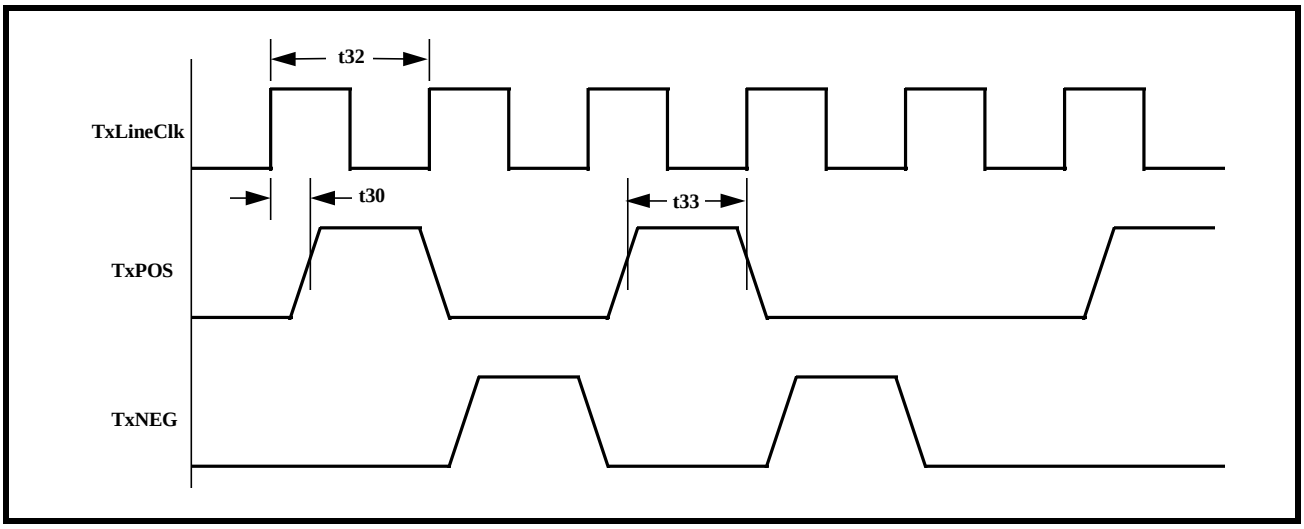
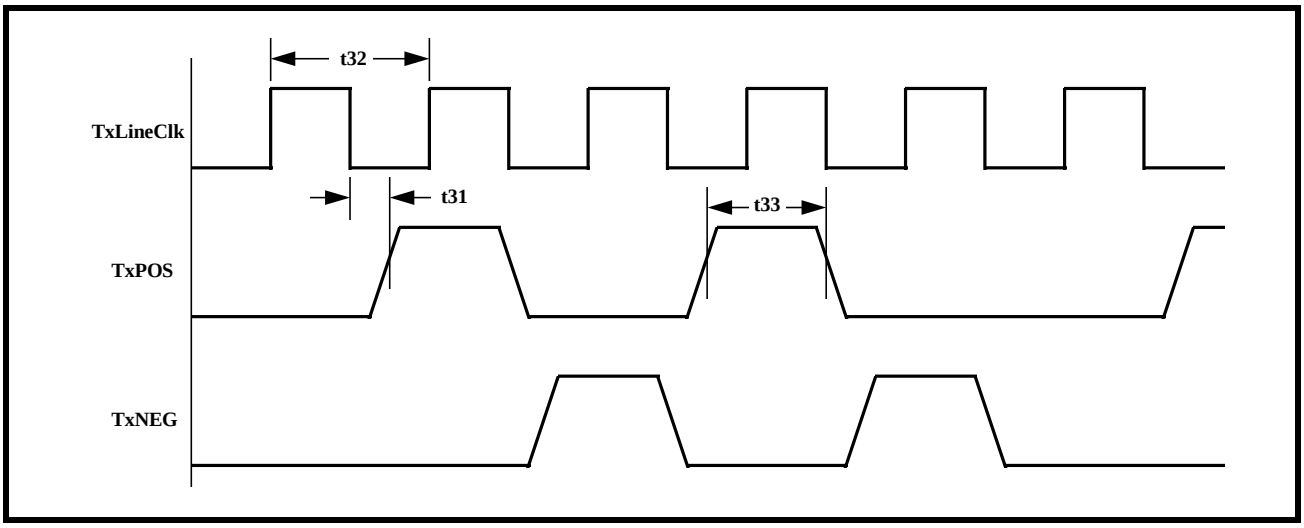


FIGURE 90. WAVEFORM/TIMING RELATIONSHIP BETWEEN TXLINECLK, TXPOS AND TXNEG - TXPOS AND TXNEG ARE CONFIGURED TO BE UPDATED ON THE FALLING EDGE OF TXLINECLK



4.2.6 Transmit Section Interrupt Processing

The "Transmit Section" of the XRT72L13 can generate an interrupt to the Microcontroller/Microprocessor for the following two reasons.

- Completion of Transmission of FEAC Message
- Completion of Transmission of LAPD Message

4.2.6.1 Enabling "Transmit Section" Interrupts

As mentioned in Section 1.6, the Interrupt Structure, within the XRT72L13 contains two hierarchical levels:

- Block Level
- Source Level

The Block Level

The "Enable" State of the "Block" Level for the Transmit Section Interrupts dictates whether or not interrupts (if enabled at the source level), are actually enabled.

The user can enable or disable these “Transmit Section” interrupts, at the “Block Level” by writing the appropriate data into Bit 1 (“Tx DS3/E3 Interrupt En-

able) within the “Block Interrupt Enable” register (Address = 0x04); as illustrated below.

BLOCK INTERRUPT ENABLE REGISTER (ADDRESS = 0X04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxDS3/E3 Interrupt Enable	Not Used		M13 Interrupt Enable	Not Used		TxDS3/E3 Interrupt Enable	One Second Interrupt Enable
R/W	R/O	R/O	R/W	RO	RO	R/W	R/W
0	0	0	0	0	0	0	0

Setting this bit-field to “1” enables the “Transmit Section” (at the “Block Level”) for Interrupt Generation. Conversely, setting this bit-field to “0” disables the “Transmit Section” for interrupt generation.

What does it mean for the “Transmit Section” Interrupts to be “enabled” or “disabled” at the “Block Level”?

If the “Transmit Section” is disabled (for interrupt generation) at the “Block” Level; then ALL “Transmit Section” interrupts are disabled, independent of the “interrupt enable/disable” state of the source level interrupts.

If the “Transmit Section” is enabled (for interrupt generation) at the “block” level; then a given interrupt will be enabled at the “source” level. Conversely, if the “Transmit Section” is enabled (for interrupt generation) at the “Block” level; then a given interrupt will still be disabled, if it is disabled at the “source” level.

As mentioned earlier, the “Transmit Section” of the XRT72L13 Framer IC contains the following two interrupts

- Completion of Transmission of FEAC Message Interrupt.
- Completion of Transmission of LAPD Message Interrupt.

The “Enabling/Disabling and Servicing” of each of these interrupts is described below.

4.2.6.1.1 The “Completion of Transmission of FEAC Message” Interrupt.

If the “Transmit Section” interrupts have been enabled at the “Block” level, then the user can enable or disable the “Completion of Transmission of a FEAC Message” Interrupt by writing the appropriate value into Bit 4 (Tx FEAC Interrupt Enable) within the “Transmit DS3 FEAC Configuration & Status” Register (Address = 0x31) as illustrated below.

TRANSMIT DS3 FEAC CONFIGURATION & STATUS REGISTER (ADDRESS = 0X31)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			Tx FEAC Interrupt Enable	TxFEAC Interrupt Status	TxFEAC Enable	TxFEAC GO	TxFEAC Busy
RO	RO	RO	R/W	RUR	R/W	R/W	RO
0	0	0	X	0	0	0	0

Setting this bit-field to “1” enables the “Completion of Transmission of a FEAC Message” Interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

4.2.6.1.2 Servicing the “Completion of Transmission of a FEAC Message Interrupt

As mentioned earlier, once the user commands the “Transmit FEAC Processor” to begin its transmission of a FEAC Message, it will do the following.

1. It will read in the “six-bit” contents of the “Tx DS3 FEAC” Register (Address = 0x32); and encapsulate these 6 bits into a 16-bit data structure.
2. The Transmit FEAC Processor will then begin to transmit this “16-bit” data structure (to the Remote Terminal Equipment); repeatedly for 10 consecutive times.
3. Upon completion of the 10th transmission, the XRT72L13 Framer IC will generate the “Completion of Transmission of a FEAC Message” Inter-

rupt to the Microcontroller/Microprocessor. Once the XRT72L13 Framer IC generates this interrupt, it will do the following.

- Assert the "Interrupt Output" pin (INT) by toggling it "LOW".
- Set Bit 3 (Tx FEAC Interrupt Status) within the "Tx DS3 FEAC Configuration & Status Register, as illustrated below.

TRANSMIT DS3 FEAC CONFIGURATION & STATUS REGISTER (ADDRESS = 0X31)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			Tx FEAC Interrupt Enable	TxFEAC Interrupt Status	TxFEAC Enable	TxFEAC GO	TxFEAC Busy
RO	RO	RO	R/W	RUR	R/W	R/W	RO
0	0	0	1	1	0	0	0

The purpose of this interrupt is to alert the Microcontroller/Microprocessor that the "Transmit FEAC Processor" has completed its transmission of a given FEAC message and is now ready to transmit the next FEAC Message, to the Remote Terminal Equipment.

4.2.6.1.3 The "Completion of Transmission of the LAPD Message Interrupt

If the "Transmit Section" interrupts have been enabled at the "Block" level, then the user can enable or disable the "Completion of Transmission of a LAPD Message" Interrupt; by writing the appropriate value into Bit 1 (TxLAPD Interrupt Enable) within the "Tx DS3 LAPD Status & Interrupt" Register (Address = 0x34); as illustrated below.

TXDS3 LAPD STATUS AND INTERRUPT REGISTER (ADDRESS = 0X34)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used				TxDL Start	TxDL Busy	TxLAPD Interrupt Enable	TxLAPD Interrupt Status
RO	RO	RO	RO	R/W	RO	R/W	RUR
0	0	0	0	0	0	0	0

Setting this bit-field to "1' enables the "Completion of Transmission of a LAPD Message" Interrupt. Conversely, setting this bit-field to "0" disables the "Completion of Transmission of a LAPD Message" interrupt.

4.2.6.1.4 Servicing the "Completion of Transmission of a LAPD Message" Interrupt

As mentioned earier, once the user commands the "LAPD Transmitter" to begin its transmission of a LAPD Message, it will do the following.

1. It will parse through the contents of the Transmit LAPD Message Buffer (located at address locations 0x86 through 0xDD); and search for a string of five (5) consective "1s". If the LAPD Transmitter finds a string of five consecutive "1s" (within the content of the LAPD Message Buffer, then it will insert a "0" immediately after this string.
2. It will compute the FCS (Frame Check Sequence) value; and append this value to the "back-end" of the "user-message".
3. It will read out of the content of the user (zero-stuffed) message and will encapsulate this data into a LAPD Message frame.
4. Finally, it will begin transmitting the contents of this LAPD Message frame via the "DL" bits, within each "outbound" DS3 frame.
5. Once the LAPD Transmitter has completed its transmission of this LAPD Message frame (to the Remote Terminal Equipment), the XRT72L13 Framer IC will generate the "Completion of Transmission of a LAPD Message" Interrupt to the Microcontroller/Microprocessor. Once the XRT72L13 Framer IC generates this interrupt, it will do the following.

- Assert the "Interrupt Output" pin (INT) by toggling it "LOW".

- Set Bit 0 (TxLAPD Interrupt Status) within the "TxDS3 LAPD Status and Interrupt" Register, as illustrated below.

TXDS3 LAPD STATUS AND INTERRUPT REGISTER (ADDRESS = 0X34)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used				TxDL Start	TxDL Busy	TxLAPD Interrupt Enable	TxLAPD Interrupt Status
RO	RO	RO	RO	R/W	RO	R/W	RUR
0	0	0	0	0	0	0	1

The purpose of this interrupt is to alert the Microcontroller/MIcroprocessor that the "LAPD Transmitter" has completed its transmission of a given LAPD (or PMDL) Message, and is now ready to transmit the next PMDL Message, to the Remote Terminal Equipment.

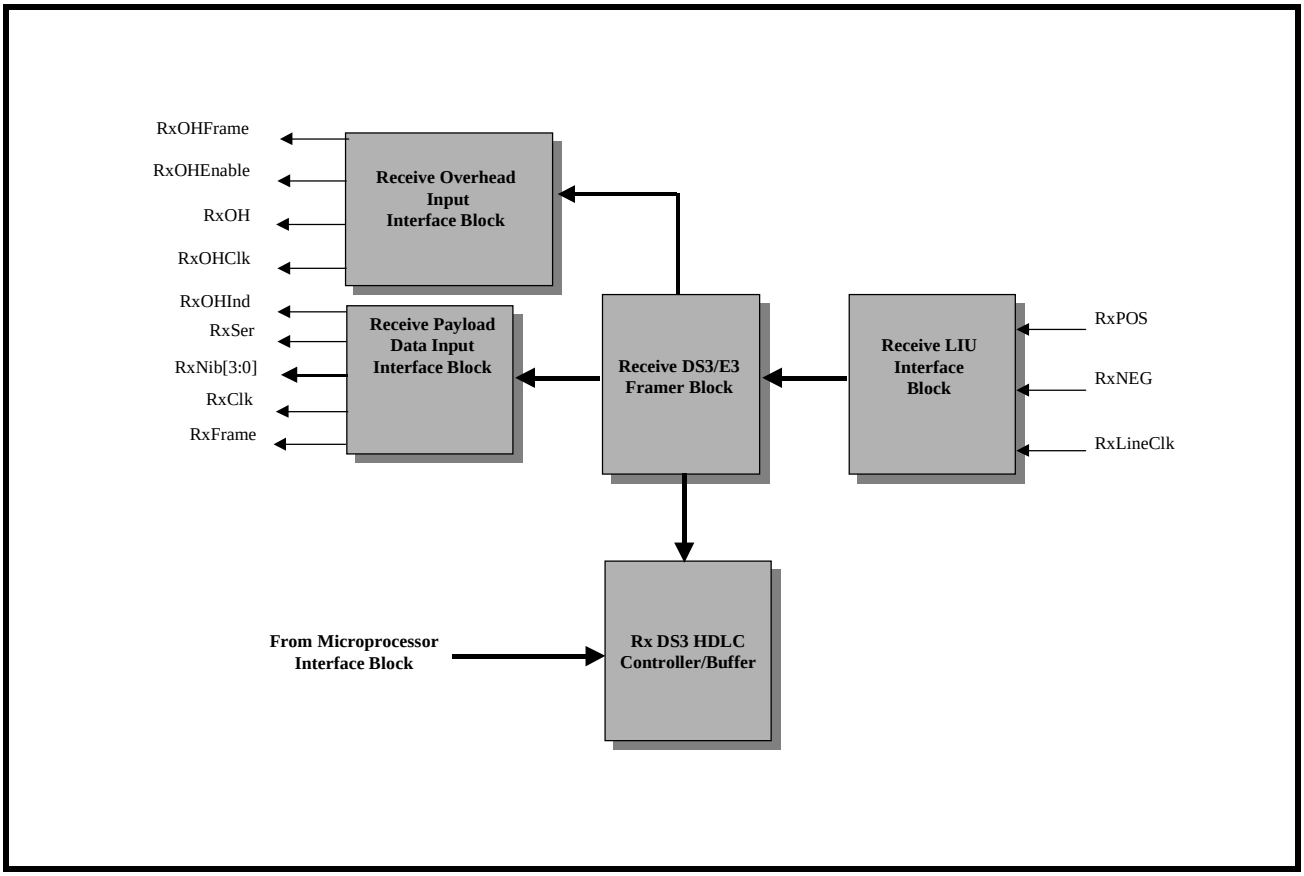
4.3 THE RECEIVE SECTION OF THE XRT72L13 (DS3 MODE OPERATION)

When the XRT72L13 has been configured to operate in the DS3 Mode, the Receive Section of the XRT72L13 consists of the following functional blocks.

- Receive LIU Interface block
- Receive HDLC Controller block
- Receive DS3 Framer block
- Receive Overhead Data Output Interface block
- Receive Payload Data Output Interface block

Figure 91 presents a simple illustration of the Receive Section of the XRT72L13 Framer IC.

FIGURE 91. A SIMPLE ILLUSTRATION OF THE RECEIVE SECTION OF THE XRT72L13, WHEN IT HAS BEEN CONFIGURED TO OPERATE IN THE DS3 MODE



Each of these functional blocks will be discussed in detail in this document.

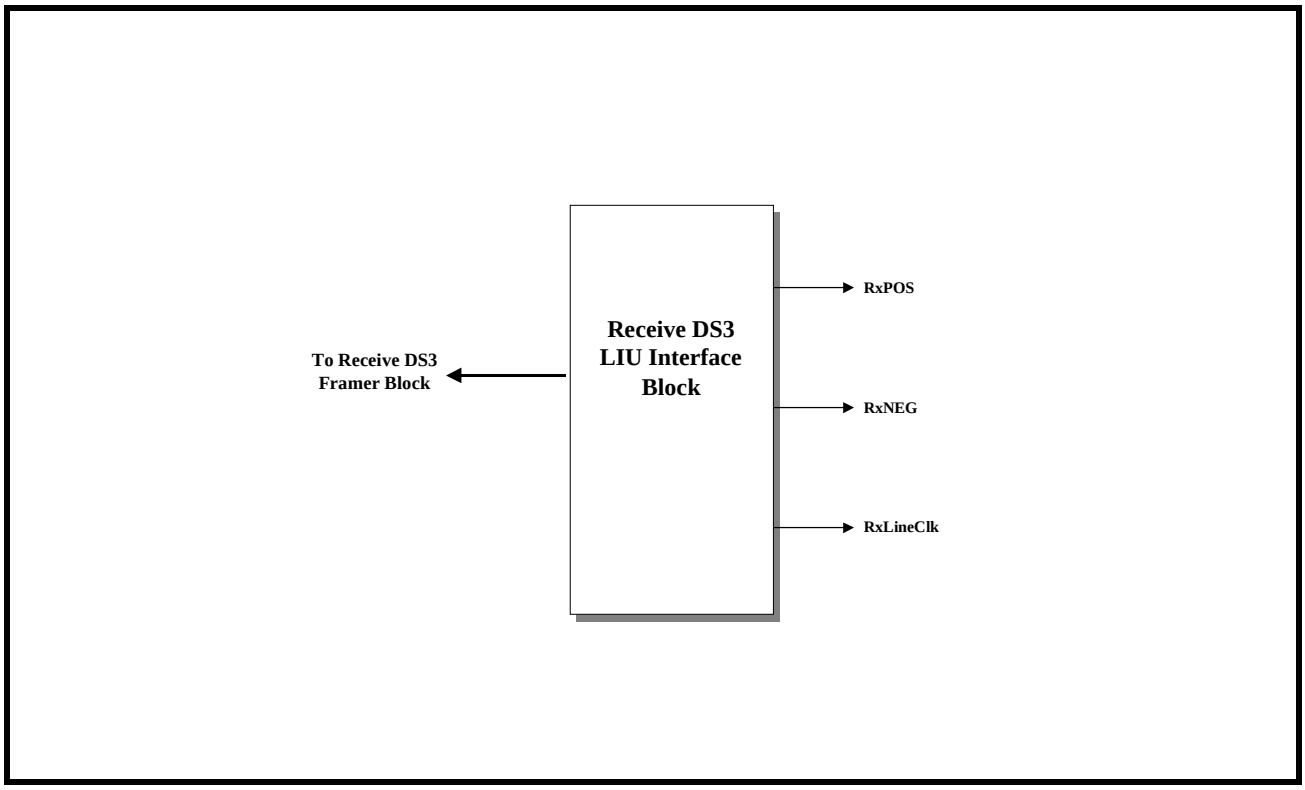
4.3.1 The Receive DS3 LIU Interface Block

The purpose of the Receive DS3 LIU Interface block is two-fold:

1. To receive "encoded" digital data from the DS3 LIU IC.
2. To decode this data, convert it into a binary data stream and to route this data to the "Receive DS3 Framer" block.

Figure 92 presents a simple illustration of the "Receive DS3 LIU Interface" block.

FIGURE 92. A SIMPLE ILLUSTRATION OF THE "RECEIVE DS3 LIU INTERFACE" BLOCK



The Receive Section of the XRT72L13 will via the Receive DS3 LIU Interface Block receive timing and data information from the incoming DS3 data stream. The DS3 Timing information will be received via the “RxLineClk” input pin; and the DS3 data information will be received via the “RxPOS” and “RxNEG” input pins. The Receive DS3 LIU Interface block is capable of receiving DS3 data pulses in unipolar or bipolar format. If the Receive DS3 framer is operating in the bipolar format, then it can be configured to decode either AMI or B3ZS line code data. Each of these input formats and line codes will be discussed in detail, below.

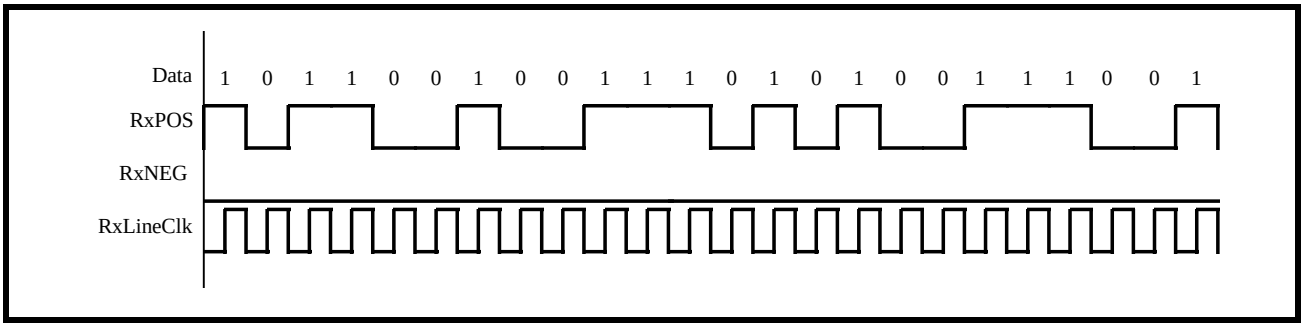
4.3.1.1 Unipolar Decoding

If the Receive DS3 LIU Interface block is operating in the Unipolar (single-rail) mode, then it will receive the Single Rail NRZ DS3 data pulses via the RxPOS input pin. The "Receive DS3 LIU Interface" block will also receive its timing signal via the RxLineClk signal.

NOTE: *The "RxLineClk" signal will function as the timing source for the entire Receive Section of the XRT72L13.*

No data pulses will be applied to the RxNEG input pin. The "Receive DS3 LIU Interface" block receives a logic "1" when a logic "1" level signal is present at the RxPOS pin, during the sampling edge of the RxLineClk signal. Likewise, a logic "0" is received when a logic "0" level signal is applied to the RxPOS pin. Figure 93 presents an illustration of the behavior of the RxPOS, RxNEG and RxLineClk input pins when the "Receive DS3 LIU Interface" block is operating in the "Unipolar" mode.

FIGURE 93. BEHAVIOR OF THE RXPOS, RXNEG AND RXLINECLK SIGNALS DURING DATA RECEPTION OF UNIPOLAR DATA



The user can configure the Receive DS3 LIU Interface block to operate in either the Unipolar or the Bipolar Mode by writing the appropriate data to the “I/O Control” Register, as depicted below.

II/O CONTROL REGISTER (ADDRESS = 0X01)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Disable TxLOC	LOC	Disable RxLOC	AMI/ ZeroSup*	Unipolar/ Bipolar*	TxLine CLK Invert	RxLine CLK Invert	Reframe
R/W	RO	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	0	0	0	0

Table 29 relates the value of this bit-field to the Receive DS3 LIU Interface Input Mode.

TABLE 29: THE RELATIONSHIP BETWEEN THE CONTENTS OF BIT 2 (TXLINECLK INV) WITHIN THE "I/O CONTROL" REGISTER AND THE TXLINECLK CLOCK EDGE THAT TXPOS AND TXNEG ARE UPDATED ON

BIT 3	RECEIVE DS3 LIU INTERFACE INPUT MODE
0	.**Bipolar Mode (Dual Rail):** AMI or B3ZS Line Codes are Transmitted and Received.
1	**Unipolar Mode (Single Rail) Mode** of transmission and reception of DS3 data is selected..

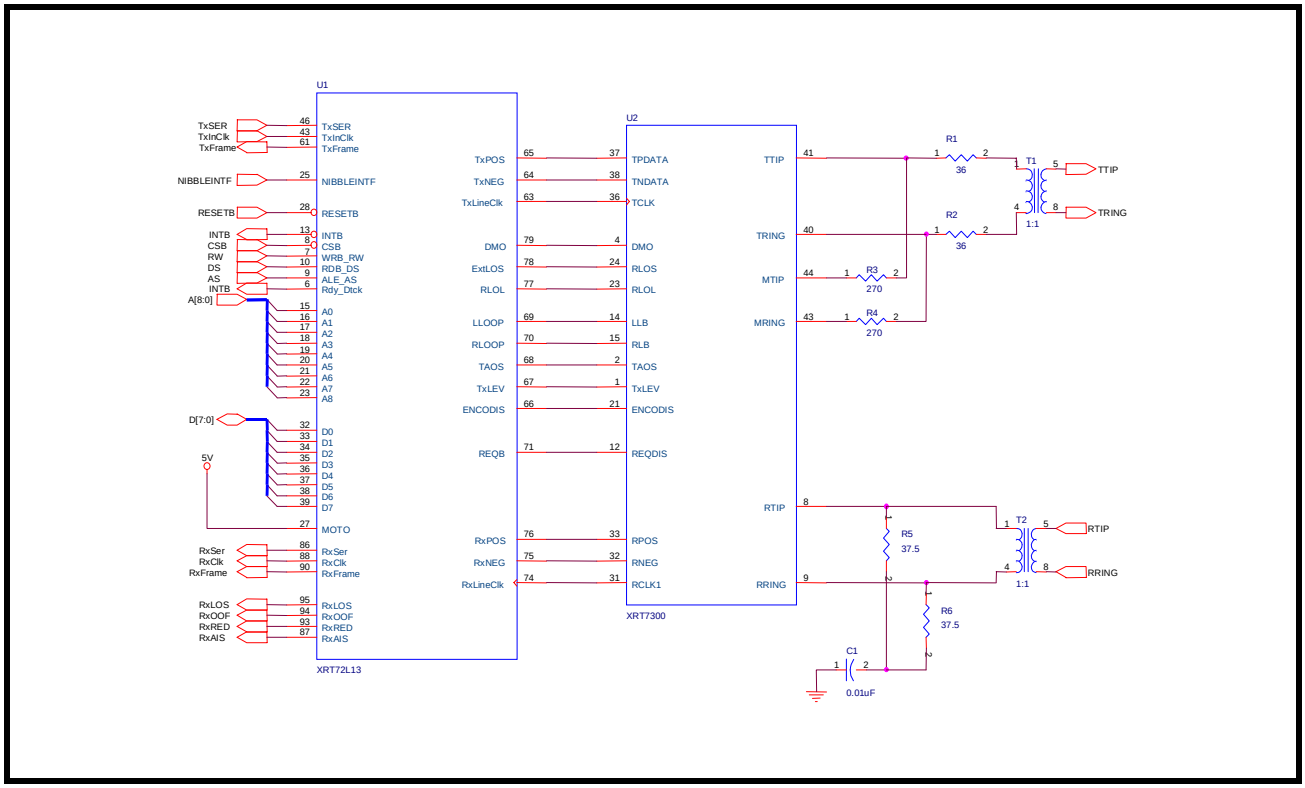
NOTES:

1. *The default condition is the Bipolar Mode.*
2. *This selection also effects the Transmit DS3 Framer Line Interface Output Mode*

4.3.1.2 Bipolar Decoding

If the "Receive DS3 LIU Interface" block is operating in the Bipolar Mode, then it will receive the DS3 data pulses via both the RxPOS, RxNEG, and the RxLineClk input pins. Figure 94 presents a circuit diagram illustrating how the Receive DS3 LIU Interface block interfaces to the Line Interface Unit while the Framer is operating in Bipolar mode. The Receive DS3 LIU Interface block can be configured to decode the incoming data from either the AMI or B3ZS line codes.

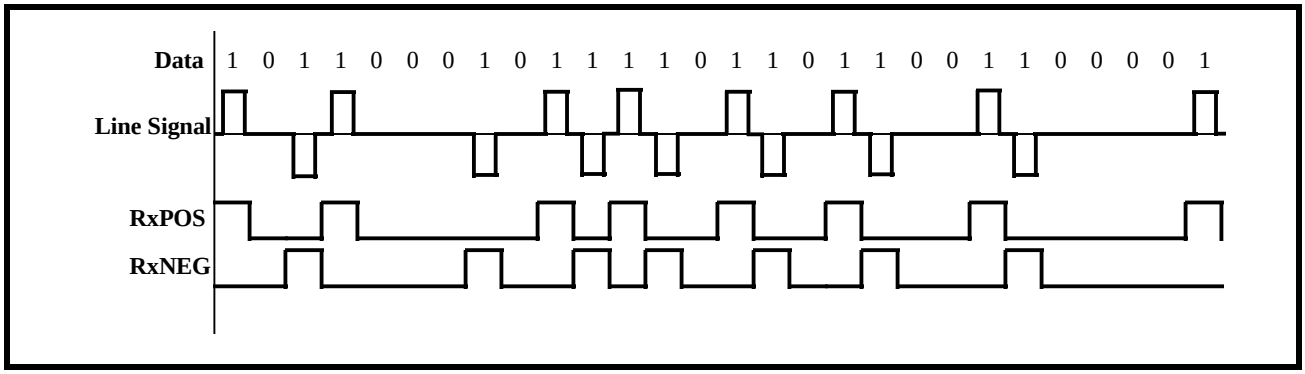
FIGURE 94. ILLUSTRATION ON HOW THE RECEIVE DS3 FRAMER (WITHIN THE XRT72L13 FRAMER IC) BEING INTERFACE TO THEXRT7300 LINE INTERFACE UNIT, WHILE THE FRAMER IS OPERATING IN BIPOLAR MODE



4.3.1.2.1 AMI Decoding

AMI or Alternate Mark Inversion, means that consecutive "one's" pulses (or marks) will be of opposite polarity with respect to each other. This line code involves the use of three different amplitude levels: +1, 0, and -1. The +1 and -1 amplitude signals are used to represent one's (or mark) pulses and the "0" amplitude pulses (or the absence of a pulse) are used to represent zeros (or space) pulses. The general rule for the AMI line code is: if a given "mark" pulse is of positive polarity, then the very next "mark" pulse will be of negative polarity and vice versa. This alternating-polarity relationship exists between two consecutive mark pulses, independent of the number of zeros that exist between these two pulses. Figure 95 presents an illustration of the AMI Line Code as would appear at the “RxPOS” and “RxNEG” input pins of the Framer, as well as the corresponding output signal on the line.

FIGURE 95. ILLUSTRATION OF AMI LINE CODE



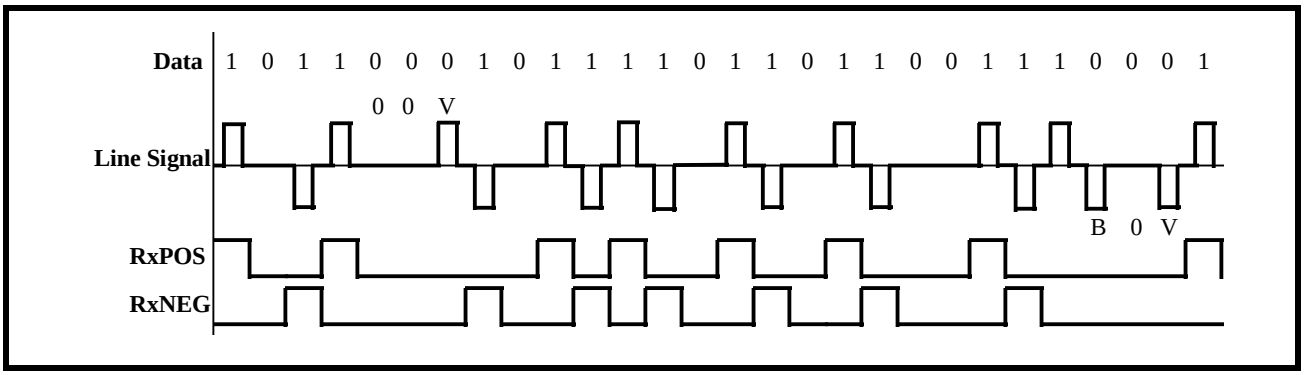
NOTE: *One of the reasons that the AMI Line Code has been chosen for driving copper medium, isolated via transformers, is that this line code has no dc component; thereby eliminating dc distortion in the line.*

4.3.1.2.2 B3ZS Decoding

The Transmit DS3 LIU Interface block and the associated LIU embed and combine the data and clocking information into the line signal that is transmitted to the remote terminal equipment. The "remote terminal" equipment has the task of recovering this data and timing information from the incoming DS3 data stream. Most clock and data recovery schemes rely on the use of Phase-Locked-Loop technology. One of the problems of using Phase-Locked-Loop (PLL) technology for clock recovery is that it relies on transitions in the line signal, in order to maintain “lock” with the incoming DS3 data-stream. Therefore, these clock recovery scheme, are vulnerable to the occurrence of a long stream of consecutive zeros (e.g., no transitions in the line). This scenario can cause the PLL to lose "lock" with the incoming DS3 data, thereby causing the "clock" and data recovery process of the receiver to fail. Therefore, some approach is needed to insure that such a long string of consecutive zeros can never happen. One such technique is B3ZS (or Bipolar 3 Zero Substitution) encoding.

In general the B3ZS line code behaves just like AMI; with the exception of the case when a long string of consecutive zeros occurs on the line. Any 3 consecutive zeros will be replaced with either a "00V" or a "B0V" where "B" refers to a Bipolar pulse (e.g., a pulse with a polarity that is compliant with the alternating polarity scheme of the AMI coding rule). And "V" refers to a Bipolar Violation pulse (e.g., a pulse with a polarity that violates the alternating polarity scheme of AMI.) The decision between inserting an "00V" or a "B0V" is made to insure that an odd number of Bipolar (B) pulses exist between any two Bipolar Violation (V) pulses. The Receive DS3 Framer, when operating with the B3ZS Line Code is responsible for decoding the B3ZS-encoded data back into a unipolar (binary-format). For instance, if the Receive DS3 Framer detects a "00V" or a "B0V" pattern in the incoming pattern, the Receive DS3 Framer will replace it with three consecutive zeros. Figure 96 presents a timing diagram that illustrates examples of B3ZS decoding.

FIGURE 96. ILLUSTRATION OF TWO EXAMPLES OF B3ZS DECODING



4.3.1.2.3 Line Code Violations

The "Receive DS3 LIU Interface" block will also check the incoming DS3 data stream for line code violations. For example, when the Receive DS3 LIU Interface block detects a valid bipolar violation (e.g., in B3ZS line code), it will substitute three zeros into the binary data stream. However, if the bipolar violation is invalid, then an LCV (Line Code Violation) is flagged and the "PMON LCV Event Count" Register (Address = 0x50 and 0x51) will also be incremented. Additionally, the "LCV-One Second Accumulation" Registers (Address = 0x6E and 0x6F) will be incremented. For example: If the incoming DS3 data is B3ZS encoded, the Receive DS3 LIU Interface block will also increment the "LCV One Second Accumulation" Register if three (or more) consecutive zeros are received.

4.3.1.2.4 RxLineClk Clock Edge Selection

The incoming unipolar or bipolar data, applied to the RxPOS and the RxNEG input pins are clocked into the Receive DS3 LIU Interface block via the RxLineClk signal. The Framer IC allows the user to specify which edge (e.g, rising or falling) of the RxLineClk signal will sample and latch the signal at the RxPOS and RxNEG input signals into the Framer IC. This feature was included in the XRT72L13 design in order to insure that the user can always meet the “RxPOS” and “RxNEG” to “RxLineClk” set-up and hold time requirements. The user can make this selection by writing the appropriate data to bit 1 of the "I/O Control" Register, as depicted below.

II/O CONTROL REGISTER (ADDRESS = 0X01)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Disable TxLOC	LOC	Disable RxLOC	AMI/ ZeroSup*	Unipolar/ Bipolar*	TxLine CLK Invert	RxLine CLK Invert	Reframe
R/W	RO	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	0	0	0	0

Table 30 depicts the relationship between the value of this bit-field to the sampling clock edge of RxLineClk.

TABLE 30: THE RELATIONSHIP BETWEEN THE CONTENTS OF BIT 1 (RXLINECLK INV) OF THE I/O CONTROL REGISTER, AND THE SAMPLING EDGE OF THE RXLINECLK SIGNAL

RXCLKINV (BIT 1)	RESULT
0	**Rising Edge:** RxPOS and RxNEG are sampled at the rising edge of RxLineClk. See Figure 97 for timing relationship between RxLineClk, RxPOS, and RxNEG.
1	**Falling Edge:** RxPOS and RxNEG are sampled at the falling edge of RxLineClk. See Figure 98 for timing relationship between RxLineClk, RxPOS, and RxNEG.

Figure 97 and Figure 98 present the Waveform and Timing Relationships between RxLineClk, RxPOS and RxNEG for each of these configurations.

FIGURE 97. WAVEFORM/TIMING RELATIONSHIP BETWEEN RXLINECLK, RXPOS AND RXNEG - WHEN RXPOS AND RXNEG ARE TO BE SAMPLED ON THE RISING EDGE OF RXLINECLK

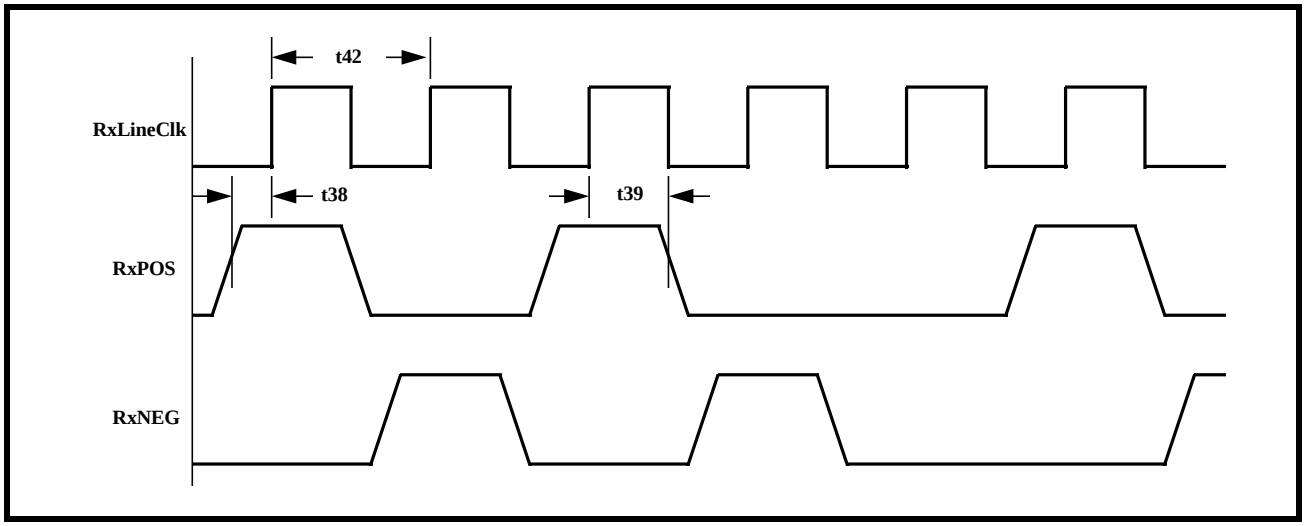
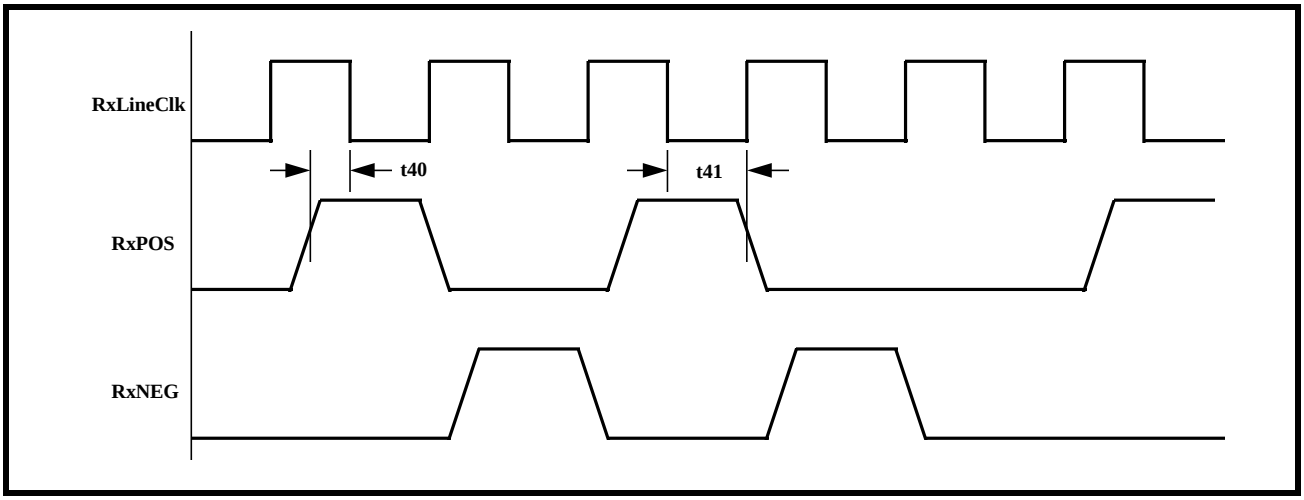


FIGURE 98. WAVEFORM/TIMING RELATIONSHIP BETWEEN RXLINECLK, RXPOS AND RXNEG - WHEN RXPOS AND RXNEG ARE TO BE SAMPLED ON THE FALLING EDGE OF RXLINECLK



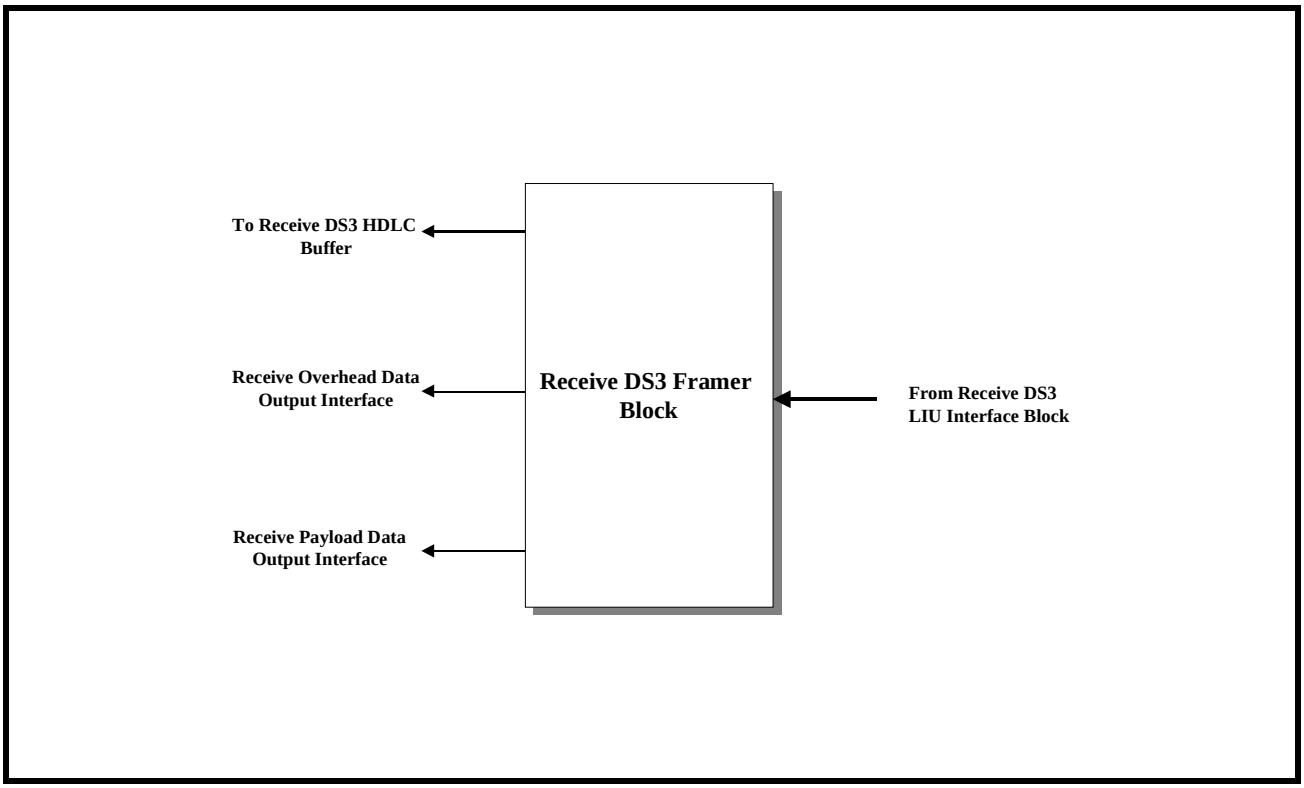
4.3.2 The Receive DS3 Framer Block

The Receive DS3 Framer block accepts decoded DS3 data from the "Receive DS3 LIU Interface" block, and routes data to the following destinations.

- The "Receive Payload Data Output Interface Block"
- The “Receive Overhead Data Output Interface" Block.
- The “Receive DS3 HDLC Controller” Block

Figure 99 presents a simple illustration of the "Receive DS3 Framer" block; along with the associated paths to the other functional blocks within the Framer chip.

FIGURE 99. A SIMPLE ILLUSTRATION OF THE RECEIVE DS3 FRAMER BLOCK AND THE ASSOCIATED PATHS TO THE OTHER FUNCTIONAL BLOCKS

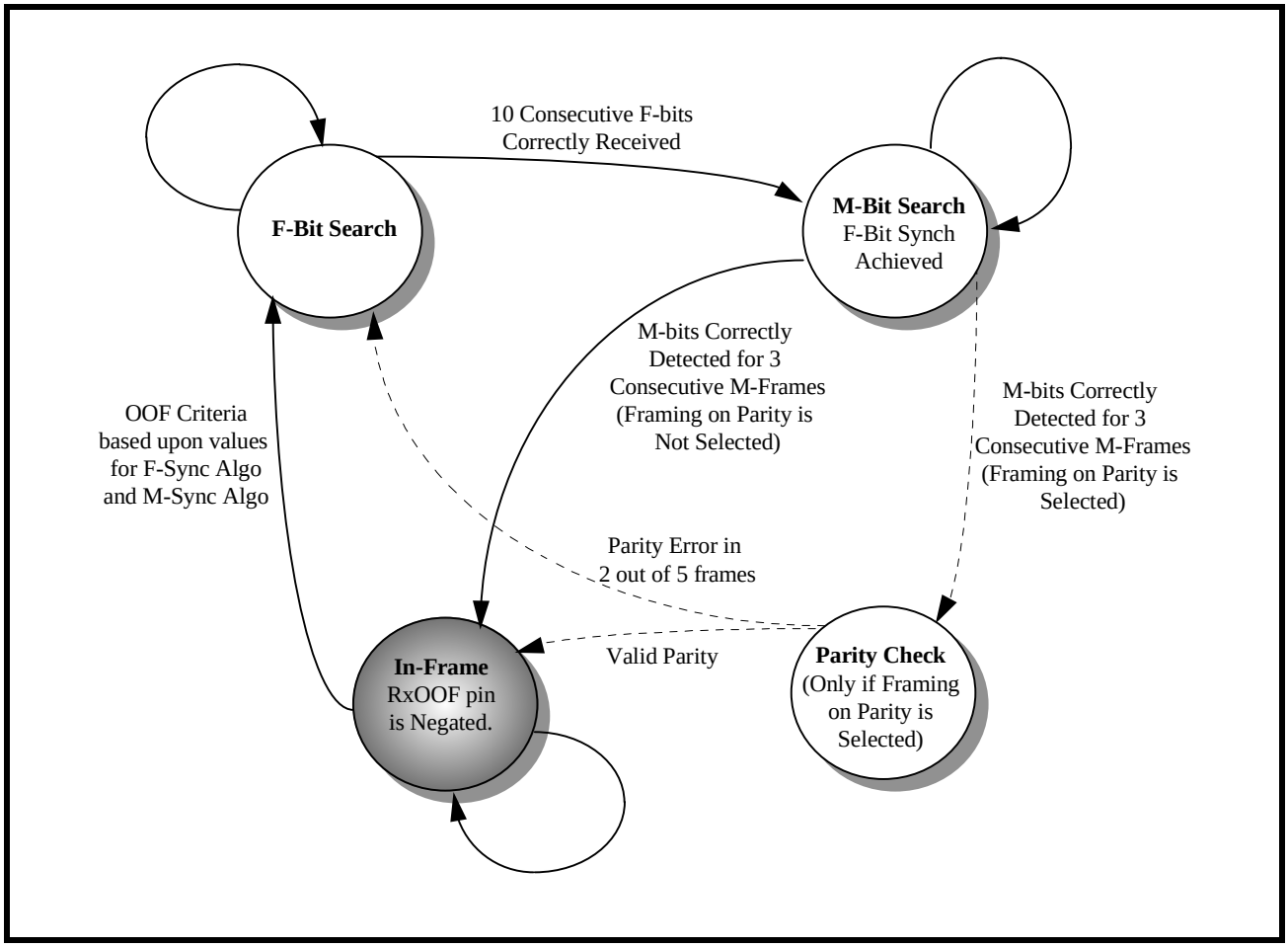


Once the B3ZS (or AMI) encoded data has been decoded into a binary data-stream, the "Receive DS3 Framer" block will use portions of this data-stream in order to synchronize itself to the "remote terminal equipment". At any given time, the "Receive DS3 Framer" block will be operating in one of two modes.

- **The Frame Acquisition Mode:** In this mode, the "Receive DS3 Framer" block is trying to acquire synchronization with the incoming DS3 frames, or
- **The Frame Maintenance Mode:** In this mode, the "Receive DS3 Framer" block is trying to maintain frame synchronization with the incoming DS3 Frames.

Figure 100 presents a State Machine diagram that depicts the "Receive DS3 Framer" block's "DS3 Frame Acquisition/Maintenance" Algorithm.

FIGURE 100. THE STATE MACHINE DIAGRAM FOR THE "RECEIVE DS3 FRAMER" BLOCK'S "FRAME ACQUISITION/ MAINTENANCE" ALGORITHM



4.3.2.1 Frame Acquisition Mode Operation

The "Receive DS3 Framer" block will be performing "Frame Acquisition" operation while it is operating in any of the following states (per the "DS3 Frame Acquisition/Maintenance" algorithm State Machine diagram, as depicted in Figure 100 .)

- The "F-bit Search" state
- The "M-bit Search" state
- The "P-Bit Check" state (optional)

Once the "Receive DS3 Framer" block enters the "In-Frame" state (per Figure 100), then it will begin "Frame Maintenance" operation.

When the "Receive DS3 Framer" block is in the "frame-acquisition" mode, it will begin to look for valid DS3 frames by first searching for the F-bits in the incoming DS3 data stream. At this "initial point" the "Receive DS3 Framer" block will be operating in the "F-Bit Search" state within the "DS3 Frame Acquisition/Maintenance" algorithm state machine diagram (see Figure 100). Recall from the discussion in Sec-

tion 4.1, that each DS3 F-frame consists of four (4) F-bits that occur in a repeating "1001" pattern. The "Receive DS3 Framer" block will attempt to locate this F-bit pattern by performing five (5) different searches in parallel. The F-bit search has been declared successful if at least 10 consecutive F-bits are detected. After the F-bit match has been declared, the "Receive DS3 Framer" block will then transition into the "M-Bit Search" state within the "DS3 Frame Acquisition/ Maintenance" algorithm (per Figure 100). When the "Receive DS3 Framer" block reaches this state, it will begin searching for valid M-bits. Recall from the discussion in Section 3.1 that each DS3 "M-frame" consists of three (3) M-bits that occur in a repeating "010" pattern. The "M-bit" search is declared successful if three consecutive "M-frames" (or 21 "F-frames") are detected correctly. Once this occurs an "M-frame lock" is declared, and the "Receive DS3 Framer" block will then transition to the "In-Frame" state. At this point, the "Receive DS3 Framer" block will declare itself in the "In-Frame" condition, and will begin "Frame Maintenance" operations. The "Receive DS3 Framer" block will then indicate that it has transitioned from the "OOF" condition into the "In-Frame" condition by doing the following.

- Generate a "Change in OOF Condition" interrupt to the local µP.
- Negate the RxOOF output pin (e.g., toggle it "low").
- Negate the "Rx OOF" bit-field (Bit 4) within the Receive DS3 Configuration and Status Register.

The user can configure the Receive DS3 Framer to operate such that 'valid parity' (P-bits) must also be detected before the Receive DS3 Framer can declare itself "In Frame". The user can set this configuration by writing the appropriate data to the "Rx DS3 Configuration and Status" Register, as depicted below.

RX DS3 CONFIGURATION AND STATUS REGISTER, (ADDRESS = 0X10)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Rx AIS	Rx LOS	Rx Idle	Rx OOF	Reserved	Framing on Parity	F-Sync Algo	M-Sync Algo
RO	RO	RO	RO	R/O	R/W	R/W	R/W
X	X	X	X	X	X	X	X

Table 31 relates the contents of this bit field to the framing acquisition criteria.

TABLE 31: THE RELATIONSHIP BETWEEN THE CONTENTS OF BIT 2 (FRAMING ON PARITY) WITHIN THE "RX DS3 CONFIGURATION AND STATUS" REGISTER, AND THE RESULTING "FRAMING ACQUISITION CRITERIA

FRAMING ON PARITY (BIT 2)	FRAMING ACQUISITION CRITERIA
0	The "In-frame" is declared after F-bit synchronization (10 F-bit matches) followed by M-bit synchronization (M-bit matches for 3 DS3 M-frames)
1	The "In-frame" condition is declared after F-bit synchronization, followed by M-bit synchronization, with valid parity over the frames. Also, the occurrence of parity errors in 2 or more out of 5 frames starts a frame search

Once the "Receive DS3 Framer" block is operating in the "In-Frame" condition, normal data recovery and processing of the DS3 data stream begins. The maximum average reframing time is less than 1.5 ms.

4.3.2.2 Frame Maintenance Mode Operation

When the "Receive DS3 Framer" block is operating in the "In-Frame" state (per Figure 100), it will then begin to perform "Frame Maintenance" operations; where it will continue to verify that the F- and M-bits are present, at their proper locations. While the "Receive DS3 Framer" block is operating in the "Frame Maintenance" mode, it will declare an "Out-of-Frame" (OOF) condition if 3 or 6 F-bits (depending upon user selection) out of 16 consecutive F-bits are in error. The user makes this selection for the "OOF Declaration" criteria by writing the appropriate value to bit 1 (F-Sync Algo) of the "Rx DS3 Configuration and Status" Register, as depicted below.

"RX DS3 CONFIGURATION AND STATUS" REGISTER, (ADDRESS = 0X10)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Rx AIS	Rx LOS	Rx Idle	Rx OOF	Reserved	Framing on Parity	F-Sync Algo	M-Sync Algo
RO	RO	RO	RO	R/W	R/W	R/W	R/W
X	X	X	X	X	X	X	X

Table 32 relates the contents of this bit-field to the "OOF Declaration" criteria

TABLE 32: THE RELATIONSHIP BETWEEN THE CONTENTS OF BIT 1 (F-SYNC ALGO) WITHIN THE RX DS3 CONFIGURATION AND STATUS REGISTER, AND THE RESULTING "F-BIT OOF DECLARATION CRITERIA" USED BY THE "RECEIVE DS3 FRAMER" BLOCK

F-SYNC ALGO (BIT 1)	OOF DECLARATION CRITERIA
0	"OOF" is declared when 6 out of 16 consecutive F-bits are in error.
1	"OOF" is declared when 3 out of 16 consecutive F-bits are in error.

NOTE: *Once the "Receive DS3 Framer" block has declared an "OOF" condition, it will transition back to the "F-Bit Search" state within the "DS3 Frame Acquisition/Maintenance" algorithm (per Figure 100).*

In addition to selecting an "OOF Declaration" criteria for the F-bits, the user has the following options for configuring the "OOF Declaration" criteria based upon M-bits.

1. M-bit errors do not cause a "OOF" Declaration, or
2. "OOF" will be declared if 3 out of 4 consecutive M-bits are in error.

The user will select between these two options by writing the appropriate value to Bit 0 (M-Sync Algo) within the "Receive DS3 Configuration and Status" Register; as depicted below.

RX DS3 CONFIGURATION AND STATUS REGISTER, (ADDRESS = 0X10)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Rx AIS	Rx LOS	Rx Idle	Rx OOF	Reserved	Framing on Parity	F-Sync Algo	M-Sync Algo
RO	RO	RO	RO	R/W	R/W	R/W	R/W
X	X	X	X	X	X	X	X

Table 33 relates the contents of this Bit Field to the "M-Bit Error" criteria for Declaration of OOF.

TABLE 33: THE RELATIONSHIP BETWEEN THE CONTENTS OF BIT 0 (M-SYNC ALGO) WITHIN THE "RX DS3 CONFIGURATION AND STATUS" REGISTER, AND THE RESULTING "M-BIT OOF DECLARATION CRITERIA" USED BY THE "RECEIVE DS3 FRAMER" BLOCK

MSYNC ALGO	OOF DECLARATION CRITERIA
0	M-Bit Errors do not result in the declaration of "OOF"
1	"OOF" is declared when 3 out of 4 M-bits are in error.

The "Framing on Parity" Criteria for OOF Declaration

Finally, the Framer IC offers the "Framing on Parity" option, which also effects the "OOF Declaration" criteria. As was mentioned earlier, the Framer IC allows the user to configure the "Receive DS3 Framer" block to detect 'valid-parity' before declaring itself "In-Frame". This same selection also configures the "Re-

ceive DS3 Framer" block to also declare an "OOF Condition" if a P-bit error is detected in 2 of the last 5 "M-frames".

Whenever the "Receive DS3 Framer" block declares "OOF" after being in the "In-Frame" State the following will happen.

- The Receive DS3 Framer will assert the "RxOOF" output pin (e.g., toggles it "high").
- Bit 4 (RxOOF) within the "Rx DS3 Configuration and Status" Register will be set to "1" as depicted below.

"Rx DS3 Configuration and Status" Register, (Address = 0x10)

RX DS3 CONFIGURATION AND STATUS REGISTER, (ADDRESS = 0X10)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Rx AIS	Rx LOS	Rx Idle	Rx OOF	Reserved	Framing on Parity	F-Sync Algo	M-Sync Algo
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
X	X	X	X	X	X	X	X

- The "Receive DS3 Framer" block will also issue a "Change in OOF Status" interrupt request, anytime there is a change in the "OOF" status.

4.3.2.3 Forcing a Reframe via Software Command

The Framer IC permits the user to force a reframe procedure of the "Receive DS3 Framer" block via software command. If the user writes a "1" into Bit 0 the “I/O Control” Register, as depicted below; then the Receive DS3 Framer will be forced into the "Frame Acquisition" Mode, (or more specifically, in the "F-Bit Search State" per Figure 100). Afterwards, the "Receive DS3 Framer" block will begin its search for valid F-Bits. The Framer IC will also respond to this command by asserting the "RxOOF" output pin, and generating a "Change in OOF Status" interrupt.

I/O CONTROL REGISTER (ADDRESS = 0X01)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Disable TxLOC	LOC	Disable RxLOC	AMI/ ZeroSup*	Unipolar/ Bipolar*	TxLine CLK Invert	RxLine CLK Invert	Reframe
R/W	RO	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	0	0	0	0

4.3.2.4 Performance Monitoring of the Receive DS3 Framer block

The user can monitor the number of framing bit errors (M and F bits) that have been detected by the "Receive DS3 Framer" block. This is accomplished by periodically reading the "PMON Framing Bit Error Count" Registers (Address = 0x52 and 0x53), as depicted below.

PMON FRAMING BIT ERROR EVENT COUNT REGISTER - MSB (ADDRESS = 0X52)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
F-Bit Error Count - High Byte							
RO	RO	RO	RO	RO	RO	RO	RO
1	0	1	0	0	0	0	0

PMON FRAMING BIT ERROR EVENT COUNT REGISTER - LSB (ADDRESS = 0X53)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
F-Bit Error Count - Low Byte							
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

When the µP/µC reads these registers, it will read in the number of framing bit errors that have been detected since the last read of these two registers. These registers are reset upon read.

4.3.2.5 DS3 Receive Alarms

The Receive DS3 Framer block is capable of detecting any of the following alarm conditions.

- LOS (Loss of Signal)
- AIS (Alarm Indication Signal)
- The "Idle Pattern".
- FERF (Far-End Receive Failure) of "Yellow Alarm" condition.
- FEBE (Far-End-Block Error)
- Change in AIC State

The methods by which the "Receive DS3 Framer" block uses to detect and declare each of these alarm conditions are described below.

4.3.2.5.1 The Loss of Signal (LOS) Alarm

The "Receive DS3 Framer" block will declare a "Loss of Signal" (LOS) state when it detects 180 consecutive incoming "0s" via the "RxPOS" and "RxNEG" input pins or if the "RLOS" input pin (from the XRT7300 DS3 LIU or the XRT7295 Line Receiver IC) is asserted (e.g., driven “high”). The "Receive DS3 Framer" block will indicate the occurrence of an LOS condition by:

1. Asserting the RxLOS output pin (e.g., toggles it "high").
2. Setting Bit 6 (RxLOS) within the "Rx DS3 Configuration and Status" Register to "1", as depicted below.

RX DS3 CONFIGURATION AND STATUS REGISTER, (ADDRESS = 0X10)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Rx AIS	Rx LOS	Rx Idle	Rx OOF	Int LOS Disable	Framing on Parity	F-Sync Algo	M-Sync Algo
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	1	0	1	x	x	x	x

3. The "Receive DS3 Framer" block will generate a "Change in LOS Status" interrupt request. (Note: The Receive DS3 Framer will also declare an "OOF" condition and perform all of the "notification procedures" as described in Section 3.3.2.2).
4. Force the "on-chip" Transmit Section to transmit a "FERF" (Far-End Receive Failure) indicator back out to the remote terminal.

The "Receive DS3 Framer" block will clear the "LOS" condition when at least 60 out of 180 consecutive received bits are "1".

NOTE: *The "Receive DS3 Framer" block will also generate the "Change in LOS Condition" interrupt, when it clears the LOS Condition.*

The Framer chip allows the user to modify the "LOS Declaration criteria" such that an LOS condition is declared only if the "RLOS" input pin (from the XRT7300 DS3/E3/STS-1 LIU IC) is asserted. In this case, the "internally-generated" LOS criteria of "180 consecutive 0s" will be disabled. The user can accomplish this by writing a "1" to bit 3 (Int LOS Disable) of the Rx DS3 Configuration and Status Register, as depicted below.

RX DS3 CONFIGURATION AND STATUS REGISTER, (ADDRESS = 0X10)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Rx AIS	Rx LOS	Rx Idle	Rx OOF	Int LOS Disable	Framing on Parity	F-Sync Algo	M-Sync Algo
RO	RO	RO	RO	R/W	R/W	R/W	R/W
X	X	X	X	1	X	X	X

NOTE: *For more information on the "RLOS" input pin, please see Section 2.1.*

4.3.2.5.2 The Alarm Indication Signal (AIS)

The "Receive DS3 Framer" block will identify and declare an "AIS" condition if it detects all of the following conditions in the incoming DS3 Data Stream:

- Valid M-bits, F-bits and P-bits
- All C-bits are zeros.
- X-bits are set to "1"
- The Payload portion of the DS3 Frame exhibits a repeating "1010..." pattern.

The "Receive DS3 Framer" block contains, within its circuitry, an "Up/Down" Counter that supports the "assertion" and "negation" of the AIS condition. This counter begins with the value of 0x00 upon power up or reset. The counter is then incremented anytime the "Receive DS3 Framer" block detects an "AIS Type" M-frame. This counter is then decremented, or kept at "zero" value, when the "Receive DS3 Framer" block detects a "non-AIS" type M-frame. The "Receive DS3 Framer" block will declare an "AIS Condition" if this counter reaches the value of 63 M-frames or greater. Explained another way, the AIS condition is declared if the number of "AIS-type" M-frames is detected, such that it meets the following conditions:

NAIS - NVALID $\geq$ 63

where:

NAIS = the number of M-frames containing the AIS pattern.

NVALID = the number of M-frames not containing the AIS pattern

If at anytime, the contents of this "Up/Down" counter exceeds 63 M-frames, then the "Receive DS3 Framer" block will:

1. Assert the "RxAIS" output pin by toggling it "high".
2. Set Bit 7 (Rx AIS) within the "Rx DS3 Configuration and Status" Register, to "1" as depicted below.

RX DS3 CONFIGURATION AND STATUS REGISTER, (ADDRESS = 0X10)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Rx AIS	Rx LOS	Rx Idle	Rx OOF	Int LOS Disable	Framing on Parity	F-Sync Algo	M-Sync Algo
1	X	X	X	X	X	X	X

3. Generate a "Change in AIS Status" Interrupt Request to the µP/µC.
4. Force the "Transmit Section" to transmit a "FERF" indication back to the remote terminal.

The "Receive DS3 Framer" block will clear the "AIS" condition when the following expression is true.

NAIS - NVALID $\leq$ 0.

In other words, once the "Receive DS3 Framer" block has detected a sufficient number of normal (or "Non-AIS") M-frames, such that this "Up/Down" counter reaches "zero", then the "Receive DS3 Framer" block will clear the "AIS Condition" indicators. The "Receive DS3 Framer" block will inform the µC/µP of this negation of the "AIS Status" by generating a "Change in AIS Status" interrupt.

4.3.2.5.3 The Idle (Condition) Alarm

The "Receive DS3 Framer" block will identify and declare an "Idle Condition" if it receives a sufficient number of "M-Frames" that meets all of the following conditions.

- Valid M-bits, F-bits, and P-bits
- The 3 CP-bits (in F-Frame #3) are zeros.
- The X-bits are set to "1"
- The payload portion of the DS3 Frame exhibits a repeating "1100..." pattern.

The "Receive DS3 Framer" block circuitry includes an "Up/Down" Counter that is used to track the number of "M-frames" that have been identified as exhibiting the "Idle Condition" by the "Receive DS3 Framer" block. The contents of this counter are set to zero upon reset or power up. This counter is then incremented whenever the "Receive DS3 Framer" block detects an "Idle-type" M-frame. The counter is decremented, or kept at zero if a "non-Idle" M-frame is detected. If the "Receive DS3 Framer" block detects a sufficient number of "Idle-type" M-frames, such that the counter reaches the number "63", then the "Receive DS3 Framer" block will declare the "Idle Condition". Explained another way, the "Receive DS3 Framer" block will declare an "Idle Condition" if the number of "Idle-Pattern" M-frames is detected such that it meets the following conditions.

NIDLE - NVALID ≥ 63,

where:

NIDLE = the number of M-frames containing the "Idle Pattern"

NVALID = the number of M-frames not exhibit the "Idle Pattern"

Anytime the contents of this "Up/Down" Counter reaches the number 63, then the "Receive DS3 Framer" block will:

1. Set Bit 5 (Rx Idle) within the "Rx DS3 Configuration and Status" Register, to "1" as depicted below.

RX DS3 CONFIGURATION AND STATUS REGISTER, (ADDRESS = 0X10)

RX DS3 CONFIGURATION AND STATUS REGISTER, (ADDRESS = 0X10)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Rx AIS	Rx LOS	Rx Idle	Rx OOF	Int LOS Disable	Framing on Parity	F-Sync Algo	M-Sync Algo
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
X	X	1	X	X	X	X	X

2. Generate a "Change in Idle Status" Interrupt Request to the local µP/µC.

The "Receive DS3 Framer" block will clear the "Idle Condition" if it has detected a sufficient number of "Non-Idle" M-frames, such that this "Up/Down" Counter reaches the value "0".

4.3.2.5.4 The Detection of (FERF) or "Yellow Alarm" Condition

The "Receive DS3 Framer" block will identify and declare a "Yellow Alarm" condition or a "Far-End Receive Failure" (FERF) condition, if it starts to receive DS3 frames with both of its X-bits set to "0".

When the "Receive DS3 Framer" block detects a "FERF" condition in the incoming DS3 frames, then it will then do the following.

1. It will assert the "RxFERF" (bit-field 4) within the Rx DS3 Status Register, as depicted below.

RX DS3 STATUS REGISTER (ADDRESS = 0X11)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Not Used			Rx FERF	RxAIC	RxFEBE [2]	RxFEBE [1]	RxFEBE [0]
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	1	X	X	X	X

This bit-field will remain asserted for the duration that the "Yellow Alarm" condition exists.

2. The "Receive DS3 Framer" block will also generate a "Change in FERF Status" interrupt to the µP/µC. Consequently, the "Receive DS3 Framer" block will also assert the "FERF Interrupt Status" bit, within the Rx DS3 Interrupt Status Register, as depicted below.

RX DS3 INTERRUPT STATUS REGISTER (ADDRESS = 0X13)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Cp Bit Error Interrupt Status	LOS Interrupt Status	AIS Interrupt Status	IDLE Interrupt Status	FERF Interrupt Status	AIC Interrupt Status	OOF Interrupt Status	P-Bit Interrupt Status
RO	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	X	X	X	1	X	X	X

The Receive DS3 Framer block will clear the "FERF" condition, when it starts to receive Receive DS3 Frames that have its "X" bits set to "1".

NOTE: *The "FERF" indicator is frequently referred to as the "Yellow Alarm".*

4.3.2.5.5 The Detection of the FEBE Events

As described in Section 3.2.4.2.1.9, a given Terminal Equipment will set the three FEBE (Far-End Block Error) bit-fields to the value [1, 1, 1] (e.g., all of the FEBE bits are set to “1”) within the “outbound” DS3 frames; if all of the following conditions are true about the “incoming” DS3 line signal.

- The Receive Circuitry (within the Terminal Equipment) detects no P-Bit Errors.
- The Receive Circuitry (within the Terminal Equipment) detects no CP-Bit Errors.

If the Receive Section of the Terminal Equipment detects any P or CP bit errors, then the Transmit Section of the Terminal Equipment will set the three FEBE bits (within the “outbound” DS3 data stream) to a value other than [1, 1, 1].

How does the Receive DS3 Framer block (within the XRT72L13) respond when it receives a DS3 frame with all three (3) of its FEBE bit-fields set to “1”?

As mentioned above, the Terminal Equipment will transmit DS3 frames, with the FEBE bits set to [1, 1, 1], during un-erred conditions. Hence, if the “Receive DS3 Framer” block (within the XRT72L13 Framer IC) receives DS3 frames with the FEBE bits set to [1, 1, 1] it will interpret this event as an un-erred event, and will continue normal operation.

However, if the Receive DS3 Framer block receives a DS3 frame with the FEBE bits set to a value other than [1, 1, 1]; then it will increment the “PMON FEBE Event Count Registers” (which are located at address locations 0x58 and 0x59 within the Framer Address space).

4.3.2.5.6 Detection of Change in the AIC State

Section 3.1 indicates that the “AIC” (Application Identification Channel) bit-field is the third overhead bit, within F-Frame # 1. This particular bit-field is set to “1” for the “C-Bit Parity” Framing Format, and is set to “0” for the M13 Framing Format.

Hence, a given Terminal Equipment receiving a DS3 data stream can identify the framing format of this DS3 data stream, by reading the value fo the “AIC” bit-field. The “Receive DS3 Framer” block permits the user’s Microcontroller/MIcroprocessor” to determine the state of the “AIC” bit-field (within the “incoming” DS3 data stream) by writing the value of the “AIC” bit-field, within the most recently received DS3 frame, into bit 3 (RxAIC) within the “Rx DS3 Status Register (Address = 0x11); as illustrated below.

RXDS3 STATUS REGISTER (ADDRESS = 0X11)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved			RxFERF	RxAIC	RxFEBE[2:0]		
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

The Receive DS3 Framer block will also generate an interrupt if it detects a change of state in the AIC bit-field (within the incoming DS3 data stream). If this occurs, then the Receive DS3 Framer block will set

Bit 2 (AIC Interrupt Status) within the “Rx DS3 Interrupt Stauts Register (Address = 0x13) to “1” as illustrated below.r

RXDS3 INTERRUPT STATUS REGISTER (ADDRESS = 0X13)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CP-Bit Error Interrupt Status	LOS Interrupt Status	AIS Interrupt Status	Idle Interrupt Status	FERF Interrupt Status	AIC Interrupt Status	OOF Interrupt Status	P-Bit Error Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	1	0	0

4.3.2.6 Performance Monitoring of the DS3 Transport Medium

The DS3 Frame consists of some overhead bits that are used to support performance monitoring of the DS3 Transmission Link. These bits are the P-Bits and the CP-Bits.

4.3.2.6.1 P-Bit Checking/Options

The "remote" Transmit DS3 Framer will compute the even parity of the payload portion of an “outbound” DS3 Frame and will place the resulting parity bit value in the 2 P-bit-fields within the very next "outbound" DS3 Frame. The value of these two bits fields is expected to be the identical.

The "Receive DS3 Framer" block, while receiving each of these DS3 Frames (from the "remote" Transmit DS3 Framer), will compute the even-parity of the payload portion of the frame. The "Receive DS3 Framer" block will then compare this "locally computed" parity value to that of the P-bit fields within the very next DS3 Frame. If the "Receive DS3 Framer" block detects a parity error, then two things will happen:

1. The "Receive DS3 Framer" block will inform the µP/µC of this occurrence by generating a "Detection of P-Bit Error" interrupt;
2. The "Receive DS3 Framer" block will alter the value of the "FEBE" bits, (to a pattern other than "111") that the "Near-End" Transmit DS3 Framer will be transmitting back to the "remote" Terminal.
3. The XRT72L13 Framer IC will increment the "PMON Parity Error Event Count" Registers (Address = 0x54 and 0x55) for each detected parity error, in the incoming DS3 data stream. The bit-format of these two registers follows.

PMON PARITY ERROR EVENT COUNT REGISTER - MSB (ADDRESS = 0X54)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Parity Error Count - High Byte							
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

PMON PARITY ERROR EVENT COUNT REGISTER - LSB (ADDRESS = 0X55)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Parity Error Count - Low Byte							
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

When the µP reads these registers, it will read in the number of parity-bit errors that have been detected by the "Receive DS3 Framer" block, since the last time these registers were read. These registers are "reset upon read".

NOTE: *When the "Framing with Parity" option is selected, the "Receive DS3 Framer" block will declared an "OOF" condition if P-bit errors were detected in two out of 5 consecutive DS3 "M-frames".*

3.3.2.6.2 CP-Bit Checking/Options

CP-bits are very similar to P-bits except for the following.

1. CP-bits are used to permit performance monitoring over an entire DS3 path (e.g., from the "source" terminal); through any number of "mid-network" terminals to the "sink" terminal).
2. P-bits are used to permit performance monitoring of a DS3 data stream, as it is transmitted from one terminal to an adjacent terminal.

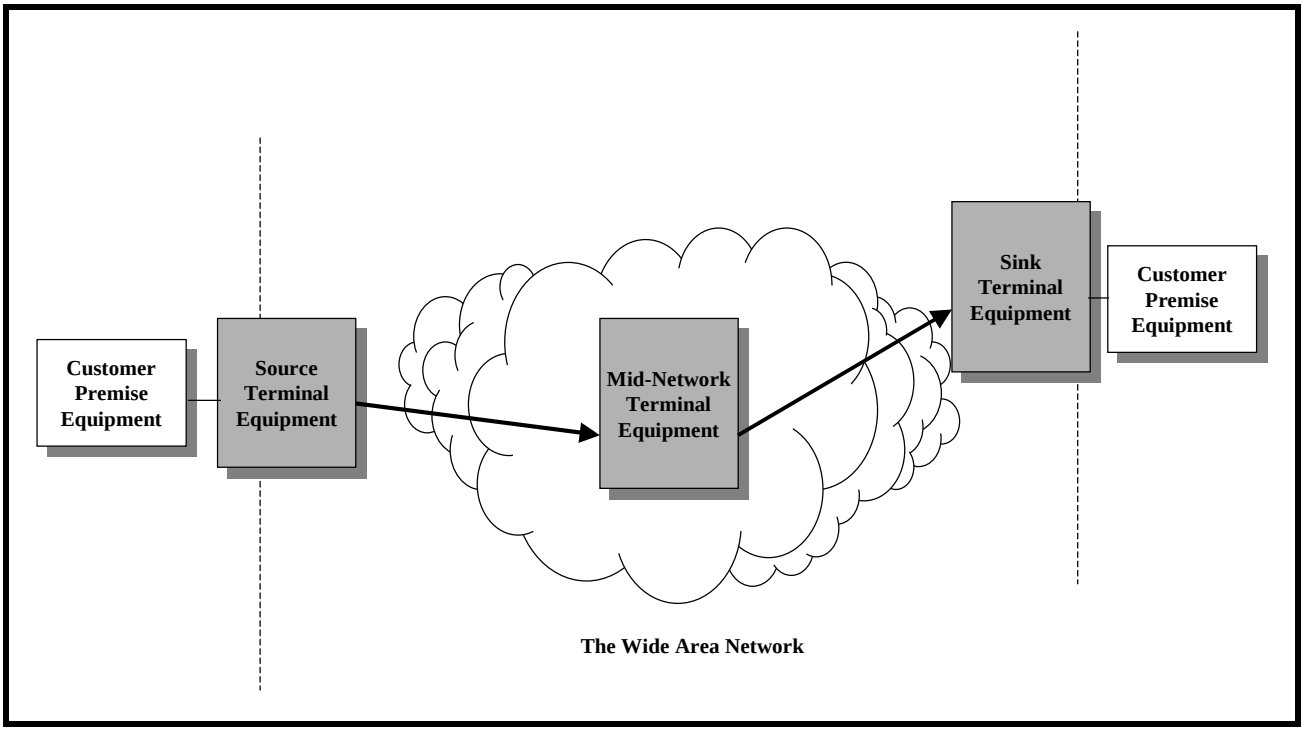
How CP-Bits are Processed

The following section describes how the CP-bits are processed at three locations.

- The "Source" Terminal Equipment
- The "Mid-Network" Terminal Equipment
- The "Sink" Terminal Equipment

Figure_62 presents a simple illustration of the locations of these three types of Terminal Equipment, within the Wide-Area Network.

FIGURE 101. A SIMPLE ILLUSTRATION OF THE LOCATIONS OF THE "SOURCE", "MID-NETWORK" AND "SINK" TERMINAL EQUIPMENT (FOR CP-BIT PROCESSING)



NOTE: *The user of the terms "Source" and "Sink" Terminal Equipment are used to simplify this discussion of CP-Bit Processing. In reality, the "Source" Terminal Equipment (in Figure_62) will also function as the "Sink" Terminal Equipment (for DS3 traffic traveling in the opposite direction). Likewise, the "Sink" Terminal Equipment (in Figure_62) will also function as the "Source" Terminal Equipment.*

Processing at the "Source" Terminal Equipment

The "Source" Terminal Equipment (located at one edge of the wide-area network) will typically receive its DS3 payload data from some Customer Premise Equipment (CPE). As the "Source" Terminal Equipment receives this data from the CPE, it will compute the even-parity value over all bits within a given "outbound" DS3 frame. The Terminal Equipment will then insert this even parity value into both of the P-bit fields and both the CP-bits fields, within the very next "outbound" DS3 frame.

Hence, both the P-bit values and CP-bit values will originate at the "Source" Terminal Equipment.

Processing at the "Mid-Network" Terminal Equipment

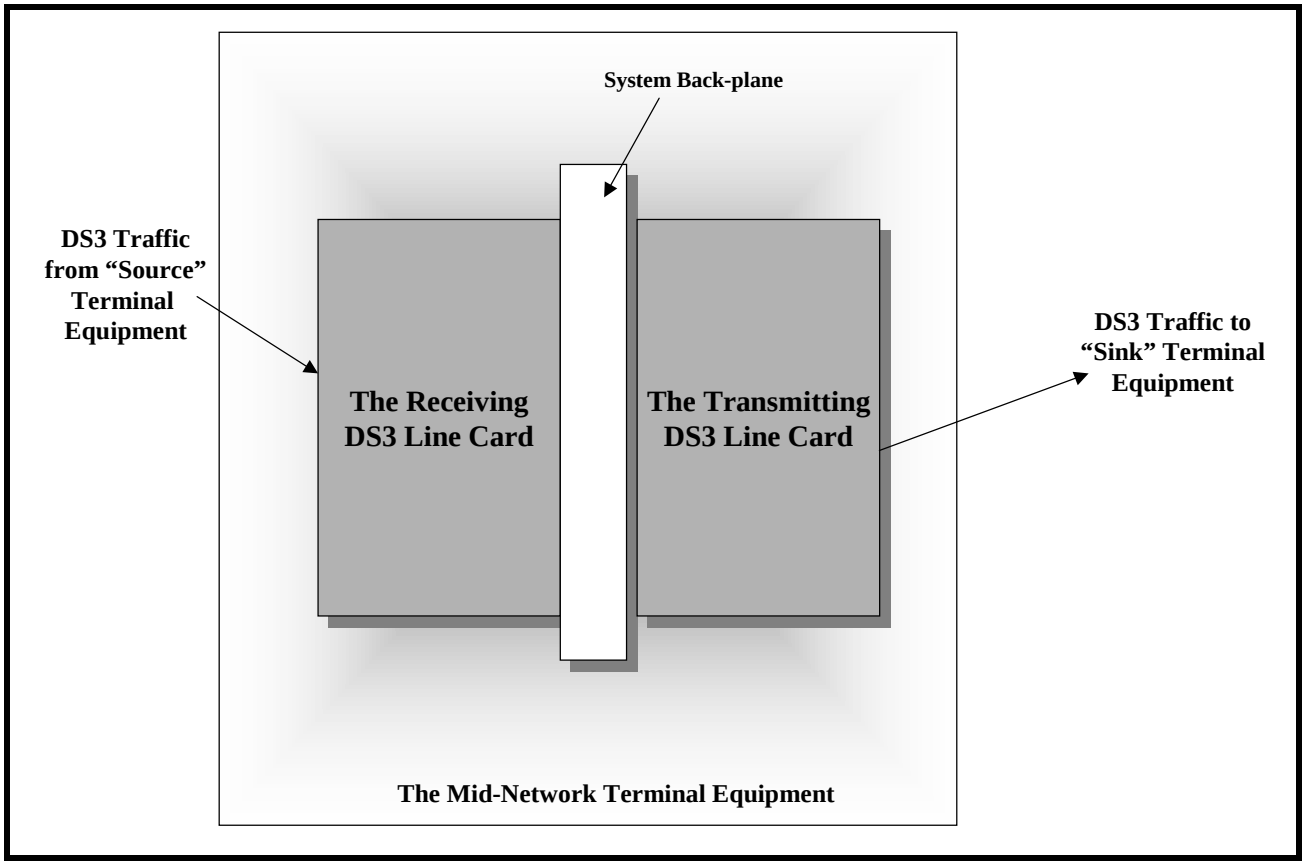
The "Mid-Network" Terminal Equipment has the task of doing the following.

- Receiving a DS3 data stream, via the "Receive WAN Interface" Line Card.

- Transmitting this same DS3 data stream (out to another Remote Terminal Equipment) via the "Transmit WAN Interface" Line Card.

Figure 102 presents an illustration of the basic architecture of the "Mid-Network" Terminal Equipment.

FIGURE 102. ILLUSTRATION OF THE "PRESUMED CONFIGURATION" OF THE MID-NETWORK TERMINAL EQUIPMENT



Operation of the "Receive WAN Interface" Card

The "Receive WAN Interface" card receives a DS3 data stream from some remote Terminal Equipment. As the "Receive WAN Interface" card does this, it will also do the following:

1. Compute and verify the "P-Bits" of each "inbound" DS3 frame.
2. Compute and verify the "CP-Bits" of each "inbound" DS3 frame.
3. Output both the "payload" and "overhead" bits to the system back-plane.

Operation of the "Transmit WAN Interface" Card

The "Transmit WAN Interface" Line Card receives the "outbound" DS3 data stream from the system back-plane. As the "Transmit WAN Interface" receives this data it will also do the following.

1. Extract out the "CP-bit" values, from the "Receive WAN Interface" line card (via the system back-plane) and insert these values into the CP-bit fields, within the "outbound" DS3 data stream; via the "Transmit Overhead Data Input Interface" block of the XRT72L13 Framer IC.
2. Compute the even-parity over all bits, within a given "outbound" DS3 frame, and insert this value into the "P" bits within the very next "outbound" DS3 frame.
3. Transmit this resulting DS3 data stream to the remote terminal equipment.

Processing at the "Sink" Terminal

The "Sink" Terminal Equipment (located at the opposite edge of the wide-area-network, from the "Source" Terminal Equipment) will receive and terminate this DS3 data stream. As the "Sink" Terminal Equipment receives this DS3 data stream; it will also do the following.

1. Compute and verify the "P"-bits within each "inbound" DS3 frame.
2. Compute and verify the "CP" bits within each "inbound" DS3 frame.

4.3.3 The Receive HDLC Controller Block

The Receive DS3 HDLC Controller block can be used to receive either "bit-oriented signaling" (BOS) or "message-oriented signaling" (MOS) type data link messages. The Receive DS3 HDLC Controller block can also be configured to receive both types of message from the remote terminal equipment.

Both "BOS" and "MOS" types of HDLC message processing are discussed in detail below.

4.3.3.1 Bit-Oriented Signaling (or FEAC) Processing via the Receive DS3 HDLC Controller.

The "Receive DS3 HDLC Controller" block consists of two major "sub-blocks"

- The "Receive FEAC" Processor
- The "LAPD Receiver"

This section describes how to operate the "Receive FEAC Processor".

If the "Receive DS3 Framer" block is operating in the "C-bit Parity" Framing format, then the FEAC bit-field within the DS3 Frame can be used to receive FEAC (Far End Alarm and Control) messages (See Figure 103). Each FEAC code word is actually six bits in length. However, this six bit FEAC Code word is encapsulated with 10 framing bits to form a 16 bit message of the form:

	FEAC Code Word						Framing								
0	d5	d4	d3	d2	d1	d0	0	1	1	1	1	1	1	1	1

Where, "[d5, d4, d3, d2, d1, d0]" is the FEAC Code word. The rightmost bit of the 16-bit data structure (e.g., a "1") will be received first. Since each DS3 Frame contains only 1 FEAC bit-field, 16 DS3 Frames are required to transmit the 16 bit FEAC code message. The six bits, labeled "d5" through "d0"" can represent 64 distinct messages, of which 43 have been defined in the standards.

The Receive FEAC Processor frames and "validates" the incoming FEAC data from the "remote" Transmit FEAC Processor via the received FEAC channel. Additionally, the Receive FEAC Processor will write the "Received FEAC code words" into an 8 bit "Rx-FEAC" register. Framing is performed by looking for two "0s" spaced 6 bits apart preceded by 8 "1s". The Receive DS3 HDLC Controller contains two registers that support FEAC Message Reception.

- Rx DS3 FEAC Register (Address = 0x16)
- Rx DS3 FEAC Interrupt Enable/Status Register (Address = 0x17)

The Receive FEAC Processor generates an interrupt upon "validation" and "removal" of the incoming FEAC Code words.

Operation of the Receive DS3 FEAC Processor

The Receive FEAC Processor will "validate" or "remove" FEAC code words; that it receives from the "remote" Transmit FEAC Processor. The "FEAC Code Validation" and "Removal" functions are described below.

FEAC Code Validation

When the remote terminal equipment wishes to send a FEAC message to the "Local" Receive FEAC Processor, it (the remote terminal equipment) will transmit this 16 bit message, repeatedly for a total of 10 times. The Receive FEAC Processor will frame to this incoming FEAC Code Message, and will attempt to "validate" this message. Once the Receive FEAC Processor has received the same FEAC code word in at least 8 out of the last 10 received codes, it will "validate" this code word by writing this 6 bit code word into the "Receive DS3 FEAC" Register. The Receive FEAC Processor will then inform the µC/µP of this "Receive FEAC validation" event by generating a "Rx FEAC Valid" interrupt and asserting the "FEAC Valid" and the Rx FEAC Valid Interrupt Status Bits in the Rx DS3 Interrupt Enable/Status Register, as depicted below. The Bit Format of the Rx DS3 FEAC Register is presented below.

RX DS3 FEAC INTERRUPT ENABLE/STATUS REGISTER (ADDRESS = 0X17)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit2	Bit 1	Bit 0
Not Used	Not Used	Not Used	FEAC Valid	RxFEAC Remove Interrupt Enable	RxFEAC Remove Interrupt status	RxFEAC Valid Interrupt Enable	RxFEAC Valid Interrupt Status
RO	RO	RO	RO	R/W	RUR	R/W	RUR
X	X	X	1	X	0	1	1

The bit-format of the "Rx DS3 FEAC" register is presented below. It is important to note that the "last validated" FEAC code word will be written into the "shaded" bit-fields below.

RX DS3 FEAC REGISTER (ADDRESS = 0X16)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Not Used	RxFEAC [5]	RxFEAC [4]	RxFEAC [3]	RxFEAC [2]	RxFEAC [1]	RxFEAC [0]	Not Used
RO	RO	RO	RO	RO	RO	RO	RO
0	d5	d4	d3	d2	d1	d0	0

The purpose of generating an interrupt to the µP, upon "FEAC Code Word Validation" is to inform the local µP that the Framer has a "newly received" FEAC message that needs to be read. The local µP would read-in this FEAC code word from the Rx DS3 FEAC Register (Address = 0x16).

FEAC Code Removal

After the 10th transmission of a given FEAC code word, the remote terminal equipment may proceed to transmit a different FEAC code word. When the Receive FEAC processor detects this occurrence, it must "Remove" the FEAC codeword that is presently residing in the "Rx DS3 FEAC" Register. The Receive FEAC Processor will "remove" the existing FEAC code word when it detects that 3 (or more) out of the last 10 received FEAC codes are different from the latest "validated" FEAC code word. The Receive FEAC Processor will inform the local µP/µC of this "removal" event by generating a "Rx FEAC Removal" interrupt, and asserting the "RxFEAC Remove Interrupt Status" bit in the Rx DS3 Interrupt Enable/Status Register, as depicted below.

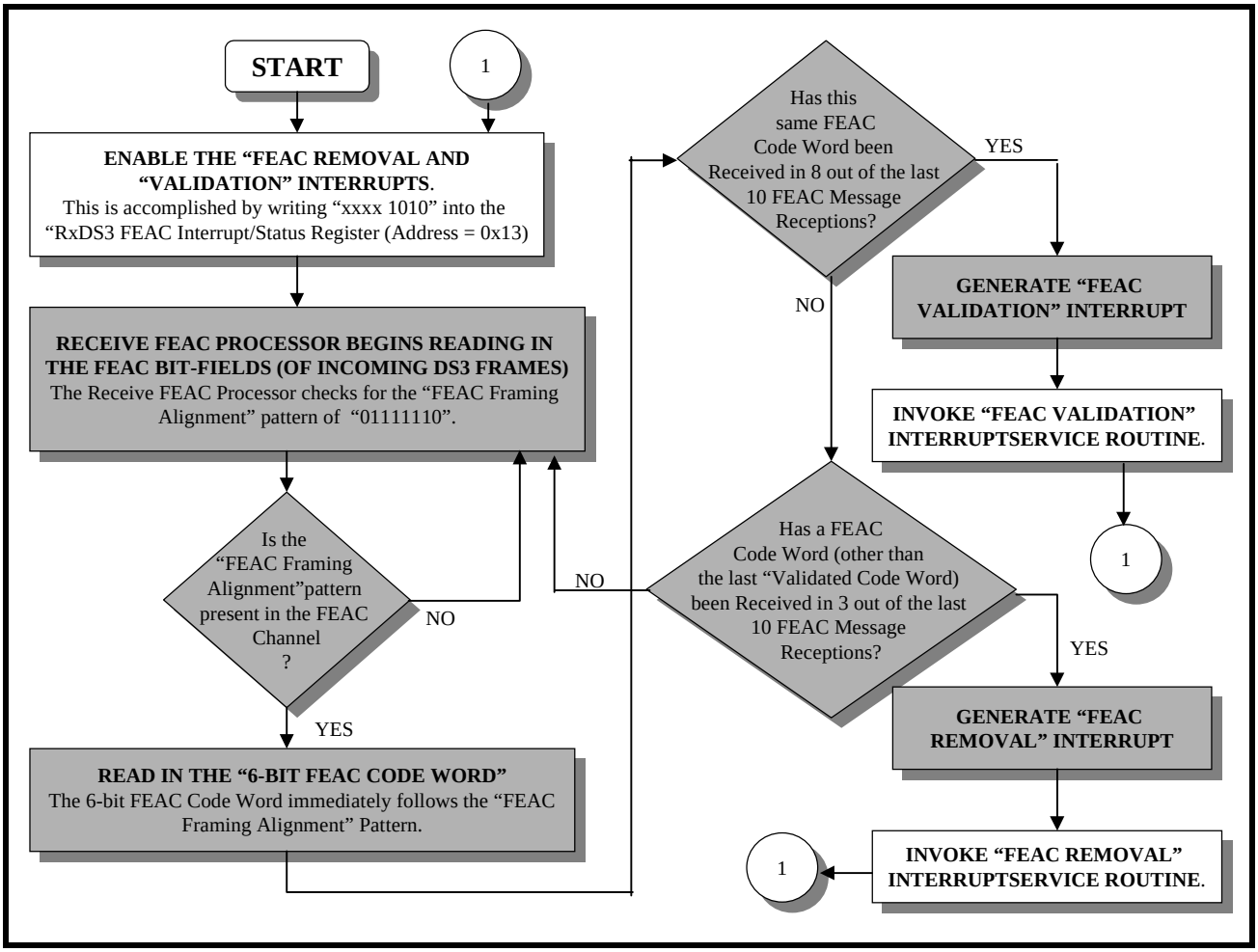
RX DS3 FEAC INTERRUPT ENABLE/STATUS REGISTER (ADDRESS = 0X17)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Not Used	Not Used	Not Used	FEAC Valid	RxFEAC Remove Interrupt Enable	RxFEAC Remove Interrupt status	RxFEAC Valid Interrupt Enable	RxFEAC Valid Interrupt Status
RO	RO	RO	RO	R/W	RUR	R/W	RUR
X	X	X	0	1	1	X	0

Additionally, the Receive FEAC processor will also denote the "removal" event by setting the "FEAC Valid" bit-field (Bit 4), within the "Rx DS3 FEAC Interrupt Enable/Status" Register to "0", as depicted above.

The description of Bits 0 through 3 within this register, all support Interrupt Processing, and will therefore be presented in Section 3.3.6. Figure 103 presents a flow diagram depicting how the Receive FEAC Processor functions.

FIGURE 103. FLOW DIAGRAM DEPICTING HOW THE RECEIVE FEAC PROCESSOR FUNCTIONS



NOTES:

1. *The "white" (e.g., unshaded) boxes reflect tasks that the user's system must perform in order to configure the "Receive FEAC Processor" to receive FEAC messages.*
2. *A brief description of the steps that must exist within the "FEAC Validation" and "FEAC Removal" Interrupt Service Routines exists in Section 3.6*

4.3.3.2 The Message Oriented Signaling (e.g., LAP-D) Processing via the "Receive DS3 HDLC Controller" block

The LAPD Receiver (within the "Receive DS3 HDLC Controller" block) allows the user to receive PMDL messages from the remote terminal equipment, via the "inbound" DS3 frames. In this case, the "inbound" message bits will be carried by the 3 "DL" bit-fields of F-Frame 5, within each DS3 "M-Frame". The remote LAPD Transmitter will transmit a LAPD Message to the "Near-End" Receiver via these three bits within each DS3 Frame. The LAPD Receiver will receive and store the information portion of the received LAPD frame into the "Receive LAPD Message" Buffer, which is located at addresses: 0xDE through 0x135 within the on-chip RAM. The LAPD Receiver has the following responsibilities.

- Framing to the incoming LAPD Messages
- Filtering out stuffed "0s" (within the information payload)
- Storing the Frame Message into the "Receive LAPD Message" Buffer
- Perform Frame Check Sequence (FCS) Verification
- Provide status indicators for
  - End of Message (EOM)
  - Flag Sequence Byte detected
  - Abort Sequence detected
  - Message Type
  - C/R Type
  - The occurrence of FCS Errors

The LAPD receiver's actions are facilitated via the following two registers.

- Rx DS3 LAPD Control Register
- Rx DS3 LAPD Status Register

Operation of the LAPD Receiver

The LAPD Receiver, once enabled, will begin searching for the boundaries of the incoming LAPD message. The LAPD Message Frame boundaries are delineated via the "Flag Sequence" octets (0x7E), as depicted in Figure 104 .

FIGURE 104. LAPD MESSAGE FRAME FORMAT

Flag Sequence (8 bits)		
SAPI (6-bits)	C/R	EA
TEI (7 bits)		EA
Control (8-bits)		
76 or 82 Bytes of Information (Payload)		
FCS - MSB		
FCS - LSB		
Flag Sequence (8-bits)		

Where: Flag Sequence = 0x7E

SAPI + CR + EA = 0x3C or 0x3E

TEI + EA = 0x01

Control = 0x03

The 16 bit FCS is calculated using CRC-16, x16 + x12 + x5 + 1

The microprocessor/microcontroller (at the remote terminal), while assembling the LAPD Message frame, will insert an additional byte at the beginning of the information (payload) field. This first byte of the information field indicates the type and size of the message being transferred. The value of this information field and the corresponding message type/size follow:

CL Path Identification = 0x38 (76 bytes)

IDLE Signal Identification = 0x34 (76 bytes)

Test Signal Identification = 0x32 (76 bytes)

ITU-T Path Identification = 0x3F (82 bytes)

The LAPD Receiver must be enabled before it can begin receiving any LAPD messages. The LAPD Receiver can be enabled by writing a "1" into Bit 2 (RxLAPD Enable) within the "Rx DS3 LAPD Control" Register. The bit format of this register is depicted below.

RX DS3 LAPD CONTROL REGISTER (ADDRESS = 0X18)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Not Used	Not Used	Not Used	Not Used	Not Used	RxLAPD Enable	RxLAPD Interrupt Enable	RxLAPD Interrupt Status
RO	RO	RO	RO	RO	R/W	R/W	RUR
0	0	0	0	0	1	X	X

Once the LAPD Receiver has been enabled, it will begin searching for the Flag Sequence octets (0x7E), in the "DL" bit-fields, within the incoming DS3 frames. When the LAPD Receiver finds the flag sequence byte, it will assert the "Flag Present" bit (Bit 0) within the "Rx DS3 LAPD Status" Register, as depicted below.

RX DS3 LAPD STATUS REGISTER (ADDRESS = 0X19)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT 1	BIT 0
Not Used	RxAbort	RxLAPD Type[1, 0]		RxCR Type	RxFCS Error	End of Message	Flag Present
X	X	X	X	X	X	X	1

The receipt of the Flag Sequence octet can mean one of two things.

1. The Flag Sequence byte marks the beginning or end of an incoming LAPD Message.
2. The received Flag Sequence octet could be just one of many Flag Sequence octets that are transmitted via the DS3 Transport Medium, during idle periods between the transmission of LAPD Messages.

The LAPD Receiver will clear the "Flag Present" bit as soon as it has received an octet that is something other than the "Flag Sequence" octet. At this point, the LAPD Receiver should be receiving either octet #2 of the incoming LAPD Message, or an Abort Sequence (e.g., a string of seven or more consecutive "1s"). If this next set of data is an abort sequence, then the LAPD Receiver will assert the RxAbort bit (Bit 6) within the "Rx DS3 LAPD Status" Register. However, if this next octet is Octet #2 of an incoming LAPD Message, then the "Rx DS3 LAPD Status" Register will begin to present some additional status information on this incoming message. Each of these indicators is presented below in sequential order.

Bit 3 - RxCR Type - C/R (Command/Response) Type

This bit-field reflects the contents of the C/R bit-field within octet #2 of the LAPD Frame Header. When this bit is "0" it means that this message is originating from a customer installation. When this bit is "1" it means that this message is originating from a network terminal.

Bit 4,5 - RxLAPD Type[1, 0] - LAPD Message Type

The combination of these two bit fields indicate the Message Type and the Message Size of the incoming LAPD Message frame. Table 34 relates the values of Bits 4 and 5 to the Incoming LAPD Message Type/Size.

TABLE 34: THE RELATIONSHIP BETWEEN RXLAPDTYPE[1:0] AND THE RESULTING LAPD MESSAGE TYPE AND SIZE

RXLAPD TYPE[1, 0]	MESSAGE TYPE	MESSAGE SIZE
00	Test Signal Identification	76 bytes
01	Idle Signal Identification	76 bytes
10	CL Path Identification	76 bytes
11	TU-T Path Identification	82 bytes

NOTE: *The Message Size pertains to the size of the "Information portion" of the LAPD Message Frame (as presented in Figure 104).*

Bit 3 - Flag Present

The LAPD Receiver should receive another "Flag Sequence" octet, which marks the End of the Message. Therefore, this bit field should be asserted once again.

Bit 1 - EndOfMessage - End of LAPD Message Frame

Upon receipt of the closing "Flag Sequence" octet, this bit-field should be asserted. The assertion of this bit-field indicates that a LAPD Message Frame has been completely received. Additionally, if this newly received LAPD Message is different from the previous message, then the LAPD Receiver will inform the µC/µP of the "EndOfMessage" event by generating an interrupt.

Bit 2 - RxFCSErr - Frame Check Sequence Error Indicator

The LAPD Receiver will take the incoming LAPD Message and compute its own version of the Frame Check Sequence (FCS) word. Afterwards, the LAPD Receiver will compare its computed value with that it has received from the remote LAPD Transmitter. If these two values match, then the LAPD Receiver will presume that the LAPD Message has been properly received; and the contents of the Received LAPD Message (payload portion) will be retained at locations 0xDE through 0x135 in on-chip RAM. The

LAPD Receiver will indicate an "error-free" reception of the LAPD Message by keeping this bit field negated (Bit 2 = 0). However, if these two FCS values do not match, then the received LAPD Message is corrupted; and the user is advised not to process this erroneous information. The LAPD Receiver will indicate an erred receipt of this message by setting this bit-field to "1".

NOTE: *The Receive DS3 HDLC Controller block will not generate an interrupt to the µP due to the detection of an FCS error. Therefore, the user is advised to "validate" each and every received LAPD message by checking this bit-field prior to processing the LAPD message.*

Removal of Stuff Bits from the Payload Portion of the incoming LAPD Message

While the LAPD Receiver is receiving a LAPD Message, it has the responsibility of removing all of the "0" stuff bits from the Payload Portion of the incoming LAPD Message Frame. Recall that the text in Section 3.2.3.2 indicated that the LAPD Transmitter (at the remote terminal) will insert a "0" immediately following a string of 5 consecutive "1s" within the payload portion of the LAPD Message frame. The LAPD Transmitter performs this bit-stuffing procedure in order to prevent the user data from mimicking the Flag Sequence octet (0x7E) or the ABORT sequence. Therefore, in order to recover the user data to its original content (prior to the bit-stuffing), the LAPD Receiver will remove the "0" that immediately follows a string of 5 consecutive "1s".

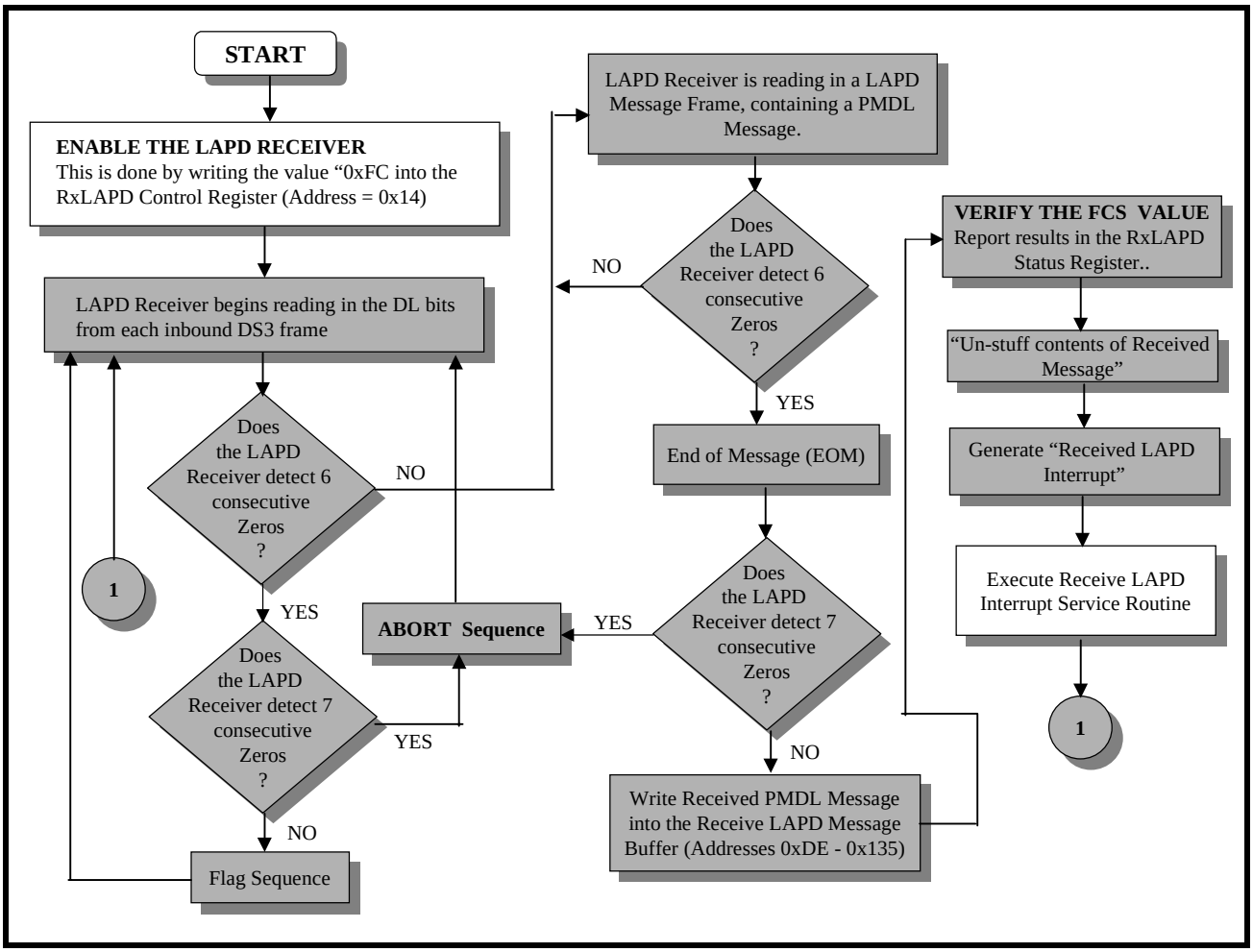
Writing the Incoming LAPD Message into the "Receive LAPD Message" Buffer

The LAPD receiver will obtain the LAPD Message frame from the incoming DS3 data-stream. In addition to processing the framing overhead octets, performing error checking (via FCS) and removing the stuffed "0s" from the user payload data. The LAPD Receiver will also write the payload portion of the LAPD Frame into the "Receive LAPD Message" buffer at locations 0xDE through 0x135 in on-chip RAM.

Therefore, the local µP/µC must read this location when it wishes to process this newly received LAPD Message.

Figure 105 presents a flow chart depicting how the LAPD Receiver works.

FIGURE 105. FLOW CHART DEPICTING THE FUNCTIONALITY OF THE LAPD RECEIVER



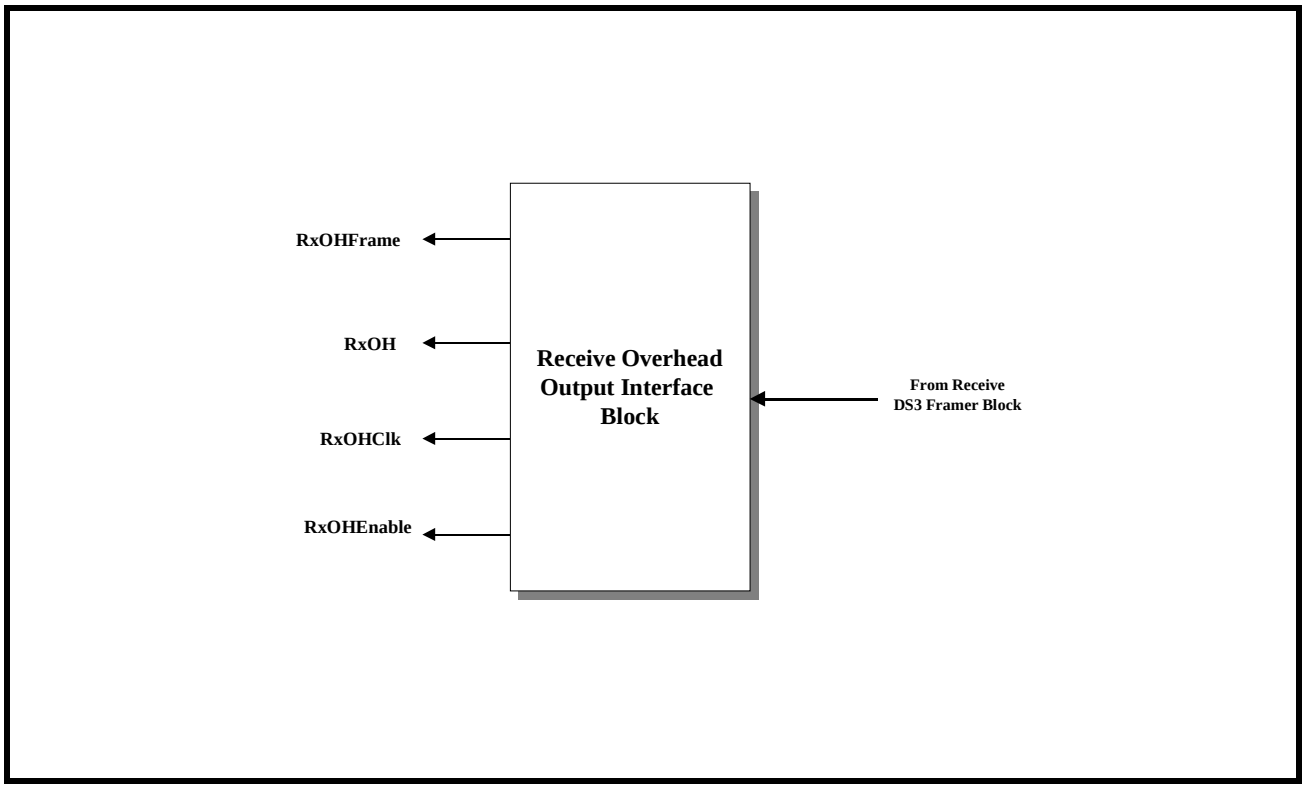
NOTES:

1. *The "white" (e.g., unshaded) boxes reflect tasks that the user's system must perform in order to configure the "LAPD Receiver" to receive LAPD Messages.*
2. *A brief description of the steps that must exist within the "Receive LAPD Interrupt Service" routine exists in Section 3.3.6.*

4.3.4 The Receive Overhead Data Output Interface

Figure 106 presents a simple illustration of the "Receive Overhead Data Output Interface" block within the XRT72L13.

FIGURE 106. A SIMPLE ILLUSTRATION OF THE "RECEIVE OVERHEAD OUTPUT INTERFACE" BLOCK



The DS3 frame consists of 4760 bits. Of these bits, 4704 bits are “payload” bits and the remaining 56 bits are “overhead” bits. The XRT72L13 has been designed to handle and process both the “payload” type and “overhead” type bits for each DS3 frame.

The “Receive Payload Data Output Interface” block, within the “Receive Section” of the XRT72L13, has been designed to handle the payload bits. Likewise, the “Receive Overhead Data Output Interface” block has been designed to handle and process the overhead bits.

The “Receive Overhead Data Output Interface” block unconditionally outputs the contents of all overhead bits within the incoming DS3 data stream. The XRT72L13 does not offer the user a means to “shut off” this transmission of data. However, the “Receive Overhead Output Interface” block does provide the user with the appropriate output signals for “external Data Link Layer” equipment to sample and process these overhead bits, via the following two methods.

- Method 1- Using the “RxOHClk” clock signal.
- Method 2 - Using the “RxClk” and “RxOHEnable” output signals.

Each of these methods are described below.

4.3.4.1 Method 1 - Using the RxOHClk Clock signal

The “Receive Overhead Data Output Interface” block consists of four (4) signals. Of these four signals, the following three signals are to be used when sampling the DS3 overhead bits via “Method 1”.

- RxOH
- RxOHClk
- RxOHFrame

Each of these signals are listed and described below in Table 35 .

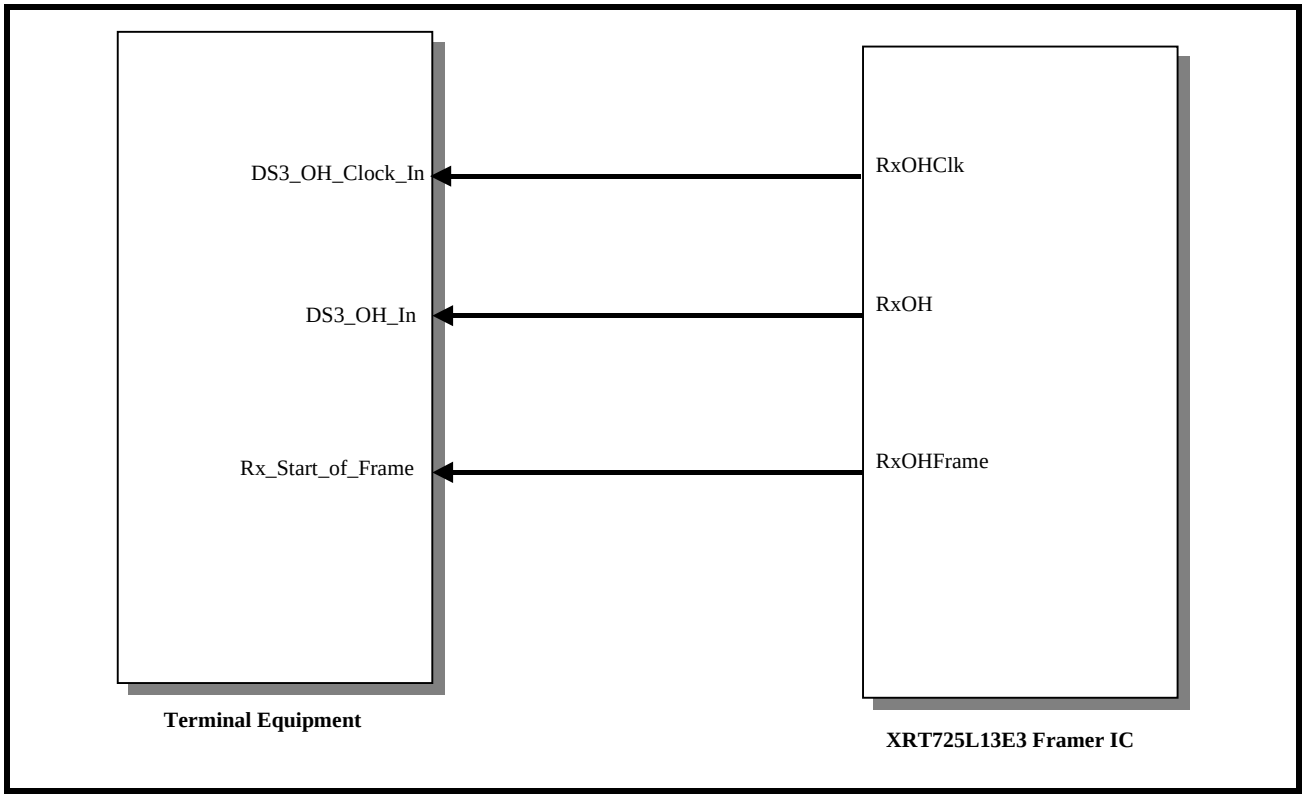
TABLE 35: LISTING AND DESCRIPTION OF THE PIN ASSOCIATED WITH THE RECEIVE OVERHEAD DATA OUTPUT INTERFACE" BLOCK

SIGNAL NAME	TYPE	DESCRIPTION
RxOH	Output	**Receive Overhead Data Output pin:** The XRT72L13 will output the overhead bits, within the incoming DS3 frames, via this pin. The Receive Overhead Data Output Interface block will output a given overhead bit, upon the falling edge of "RxOHClk". Hence, the external data link equipment should sample the data, at this pin, upon the rising edge of "RxOHClk". The XRT72L13 will always output the "DS3 Overhead" bits via this output pin. There are no external input pins or register bit settings available that will disable this output pin.
RxOHClk	Output	**Receive Overhead Data Output Interface Clock Signal:** The XRT72L13 will output the Overhead bits (within the incoming DS3 frames), via the "RxOH" output pin, upon the falling edge of this clock signal. As a consequence, the "user's data link equipment" should use the rising edge of this clock signal to sample the data on both the "RxOH" and "RxOHFrame" output pins. This clock signal is always active.
RxOHFrame	Output	**Receive Overhead Data Output Interface - Start of Frame Indicator:** The XRT72L13 will drive this output pin "high" (for one period of the "RxOHClk" signal); whenever the first overhead bit within a given DS3 frame is being driven onto the "RxOH" output pin.

Interfacing the "Receive Overhead Data Output Interface" block to the Terminal Equipment (Method 1)

Figure 107 illustrates how one should interface the "Receive Overhead Data Output Interface" block to the Terminal Equipment; when using "Method 1" to sample and process the overhead bits from the "inbound" DS3 data stream.

FIGURE 107. ILLUSTRATION OF HOW TO INTERFACE THE TERMINAL EQUIPMENT TO THE "RECEIVE OVERHEAD DATA OUTPUT INTERFACE" BLOCK (FOR METHOD 1).



Method 1 Operation of the Terminal Equipment

If the Terminal Equipment intends to sample any overhead data from the "inbound" DS3 data stream (via the Receive Overhead Data Output Interface" block) then it is expected to do the following:

1. Sample the state of the "RxOHFrame" signal (e.g., the "Rx_Start_of_Frame" input signal) on the rising edge of the "RxOHClk" (e.g., the "DS3_OH_Clock_In") signal.
2. Keep track of the number of rising clock edges that have occurred in the "RxOHClk" (e.g., the "DS3_OH_Clock_In") signal, since the last time the "RxOHFrame" signal was sampled "high". By doing this, the Terminal Equipment will be able to keep track of which overhead bit is being output via the "RxOH" output pin. Based upon this information, the Terminal Equipment will be able to derive some meaning from these overhead bits.

Table 36 relates the number of rising clock edges (in the "RxOHClk" signal, since the "RxOHFrame" signal was last sampled "high") to the DS3 Overhead bit that is being output via the "RxOH" output pin.

TABLE 36: THE RELATIONSHIP BETWEEN THE NUMBER OF RISING CLOCK EDGES IN RXOHCLK, (SINCE "RXOHFRAME" WAS LAST SAMPLED "HIGH") TO THE DS3 OVERHEAD BIT, THAT IS BEING OUTPUT VIA THE "RXOH" OUTPUT PIN

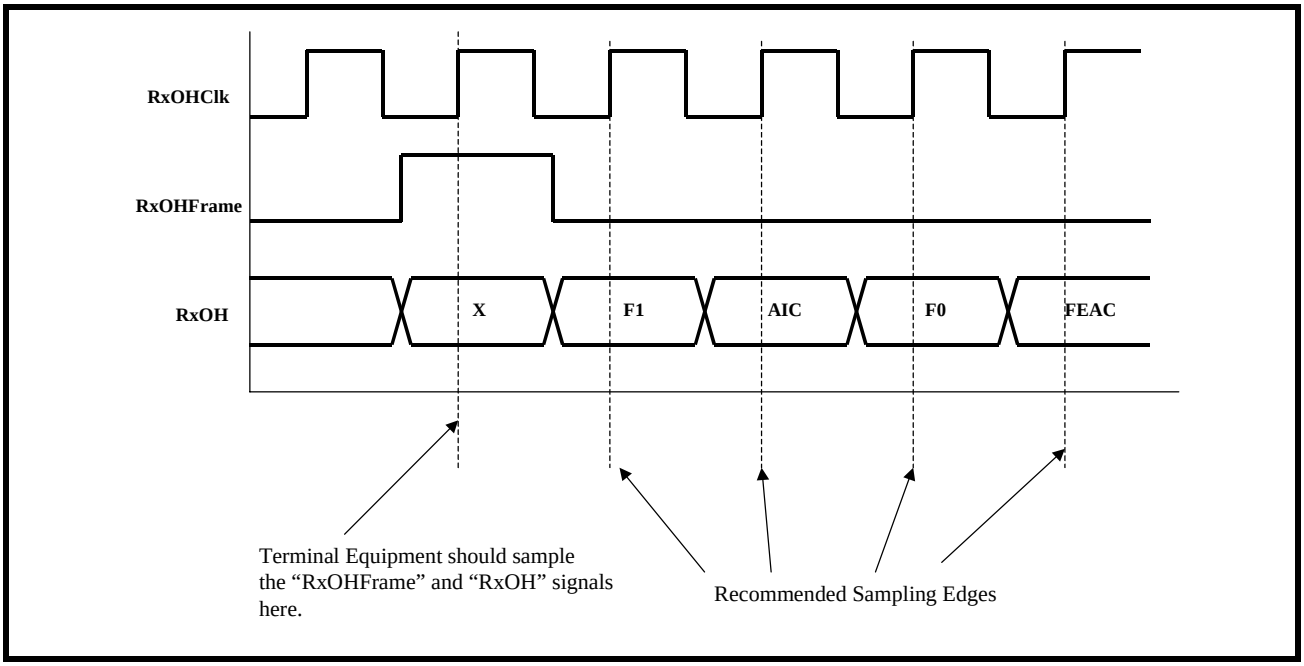
NUMBER OF RISING CLOCK EDGES IN RXOHCLK	THE OVERHEAD BIT BEING OUTPUT BY THE "XRT72L13"
0 (Clock edge is coincident with RxOHFrame being detected "high")	X
1	F1
2	AIC
3	F0
4	NA
5	F0
6	FEAC
7	F1
8	X
9	F1
10	UDL
11	F0
12	UDL
13	F0
14	UDL
15	F1
16	P
17	F1
18	CP
19	F0
20	CP
21	F0
22	CP
23	F1
24	P
25	F1
26	FEBE
27	F0
28	FEBE
29	F0

TABLE 36: THE RELATIONSHIP BETWEEN THE NUMBER OF RISING CLOCK EDGES IN RXOHCLK, (SINCE "RXOHFRAME" WAS LAST SAMPLED "HIGH") TO THE DS3 OVERHEAD BIT, THAT IS BEING OUTPUT VIA THE "RXOH" OUTPUT PIN

NUMBER OF RISING CLOCK EDGES IN RXOHCLK	THE OVERHEAD BIT BEING OUTPUT BY THE "XRT72L13"
30	FEBE
31	F1
32	M0
33	F1
34	DL
35	F0
36	DL
37	F0
38	DL
39	F1
40	M1
41	F1
42	UDL
43	FO
44	UDL
45	FO
46	UDL
47	F1
48	M0
49	F1
50	UDL
51	F0
52	UDL
53	F0
54	UDL
55	F1

Figure 108 presents the typical behavior of the "Receive Overhead Data Output Interface" block, when Method 1 is being used to sample the "incoming" DS3 overhead bits.

FIGURE 108. ILLUSTRATION OF THE SIGNALS THAT ARE OUTPUT VIA THE "RECEIVE OVERHEAD OUTPUT INTERFACE (FOR METHOD 1).



Method 2 - Using "RxOutClk" and the "RxOHEnable" signals

Method 1 requires that the Terminal Equipment be able to handle an additional clock signal; "RxOHClk". However, there may be a situation in which the Terminal Equipment circuitry does not have the means to accommodate and process this extra clock signal, in order to use the "Receive Overhead Data Output" Interface. Hence, Method 2 is available. Method 2 involves the use of the following signals.

- RxOH
- RxOutClk
- RxOHEnable
- RxOHFrame

Each of these signals are listed and described below in Table 37 .

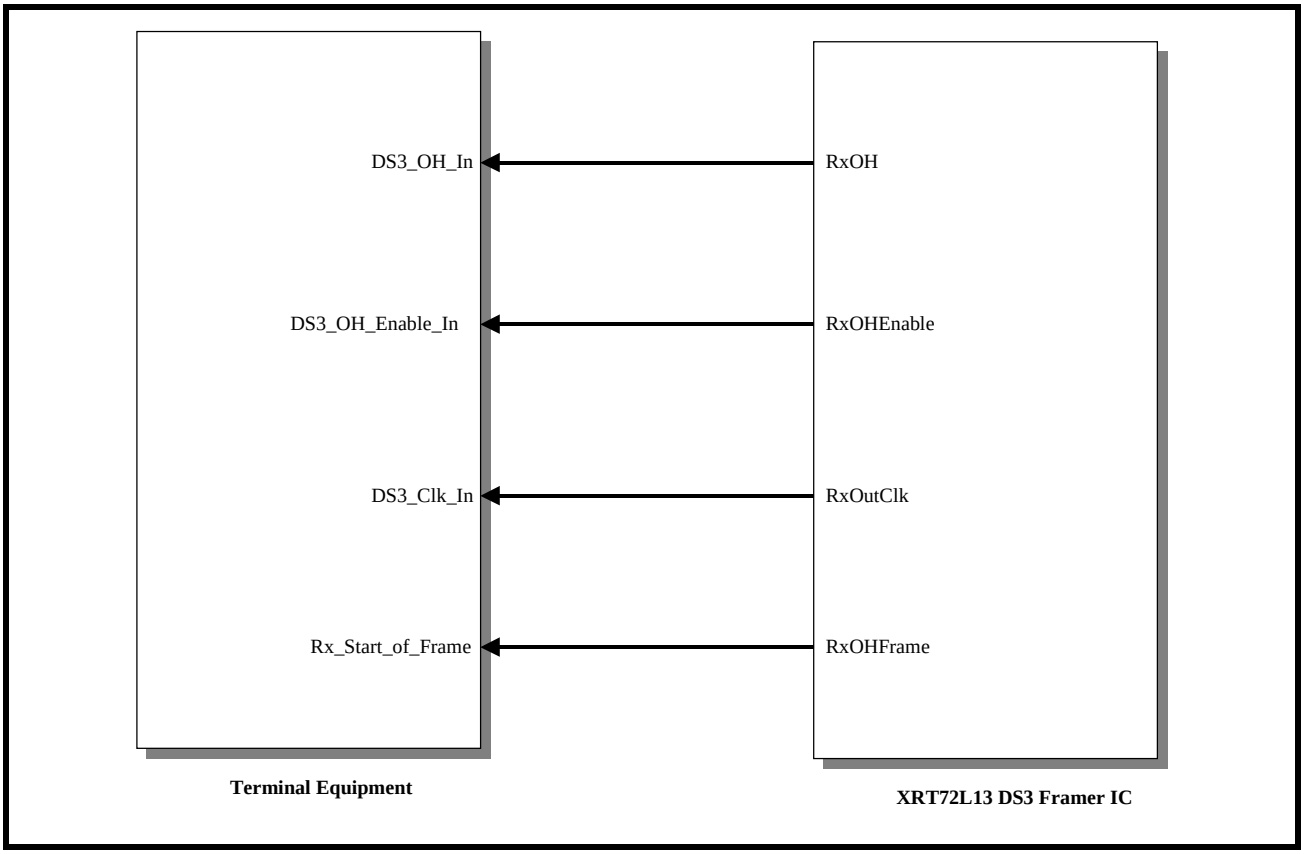
TABLE 37: LISTING AND DESCRIPTION OF THE PIN ASSOCIATED WITH THE RECEIVE OVERHEAD DATA OUTPUT INTERFACE" BLOCK (METHOD 2)

SIGNAL NAME	TYPE	DESCRIPTION
RxOH	Output	**Receive Overhead Data Output pin:** The XRT72L13 will output the overhead bits, within the incoming DS3 frames, via this pin. The Receive Overhead Output Interface will pulse the “RxOHEnable” output pin (for one “RxOutClk” period) at approximately the middle of the “RxOH” bit period. The user is advised to design the Terminal Equipment to latch the contents of the “RxOH” output pin, whenever the “RxOHEnable” output pin is sampled “high” on the falling edge of “RxOutClk”.
RxOHEnable	Output	**Receive Overhead Data Output Enable - Output pin:** The XRT72L13 will assert this output signal for one “RxOutClk” period when it is safe for the Terminal Equipment to sample the data on the “RxOH” output pin.
RxOHFrame	Output	**Receive Overhead Data Output Interface - Start of Frame Indicator:** The XRT72L13 will drive this output pin “high” (for one period of the “RxOH” signal), whenever the first overhead bit, within a given DS3 frame is being driven onto the “RxOH” output pin.
RxOutClk	Output	**Receive Section Output Clock Signal:** This clock signal is derived from the “RxLineClk” signal (from the LIU) for loop-timing applications, and the “TxInClk” signal (from a local oscillator) for local-timing applications. For DS3 applications, this clock signal will operate at 44.736MHz. The user is advised to design the Terminal Equipment to latch the contents of the “RxOH” pin, anytime the “RxOHEnable” output signal is sampled “high” on the falling edge of this clock signal.

Interfacing the “Receive Overhead Data Output Interface” block to the Terminal Equipment (Method 2)

Figure 109 illustrates how one should interface the “Receive Overhead Data Output Interface” block to the Terminal Equipment, when using “Method 2” to sample and process the overhead bits from the “inbound” DS3 data stream.

FIGURE 109. ILLUSTRATION OF HOW TO INTERFACE THE TERMINAL EQUIPMENT TO THE "RECEIVE OVERHEAD DATA OUTPUT INTERFACE" BLOCK (FOR METHOD 2).



Method 2 Operation of the Terminal Equipment

If the Terminal Equipment intends to sample any overhead data from the "inbound" DS3 data stream (via the "Receive Overhead Data Output Interface), then it is expected to do the following.

1. Sample the state of the "RxOHFrame" signal (e.g., the "Rx_Start_of_Frame" input) on the falling edge of the "RxOutClk" clock signal; whenever the "RxOHEnable" output signal is also sampled "high".
2. Keep track of the number of times that the "RxOHEnable" signal has been sampled "high" since the last time the "RxOHFrame" was also sampled "high". By doing this, the Terminal Equipment will be able to keep track of which overhead bit is being output via the "RxOH" output pin. Based upon this information, the Terminal Equipment will be able to derive some meaning from these overhead bits.
3. Table 38 relates the number of "RxOHEnable" output pulses (that have occurred since both the "RxOHFrame" and the "RxOHEnable" pins were both sampled "high") to the DS3 overhead bit that is being output via the "RxOH" output pin.

TABLE 38: THE RELATIONSHIP BETWEEN THE NUMBER OF "RXOHENABLE" OUTPUT PULSES ((SINCE "RXOHFRAME" WAS LAST SAMPLED "HIGH") TO THE DS3 OVERHEAD BIT, THAT IS BEING OUTPUT VIA THE "RXOH" OUTPUT PIN

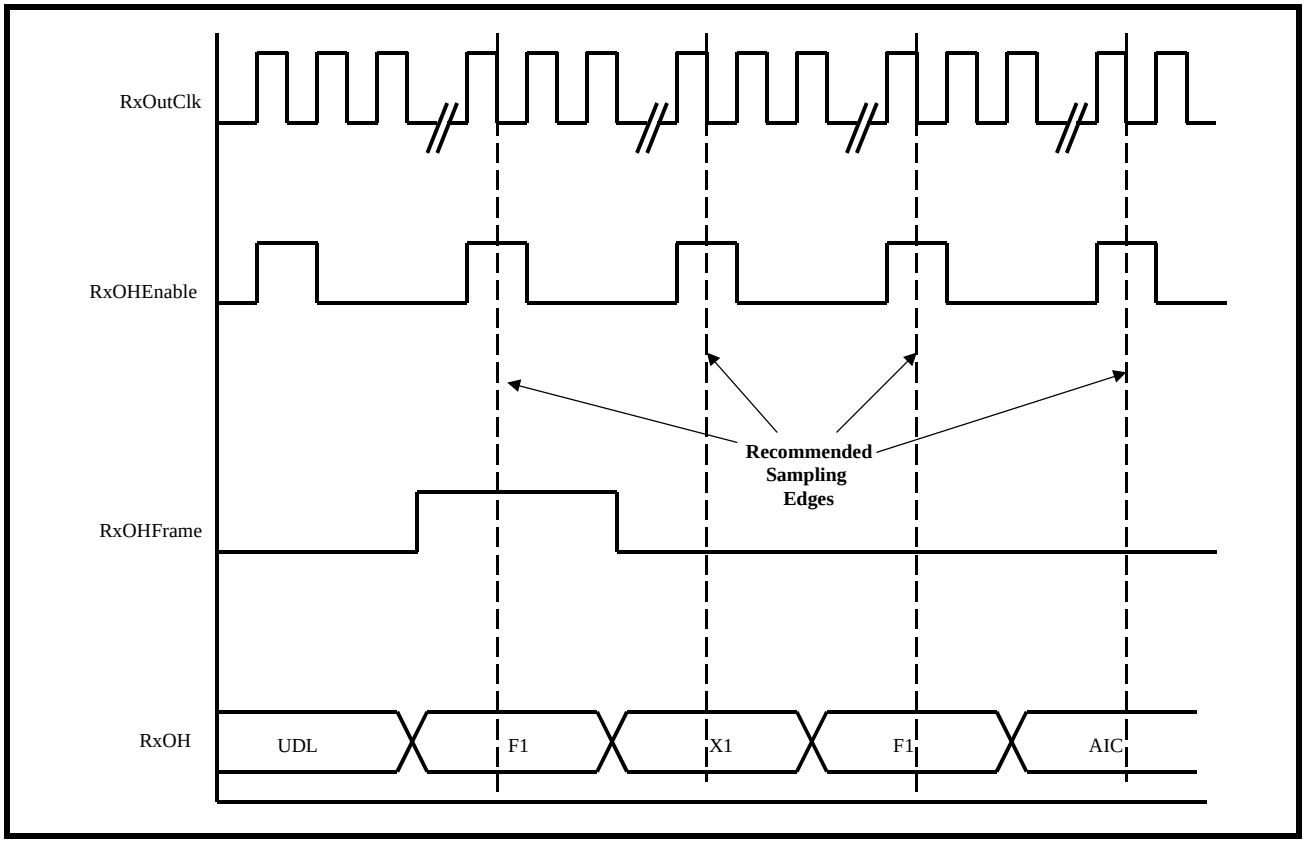
NUMBER OF "RXOHENABLE" OUTPUT PULSES	THE OVERHEAD BIT BEING OUTPUT BY THE "XRT72L13"
0 (The "RxOHEnable" and "RxOHFrame" signals are both sampled "high")	X
1	F1
2	AIC
3	F0
4	NA
5	F0
6	FEAC
7	F1
8	X
9	F1
10	UDL
11	F0
12	UDL
13	F0
14	UDL
15	F1
16	P
17	F1
18	CP
19	F0
20	CP
21	F0
22	CP
23	F1
24	P
25	F1
26	FEBE
27	F0
28	FEBE
29	F0

TABLE 38: THE RELATIONSHIP BETWEEN THE NUMBER OF "RXOHENABLE" OUTPUT PULSES ((SINCE "RXOHFRAME" WAS LAST SAMPLED "HIGH") TO THE DS3 OVERHEAD BIT, THAT IS BEING OUTPUT VIA THE "RXOH" OUTPUT PIN

NUMBER OF "RXOHENABLE" OUTPUT PULSES	THE OVERHEAD BIT BEING OUTPUT BY THE "XRT72L13"
30	FEBE
31	F1
32	M0
33	F1
34	DL
35	F0
36	DL
37	F0
38	DL
39	F1
40	M1
41	F1
42	UDL
43	FO
44	UDL
45	FO
46	UDL
47	F1
48	M0
49	F1
50	UDL
51	F0
52	UDL
53	F0
54	UDL
55	F1

Figure 110 presents the typical behavior of the "Receive Overhead Data Output Interface" block, when Method 2 is being used to sample the "incoming" DS3 overhead bits.

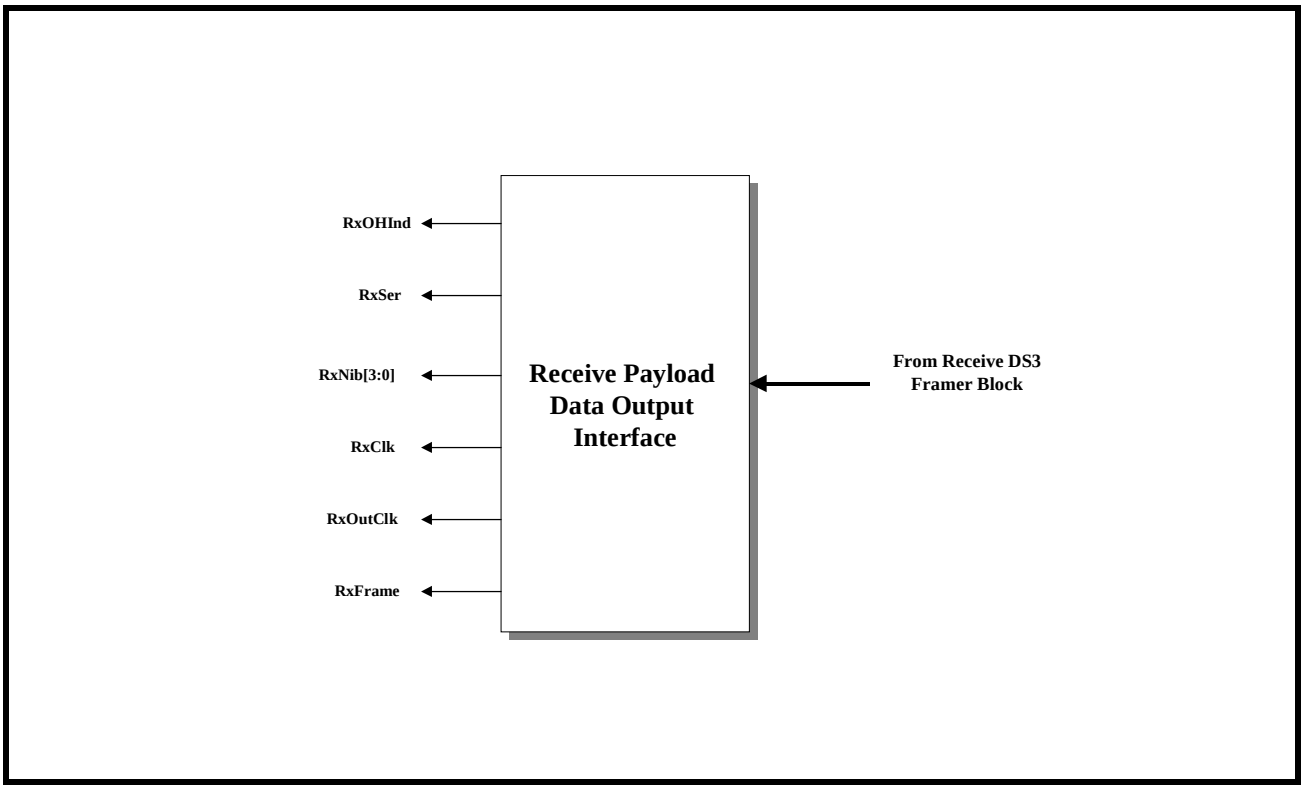
FIGURE 110. ILLUSTRATION OF THE SIGNALS THAT ARE OUTPUT VIA THE "RECEIVE OVERHEAD DATA OUTPUT INTERFACE" BLOCK (FOR METHOD 2).



4.3.5 The Receive Payload Data Output Interface

Figure 111 presents a simple illustration of the "Receive Payload Data Output Interface" block.

FIGURE 111. A SIMPLE ILLUSTRATION OF THE "RECEIVE PAYLOAD DATA OUTPUT INTERFACE" BLOCK



Each of the output pins of the "Receive Payload Data Output Interface" block are listed in Table 39 and described below. The exact role that each of these output pins assume, for a variety of operating scenarios are described throughout this section.

TABLE 39: LISTING AND DESCRIPTION OF THE PIN ASSOCIATED WITH THE RECEIVE PAYLOAD DATA OUTPUT INTERFACE BLOCK

SIGNAL NAME	TYPE	DESCRIPTION
RxSer	Output	**Receive Serial Payload Data Output pin:** If the user opts to operate the XRT72L13 in the "serial" mode, then the chip will output the payload data, of the incoming DS3 frames, via this pin. The XRT72L13 will output this data upon the rising edge of RxClk. The user is advised to design the Terminal Equipment such that it will sample this data on the falling edge of RxClk. This signal is only active if the "NibInt" input pin is pulled "low".
RxNib[3:0]	Output	**Receive Nibble-Parallel Payload Data Output pins:** If the user opts to operate the XRT72L13 in the "nibble-parallel" mode, then the chip will output the payload data, of the incoming DS3 frames, via these pins. The XRT72L13 will output data via these pins, upon the falling edge of the RxClk output pin. The user is advised to design the Terminal Equipment such that it will sample this data upon the rising edge of RxClk. These pins are only active if the "NibInt" input pin is pulled "high".
RxClk	Output	**Receive Payload Data Output Clock pin:** The exact behavior of this signal depends upon whether the XRT72L13 is operating in the "Serial" or in the "Nibble-Parallel-Mode". **Serial Mode Operation** In the "serial" mode, this signal is a 44.736MHz clock output signal. The Receive Payload Data Output Interface will update the data via the RxSer output pin, upon the rising edge of this clock signal. The user is advised to design (or configure) the Terminal Equipment to sample the data on the "RxSer" pin, upon the falling edge of this clock signal. **Nibble-Parallel Mode Operation** In this Nibble-Parallel Mode, the XRT72L13 will derive this clock signal, from the RxLineClk signal. The XRT72L13 will pulse this clock 1176 times for each "inbound" DS3 frame. The Receive Payload Data Output Interface will update the data, on the "RxNib[3:0]" output pins upon the falling edge of this clock signal. The user is advised to design (or configure) the Terminal Equipment to sample the data on the "RxNib[3:0] output pins, upon the rising edge of this clock signal
RxOHInd	Output	**Receive Overhead Bit Indicator Output:** This output pin will pulse "high" whenever the "Receive Payload Data Output Interface" outputs an "overhead" bit via the "RxSer" output pin. The purpose of this output pin is to alert the Terminal Equipment that the current bit, (which is now residing on the RxSer output pin), is an overhead bit and should not be processed by the Terminal Equipment. The XRT72L13 will update this signal, upon the rising edge of the “RxClk" signal. The user is advised to design (or configure) the Terminal Equipment to sample this signal (along with the data on the "RxSer" output pin) on the falling edge of the RxClk signal. For DS3 applications, this output pin is only active if the XRT72L13 is operating in the "Serial Mode". This output pin will be "low" if the device is operating in the "Nibble-Parallel" Mode.
RxFrame	Output	**Receive "Start of Frame" Output Indicator:** The exact behavior of this pin, depends upon whether the XRT72L13 has been configured to operate in the "Serial" Mode or the "Nibble-Parallel" Mode. **Serial Mode Operation:** The Receive Section of the XRT72L13 will pulse this output pin "high" (for one bit period) when the "Receive Payload Data Output Interface" block is driving the very first bit (or "Nibble") of a given DS3 frame, onto the RxSer output pin. **Nibble-Parallel Mode Operation:** The "Receive Section" of the XRT72L13 will pulse this output pin "high" (for one nibble period), when the "Receive Payload Data Output Interface" is driving the very first nibble of a given DS3 frame, onto the "RxNib[3:0] output pins.

Operation of the Receive Payload Data Output Interface block

The Receive Payload Data Output Interface permits the user to read out the payload data of "inbound" DS3 frames, via either of the following modes.

- Serial Mode
- Nibble-Parallel Mode

Each of these modes are described in detail, below.

4.3.5.1 Serial Mode Operation

Behavior of the XRT72L13

If the XRT72L13 has been configured to operate in the “Serial” mode, then the XRT72L13 will behave as follows.

Payload Data Output

The XRT72L13 will output the payload data, of the incoming DS3 frames via the “RxSer” output, upon the rising edge of RxClk.

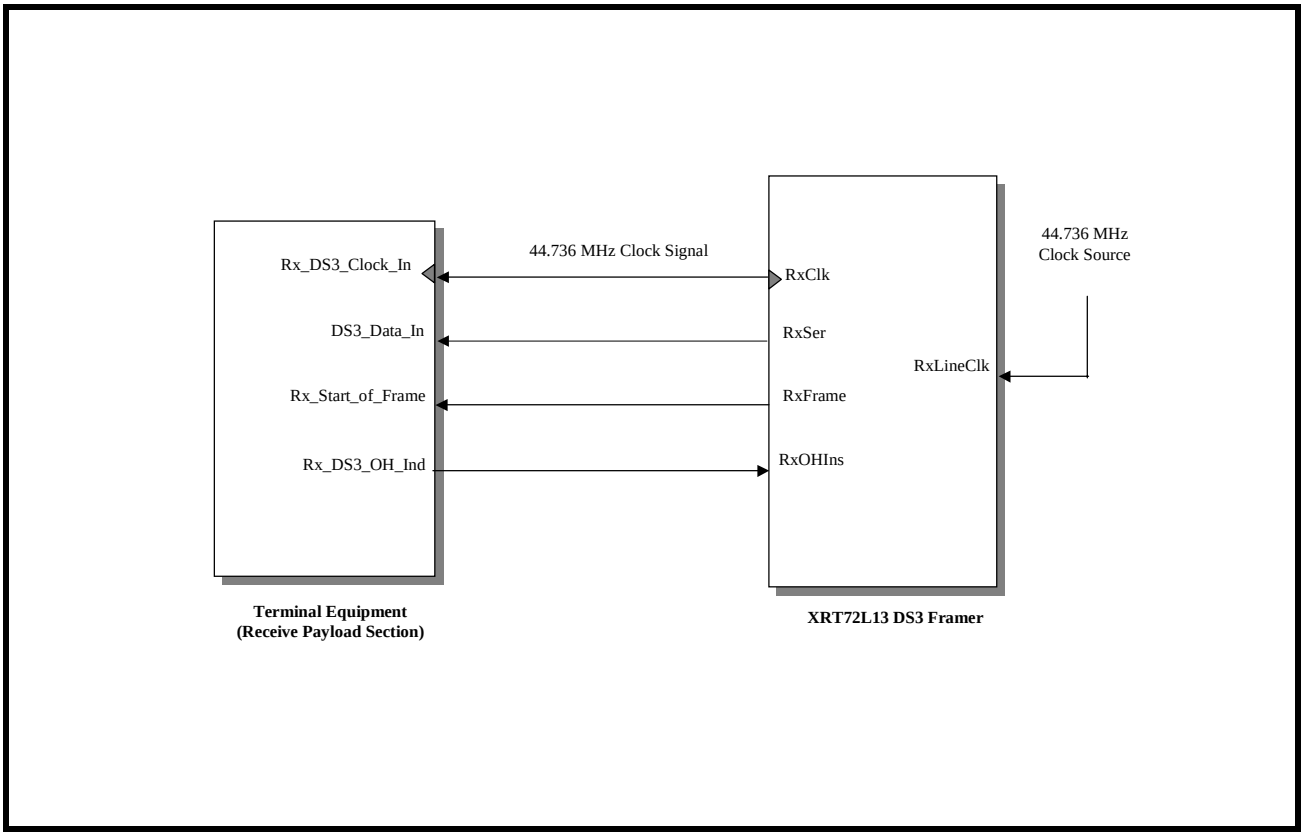
Delineation of "inbound" DS3 Frames

The XRT72L13 will pulse the "RxFrame" output pin "high" for one bit-period; coincident with it driving the first bit within a given DS3 frame, via the "RxSer" output pin.

Interfacing the XRT72L13 to the "Receive Terminal Equipment"

Figure 112 presents a simple illustration as how the user should interface the XRT72L13 to that terminal equipment which processes "Receive Direction" payload data.

FIGURE 112. ILLUSTRATION OF THE XRT72L13 DS3/E3 FRAMER IC BEING INTERFACED TO THE "RECEIVE" TERMINAL EQUIPMENT (SERIAL MODE OPERATION)



Required Operation of the Terminal Equipment

The XRT72L13 will update the data on the RxSer output pin, upon the rising edge of "RxClk". However, because the “rising edge” of “RxClk” to data delay is between 14ns to 16ns; the Terminal Equipment should sample the data on the "RxSer" output pin (or the "DS3_Data_In" pin at the Terminal Equipment) upon the rising edge of RxClk. This will still permit the Terminal Equipment with a “RxSer” to “RxClk” set-up time of approximately 6ns; and a hold time fo 14 to 16ns. As the Terminal Equipment samples "RxSer" with each rising edge of "RxClk" it should also be sampling the following signals.

- RxFrame
- RxOHInd

The Need for sampling "RxFrame"

The XRT72L13 will pulse the "RxFrame" output pin "high" coincident with it driving the very first bit of a given DS3 frame onto the "RxSer" output pin. If knowledge of the "DS3 Frame Boundaries" is important for the operation of the Terminal Equipment, then this is a very important signal for it to sample.

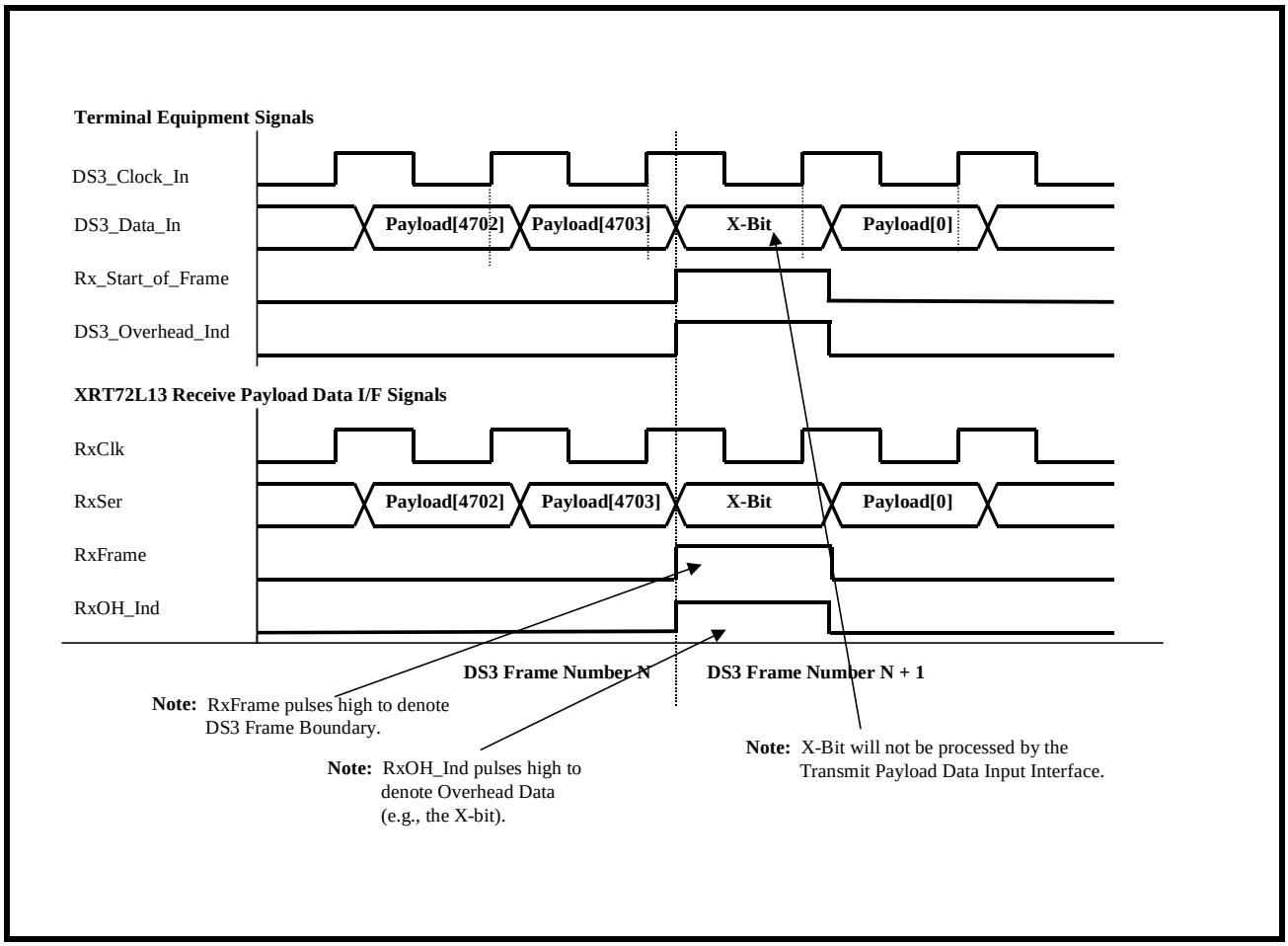
The Need for sampling "RxOHInd"

The XRT72L13 will indicate that it is currently driving an "overhead" bit onto the "RxSer" output pin, by pulsing the "RxOHInd" output pin "high". If the Terminal Equipment samples this signal "high", then it should know that the bit, that it is currently sampling via the "RxSer" pin is an "overhead" bit and should not be processed.

The Behavior of the Signals between the "Receive Payload Data Output Interface" block and the Terminal Equipment

The behavior of the signals between the XRT72L13 and the Terminal Equipment for DS3 Serial Mode Operation is illustrated in Figure 113 .

FIGURE 113. AN ILLUSTRATION OF THE BEHAVIOR OF THE SIGNALS BETWEEN THE "RECEIVE PAYLOAD DATA OUTPUT INTERFACE" BLOCK (OF THE XRT72L13) AND THE TERMINAL EQUIPMENT (SERIAL MODE OPERATION)



4.3.5.2 Nibble-Parallel Mode Operation

Behavior of the XRT72L13

If the XRT72L13 has been configured to operate in the "Nibble-Parallel" Mode, then the XRT72L13 will behave as follows.

Payload Data Output

The XRT72L13 will output the payload data of the incoming DS3 frames, via the "RxNib[3:0] output pins, upon the falling edge of "RxClk".

NOTES:

1. *In this case, "RxClk" will function as the "Nibble Clock" signal between the XRT72L13 the Terminal Equipment. The XRT72L13 will pulse the "RxClk" output signal "high" 1176 times, for each "inbound" DS3 frame.*
2. *Unlike "Serial Mode" operation, the duty cycle of RxClk, in "Nibble-Parallel" Mode operation is approximately 25%.*

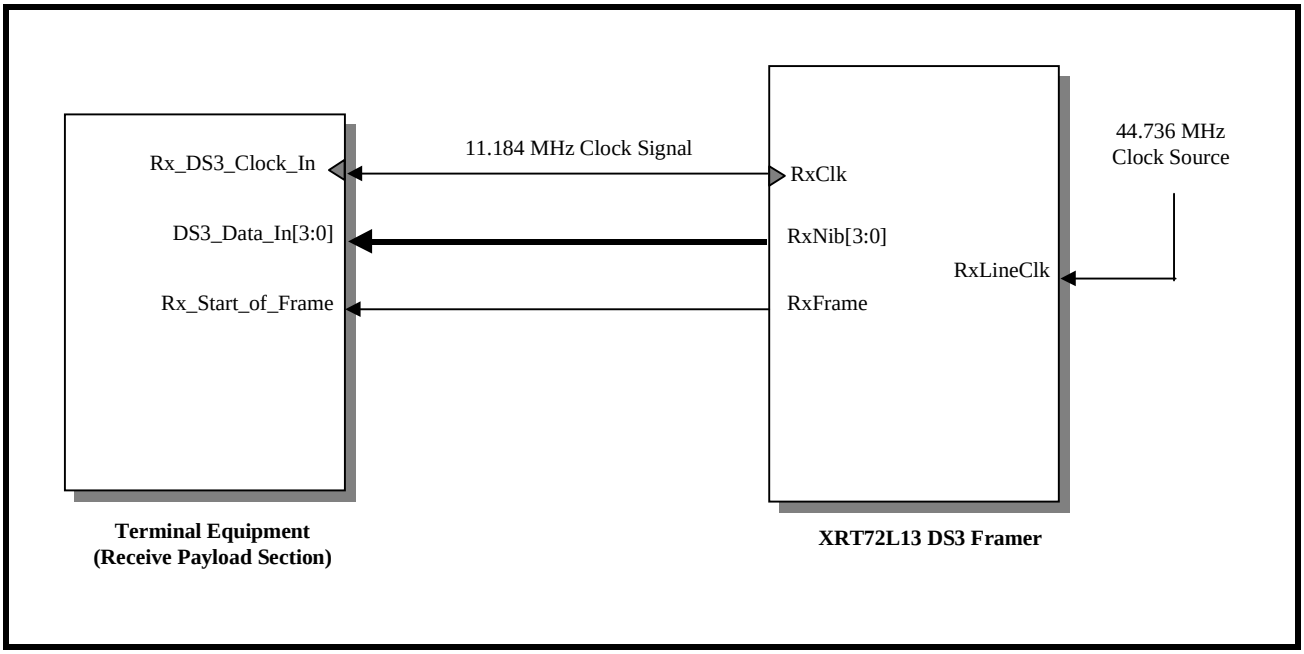
Delineation of "Inbound" DS3 Frames

The XRT72L13 will pulse the "RxFrame" output pin "high" for one "nibble-period" coincident with it driving the very first nibble, within a given "inbound" DS3 frame, via the "RxNib[3:0] output pins.

Interfacing the XRT72L13 the Terminal Equipment.

Figure 114 presents a simple illustration as how the user should interface the XRT72L13 to that terminal equipment which processes "Receive Direction" payload data.

FIGURE 114. ILLUSTRATION OF THE XRT72L13 DS3/E3 FRAMER IC BEING INTERFACED TO THE RECEIVE SECTION OF THE TERMINAL EQUIPMENT (NIBBLE-MODE OPERATION)



Required Operation of the Terminal Equipment

The XRT72L13 will update the data on the "RxNib[3:0]" line, upon the falling edge of "RxClk". Hence, the Terminal Equipment should sample the data on the "RxNib[3:0]" output pins (or the "DS3_Data_In[3:0]" input pins at the Terminal Equipment) upon the rising edge of "RxClk". As the Terminal Equipment samples "RxSer" with each rising edge of "RxClk" it should also be sampling the "RxFrame" signal.

The Need for Sampling "RxFrame"

The XRT72L13 will pulse the "RxFrame" output pin "high" coincident with it driving the very first nibble of a given DS3 frame, onto the "RxNib[3:0]" output pins.

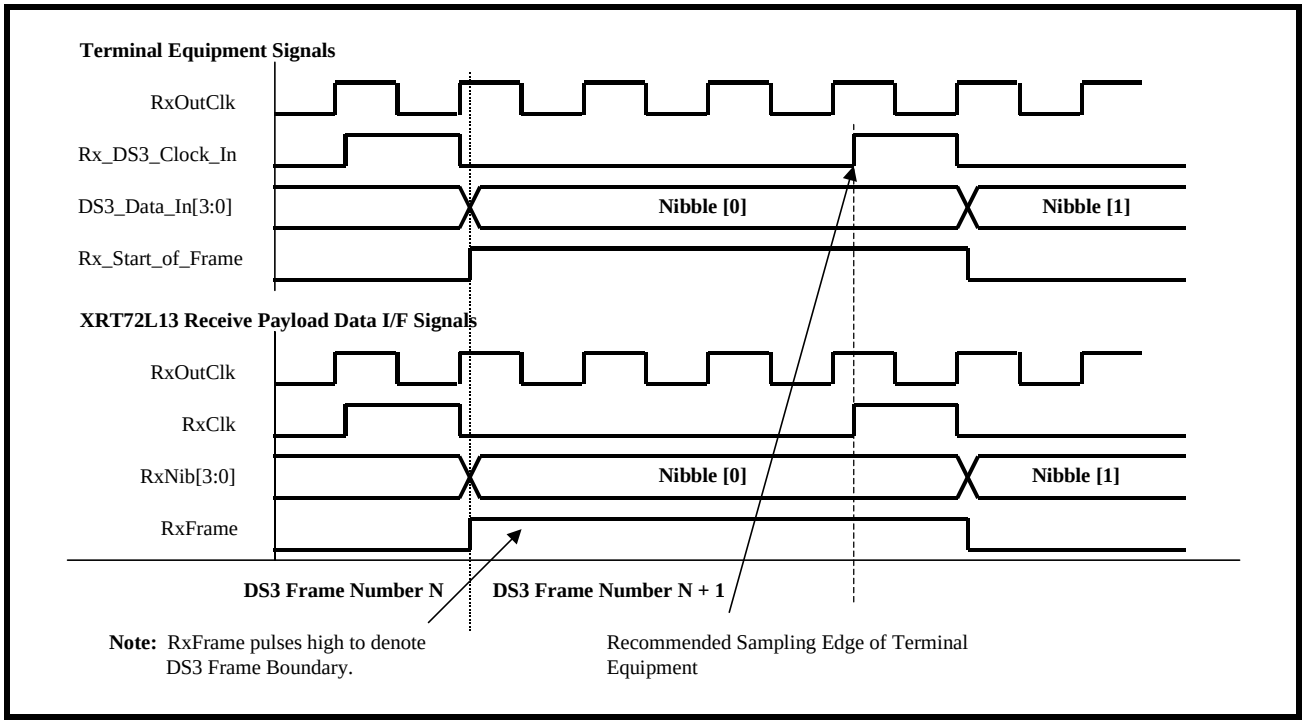
If knowledge of the "DS3 Frame Boundaries" is important for the operation of the Terminal Equipment, then this is a very important signal for it to sample.

NOTE: *For DS3/Nibble-Parallel Mode Operation, none of the Overhead bits will be output via the "RxNib[3:0]" output pins. Hence, the "RxOH_Ind" output pin will be in-active in this mode.*

The Behavior of the Signals between the "Receive Payload Data Output Interface" block and the "Terminal Equipment"

The behavior of the signals between the XRT72L13 and the Terminal Equipment for "DS3 Nibble-Mode" operation is illustrated in Figure 115 .

FIGURE 115. AN ILLUSTRATION OF THE BEHAVIOR OF THE SIGNALS BETWEEN THE "RECEIVE PAYLOAD DATA OUTPUT INTERFACE" BLOCK (OF THE XRT72L13) AND THE TERMINAL EQUIPMENT (NIBBLE-MODE OPERATION).



4.3.6 Receive Section Interrupt Processing

The "Receive Section" of the XRT72L13 can generate an interrupt to the Microcontroller/Microprocessor for the following reasons.

- Change of State of Receive LOS (Loss of Signal) condition
- Change of State of Receive OOF (Out of Frame) condition
- Change of State of Receive AIS (Alarm Indicator Signal) condition
- Change of State of Receive Idle Condition.
- Change of State of Receive FERF (Far-End Receive Failure) condition.
- Change of State of AIC (Application Identification Channel) bit.
- Detection of P-Bit Error in a DS3 frame
- Detection of CP-Bit Error in a DS3 frame
- The Receive FEAC Message - Validation Interrupt
- The Receive FEAC Message - Removal Interrupt
- Completion of Reception of a LAPD Message

4.3.6.1 Enabling "Receive Section" Interrupts

As mentioned in Section 1.6, the Interrupt Structure, within the XRT72L13 contains two hierarchical levels.

- Block Level
- Source Level

The Block Level

The "Enable" state of the "Block" level for the Receive Section Interrupts dictates whether or not interrupts (if enabled at the source level), are actually enabled.

The user can enable or disable these "Receive Section" interrupts, at the "Block Level" by writing the appropriate data into Bit 7 (Rx DS3/E3 Interrupt Enable) within the "Block Interrupt Enable" register (Address = 0x04); as illustrated below.

BLOCK INTERRUPT ENABLE REGISTER (ADDRESS = 0X04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxDS3/E3 Interrupt Enable	Not Used		M13 Interrupt Enable	Unused		TxDS3/E3 Interrupt Enable	One Second Interrupt Enable
R/W	RO	RO	RO	RO	RO	R/W	R/W
X	0	0	0	0	0	0	0

Setting this bit-field to "1" enables the "Receive Section" (at the Block Level) for interrupt generation. Conversely, setting this bit-field to "0" disables the "Receive Section" for interrupt generation.

4.3.6.2 Enabling/Disabling and Servicing Receive Section Interrupts

As mentioned earlier, the "Receive Section" of the XRT72L13 Framer IC contains numerous interrupts. The "Enabling/Disabling and Servicing of each of these interrupts is described below.

4.3.6.2.1 The "Change of State" on Receive LOS Interrupt

If the "Change of State on Receive LOS (Loss of Signal)" Interrupt is enabled, then the XRT72L13 Framer IC will generate an interrupt in response to either of the following conditions.

1. When the XRT72L13 Framer IC declares an LOS (Loss of Signal) condition, and
2. When the XRT72L13 Framer IC clears the LOS (Loss of Signal) condition.

Conditions causing the XRT72L13 Framer IC to declare an LOS condition

- If the XRT7300 LIU IC declares an LOS condition, and drives the "RLOS" input pin (of the XRT72L13 Framer IC) "HIGH".
- If the XRT72L13 Framer IC detects a 180 consecutive "0s", via the "RxPOS" and "RxNEG" input pins.

Conditions causing the XRT72L13 Framer IC to clear the LOS condition.

- When the XRT7300 LIU IC ceases declaring an LOS condition and drives the "RLOS" input pin (of the XRT72L13 Framer IC) "LOW".
- When the XRT72L13 Framer IC detects at least 60 marks (via the "RxPOS" and "RxNEG" input pins) out of 180 bit-periods.

Enabling and Disabling the "Change of State on Receive LOS Interrupt:

The user can enable or disable the "Change of State on Receive LOS" Interrupt, by writing the appropriate value into Bit 6 (LOS Interrupt Enable) within the "RxDS3 Interrupt Enable" Register, as illustrated below.

RXDS3 INTERRUPT ENABLE REGISTER (ADDRESS = 0X12)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CP Bit Error Interrupt Enable	LOS Interrupt Enable	AIS Interrupt Enable	Idle Interrupt Enable	FERF Interrupt Enable	AIC Interrupt Enable	OOF Interrupt Enable	P-Bit Error Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Setting this bit-field to "1" enables this interrupt. Conversely, setting this bit-field to "0" disables this interrupt.

Servicing the "Change of State" on Receive LOS Interrupt

Whenever the XRT72L13 Framer IC detects this interrupt, it will do all of the following.

- It will assert the Interrupt Request output pin (INT*) by driving this pin "LOW".

- It will set Bit 6 (LOS Interrupt Status) within the "RxDS3 Interrupt Status" register to "1", as illustrated below.

RXDS3 INTERRUPT STATUS REGISTER (ADDRESS = 0X13)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CP-Bit Error Interrupt Status	LOS Interrupt Status	AIS Interrupt Status	Idle Interrupt Status	FERF Interrupt Status	AIC Interrupt Status	OOF Interrupt Status	P-Bit Error Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	1	0	0	0	0	0	0

Whenever the user's system encounters the "Change of LOS on Receive" Interrupt, then it should do the following.

1. It should determine the current state of the "LOS" condition. Recall, that this interrupt can generated, whenever the XRT72L13 Framer declares or clears the LOS defects. Hence, the user can determine the current state of the LOS defect by reading the state of Bit 6 (RxLOS), within the "RxDS3 Configuration & Status" Registers, as illustrated below.

RXDS3 CONFIGURATION & STATUS REGISTER (ADDRESS = 0X10)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxAIS	RxLOS	RxIdle	RxOOF	Reserved	Framing On Parity	FSync Algo	MSync Algo
RO	RO	RO	RO	RO	RO	RO	RUR
0	1	0	0	0	0	0	0

If the LOS State is "TRUE"

1. It should transmit a FERF (Far-End Receive Failure) to the "Remote Terminal Equipment". The XRT72L13 Framer IC automatically supports this action via the "FERF-upon-LOS" feature.
2. It should transmit the appropriate FEAC Message (per Bellcore GR-499-CORE), to the Remote Terminal, indicating that a "Loss of Signal" condition has been declared.

If the LOS State is "FALSE"

1. It should cease transmitting a FERF indicator to the "Remote Terminal Equipment". The XRT72L13 Framer IC automatically supports this action via the "FERF-upon-LOS" feature.
2. It should transmit the appropriate FEAC Message (per Bellcore GR-499-CORE), to the Remote Terminal Equipment, indicating that the "Loss of Signal" condition has been cleared.

4.3.6.2.2 The "Change of State" on Receive OOF Interrupt

If the "Change of State on Receive OOF (Out-of-Frame)" Interrupt is enabled, then the XRT72L13 Framer IC will generate an interrupt in response to either of the following conditions.

1. When the XRT72L13 Framer IC declares an OOF (Out of Frame) condition, and
2. When the XRT72L13 Framer IC clears the OOF (Out of Frame) condition.

Conditions causing the XRT72L13 Framer IC to declare an OOF condition

- If the Receive DS3 Framer block (within the XRT72L13 Framer IC) detects at least either 3 or 6 F-bit errors, in the last 16 F-bits.

Conditions causing the XRT72L13 Framer IC to clear the OOF condition.

- Whenever, the "Receive DS3 Framer" block transitions from the "M-Bit Search" into the "In-Frame" state (within the "Frame Acquisition/Maintenance State Machine Diagram).

Enabling and Disabling the "Change of State on Receive OOF Interrupt:

The user can enable or disable the "Change of State on Receive OOF" Interrupt, by writing the appropriate value into Bit 1 (OOF Interrupt Enable) within the

"RxDS3 Interrupt Enable" Register, as illustrated below.

RXDS3 INTERRUPT ENABLE REGISTER (ADDRESS = 0X12)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CP Bit Error Interrupt Enable	LOS Interrupt Enable	AIS Interrupt Enable	Idle Interrupt Enable	FERF Interrupt Enable	AIC Interrupt Enable	OOF Interrupt Enable	P-Bit Error Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Setting this bit-field to "1" enables this interrupt. Conversely, setting this bit-field to "0" disables this interrupt.

Servicing the "Change of State" on Receive OOF Interrupt

Whenever the XRT72L13 Framer IC detects this interrupt, it will do all of the following.

- It will assert the Interrupt Request output pin (INT*) by driving this pin "LOW".
- It will set Bit 1 (OOF Interrupt Status), within the "RxDS3 Interrupt Status" Register to "1", as indicated below.

RXDS3 INTERRUPT STATUS REGISTER (ADDRESS = 0X13)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CP-Bit Error Interrupt Status	LOS Interrupt Status	AIS Interrupt Status	Idle Interrupt Status	FERF Interrupt Status	AIC Interrupt Status	OOF Interrupt Status	P-Bit Error Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	1	0

Whenever the Terminal Equipment encounters a "Change in OOF on Receive" Interrupt, then it should do the following.

1. It should determine the current state of the "OOF" condition. Recall, that this interrupt can generated, whenever the XRT72L13 Framer declares or clears the OOF defects. Hence, the user can determine the current state of the OOF defect by reading the state of Bit 4 (RxOOF), within the "RxDS3 Configuration & Status" Registers, as illustrated below.

RXDS3 CONFIGURATION & STATUS REGISTER (ADDRESS = 0X10)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxAIS	RxLOS	RxIdle	RxOOF	Reserved	Framing On Parity	FSync Algo	MSync Algo
RO	RO	RO	RO	RO	RO	RO	RUR
0	0	0	0	0	0	0	0

If OOF is "TRUE".

1. It should transmit a FERF (Far-End Receive Failure) to the "Remote Terminal Equipment". The XRT72L13 Framer IC automatically supports this action via the "FERF-upon-OOF" feature.
2. It should transmit the appropriate FEAC Message (per Bellcore GR-499-CORE), to the Remote Terminal, indicating that a "Service Affecting" condition has been detected in the Local Terminal Equipment.

if OOF is "FALSE"

1. It should cease transmitting a FERF (Far-End Receive Failure) indicator to the "Remote Terminal Equipment". The XRT72L13 Framer IC automatically supports this action via the "FERF-upon-OOF" feature.
2. It should transmit the appropriate FEAC Message (per Bellcore GR-499-CORE), to the "Remote Terminal Equipment, indicating that the "Service Affecting" condition has been cleared.

4.3.6.2.3 The "Change of State" of Receive AIS Interrupt

If the "Change of State on Receive AIS (Alarm Indication Signal)" Interrupt is enabled, then the XRT72L13 Framer IC will generate an interrupt in response to either of the following conditions.

1. When the XRT72L13 Framer IC detects an AIS pattern, in the "incoming" DS3 data stream, and
2. When the XRT72L13 Framer IC no longer detects the AIS pattern in the "incoming" DS3 data stream.

Conditions causing the XRT72L13 Framer IC to declare an AIS condition

- If the Receive DS3 Framer block (within the XRT72L13 Framer IC) detects at least 63 DS3 frames, which contains the AIS pattern.

Conditions causing the XRT72L13 Framer IC to clear the AIS condition.

- Whenever, the "Receive DS3 Framer" block detects 63 DS3 frames, which do not contain the AIS pattern.

Enabling and Disabling the "Change of State on Receive AIS Interrupt:

The user can enable or disable the "Change of State on Receive AIS" Interrupt, by writing the appropriate value into Bit 5 (AIS Interrupt Enable) within the "RxDS3 Interrupt Enable" Register, as illustrated below.

RXDS3 INTERRUPT ENABLE REGISTER (ADDRESS = 0X12)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CP Bit Error Interrupt Enable	LOS Interrupt Enable	AIS Interrupt Enable	Idle Interrupt Enable	FERF Interrupt Enable	AIC Interrupt Enable	OOF Interrupt Enable	P-Bit Error Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Setting this bit-field to "1" enables this interrupt. Conversely, setting this bit-field to "0" disables this interrupt.

Servicing the "Change of State" on Receive AIS Interrupt

Whenever the XRT72L13 Framer IC detects this interrupt, it will do all of the following.

- It will assert the "Interrupt Request" output pin (INT*) by driving it "LOW".
- It will set Bit 5 (AIS Interrupt Status) within the "RxDS3 Interrupt Status" Register, to "1", as indicated below.

RXDS3 INTERRUPT STATUS REGISTER (ADDRESS = 0X13)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CP-Bit Error Interrupt Status	LOS Interrupt Status	AIS Interrupt Status	Idle Interrupt Status	FERF Interrupt Status	AIC Interrupt Status	OOF Interrupt Status	P-Bit Error Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	1	0	0	0	0	0

Whenever the "Terminal Equipment" encounters a "Change in AIS on Receive" interrupt, it should do the following.

1. It should determine the current state of the "AIS" condition. Recall, that this interrupt can generated, whenever the XRT72L13 Framer declares or clears the AIS defects. Hence, the user can determine the current state of the AIS defect by reading the state of Bit 7 (RxAIS), within the "RxDS3 Configuration & Status" Registers, as illustrated below

RXDS3 CONFIGURATION & STATUS REGISTER (ADDRESS = 0X10)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxAIS	RxLOS	RxIdle	RxOOF	Reserved	Framing On Parity	FSync Algo	MSync Algo
RO	RO	RO	RO	RO	RO	RO	RUR
0	0	0	0	0	0	0	0

If the AIS Condition is TRUE

1. The Local Terminal EquipmenIt should transmit a FERF (Far-End Receive Failure) to the "Remote Terminal Equipment". The XRT72L13 Framer IC automatically supports this action via the "FERF-upon-AIS" feature.
2. It should transmit the appropriate FEAC Message (per Bellcore GR-499-CORE), to the Remote Terminal, indicating that a "Service Affecting" condition has been detected in the Local Terminal Equipment.

If the AIS Condition is FALSE

1. The Local Terminal Equipment should cease transmitting a FERF (Far-End Receive Failure) indicator to the "Remote Terminal Equipment". The XRT72L13 Framer IC automatically supports this action via the "FERF-upon-AIS" feature.
2. It should transmit the appropriate FEAC Message (per Bellcore GR-499-CORE) to the Remote Terminal, indicates that the "Service Affecting" condition no longer exists.

4.3.6.2.4 The "Change of State" of Receive Idle Interrupt

If the "Change of State on Receive Idle" Interrupt is enabled, then the XRT72L13 Framer IC will generate an interrupt in response to either of the following conditions.

1. When the XRT72L13 Framer IC detects an Idle pattern, in the "incoming" DS3 data stream, and
2. When the XRT72L13 Framer IC no longer detects the Idle pattern in the "incoming" DS3 data stream.

Conditions causing the XRT72L13 Framer IC to declare an Idle condition

- If the Receive DS3 Framer block (within the XRT72L13 Framer IC) detects at least 63 DS3 frames, which contains the Idle pattern.

Conditions causing the XRT72L13 Framer IC to clear the Idle condition.

- Whenever, the "Receive DS3 Framer" block detects 63 DS3 frames, which do not contain the Idle pattern.

Enabling and Disabling the "Change of State on Receive Idle Interrupt:

The user can enable or disable the "Change of State on Receive Idle" Interrupt, by writing the appropriate value into Bit 4 (Idle Interrupt Enable) within the "RxDS3 Interrupt Enable" Register, as illustrated below.

RXDS3 INTERRUPT ENABLE REGISTER (ADDRESS = 0X12)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CP Bit Error Interrupt Enable	LOS Interrupt Enable	AIS Interrupt Enable	Idle Interrupt Enable	FERF Interrupt Enable	AIC Interrupt Enable	OOF Interrupt Enable	P-Bit Error Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Setting this bit-field to "1" enables this interrupt. Conversely, setting this bit-field to "0" disables this interrupt.

Servicing the "Change of State" on Receive Idle Interrupt

Whenever the XRT72L13 Framer IC detects this interrupt, it will do all of the following.

- It will assert the "Interrupt Request" Output pin (INT*) by driving it "LOW".
- It will set Bit 4 (Idle Interrupt Status), within the "Rx DS3 Interrupt Status" Register to "1", as indicated below.
-

RXDS3 INTERRUPT STATUS REGISTER (ADDRESS = 0X13)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CP-Bit Error Interrupt Status	LOS Interrupt Status	AIS Interrupt Status	Idle Interrupt Status	FERF Interrupt Status	AIC Interrupt Status	OOF Interrupt Status	P-Bit Error Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	1	0	0	0	0

Whenever the Terminal Equipment encounters the "Change in Idle Condition Receive" Interrupt, it should do the following.

1. It should determine the current state of the "Idle" condition. Recall, that this interrupt can generated, whenever the XRT72L13 Framer declares or clears the Idle condition. Hence, the user can determine the current state of the Idle condition by reading the state of Bit 5 (RxIdle), within the "RxDS3 Configuration & Status" Registers, as illustrated below

RXDS3 CONFIGURATION & STATUS REGISTER (ADDRESS = 0X10)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxAIS	RxLOS	RxIdle	RxOOF	Reserved	Framing On Parity	FSync Algo	MSync Algo
RO	RO	RO	RO	RO	RO	RO	RUR
0	0	0	0	0	0	0	0

4.3.6.2.5 The "Change of State" of Receive FERF Interrupt

If the "Change of State on Receive FERF" Interrupt is enabled, then the XRT72L13 Framer IC will generate an interrupt in response to either of the following conditions.

1. When the XRT72L13 Framer IC detects the FERF indicator, in the "incoming" DS3 data stream, and
2. When the XRT72L13 Framer IC no longer detects the FERF indicator, in the "incoming" DS3 data stream.

Conditions causing the XRT72L13 Framer IC to declare an FERF (Far-End-Receive Failure) condition

- If the Receive DS3 Framer block (within the XRT72L13 Framer IC) detects some "incoming" DS3 frames with both of the "X" bits set to "0".

Conditions causing the XRT72L13 Framer IC to clear the FERF condition.

- Whenever, the "Receive DS3 Framer" block starts to detect some "incoming" DS3 frames, in which the "X" bits are not set to "0".

Enabling and Disabling the "Change of State on Receive FERF Interrupt:

The user can enable or disable the "Change of State on Receive FERF" Interrupt, by writing the appropriate value into Bit 3 (FERF Interrupt Enable) within the

"RxDS3 Interrupt Enable" Register, as illustrated below.

RXDS3 INTERRUPT ENABLE REGISTER (ADDRESS = 0X12)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CP Bit Error Interrupt Enable	LOS Interrupt Enable	AIS Interrupt Enable	Idle Interrupt Enable	FERF Interrupt Enable	AIC Interrupt Enable	OOF Interrupt Enable	P-Bit Error Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Setting this bit-field to "1" enables this interrupt. Conversely, setting this bit-field to "0" disables this interrupt.

Servicing the "Change of State" on Receive FERF Interrupt

Whenever the XRT72L13 Framer IC detects this interrupt, it will do all of the following.

- It will assert the "Interrupt Request" Output pin (INT*) by driving it "high".
- It will set Bit 3 (FERF Interrupt Status), within the "Rx DS3 Interrupt Status" Register, to "1", as indicated below.
-

RXDS3 INTERRUPT STATUS REGISTER (ADDRESS = 0X13)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CP-Bit Error Interrupt Status	LOS Interrupt Status	AIS Interrupt Status	Idle Interrupt Status	FERF Interrupt Status	AIC Interrupt Status	OOF Interrupt Status	P-Bit Error Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	1	0	0	0

Whenever the Terminal Equipment encounters a "Change in FERF Condition on Receive" Interrupt, it should do the following.

1. It should determine the current state of the "FERF" condition. Recall, that this interrupt can generated, whenever the XRT72L13 Framer declares or clears the FERF condition. Hence, the user can determine the current state of the FERF condition by reading the state of Bit 5 (RxIdle), within the "RxDS3 Configuration & Status" Registers, as illustrated below

RXDS3 STATUS REGISTER (ADDRESS = 0X11)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved			RxFERF	RxAIC	RxFEBE[2:0]		
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

4.3.6.2.6 The "Change of State" of Receive AIC Interrupt

If the "Change of State of Receive AIC" Interrupt is enabled, then the XRT72L13 Framer IC will generate an interrupt, anytime the "Receive DS3 Framer" block has detected a change in the value of the "AIC" bit, within the "incoming" DS3 data stream.

Enabling and Disabling the "Change of State of Receive AIC Interrupt:

The user can enable or disable the "Change of State on Receive AIC" Interrupt, by writing the appropriate value into Bit 2 (AIC Interrupt Enable) within the

"RxDS3 Interrupt Enable" Register, as illustrated below.

RXDS3 INTERRUPT ENABLE REGISTER (ADDRESS = 0X12)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CP Bit Error Interrupt Enable	LOS Interrupt Enable	AIS Interrupt Enable	Idle Interrupt Enable	FERF Interrupt Enable	AIC Interrupt Enable	OOF Interrupt Enable	P-Bit Error Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Setting this bit-field to "1" enables this interrupt. Conversely, setting this bit-field to "0" disables this interrupt.

Servicing the "Change of State" on Receive AIC Interrupt

Whenever the XRT72L13 Framer IC detects this interrupt, it will do all of the following.

- It will assert the "Interrupt Request" Output pin (INT*) by driving it "high".
- It will set Bit 3 (AIC Interrupt Status), within the "Rx DS3 Interrupt Status" Register, to "1", as indicated below.

RXDS3 INTERRUPT STATUS REGISTER (ADDRESS = 0X13)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CP-Bit Error Interrupt Status	LOS Interrupt Status	AIS Interrupt Status	Idle Interrupt Status	FERF Interrupt Status	AIC Interrupt Status	OOF Interrupt Status	P-Bit Error Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	1	0	0

Whenever the Terminal Equipment encounters this interrupt, it should do the following.

- It should continue to check the state of the AIC bit, in order to see if this change is constant.
- If this change is constant, then the user should configure the XRT72L13 Framer IC to operate in the "M13" framing format, if the AIC bit-field is "0".
- Conversely, if the AIC bit-field is "1", then the user should configure the XRT72L13 Framer IC to operate in the "C-bit Parity" framing format.

4.3.6.2.7 The "Detection of P-Bit Error" Interrupt

If the "Detection of P-Bit Error" Interrupt is enabled, then the XRT72L13 Framer IC will generate an interrupt, anytime the "Receive DS3 Framer" block has detected a P-bit error, within the "incoming" DS3 data stream.

Enabling and Disabling the "Detection of P-Bit Error" Interrupt:

The user can enable or disable the "Detection of P-Bit Error" Interrupt, by writing the appropriate value into Bit 0 (P-Bit Error Interrupt Enable) within the "RxDS3 Interrupt Enable" Register, as illustrated below.

RXDS3 INTERRUPT ENABLE REGISTER (ADDRESS = 0X12)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CP Bit Error Interrupt Enable	LOS Interrupt Enable	AIS Interrupt Enable	Idle Interrupt Enable	FERF Interrupt Enable	AIC Interrupt Enable	OOF Interrupt Enable	P-Bit Error Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Servicing the “Detection of P-Bit Error” Interrupt

Whenever the XRT72L13 Framer IC detects this interrupt, it will do all of the following.

- It will assert the “Interrupt Request” output pin (INT*) by driving it “HIGH”.
- It will set Bit 0 (P-Bit Error Interrupt Status) within the “Rx DS3 Interrupt Status” Register, to “1”, as indicated below.

RXDS3 INTERRUPT STATUS REGISTER (ADDRESS = 0X13)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CP-Bit Error Interrupt Status	LOS Interrupt Status	AIS Interrupt Status	Idle Interrupt Status	FERF Interrupt Status	AIC Interrupt Status	OOF Interrupt Status	P-Bit Error Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	1

Whenever the “Terminal Equipment” encounters the “Detection of P-bit Error” Interrupt, it should do the following.

- It should read contents of “PMON Parity Error Count” Register (located at 0x54 and 0x55), in order to determine the number of P-bit errors recently received.

4.3.6.2.8 The “Detection of CP-Bit Error” Interrupt

If the “Detection of CP-Bit Error” Interrupt is enabled, then the XRT72L13 Framer IC will generate an interrupt, anytime the “Receive DS3 Framer” block has detected a CP-bit error, within the “incoming” DS3 data stream.

Enabling and Disabling the “Detection of CP-Bit Error” Interrupt:

The user can enable or disable the “Detection of CP-Bit Error” Interrupt, by writing the appropriate value into Bit 7 (CP-Bit Error Interrupt Enable) within the “RxDS3 Interrupt Enable” Register, as illustrated below.

RXDS3 INTERRUPT ENABLE REGISTER (ADDRESS = 0X12)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CP Bit Error Interrupt Enable	LOS Interrupt Enable	AIS Interrupt Enable	Idle Interrupt Enable	FERF Interrupt Enable	AIC Interrupt Enable	OOF Interrupt Enable	P-Bit Error Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Servicing the "Detection of CP-Bit Error" Interrupt

Whenever the XRT72L13 Framer IC detects this interrupt, it will do all of the following.

- It will assert the "Interrupt Request" output pin (INT*) by driving it "HIGH".
- It will set Bit 7 (CP-Bit Error Interrupt Status) within the "Rx DS3 Interrupt Status" Register, to "1", as indicated below.

RXDS3 INTERRUPT STATUS REGISTER (ADDRESS = 0X13)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CP-Bit Error Interrupt Status	LOS Interrupt Status	AIS Interrupt Status	Idle Interrupt Status	FERF Interrupt Status	AIC Interrupt Status	OOF Interrupt Status	P-Bit Error Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
1	0	0	0	0	0	0	1

Whenever the "Terminal Equipment" encounters the "Detection of CP-bit Error" Interrupt, it should do the following.

- It should read contents of "PMON Frame CP-Bit Error Count" Register (located at 0x72 and 0x73), in order to determine the number of CP-bit errors recently received.

4.3.6.2.9 The "Receive FEAC Message - Validation" Interrupt

If the "Receive FEAC Message - Validation" Interrupt is enabled, then the XRT72L13 Framer IC will generate an interrupt any time the "Receive FEAC Processor" validates a new FEAC (Far-End Alarm & Control) Message.

In partcular, the "Receive FEAC Processor" will validate a FEAC Message, it that same FEAC Message has been received in 8 of the last 10 FEAC Message receptions.

Enabling/Disabling the "Receive FEAC Message - Validation" Interrupt

The user can enable or disable the "Receive FEAC Message - Validation" Interrupt, by writing the appropriate data into Bit 1 (RxFEAC Valid Interrupt Enable) within the "RxDS3 FEAC Interrupt Enable/Status" Register, as indicated below.

RXDS3 FEAC INTERRUPT ENABLE/STATUS REGISTER (ADDRESS = 0X17)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			FEAC Valid	RxFEAC Remove Interrupt Enable	RxFEAC Remove Interrupt Status	RxFEAC Valid Interrupt Enable	RxFEAC Valid Interrupt Status
RO	RO	RO	RO	R/W	RUR	R/W	RUR
0	0	0	0	0	0	X	0

Setting this bit-field to "1" enables this interrupt. Conversely, setting this bit-field to "0" disables this interrupt.

Servicing the "Receive FEAC Message - Validation" Interrupt.

Whenever the XRT72L13 Framer IC generates this interrupt, it will do the following.

- It will assert the "Interrupt Request" output pin (INT*) by driving it "LOW".
- It will set Bit 0 (RxFEAC Valid Interrupt Status), within the "RxDS3 FEAC Interrupt Enable/Status" Register to "1", as indicated below.

RXDS3 FEAC INTERRUPT ENABLE/STATUS REGISTER (ADDRESS = 0X17)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			FEAC Valid	RxFEAC Remove Interrupt Enable	RxFEAC Remove Interrupt Status	RxFEAC Valid Interrupt Enable	RxFEAC Valid Interrupt Status
RO	RO	RO	RO	R/W	RUR	R/W	RUR
0	0	0	0	0	0	1	1

- It will write the contents of this “validated” FEAC Message into the “Rx DS3 FEAC” Register, as indicated below.

RXDS3 FEAC REGISTER (ADDRESS = 0X16)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	RxFEAC[5:0]						Not Used
RO	RO	RO	RO	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

Whenever the Terminal Equipment encounters the “Receive FEAC Message - Validation” Interrupt, then it should do the following.

- It should read the contents of the “RxDS3 FEAC” Register, and respond accordingly.

4.3.6.2.10 The “Receive FEAC Message - Removal” Interrupt

if the “Receive FEAC Message - Removal” Interrupt is enabled, then the XRT72L13 Framer IC will generate an interrupt any time the “Receive FEAC Processor” removes a new FEAC (Far-End Alarm & Control) Message.

In particular, the “Receive FEAC Processor” will remove a FEAC Message, it has received a different FEAC Message (from the most recently validated message) in 3 of the last 10 FEAC Message receptions.

Enabling/Disabling the “Receive FEAC Message - Removal” Interrupt

The user can enable or disable the “Receive FEAC Message - Removal” Interrupt, by writing the appropriate data into Bit 1 (RxFEAC Remove Interrupt Enable) within the “RxDS3 FEAC Interrupt Enable/Status” Register, as indicated below.

RXDS3 FEAC INTERRUPT ENABLE/STATUS REGISTER (ADDRESS = 0X17)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			FEAC Valid	RxFEAC Remove Interrupt Enable	RxFEAC Remove Interrupt Status	RxFEAC Valid Interrupt Enable	RxFEAC Valid Interrupt Status
RO	RO	RO	RO	R/W	RUR	R/W	RUR
0	0	0	0	X	0	X	0

Setting this bit-field to “1” enables this interrupt. Conversely, setting this bit-field to “0” disables this interrupt.

Servicing the “Receive FEAC Message - Validation” Interrupt.

Whenever the XRT72L13 Framer IC generates this interrupt, it will do the following.

- It will assert the “Interrupt Request” output pin (INT*) by driving it “LOW”.
- It will set Bit 2 (RxFEAC Remove Interrupt Status), within the “RxDS3 FEAC Interrupt Enable/Status” Register to “1”, as indicated below.

RXDS3 FEAC INTERRUPT ENABLE/STATUS REGISTER (ADDRESS = 0X17)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used			FEAC Valid	RxFEAC Remove Interrupt Enable	RxFEAC Remove Interrupt Status	RxFEAC Valid Interrupt Enable	RxFEAC Valid Interrupt Status
RO	RO	RO	RO	R/W	RUR	R/W	RUR
0	0	0	0	0	0	1	1

- It will write the delete contents of the most recently “validated” FEAC Message from the “Rx DS3 FEAC” Register, as indicated below.

RXDS3 FEAC REGISTER (ADDRESS = 0X16)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	RxFEAC[5:0]						Not Used
RO	RO	RO	RO	R/O	R/O	R/O	R/O
0	X	X	X	X	X	X	0

4.3.6.2.11 The “Completion of Reception of a LAPD Message” Interrupt

If the “Completion of Reception of a LAPD Message” interrupt is enabled, then the XRT72L13 Framer IC will generate an interrupt anytime the “Receive HDLC Controller” block has received a new LAPD Message buffer, from the Remote Terminal Equipment, and has stored the contents of this message in the “Receive LAPD Message” Buffer.

Enabling/Disable the “Receive LAPD Message” Interrupt

The user can enable or disable the Receive LAPD Message” Interrupt by writing the appropriate data into Bit 1 (RxLAPD Interrupt Enable) within the “RxDS3 LAPD Control” Register, as indicated below.

RXDS3 LAPD CONTROL REGISTER (ADDRESS = 0X18)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used					RxLAPD Enable	RxLAPD Interrupt Enable	RxLAPD Interrupt Status
RO	RO	RO	RO	RO	R/W	R/W	RUR
0	0	0	0	0	0	X	0

Writing a “1” into this bit-field enables the “Receive LAPD Message” Interrupt. Conversely, writing a “0” into this bit-field disables the “Receive LAPD Message” interrupt.

Servicing the “Receive LAPD Message” Interrupt

Whenever the XRT72L13 Framer IC generates this interrupt, it will do the following.

- It will assert the “Interrupt Request” output pin (INT*) by driving it “LOW”.

- It will set Bit 0 (RxLAPD Interrupt Status), within the "Rx DS3 LAPD Control" Register to "1", as indicated below.

RXDS3 LAPD CONTROL REGISTER (ADDRESS = 0X18)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used					RxLAPD Enable	RxLAPD Interrupt Enable	RxLAPD Interrupt Status
RO	RO	RO	RO	RO	R/W	R/W	RUR
0	0	0	0	0	0	1	1

- It will write the contents of this "newly" Received LAPD Message into the "Receive LAPD Message" buffer (located at 0xDE through 0x135).

Whenever the "Terminal Equipment" encounters the "Receive LAPD Interrupt", then it should read out the contents of the "Receive LAPD Message" buffer, and respond accordingly.

5.0 CHANNELIZED (M13) MODE OPERATION OF THE XRT72L13

This section will provide a detailed discussion the operation of the XRT72L713 device, when it has been configured to operate in the "Channelized" Mode.

Configuring the XRT72L13 to Operate in the "Channelized" Mode

The XRT72L13 can be configured to operate in the "Channelized" Mode by setting bit 6 (Payload HDLC Controller Enable) to "1" and bit 4 (M13 Disable) to "0", within the "M22 Configuration" Register, as illustrated below..

M23 CONFIGURATION REGISTER (ADDRESS = 0X07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	Payload HDLC Controller Enable	RxDS1Clk Gapped (CRC-32)	M13 Disable	M13 Loopback/ (Remote Loopback)	Tributary Polarity	M23 Loopback Code[1]	M23 Loopback Code[0]
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	1	X	0	X	X	X	X

5.1 AN OVERVIEW OF CHANNELIZED OPERATION

In simple terms, the XRT72L13, when it is configured to operate in the "Channelized" Mode will multiplex and de-multiplex signals via a "two-step" process. This "two-step" process is briefly discussed below.

5.1.1 In North American Applications

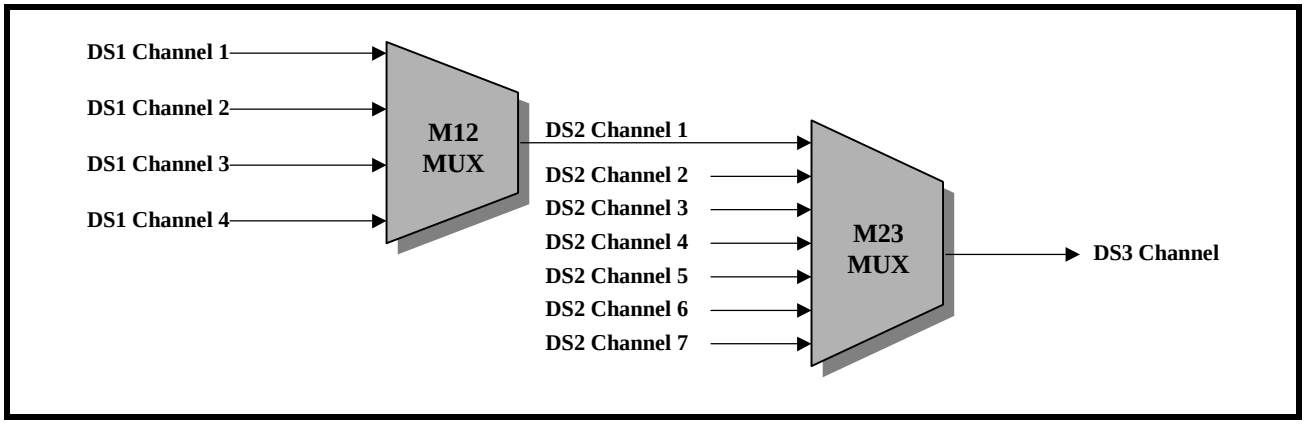
A very simple, general overview of both the "Multiplexing" and "Demultiplexing" schemes that are typically applied to DS1 and DS3 signals are briefly described below.

In the Transmit Direction:

1. The XRT72L13 will accept 28 DS1 signals, via seven (7) M12 MUX blocks. These M12 MUX blocks will multiplex these 28 DS1 signals into seven DS2 signals.
2. These seven DS2 signals will then be routed to the M23 MUX block. The M23 MUX block will multiplex these seven DS2 signals into a DS3 data stream.

This "two-step" Multiplexing Process is illustrated below in Figure 116.

FIGURE 116. SIMPLE ILLUSTRATION OF THE OVERALL SCHEME TO MUX 28 DS1 SIGNALS INTO A DS3 SIGNAL

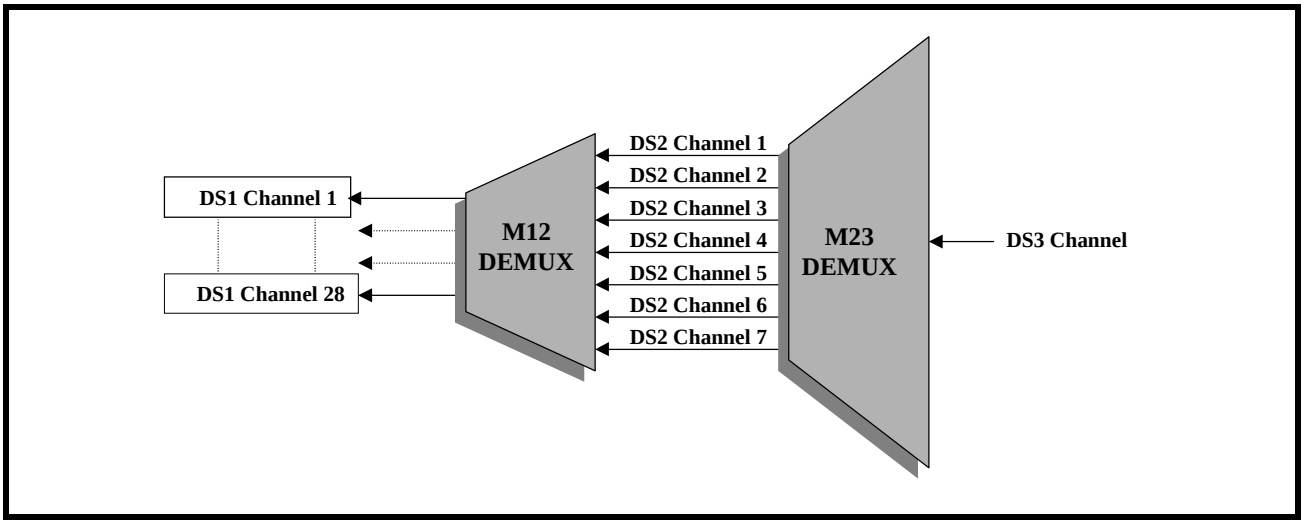


In the Receive Direction:

1. The M23 DEMUX block (within the XRT72L13) will receive a DS3 data stream and will de-multiplex it into seven DS2 signals. Each of these seven DS2 signals will then be routed to one of the 7 M12 DEMUX Blocks.
2. Each of these M12 DEMUX blocks will then de-multiplex these DS2 signals into 4 DS1 signals. Hence, a total of 28 DS1 signals will be de-multiplexed (from the DS3 signal) and will be output via the XRT72L13.

This “two-step” De-Multiplexing Process is illustrated below in Figure 117.

FIGURE 117. SIMPLE ILLUSTRATION OF THE OVERALL SCHEME TO DEMUX A DS3 SIGNAL INTO 28 DS1 SIGNALS



5.1.2 .ITU-T G.747 Applications

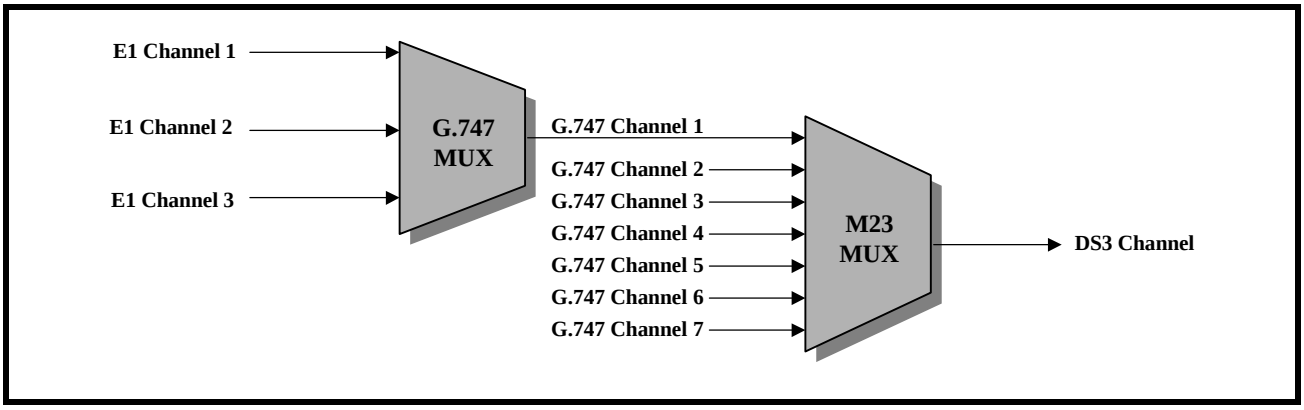
A very simple, general overview of both the “Multiplexing” and “Demultiplexing” schemes that are typically applied to E1 and DS3 signals (in “ITU-T G.747” applications) are briefly described below.

In the Transmit Direction:

1. The XRT72L13 will accept 21 E1 signals, via seven (7) M12 MUX blocks. These M12 MUX blocks will multiplex these 21 E1 signals into seven “ITU-T G.747” signals.
2. These seven “ITU-T G.747” signals will then be routed to the M23 MUX block. The M23 MUX block will multiplex these seven “ITU-T G.747” signals into a DS3 data stream.

This “two-step” Multiplexing Process is illustrated below in Figure 118.

FIGURE 118. SIMPLE ILLUSTRATION OF THE OVERALL SCHEME TO MUX 21 E1 SIGNALS INTO A DS3 SIGNAL

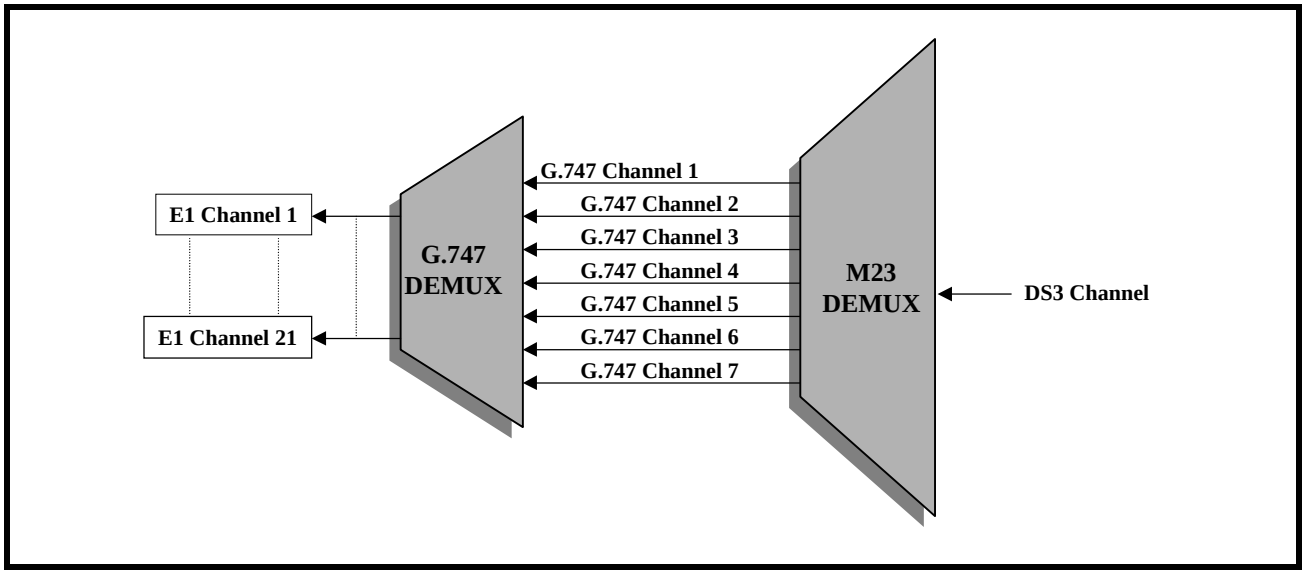


In the Receive Direction:

1. The M23 DEMUX block (within the XRT72L13) will receive a DS3 data stream and will de-multiplex it into seven “ITU-T G.747” signals. Each of these seven “ITU-T G.747” signals will then be routed to one of the 7 M12 DEMUX blocks.
2. Each of these M12 DEMUX blocks will de-multiplex these “ITU-T G.747” signals into 3 E1 signals. Hence, a total of 21 E1 signals will be multiplexed (from the DS3 signal) and will be output via the XRT72L13.

This “two-step” de-multiplexing process is illustrated below in Figure 119.

FIGURE 119. SIMPLE ILLUSTRATION OF THE OVERALL SCHEME TO DEMUX 21 E1 SIGNALS FROM A DS3 SIGNAL



5.1.3 Real Configuration Options Offered by the XRT72L13

The above-mentioned “channelized” cases were somewhat simplistic. In one case, a discussion of MUXing and DEMUXing 28 DS1 signals into/from a DS3 signal was discussed. In the other case, a discussion of MUXing and DEMUXing 21 E1 signals into/from a DS3 signal was discussed.

In reality, the XRT72L13 permits the user to MUX/DEMUX certain mixtures of DS1 and E1 signals into/from DS3 signals. The details and procedures for handling these mixtures are presented below.

5.2 CHANNELIZED OPERATION IN THE TRANSMIT DIRECTION

The XRT72L13, while operating in the “Channelized” Mode, can be configured to support either the “C-bit Parity” or “M13” Framing formats. When the XRT72L13 is configured to operate in either one of these framing formats, it affects “Channelized” Operation. As a consequence, the discussion of “Channelized Operation” of the XRT72L13 will be divided into two sections.

Section 5.1.1 - Channelized Operation of the XRT72L13, while it is configured to operate in the “M13” Framing Format.

Section 5.1.2 - Channelized Operation of the XRT72L13, while it is configured to operate in the “C-Bit Parity” Framing Format.

Each of these two sections are presented below.

5.2.1 Channelized Operation, while the XRT72L13 is operating in the “M13” Framing Format.

When the XRT72L13 has been configured to operate in the “Channelized” Mode, then each of the following blocks become active.

- The M23 MUX/DEMUX Blocks
- Seven (7) M12 MUX/DEMUX Blocks

Since section 5.1 addresses “Channelized Operation” in the “Transmit” Direction, the M12 MUX and the M23 MUX Blocks will be discussed below.

5.2.1.1 Operation of the M12 MUX Blocks

The XRT72L13 consists of seven M12 MUX blocks. The purpose of each of these MUX blocks are to

- Accept 4 DS1 signals (along with 4 corresponding DS1 clock signals) and multiplex this data into a DS2 stream.
- Accept 3 E1 signals (along with 3 corresponding E1 clock signals) and multiplex this data into an “ITU-T G.747” Data Stream.
- Accept a DS2 signal (along with the corresponding clock signal) and route this signal directly to the M23 MUX.

A more detailed description of the Operation of the M12 MUX is presented below.

5.2.1.1.1 DS1 Operation of the M12 MUX

As mentioned earlier, the XRT72L13 consists of seven (7) M12 MUX Blocks. Each of these M12 MUX blocks can be independently configured to operate in

either the DS1, the E1 (or ITU-T G.747) or the "DS2 Pass-Thru" Modes.

5.2.1.1.1.1 Configuring M12 MUX # 1 into the DS1 Mode

The user can configure M12 MUX # 1 to operate in the "DS1" Mode by setting Bits 4 (M12 G.747) and 5 (M12 By-Pass) to "0", within the "M12 DS2 # 1 Configuration" Register, as illustrated below.

M12 DS2 # 1 CONFIGURATION REGISTER (ADDRESS = 0X1A)

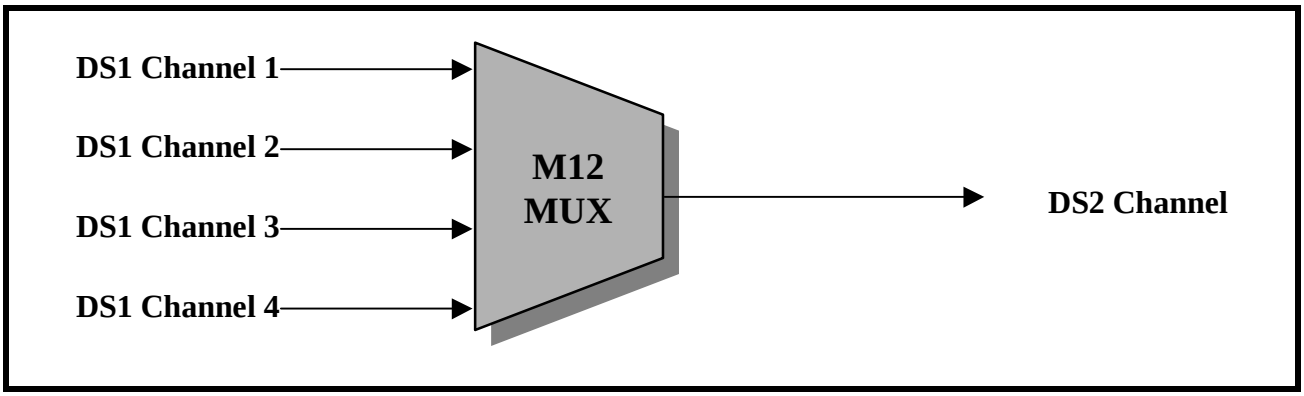
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved 7	Reserved 6	M12 Bypass	M12 G.747	M12 G.747 Res	M12 FERF	M12LBCode[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
X	X	0	0	X	X	X	X

Once the user implements this configuration setting then M12 MUX # 1 will be configured to operate in the DS1" Mode. When M12 MUX # 1 is operating in the "DS1" Mode, then it will be configured to accept four (4) DS1 signals (via the "TxDS1Data_0" through "TxDS1Data_3" input pin) and generate a DS2 signal. M12 MUX # 1 will use the rising edges of "TxDS1Clk_0" through "TxDS1Clk_3" in order to latch the contents of the "TxDS1Data[3:0] inputs into the M12 MUX # 1 circuitry.

NOTE: *Once the user configures M12 MUX #1 to operate in the "DS1" Mode, M12 DEMUX # 1 will also be configured to operate in the "DS1" Mode.*

Figure 120 presents a simple illustration of M12 MUX # 1 (which has been configured to operate in the "DS1" Mode), accepting the four DS1 signals, along with their corresponding clock signals.

FIGURE 120. ILLUSTRATION OF M12 MUX #1 BEING CONFIGURED TO OPERATE IN THE "DS1" MODE



As M12 MUX # 1 accepts these four (4) DS1 signals, it will form a "DS2" signal, by performing "bit-wise" multiplexing each of these composite DS1 signals.

As M12 MUX #1 generates this DS2 signal, it will create a data stream that has the "DS2 Framing" Structure, as presented below in Figure 121.

FIGURE 121. ILLUSTRATION OF THE DS2 FRAMING STRUCTURE

M0	I[48]	C11	I[48]	F0	I[48]	C12	I[48]	C13	I[48]	F1	I[48]
M1	I[48]	C21	I[48]	F0	I[48]	C22	I[48]	C23	I[48]	F1	I[48]
M1	I[48]	C31	I[48]	F0	I[48]	C32	I[48]	C33	I[48]	F1	I[48]
X	I[48]	C41	I[48]	F0	I[48]	C42	I[48]	C43	I[48]	F1	I[48]

Configuring the remaining M12 MUX Blocks

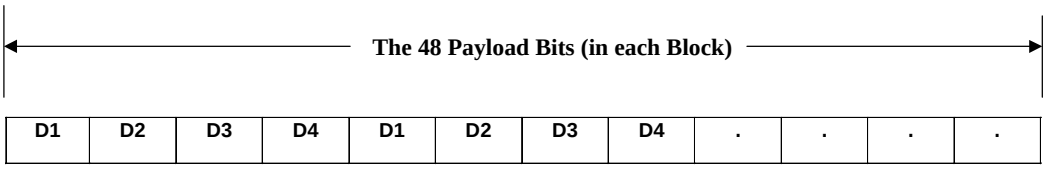
The remaining M12 MUX Blocks (e.g., M12 MUX Blocks numbers 2 through 7) can also be configured to operate in the "DS1" Mode, by setting Bits 4 (M12 G.747) and Bit 5 (M12 Bypass) to "0", within each of their corresponding "M12 DS2 Configuration" Registers (Address locations: 0x1B through 0x20).

5.2.1.1.1.1 Description of the DS2 Frames and Associated Overhead Bits

In order to fully understand and appreciate the role the M12 MUX block while it is operating in the "DS1" Mode, it is best to first describe the DS2 framing format.

The DS2 frame consists of 1176 bits, of which 24 of these bits are overhead bits, and the remaining 1152 bits are "payload" bits. The "payload" data is formatted into packets of 48 bits and the overhead (OH) bits are inserted between these payload packets. As mentioned earlier, this DS2 data stream is created by the M12 MUX performing bit-wise multiplexing of the four (input) DS1 signals. As a consequence, each of these 48-bit DS2 payload packets, consists of a repeating bit-wise multiplexing data stream, as illustrated below in Figure 122.

FIGURE 122. THE DS2 PAYLOAD BITS



NOTES:
1. D1 denotes that the source of data was from DS1 Channel #1
2. D2 denotes that the source of data was from DS1 Channel #2
3. D3 denotes that the source of data was from DS1 Channel #3
4. D4 denotes that the source of data was from DS1 Channel #4

Since each of the DS2 payload packets consists of 48 bits, then that means that each of the four DS1 signals, contributed 12 bits of data to this data stream.

The DS2 F and M Bits

Each DS2 frame consists of 8 F-bits and 3 M-bits. The purpose of these F and M bits are to permit the remote terminal equipment to acquire and maintain DS2 frame synchronization, with this data stream.

The "F" bits are used to support "sub-frame" frame synchronization; whereas the "M" bits are used to support "M" frame synchronization.

The CXX Bits

Each DS2 frame consists of 12 CXX bits. The CXX bits are used to indicate whether bit-stuffing hass occurred when the four DS1 signals were being multiplexed into this DS2 signal.

The “C1X” bits reflect the stuffing status for DS1 Channel 1 (when assembling the current DS2 frame). If all three “C1X” bits (C11, C12, and C13) are set to “0”, then stuffing was performed in DS1 Channel 1.

Conversely, if all three “C1X” bits are set to “1”, then stuffing was performed in DS1 Channel 1.

Likewise, the “C2X” bits reflect the stuffing status for DS1 Channel 2 (when assembling the current DS2 frame); and so on.

Why is Bit-Stuffing Necessary when creating the DS2 data stream

The M12 MUX accepts four (4) DS1 signals and multiplexes these signals into a DS2 signal. However, each of these four DS1 signals are asynchronous with respect to each other. Some DS1 signals may be clocked into the M12 MUX at a slightly slower or faster rate than that of another DS1 signal.

Eventually, there will be a timing slip, such that a bit (from one of the DS1 channels) which is needed to form the DS2 data stream, is not present. In this case, (in order to maintain proper timing, etc.) a “stuff” bit will be inserted into the DS2 frame. The M12 MUX will set the “CXX” bits to the appropriate value in order to reflect this bit-stuffing action. This signal will permit the “Receiving Terminal” to know what bit-stuffing has occurred, and that it should discard this extra bit.

The DS2 X-Bit

Each DS2 frame consists of a single “X” bit. The DS2 X-bit functions as the “Yellow Alarm” indicator. If a given terminal detects an LOS (Loss of Signal), AIS or LOF (Loss of Framing) condition, then that terminal will set the “X” bits (within its “outbound” DS2 frames) to “1”. The terminal will continue to set the “X” bits (within each “outbound” DS2 frame) to “1” for the duration that this defect exists. The terminal will set the “X” bits (within each “outbound” DS2 frame) to “0” during non-alarm conditions.

5.2.1.1.1.2 Additional Roles of the M12 MUX Block - DS1 Mode

As the M12 MUX block accepts the four (4) DS1 signals and multiplexes these signals into a DS2 data stream, the M12 MUX block will also do the following.

- It will insert the necessary “F” and “M” bits in order to permit an M12 DEMUX block (at the remote terminal equipment) in order to acquire and maintain DS2 frame synchronization with this particular DS2 data stream.
- It will insert the necessary “stuff-bits” and will reflect the “stuff” status within the “CXX” bits, within each outbound DS2 frame.
- If the companion M12 DEMUX block (within the XRT72L13) detects and declares a “RED Alarm” condition (e.g., an LOS, AIS or LOF condition), then the M12 MUX will set the “X” bit (within each outbound DS2 frame) to “1”. This form of siganling is also known as transmitting a “DS2 Yellow Alarm” or DS2 FERF (Far-End-Receive Failure) indicator to the remote terminal equipment. The M12 MUX will continue to set the “X” bit to “1” for the duration that this “RED Alarm” condition persists. If the corresponding M12 DEMUX block does not detect any “RED Alarm” conditions, then the M12 MUX block will set the “X” bits to “0”, which denotes the normal condition.

Obviously this “X” bit, along with the remaining DS2 bits will be multiplexed into a DS3 data stream (via the M23 MUX block). However, as this DS3 data stream is transmitted to the remote terminal equipment, and the remote terminal de-multiplexes this signal back into the seven DS2 signals, the corresponding M12 DEMUX (at the remote terminal equipment) will receive this “DS2 Yellow Alarm” indicator.

5.2.1.1.1.2.1 Forcing the “DS2 FERF” Condition

The XRT72L13 permits the user to configure (or force) a given M12 MUX block to transmit a DS2 FERF indicator to the remote terminal equipment. This can be accomplished by setting bit 2 (M12 FERF), within the appropriate “M12 DS2 Configuration” Register to “1”.

For example, if the user sets bit 2 (M12 FERF), within the “M12 DS2 Configuration” Register to “1” (as illustrated below); then M12 MUX block # 1 will begin to

transmit the “DS2 FERF” indicator to the remote terminal equipment.

M12 DS2 # 1 CONFIGURATION REGISTER (ADDRESS = 0X1A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved 7	Reserved 6	M12 Bypass	M12 G.747	M12 G.747 Res	M12 FERF	M12LBCode[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	X	1	X	X

The user can terminate this forced transmission of the “DS2 FERF” indicator by setting Bit 2 (M12 FERF) to “0”. At this point, the M12 MUX block will set the “X” bits, based upon “receive conditions” as detected by M12 DEMUX block # 1.

The user can configure any of the remaining seven (7) M12 MUX blocks to transmit a FERF condition by also setting the Bit 2 (M12 FERF), within the corresponding “M12 DS2 Configuration” Register (Address Locations 0x1B through 0x20), to “1”.

5.2.1.1.1.2.2 Forcing the “DS1 AIS” Condition

The XRT72L13 permits the user to configure (or force) a given M12 MUX block to transmit a DS1 AIS signal. This can be accomplished by setting the corresponding bits (within the appropriate “M12 DS2 AIS” Register to “1”).

An illustration of the “M12 DS2 # 1 AIS” Register, is presented below. This particular register permits the user to command the M12 MUX block to overwrite DS1 Channels 0 through 3 (e.g., the DS1 Channels associated with M12 MUX block # 1), with a DS1 AIS pattern..

M12 DS2 # 1 AIS REGISTER (ADDRESS = 0X21)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Insert AIS Rx DS1 Channel 3	Insert AIS Rx DS1 Channel 2	Insert AIS Rx DS1 Channel 1	Insert AIS Rx DS1 Channel 0	Insert AIS Tx DS1 Channel 3	Insert AIS Tx DS1 Channel 2	Insert AIS Tx DS1 Channel 1	Insert AIS Tx DS1 Channel 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	1	1	1	1

The XRT72L13 also contains “M12 DS2 AIS” Registers, which corresponds to the remaining M12 MUX blocks. Each of these register also provide bit-fields with permits the user to configure these M12 MUX blocks to overwrite any of these DS1 channels with a DS1 AIS pattern.

5.2.1.1.1.2.3 Forcing the DS2 AIS Pattern

In addition to be able to transmit a DS1 AIS pattern, the XRT72L13 permits the user to force the transmission of a DS2 AIS pattern.

This can be accomplished by setting the appropriate bit-field, within the “M23 TX DS2 AIS” Register (Address = 0x08) to “1”.

M23 TX DS2 AIS REGISTER (ADDRESS = 0X08)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	TxDS2 AIS Channel 6	TxDS2 AIS Channel 5	TxDS2 AIS Channel 4	TxDS2 AIS Channel 3	TxDS2 AIS Channel 2	TxDS2 AIS Channel 1	TxDS2 AIS Channel 0
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

For example, setting Bit 3 (TxDS2 AIS Channel 3), within the “M23 Tx DS2 AIS” register, to “1” configures M12 MUX Block # 4 to transmit a DS2 AIS signal to the remote terminal equipment. Setting this particular bit-field to “0” terminates the transmission of the DS2 AIS signal.

5.2.1.1.2 E1 (ITU-T G.747) Operation of the M12 MUX

This section discusses the various configuration options and features that are available whenever the XRT72L13 has been configured to operate in the "ITU-T G.747" Mode.

5.2.1.1.2.1 Configuring M12 MUX # 1 into the "ITU-T G.747" Mode

The user can configure M12 MUX # 1 to operate in the "ITU-T G.747" Mode by setting Bit 4 (M12 G.747) to "1" and Bit 5 (M12 By-Pass) to "0", within the "M12 DS2 # 1 Configuration" Register, as illustrated below.

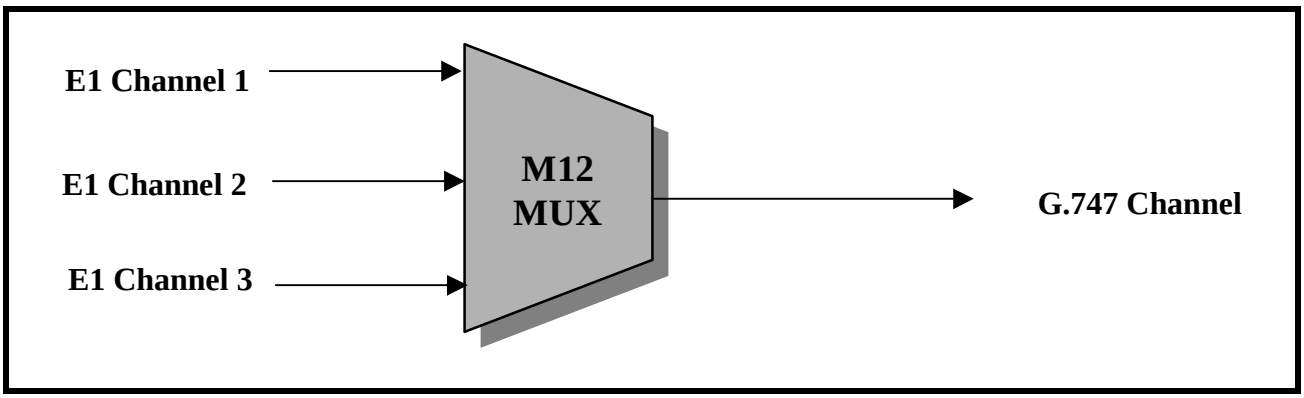
M12 DS2 # 1 CONFIGURATION REGISTER (ADDRESS = 0X1A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved 7	Reserved 6	M12 Bypass	M12 G.747	M12 G.747 Res	M12 FERF	M12LBCode[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
X	X	0	1	X	X	X	X

Once the user implements this configuration setting then M12 MUX # 1 will be configured to operate in the "ITU-T G.747" Mode. When M12 MUX # 1 is operating in the "ITU-T G.747" Mode, then it will be configured to accept three (3) E1 signals (via the "TxDS1Data_0" through "TxDS1Data_2" input pins) and generate a "G.747" data stream. M12 MUX # 1 will use the rising edges of "TxDS1Clk_0" through "TxDS1Clk_2" in order to latch the contents of the "TxDS1Data[2:0]" inputs into the "M12 MUX # 1" circuitry.

Figure 123 presents an illustration of M12 MUX # 1 (which has been configured to operate in the "G.747" Mode, accepting the three E1 signals, along with their corresponding clock signals.

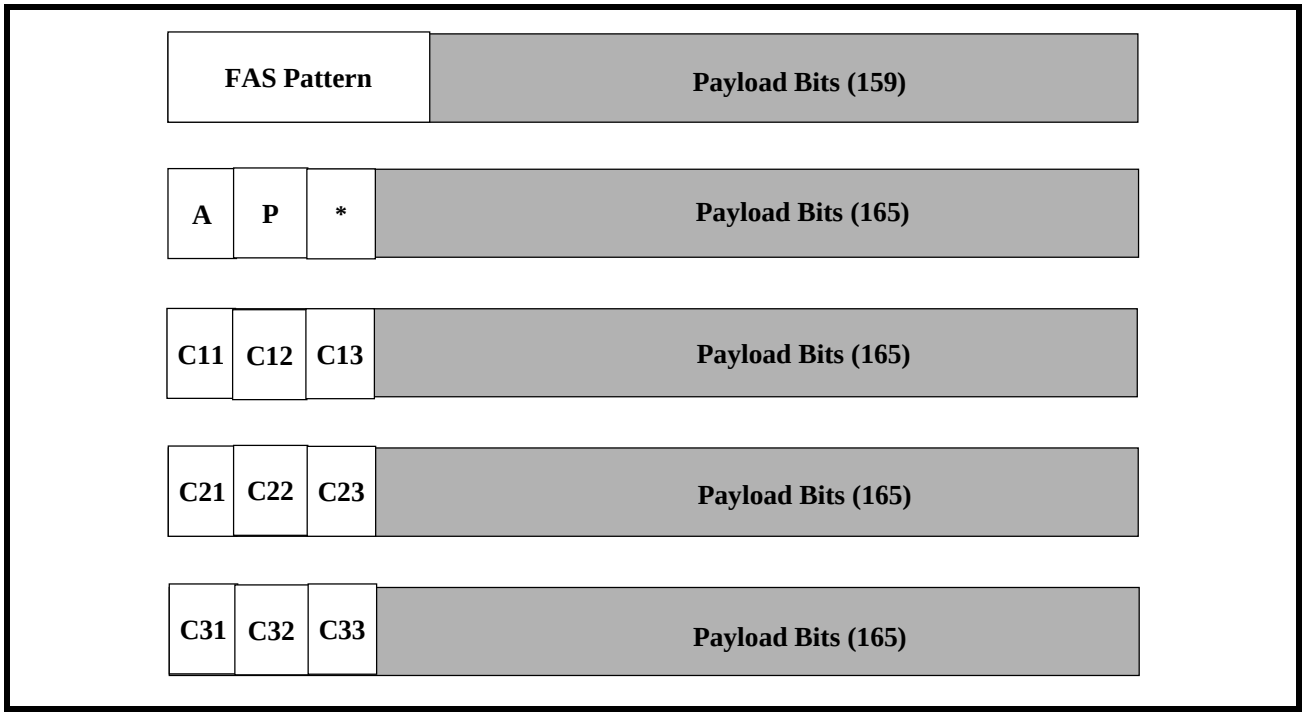
FIGURE 123. ILLUSTRATION OF THE M12 MUX # 1 BEING CONFIGURED TO OPERATE IN THE "G.747" MODE



As M12 MUX # 1 accepts these three (3) E1 signals, it will form a "G.747" data stream, by performing "bit-wise" multiplexing of the E1 signals. As M12 MUX # 1

generates this “G.747” signal, it will create a data stream that has the “G.747 Framing” structure, as presented below in Figure 124.

FIGURE 124. ILLUSTRATION OF THE “ITU-T G.747 FRAMING” STRUCTURE



Configuring the remaining M12 MUX Blocks

The remaining M12 MUX Blocks (e.g., M12 MUX Blocks numbers 2 through 7) can be configured to operate in the “G.747” Mode, by setting Bit 4 (M12 G.747) to “1” and Bit 5 (M12 Bypass) to “0”, within each of their corresponding “M12 DS2 Configuration” Registers (Address locations 0x1B through 0x20).

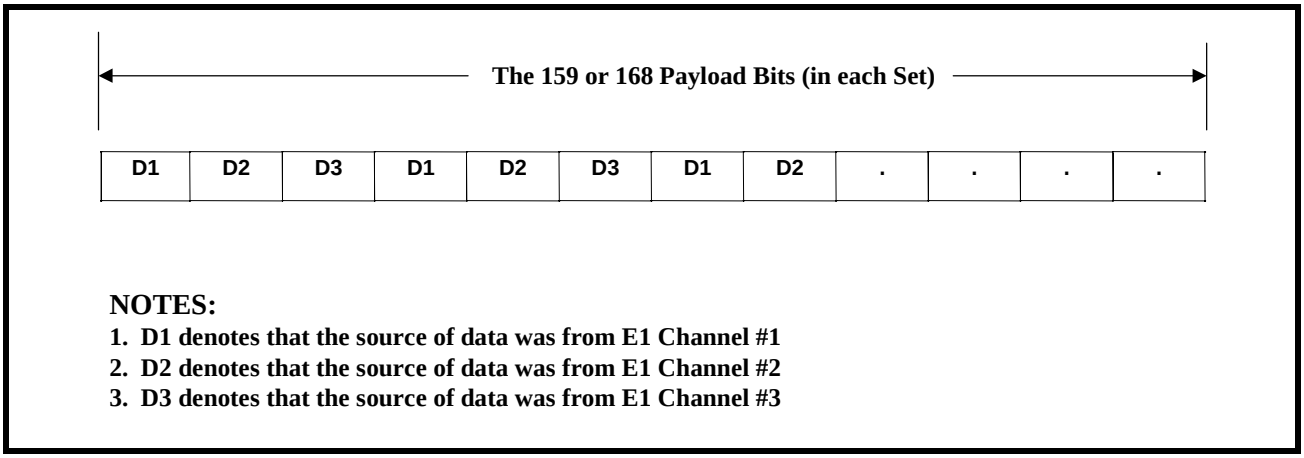
5.2.1.1.2.1.1 Description of the “ITU-T G.747” Frames and the Associated Overhead Bits

In order to fully understand and appreciate the role of the M12 MUX, it is best to first describe the “ITU-T G.747” Framing Format.

The “ITU-T G.747 Frame” consists of 840 bits, of which 24 of these bits are overhead bits, and the remaining 816 bits are “payload” bits. The “payload” data is formatted into a single packet of 159 bits (within subframe # 1); and into packets of 165 bits, within subframes # 2 through 5. As mentioned earlier, these ITU-T G.747 data streams are created by the M12 MUX performing bit-wise multiplexing of the three (input) E1 signals. As a consequence, each of these payload packets consists of a repeating bit-wise mul-

tiplexing data stream, as illustrated below in Figure 125.

FIGURE 125. THE "ITU-T G.747" PAYLOAD BITS



The "ITU-T G.747 FAS (Framing Alignment Signal) Pattern

The first nine bits, within a given "ITU-T G.747" frame functions as the Framing Alignment Signal. This nine bit quantity is assigned the following pattern.

"111010000"

This pattern permits the "Receiving Terminal" to acquire and maintain "ITU-T G.747 Frame Synchronization" with the "incoming" G.747 Frames.

The "A" Bit

The "ITU-T G.747" A bit functions as the "Yellow Alarm" indicator. If a given terminal detects an LOS (Loss of Signal), AIS or LOF (Loss of Framing) condition, then that terminal will set the "A" bit (within its "outbound" G.747 frames) to "1". The terminal will continue to set the "A" bit (within each "outbound" G.747 frame) to "1" for the duration that the defect exists. The terminal equipment will set the "A" bits (within its "outbound" G.747 frames) to "0" during "non-alarm" condition.

The "P" Bit

The "P" bits within a given G.747 frame, represents the even parity calculation result over the "payload" bits and "stuff" bits of the previous G.747 frame. This bit is used to support error detection.

The "CXX" Bits

The "CXX" bits are used to indicate whether bit-stuffing has occurred, when the three E1 signals are being multiplexed into the G.747 signal. The "C1X" bit reflects the stuffing status for E1 Channel 1 (when assembling the current G.747 frame).

If "C11" = "C12" = "C13" = 0, then no stuffing was performed in E1 channel 1. Conversely, if "C11", "C12" and "C13" are all "1", then bit-stuffing was performed in E1 channel 1. Likewise, the "C2X" bits reflect the stuffing status for E1 Channel 2 (when assembling the current G.747 frame) and the "C3X" bits reflect the stuffing status for E1 Channel 3

5.2.1.1.2.2 Additional Roles of the M12 MUX Block - G.747 Mode

As the M12 MUX block accepts the three (3) E1 signals and multiplexes these signals into an "ITU-T G.747" data stream, the M12 MUX block will also do the following.

- It will insert the "FAS" (Framing Alignment Signal) into the "outbound" G.747 data stream.
- It will compute the "P" value of a given "G.747" frame, and will insert the resulting parity value into the "P" bit-field of the very next "G.747" frame.
- It will insert the necessary "stuff" bits, and will reflect the "stuff" status within the "CXX" bits, within each "outbound" DS2 frame.
- If the "companion" M12 DEMUX block (within the XRT72L13) detects and declares a "RED Alarm" condition (e.g., an LOS, AIS or LOF condition), then the M12 MUX will set the "A" bit (within each "outbound" G.747 frame) to "1". This form of signaling is known as transmitting a "G.747 FERF" indicator to the remote terminal equipment. The M12 MUX block will continue to set the "A" bit to "1" for the duration that this "RED Alarm" condition persists. If the corresponding M12 DEMUX block does not detect any "RED Alarm" condition, then the M12 MUX block will set the "A" bit to "0", which denotes the normal condition.

5.2.1.1.2.3 Forcing the "G.747 FERF" Condition

The XRT72L13 permits the user to configure (or force) a given M12 MUX block to transmit a G.747 FERF indicator to the remote terminal equipment. This can be accomplished by setting bit 2 (M12 FERF), within the appropriate "M12 DS2 Configuration" Register, to "1".

For example, if the user sets bit 2 (M12 FERF), within the "M12 DS2 Configuration" Register to "1" (as illustrated below); then M12 MUX Block # 1 will begin to transmit the "G.747 FERF" indicator to the remote terminal equipment.

M12 DS2 # 1 CONFIGURATION REGISTER (ADDRESS = 0X1A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved 7	Reserved 6	M12 Bypass	M12 G.747	M12 G.747 Res	M12 FERF	M12LBCode[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
X	X	0	1	X	1	X	X

The user can terminate this forced transmission of the "G.747 FERF" indicator by setting Bit 2 (M12 FERF) to "0". At this point, the M12 MUX block will set the "A" bits, based upon "receive conditions" as detected by M12 DEMUX Block # 1.

5.2.1.1.2.4 Forcing the "E1 AIS" Condition

The XRT72L13 permits the user to configure (or force) a given M12 MUX block to transmit an E1 AIS signal. This can be accomplished by setting the corresponding bits (within the appropriate "M12 DS2 AIS" Register to "1").

An illustration of the "M12 DS2 # 1 AIS" Register, is presented below. This particular register permits the user to to command the M12 MUX block to overwrite E1 Channels 0 through 2 (e.g., the E1 Channels associated with M12 MUX Block # 1), with an E1 AIS signal.

M12 DS2 # 1 AIS REGISTER (ADDRESS = 0X21)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Insert AIS Rx DS1 Channel 3	Insert AIS Rx DS1 Channel 2	Insert AIS Rx DS1 Channel 1	Insert AIS Rx DS1 Channel 0	Insert AIS Tx DS1 Channel 3	Insert AIS Tx DS1 Channel 2	Insert AIS Tx DS1 Channel 1	Insert AIS Tx DS1 Channel 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	1	1	1	1

The XRT72L13 also contains "M12 DS2 AIS" Registers, which corresponds to the remaining M12 MUX blocks. Each of these registers also provide bit-fields which permits the user to configure these M12 MUX blocks to overwrite any of these E1 channels with an E1 AIS pattern.

5.2.1.1.2.5 Forcing the "G.747 AIS" Pattern

In addition to being able to transmit an E1 AIS pattern, the XRT72L13 also permits the user to force the transmission of a "G.747 AIS" pattern.

This can be accomplished by setting the appropriate bit-field, within the "M23 TX DS2 AIS" register (Address = 0x08) to "1".

M23 TX DS2 AIS REGISTER (ADDRESS = 0X08)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not Used	TxDS2 AIS Channel 6	TxDS2 AIS Channel 5	TxDS2 AIS Channel 4	TxDS2 AIS Channel 3	TxDS2 AIS Channel 2	TxDS2 AIS Channel 1	TxDS2 AIS Channel 0
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

5.2.1.1.3 DS2 "Pass-Thru" Mode Operation of the M12 MUX

This section discusses the various configuration options and features that are available whenever the XRT72L13 has been configured to operate in the "DS2 Pass-Thru" Mode.

Configuring M12 MUX # 1 into the "DS2 Pass Thru" Mode

The user can configure M12 MUX # 1 to operate in the "DS2 Pass-Thru" Mode by setting Bit 4 (M12 G.747) to "0" and Bit 5 (M12 Bypass) to "1" within the "M12 DS2 # 1 Configuration" Register, as illustrated below.

M12 DS2 # 1 CONFIGURATION REGISTER (ADDRESS = 0X1A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved 7	Reserved 6	M12 Bypass	M12 G.747	M12 G.747 Res	M12 FERF	M12LBCode[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
X	X	1	0	X	X	X	X

Once the user implements this configuration setting, then M12 MUX # 1 will be configured to operate in the "DS2 Pass-Thru" mode. When M12 MUX # 1 is operating in the "DS2 Pass-Thru" Mode, then it will be configured to accept a DS2 signal, via the "TxDS1Data_3" input pin. In this case, the M12 MUX will perform no processing on this DS2 signal, and will simply route it to the M23 MUX block.

5.2.1.2 Operation of the M23 MUX Block

As mentioned earlier, the XRT72L13 consists of seven M12 MUX blocks and a single M23 MUX block. The purpose of the M23 MUX block is to accept seven signals (which can either be DS2 signals or "ITU-T G.747" signals, from each of the seven M12 MUX blocks); and to multiplex these signals into a DS3 data stream.

5.2.2 Channelized Operation, while the XRT72L13 is operating in the "C-Bit Parity" Framing Format.

5.3 CHANNELIZED OPERATION IN THE RECEIVE DIRECTION

5.3.1 Channelized Operation, while the XRT72L13 is operating in the "M13" Framing Format.

5.3.1.1 Operation of the M23 DEMUX Block

The purpose of the M23 DEMUX Block is to accept a DS3 data stream, and to de-multiplex this data into seven signals. These signals can either be DS2 signals or "ITU-T G.747" signals. The output of the M23 DEMUX block will then be routed to each of the various M12 DEMUX Blocks.

5.3.1.2 Operation of the M12 DEMUX Blocks

The XRT72L13 consists of seven M12 DEMUX blocks. The purpose of each of these blocks are to:

- Accept a DS2 signal (from the M23 DEMUX) and to de-multiplex these signals into four DS1 signals.
- Accepts a "G.747" signal (from the M23 DEMUX) and to de-multiplex these signals into three E1 signals.
- Accept a DS2 signal from the M23 DEMUX, and (if configured) route this signal directly to the output pins.

A more detailed description of the Operation of the M12 DEMUX is presented below.

5.3.1.2.1 DS1 Operation of the M12 DEMUX

As mentioned earlier, the XRT72L13 consists of seven (7) M12 MUX blocks. Each of these M12 MUX blocks can be independently configured to operate in either DS1, the E1 (or ITU-T G.747) or the "DS2 Pass-Thru" Mode.

5.3.1.2.1.1 Configuring the M12 DEMUX # 1 into the DS1 Mode

The user can configure M12 DEMUX # 1 to operate in the "DS1" Mode by setting Bits 4 (M12 G.747) and 5 (M12 By-Pass) to "0", within the "M12 DS2 # 1 Configuration" Register, as illustrated below.

M12 DS2 # 1 CONFIGURATION REGISTER (ADDRESS = 0X1A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved 7	Reserved 6	M12 Bypass	M12 G.747	M12 G.747 Res	M12 FERF	M12LBCode[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
X	X	0	0	X	X	X	X

Once the user implements this configuration setting then M12 DEMUX # 1 will be configured to operate in the DS1" Mode. When M12 DEMUX # 1 is operating in the "DS1" Mode, then it will then be configured to accept a DS2 signal, and de-multiplex this signal into 4 DS1 signals. M12 DEMUX # 1 will then output this signal (via the "RxDS1Data_0" through "RxDS1Data_3" output pins). M12 DEMUX # 1 will output this demultiplexed data upon the rising edges of "RxDS1Clk_0" through "RxDS1Clk_3".

Configuring the remaining M12 DEMUX Blocks

The remaining M12 DEMUX blocks (e.g., M12 DE-MUX Block numbers 2 thorugh 7) can also be configured to operate in the "DS1" Mode, by setting Bits 4 (M12 G.747) and Bit 5 (M12 Bypass) to "0", within each of their corresponding "M12 DS2 Configuration" Registers (Address Locations: 0x1B through 0x20).

5.3.1.2.1.2 Additional Roles of the M12 DEMUX Blocks - DS1 Mode

As the M12 DEMUX block accepts the DS2 data stream and de-multiplexes it into 4 DS1 signals, the M12 DEMUX block will also do the following.

- It will acquire and maintain DS2 synchronization (via the "F" and "M" bits). If the M12 DEMUX were to fail to maintain DS2 frame synchronization, then it will declare a "DS2 OOF" condition.
- It will also detect and declare a "DS2 AIS" and "DS2 FERF" condition.
- It will detect and flag the occurrences of "F" and "M" bit errors.

5.3.1.2.1.2.1 Declaring and Clearing the DS2 OOF Condition

It a given M12 DEMUX declares a "DS2 OOF" condition, then it will do so by setting Bit 4 (DS2 OOF Status), within the corresponding "DS2 Framer Status" Register to "1". An illustration of Bit 4 being set to "1", within the "DS2 # 1 Framer Status" Register, is presented below.

DS2 # 1 FRAMER STATUS REGISTER (ADDRESS = 0XA3)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		DS2 COFA Status	DS2 OOF Status	DS2 FERF Status	DS2 RED Alarm Status	DS2 AIS Status	DS2 RESV Status
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	1	0	0	0	0

NOTE: *The M12 DEMUX will also generate a "Change in DS2 OOF Condition" Interrupt, if it detects or clears the "DS2 OOF" condition.*

When the M12 DEMUX ceases to declares the "DS2 OOF" condition, then it will set this bit-field back to "0", in order to reflect "normal" operation.

NOTE: *The locations of the remaining "DS2 Framer Status" register (for the remaining M12 DEMUX blocks) are at Address locations 0xA4 through 0xA9.*

5.3.1.2.1.2.2 Declaring and Clearing the DS2 AIS Condition

It a given M12 DEMUX declares a "DS2 AIS" condition, then it will do so by setting Bit 2 (DS2 AIS Status), within the corresponding "DS2 Framer Status" Register to "1". An illustration of Bit 4 being set to "1", within the "DS2 # 1 Framer Status" Register, is presented below.

DS2 # 1 FRAMER STATUS REGISTER (ADDRESS = 0XA3)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		DS2 COFA Status	DS2 OOF Status	DS2 FERF Status	DS2 RED Alarm Status	DS2 AIS Status	DS2 RESV Status
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	1	0

NOTE: *The M12 DEMUX will also generate a "Change in DS2 AIS Condition" Interrupt, if it detects or clears the "DS2 AIS" condition.*

When the M12 DEMUX ceases to declares the "DS2 AIS" condition, then it will set this bit-field back to "0", in order to reflect "normal" operation.

NOTE: The locations of the remaining "DS2 Framer Status" register (for the remaining M12 DEMUX blocks) are at Address locations 0xA4 through 0xA9.

5.3.1.2.1.2.3 Declaring and Clearing the DS2 FERF Condition

It a given M12 DEMUX declares a "DS2 FERF" condition, then it will do so by setting Bit 3 (DS2 FERF Status), within the corresponding "DS2 Framer Status" Register to "1". An illustration of Bit 3 being set to "1", within the "DS2 # 1 Framer Status" Register, is presented below.

DS2 # 1 FRAMER STATUS REGISTER (ADDRESS = 0XA3)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		DS2 COFA Status	DS2 OOF Status	DS2 FERF Status	DS2 RED Alarm Status	DS2 AIS Status	DS2 RESV Status
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	1	0	0	0

NOTE: The M12 DEMUX will also generate a "Change in DS2 FERF Condition" Interrupt, if it detects or clears the "DS2 FERF" condition.

When the M12 DEMUX ceases to declares the "DS2 FERF" condition, then it will set this bit-field back to "0", in order to reflect "normal" operation.

NOTE: The locations of the remaining "DS2 Framer Status" register (for the remaining M12 DEMUX blocks) are at Address locations 0xA4 through 0xA9.

5.3.1.2.2 E1 (ITU-T G.747) Operation

The user can configure M12 DEMUX # 1 to operate in the "ITU-T G.747" Mode by setting Bit 4 (M12 G.747) to "1" and Bit 5 (M12 By-Pass) to "0", within the "M12 DS2 # 1 Configuration" Register, as illustrated below.

M12 DS2 # 1 CONFIGURATION REGISTER (ADDRESS = 0X1A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved 7	Reserved 6	M12 Bypass	M12 G.747	M12 G.747 Res	M12 FERF	M12LBCode[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
X	X	0	1	X	X	X	X

Once the user implements this configuration setting then M12 DEMUX # 1 will be configured to operate in the "ITU-T G.747" Mode. When M12 DEMUX # 1 is operating in the "ITU-T G.747" Mode, then it will be configured to accept a "G.747" data stream, from the M23 DEMUX block, and then de-multiplex this signal into three (3) E1 signals. M12 DEMUX # 1 will then output this signal (via the "RxDS1Data_0" through "RxDS1Data_2" output pins). M12 DEMUX # 2 will output this demultiplexed data upon the rising edges of "RxDS1Clk_0" through "RxDS1Clk_2".

Configuring the remaining M12 DEMUX Blocks

The remaining M12 DEMUX blocks (e.g., M12 DEMUX Block numbers 2 thorugh 7) can also be configured to operate in the "E1" Mode, by setting Bit 4 (M12 G.747) to "1" and Bit 5 (M12 Bypass) to "0", within each of their corresponding "M12 DS2 Configuration" Registers (Address Locations: 0x1B through 0x20).

5.3.1.2.2.1 Additional Roles of the M12 DEMUX Blocks - E1 Mode

As the M12 DEMUX block accepts the DS2 data stream and de-multiplexes it into 3 E1 signals, the M12 DEMUX block will also do the following.

- It will acquire and maintain "G.747" synchronization (via the "FAS" pattern). If the M12 DEMUX were to fail to maintain G.747 frame synchronization, then it will declare a "G.747 OOF" condition.
- It will also detect and declare a "G.747 AIS" and "G.747 FERF" condition.

- It will detect and flag the occurrences of “FAS” bit errors.
- It will detect and flag the occurrences of “P” bit errors.

5.3.1.2.3 DS2 “Pass-Thru” Mode Operation

The user can configure M12 DEMUX # 1 to operate in the “DS2 Pass-Thru” Mode by setting Bit 4 (M12 G.747) to “0” and Bit 5 (M12 Bypass) to “1” within the “M12 DS2 # 1 Configuration” Register, as illustrated below.

M12 DS2 # 1 CONFIGURATION REGISTER (ADDRESS = 0X1A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved 7	Reserved 6	M12 Bypass	M12 G.747	M12 G.747 Res	M12 FERF	M12LBCode[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
X	X	1	0	X	X	X	X

Once the user implements this configuration setting, then M12 DEMUX # 1 will be configured to operate in the “DS2 Pass-Thru” mode. When M12 DEMUX # 1 is operating in the “DS2 Pass-Thru” Mode, then it will be configured to accept a DS2 signal from the M23 DEMUX. Afterwards, M12 DEMUX # 1 will simply output this signal via the “RxDS1Data_3” output pin. In this case, the M12 DEMUX will perform no processing on this DS2 signal.

Configuring the remaining M12 DEMUX Blocks

The remaining M12 DEMUX blocks (e.g., M12 DEMUX Block numbers 2 thorugh 7) can also be configured to operate in the “DS2-Pass Thru” Mode, by setting Bits 4 (M12 G.747) to “0” and Bit 5 (M12 Bypass) to “1”, within each of their corresponding “M12 DS2 Configuration” Registers (Address Locations: 0x1B through 0x20).

5.3.1.2.3.1 Additional Roles of the M12 DEMUX Blocks - DS2 Pass-Thru Mode

As the M12 DEMUX block accepts the DS2 data stream it will also do the following.

- It will acquire and maintain DS2 synchronization (via the “F” and “M” bits). If the M12 DEMUX were to fail to maintain DS2 frame synchronization, then it will declare a “DS2 OOF” condition.
- It will also detect and declare a “DS2 AIS” and “DS2 FERF” condition.
- It will detect and flag the occurrences of “F” and “M” bit errors.

5.3.1.2.3.1.1 Declaring and Clearing the DS2 OOF Condition

It a given M12 DEMUX declares a “DS2 OOF” condition, then it will do so by setting Bit 4 (DS2 OOF Status), within the corresponding “DS2 Framer Status” Register to “1”. An illustration of Bit 4 being set to “1”, within the “DS2 # 1 Framer Status” Register, is presented below.

DS2 # 1 FRAMER STATUS REGISTER (ADDRESS = 0XA3)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		DS2 COFA Status	DS2 OOF Status	DS2 FERF Status	DS2 RED Alarm Status	DS2 AIS Status	DS2 RESV Status
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	1	0	0	0	0

NOTE: *The M12 DEMUX will also generate a “Change in DS2 OOF Condition” Interrupt, if it detects or clears the “DS2 OOF” condition.*

When the M12 DEMUX ceases to declares the “DS2 OOF” condition, then it will set this bit-field back to “0”, in order to reflect “normal” operation.

NOTE: *The locations of the remaining “DS2 Framer Status” register (for the remaining M12 DEMUX blocks) are at Address locations 0xA4 through 0xA9.*

5.3.1.2.3.1.2 Declaring and Clearing the DS2 AIS Condition

It a given M12 DEMUX declares a “DS2 AIS” condition, then it will do so by setting Bit 2 (DS2 AIS Status), within the corresponding “DS2 Framer Status” Register to “1”. An illustration of Bit 4 being set to “1”, within the “DS2 # 1 Framer Status” Register, is presented below.

DS2 # 1 FRAMER STATUS REGISTER (ADDRESS = 0XA3)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		DS2 COFA Status	DS2 OOF Status	DS2 FERF Status	DS2 RED Alarm Status	DS2 AIS Status	DS2 RESV Status
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	1	0

NOTE: *The M12 DEMUX will also generate a "Change in DS2 AIS Condition" Interrupt, if it detects or clears the "DS2 AIS" condition.*

When the M12 DEMUX ceases to declares the "DS2 AIS" condition, then it will set this bit-field back to "0", in order to reflect "normal" operation.

NOTE: *The locations of the remaining "DS2 Framer Status" register (for the remaining M12 DEMUX blocks) are at Address locations 0xA4 through 0xA9.*

5.3.1.2.3.1.3 Declaring and Clearing the DS2 FERF Condition

It a given M12 DEMUX declares a "DS2 FERF" condition, then it will do so by setting Bit 3 (DS2 FERF Status), within the corresponding "DS2 Framer Status" Register to "1". An illustration of Bit 3 being set to "1", within the "DS2 # 1 Framer Status" Register, is presented below.

DS2 # 1 FRAMER STATUS REGISTER (ADDRESS = 0XA3)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		DS2 COFA Status	DS2 OOF Status	DS2 FERF Status	DS2 RED Alarm Status	DS2 AIS Status	DS2 RESV Status
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	1	0	0	0

NOTE: *The M12 DEMUX will also generate a "Change in DS2 FERF Condition" Interrupt, if it detects or clears the "DS2 FERF" condition.*

When the M12 DEMUX ceases to declares the "DS2 FERF" condition, then it will set this bit-field back to "0", in order to reflect "normal" operation.

NOTE: *The locations of the remaining "DS2 Framer Status" register (for the remaining M12 DEMUX blocks) are at Address locations 0xA4 through 0xA9.*

5.3.2 Channelized Operation, while the XRT72L13 is operating in the "C-Bit Parity" Framing Format.

5.4 DIAGNOSTIC OPERATIONS - CHANNELIZED MODE

5.4.1 M12 MUX (DS1 or E1) Loop-backs

5.4.2 M23 MUX (DS2 or G.747) Loop-backs

5.5 CHANNELIZED MODE INTERRUPTS

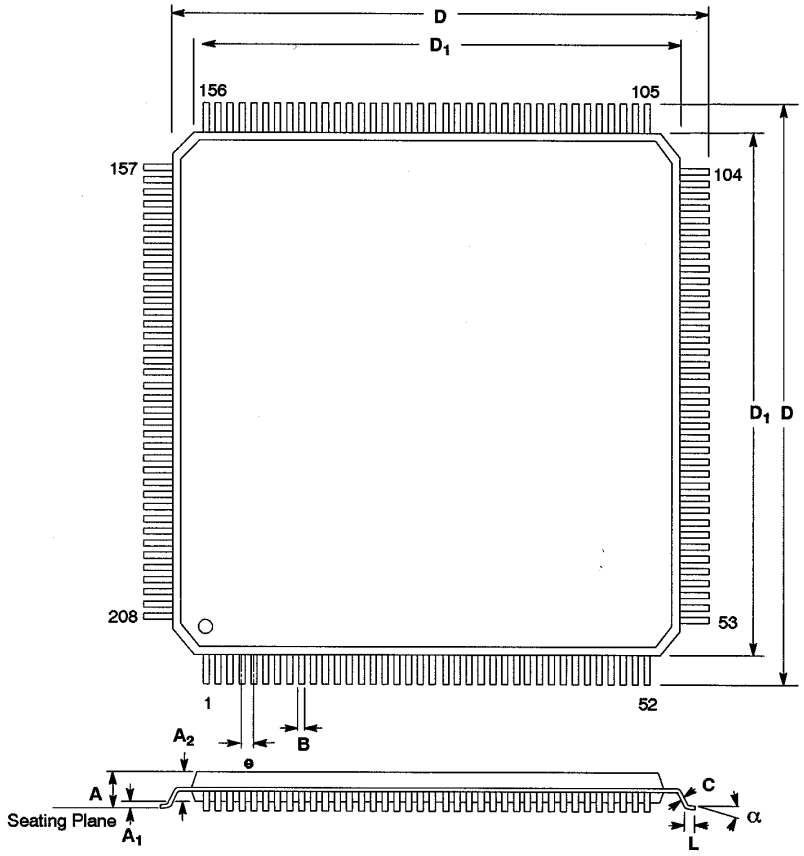
ORDERING INFORMATION

PART #	PACKAGE	OPERATING TEMPERATURE
XRT72L13IQ	208 pin PQFP	-40°C to +85°C

PACKAGE DIMENSIONS

208 LEAD PLASTIC QUAD FLAT PACK
(28 mm x 28 mm, QFP)

Rev. 1.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.128	0.161	3.25	4.10
A_1	0.002	0.020	0.05	0.50
A_2	0.126	0.142	3.20	3.60
B	0.007	0.011	0.17	0.27
C	0.004	0.008	0.09	0.20
D	1.197	1.212	30.40	30.80
D_1	1.098	1.106	27.90	28.10
e	0.0197 BSC		0.50 BSC	
L	0.018	0.030	0.45	0.75
α	0°	8°	0°	8°

Note: The control dimension is the millimeter column

REVISIONS

Rev. 1.0.4 Modified Pin Description, Sect 1 and sect 3.

Rev. 1.0.6 Added electrical tables missing from previous version.

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