

DATA SHEET

Xilinx has acquired the entire Philips CoolRunner Low Power CPLD Product Family. For more technical or sales information, please see: www.xilinx.com

XCR3064 64 macrocell CPLD

Product specification
Supersedes data of 1997 Mar 05
IC27 Data Handbook

1998 Jul 23

64 macrocell CPLD

XCR3064

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FEATURES

- Industry's first TotalCMOS™ PLD – both CMOS design and process technologies
- Fast Zero Power (FZP™) design technique provides ultra-low power and very high speed
- High speed pin-to-pin delays of 10ns
- Ultra-low static power of less than 50µA
- Dynamic power that is 70% lower at 50MHz than competing devices
- 100% routable with 100% utilization while all pins and all macrocells are fixed
- Deterministic timing model that is extremely simple to use
- 4 clocks with programmable polarity at every macrocell
- Support for asynchronous clocking
- Innovative XPLA™ architecture combines high speed with extreme flexibility
- 1000 erase/program cycles guaranteed
- 20 years data retention guaranteed
- Logic expandable to 37 product terms
- PCI compliant
- Advanced 0.5µ E²CMOS process
- Security bit prevents unauthorized access
- Design entry and verification using industry standard and Philips CAE tools
- Reprogrammable using industry standard device programmers
- Innovative Control Term structure provides either sum terms or product terms in each logic block for:
 - Programmable 3-State buffer
 - Asynchronous macrocell register preset/reset
- Programmable global 3-State pin facilitates 'bed of nails' testing without using logic resources
- Available in PLCC, TQFP, and PQFP packages
- Available in both Commercial and Industrial grades

Table 1. PZ3064 Features

| | PZ3064 |
|------------------------|--|
| Usable gates | 2000 |
| Maximum inputs | 68 |
| Maximum I/Os | 64 |
| Number of macrocells | 64 |
| Propagation delay (ns) | 10 |
| Packages | 44-pin PLCC, 44-pin TQFP, 68-pin PLCC, 84-pin PLCC, 100-pin PQFP |

DESCRIPTION

The PZ3064 CPLD (Complex Programmable Logic Device) is the second in a family of Fast Zero Power (FZP™) CPLDs from Philips Semiconductors. These devices combine high speed and zero power in a 64 macrocell CPLD. With the FZP™ design technique, the PZ3064 offers true pin-to-pin speeds of 10ns, while simultaneously delivering power that is less than 50µA at standby without the need for 'turbo bits' or other power down schemes. By replacing conventional sense amplifier methods for implementing product terms (a technique that has been used in PLDs since the bipolar era) with a cascaded chain of pure CMOS gates, the dynamic power is also substantially lower than any competing CPLD – 70% lower at 50MHz. These devices are the first TotalCMOS™ PLDs, as they use both a CMOS process technology **and** the patented full CMOS FZP™ design technique. For 5V applications, Philips also offers the high speed PZ5064 CPLD that offers these features in a full 5V implementation.

The Philips FZP™ CPLDs introduce the new patent-pending XPLA™ (eXtended Programmable Logic Array) architecture. The XPLA™ architecture combines the best features of both PLA and PAL™ type structures to deliver high speed and flexible logic allocation that results in superior ability to make design changes with fixed pinouts. The XPLA™ structure in each logic block provides a fast 10ns PAL™ path with 5 dedicated product terms per output. This PAL™ path is joined by an additional PLA structure that deploys a pool of 32 product terms to a fully programmable OR array that can allocate the PLA product terms to any output in the logic block. This combination allows logic to be allocated efficiently throughout the logic block and supports as many as 37 product terms on an output. The speed with which logic is allocated from the PLA array to an output is only 2.5ns, regardless of the number of PLA product terms used, which results in worst case t_{PD}'s of only 12.5ns from any pin to any other pin. In addition, logic that is common to multiple outputs can be placed on a single PLA product term and shared across multiple outputs via the OR array, effectively increasing design density.

The PZ3064 CPLDs are supported by industry standard CAE tools (Cadence, Mentor, Minc, Exemplar Logic, Synplicity, Synopsys, Synario, Viewlogic, MINC), using text (Abel, VHDL, Verilog) and/or schematic entry. Design verification uses industry standard simulators for functional and timing simulation. Development is supported on personal computer, Sparc, and HP platforms. Device fitting uses either Minc or Philips Semiconductors-developed tools.

The PZ3064 CPLD is reprogrammable using industry standard device programmers from vendors such as Data I/O, BP Microsystems, SMS, and others.

64 macrocell CPLD

PZ3064

ORDERING INFORMATION

| ORDER CODE | DESCRIPTION | DESCRIPTION | DRAWING NUMBER |
|--------------|-----------------------------|--|----------------|
| PZ3064-10A44 | 44-pin PLCC, 10ns t_{PD} | Commercial temp range, 3.3 volt power supply, $\pm 10\%$ | SOT187-2 |
| PZ3064-12A44 | 44-pin PLCC, 12ns t_{PD} | Commercial temp range, 3.3 volt power supply, $\pm 10\%$ | SOT187-2 |
| PZ3064I12A44 | 44-pin PLCC, 12ns t_{PD} | Industrial temp range, 3.3 volt power supply, $\pm 10\%$ | SOT187-2 |
| PZ3064I15A44 | 44-pin PLCC, 15ns t_{PD} | Industrial temp range, 3.3 volt power supply, $\pm 10\%$ | SOT187-2 |
| PZ3064-10BC | 44-pin TQFP, 10ns t_{PD} | Commercial temp range, 3.3 volt power supply, $\pm 10\%$ | SOT376-1 |
| PZ3064-12BC | 44-pin TQFP, 12ns t_{PD} | Commercial temp range, 3.3 volt power supply, $\pm 10\%$ | SOT376-1 |
| PZ3064I12BC | 44-pin TQFP, 12ns t_{PD} | Industrial temp range, 3.3 volt power supply, $\pm 10\%$ | SOT376-1 |
| PZ3064I15BC | 44-pin TQFP, 15ns t_{PD} | Industrial temp range, 3.3 volt power supply, $\pm 10\%$ | SOT376-1 |
| PZ3064-10A68 | 68-pin PLCC, 10ns t_{PD} | Commercial temp range, 3.3 volt power supply, $\pm 10\%$ | SOT188-3 |
| PZ3064-12A68 | 68-pin PLCC, 12ns t_{PD} | Commercial temp range, 3.3 volt power supply, $\pm 10\%$ | SOT188-3 |
| PZ3064I12A68 | 68-pin PLCC, 12ns t_{PD} | Industrial temp range, 3.3 volt power supply, $\pm 10\%$ | SOT188-3 |
| PZ3064I15A68 | 68-pin PLCC, 15ns t_{PD} | Industrial temp range, 3.3 volt power supply, $\pm 10\%$ | SOT188-3 |
| PZ3064-10A84 | 84-pin PLCC, 10ns t_{PD} | Commercial temp range, 3.3 volt power supply, $\pm 10\%$ | SOT189-3 |
| PZ3064-12A84 | 84-pin PLCC, 12ns t_{PD} | Commercial temp range, 3.3 volt power supply, $\pm 10\%$ | SOT189-3 |
| PZ3064I12A84 | 84-pin PLCC, 12ns t_{PD} | Industrial temp range, 3.3 volt power supply, $\pm 10\%$ | SOT189-3 |
| PZ3064I15A84 | 84-pin PLCC, 15ns t_{PD} | Industrial temp range, 3.3 volt power supply, $\pm 10\%$ | SOT189-3 |
| PZ3064-10BB1 | 100-pin PQFP, 10ns t_{PD} | Commercial temp range, 3.3 volt power supply, $\pm 10\%$ | SOT382-1 |
| PZ3064-12BB1 | 100-pin PQFP, 12ns t_{PD} | Commercial temp range, 3.3 volt power supply, $\pm 10\%$ | SOT382-1 |
| PZ3064I12BB1 | 100-pin PQFP, 12ns t_{PD} | Industrial temp range, 3.3 volt power supply, $\pm 10\%$ | SOT382-1 |
| PZ3064I15BB1 | 100-pin PQFP, 15ns t_{PD} | Industrial temp range, 3.3 volt power supply, $\pm 10\%$ | SOT382-1 |

XPLA™ ARCHITECTURE

Figure 1 shows a high level block diagram of a 64 macrocell device implementing the XPLA™ architecture. The XPLA™ architecture consists of logic blocks that are interconnected by a Zero-power Interconnect Array (ZIA). The ZIA is a virtual crosspoint switch. Each logic block is essentially a 36V16 device with 36 inputs from the ZIA and 16 macrocells. Each logic block also provides 32 ZIA feedback paths from the macrocells and I/O pins.

From this point of view, this architecture looks like many other CPLD architectures. What makes the CoolRunner™ family unique is what is inside each logic block and the design technique used to implement these logic blocks. The contents of the logic block will be described next.

Logic Block Architecture

Figure 2 illustrates the logic block architecture. Each logic block contains control terms, a PAL array, a PLA array, and 16 macrocells. The 6 control terms can individually be configured as either SUM or PRODUCT terms, and are used to control the preset/reset and output enables of the 16 macrocells' flip-flops. The PAL array consists of a programmable AND array with a fixed OR array, while the PLA array consists of a programmable AND array with a programmable OR array. The PAL array provides a high speed path through the array, while the PLA array provides increased product term density.

Each macrocell has 5 dedicated product terms from the PAL array. The pin-to-pin t_{PD} of the PZ3064 device through the PAL array is 10ns. If a macrocell needs more than 5 product terms, it simply gets the additional product terms from the PLA array. The PLA array consists of 32 product terms, which are available for use by all 16 macrocells. The additional propagation delay incurred by a macrocell using 1 or all 32 PLA product terms is just 2.5ns. So the total pin-to-pin t_{PD} for the PZ3064 using 6 to 37 product terms is 12.5ns (10ns for the PAL + 2.5ns for the PLA).

64 macrocell CPLD

PZ3064

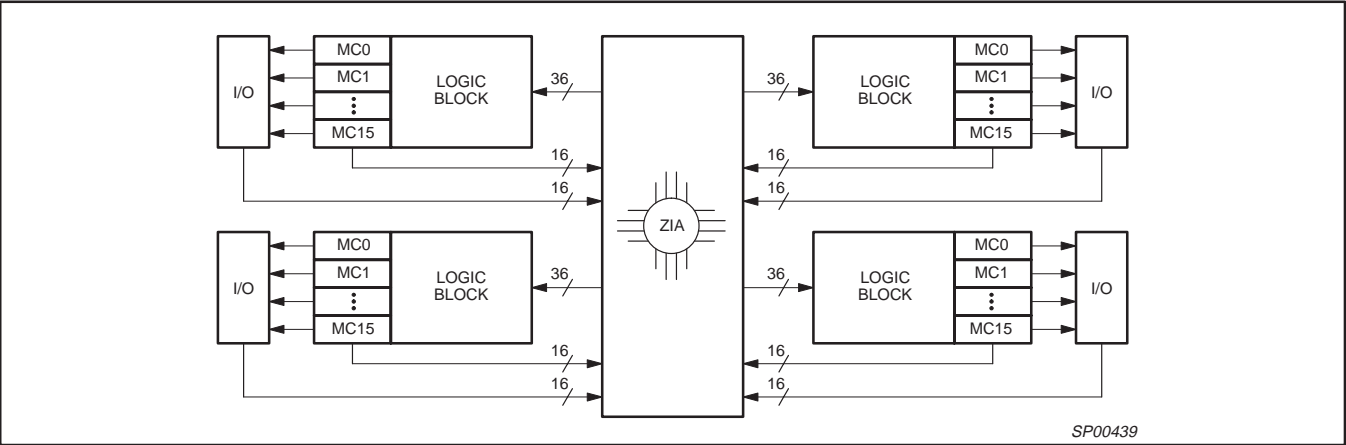


Figure 1. Philips XPLA CPLD Architecture

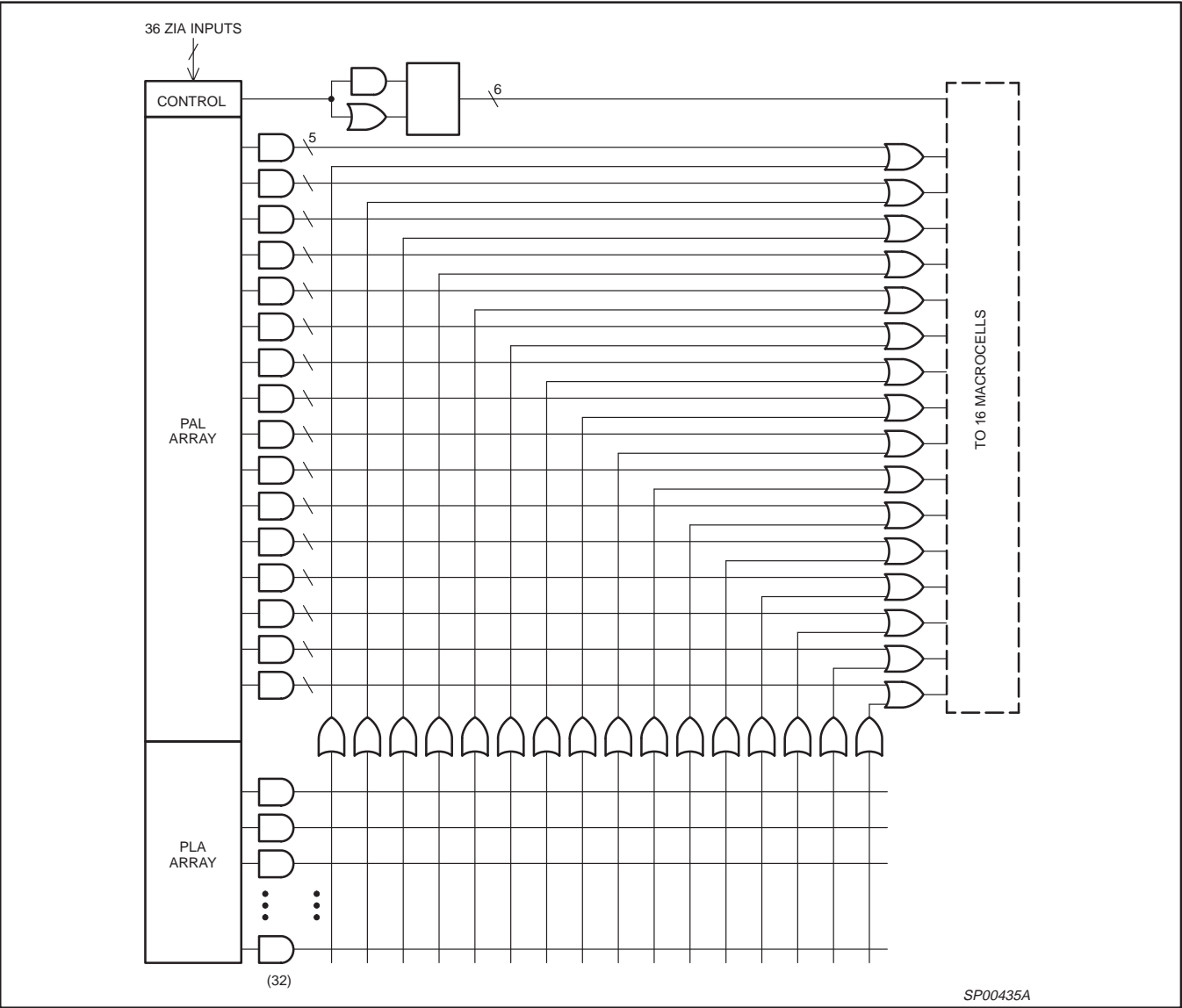


Figure 2. Philips XPLA Logic Block Architecture

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Macrocell Architecture

Figure 3 shows the architecture of the macrocell used in the CoolRunner™ family. The macrocell consists of a flip-flop that can be configured as either a D or T type. A D-type flip-flop is generally more useful for implementing state machines and data buffering. A T-type flip-flop is generally more useful in implementing counters. All CoolRunner™ family members provide both synchronous and asynchronous clocking and provide the ability to clock off either the falling or rising edges of these clocks. These devices are designed such that the skew between the rising and falling edges of a clock are minimized for clocking integrity. There are 4 clocks available on the PZ3064 device. Clock 0 (CLK0) is designated as the "synchronous" clock and must be driven by an external source. Clock 1 (CLK1), Clock 2 (CLK2), and Clock 3 (CLK3) can either be used as a synchronous clock (driven by an external source) or as an asynchronous clock (driven by a macrocell equation). The timing for asynchronous clocks is different in that the t_{CO} time is extended by the amount of time that it takes for the signal to propagate through the array and reach the clock network, and the t_{SU} time is reduced. Please see the application note titled "Understanding CoolRunner Clocking Options" for more detail.

Two of the control terms (CT0 and CT1) are used to control the Preset/Reset of the macrocell's flip-flop. The Preset/Reset feature

for each macrocell can also be disabled. Note that the Power-on Reset leaves all macrocells in the "zero" state when power is properly applied. The other 4 control terms (CT2–CT5) can be used to control the Output Enable of the macrocell's output buffers. The reason there are as many control terms dedicated for the Output Enable of the macrocell is to insure that all CoolRunner™ devices are PCI compliant. The macrocell's output buffers can also be always enabled or disabled. All CoolRunner™ devices also provide a Global Tri-State (\overline{GTS}) pin, which, when enabled and pulled Low, will 3-State all the outputs of the device. This pin is provided to support "In-Circuit Testing" or "Bed-of-Nails Testing".

There are two feedback paths to the ZIA: one from the macrocell, and one from the I/O pin. The ZIA feedback path before the output buffer is the macrocell feedback path, while the ZIA feedback path after the output buffer is the I/O pin ZIA path. When the macrocell is used as an output, the output buffer is enabled, and the macrocell feedback path can be used to feedback the logic implemented in the macrocell. When the I/O pin is used as an input, the output buffer will be 3-States and the input signal will be fed into the ZIA via the I/O feedback path, and the logic implemented in the buried macrocell can be fed back to the ZIA via the macrocell feedback path. It should be noted that unused inputs or I/Os should be properly terminated.

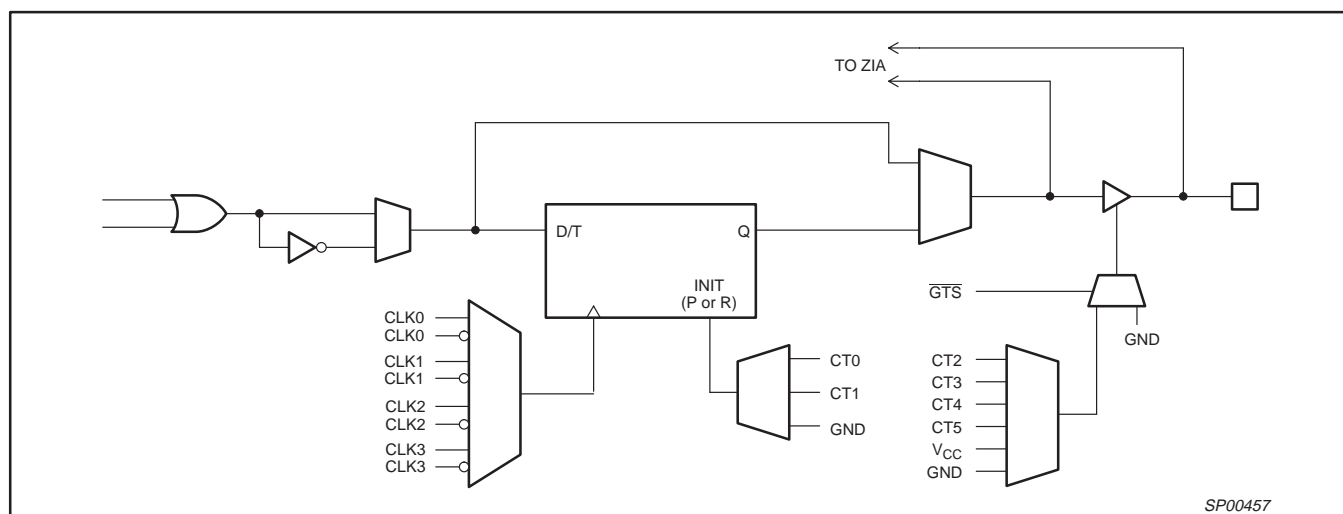


Figure 3. PZ3064 Macrocell Architecture

64 macrocell CPLD

PZ3064

Simple Timing Model

Figure 4 shows the CoolRunner™ Timing Model. The CoolRunner™ timing model looks very much like a 22V10 timing model in that there are three main timing parameters, including t_{PD} , t_{SU} , and t_{CO} . In other competing architectures, the user may be able to fit the design into the CPLD, but is not sure whether system timing requirements can be met until after the design has been fit into the device. This is because the timing models of competing architectures are very complex and include such things as timing dependencies on the number of parallel expanders borrowed, sharable expanders, varying number of X and Y routing channels used, etc. In the XPLA™ architecture, the user knows up front whether the design will meet system timing requirements. This is due to the simplicity of the timing model. For example, in the PZ3064 device, the user knows up front that if a given output uses

5 product terms or less, the $t_{PD} = 10\text{ns}$, the $t_{SU_PAL} = 6\text{ns}$, and the $t_{CO} = 7\text{ns}$. If an output is using 6 to 37 product terms, an additional 2ns must be added to the t_{PD} and t_{SU} timing parameters to account for the time to propagate through the PLA array.

TotalCMOS™ Design Technique for Fast Zero Power

Philips is the first to offer a TotalCMOS™ CPLD, both in process technology and design technique. Philips employs a cascade of CMOS gates to implement its Sum of Products instead of the traditional sense amp approach. This CMOS gate implementation allows Philips to offer CPLDs which are both high performance and low power, breaking the paradigm that to have low power, you must have low performance. Refer to Figure 5 and Table 2 showing the I_{DD} vs. Frequency of our PZ3064 TotalCMOS™ CPLD.

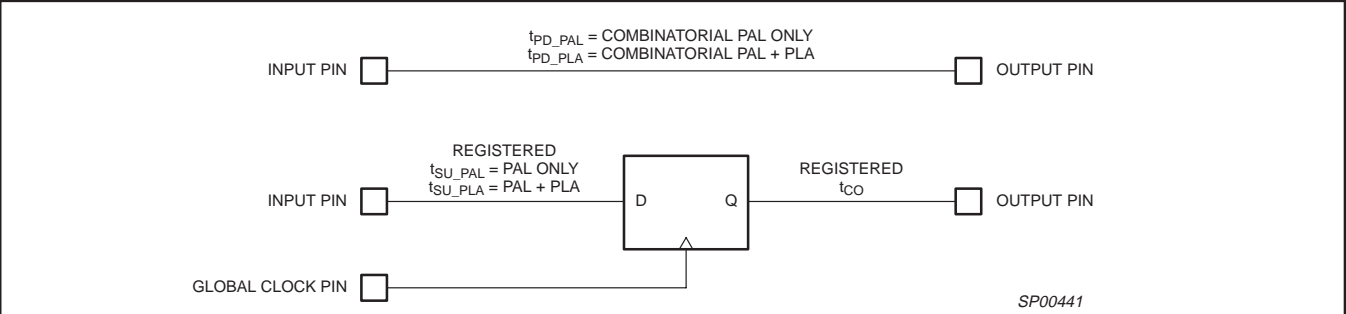


Figure 4. CoolRunner™ Timing Model

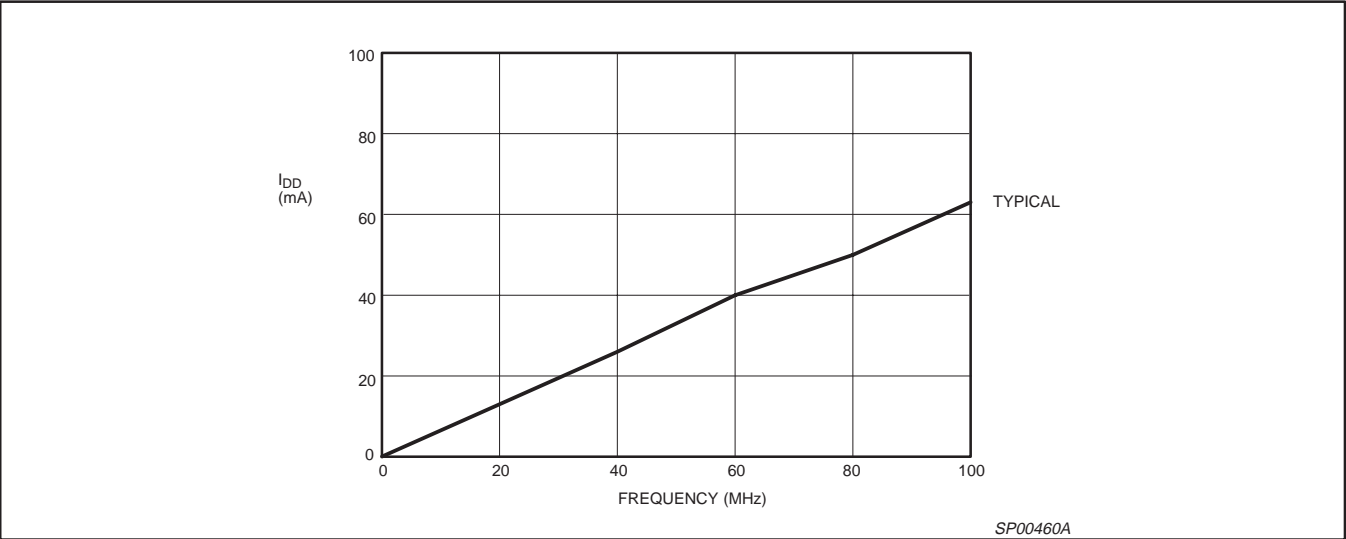


Figure 5. I_{DD} vs. Frequency @ $V_{DD} = 3.3\text{V}$, 25°C

Table 2. I_{DD} vs. Frequency

| $V_{DD} = 3.3\text{V}$ | | | | | | |
|------------------------|------|----|----|----|----|-----|
| FREQUENCY (MHz) | 0 | 20 | 40 | 60 | 80 | 100 |
| Typical I_{DD} (mA) | 0.04 | 13 | 26 | 40 | 50 | 63 |

64 macrocell CPLD

PZ3064

ABSOLUTE MAXIMUM RATINGS¹

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT |
|------------------|------------------------------|------|----------------------|------|
| V _{DD} | Supply voltage ² | −0.5 | 7.0 | V |
| V _I | Input voltage | −1.2 | V _{DD} +0.5 | V |
| V _{OUT} | Output voltage | −0.5 | V _{DD} +0.5 | V |
| I _{IN} | Input current | −30 | 30 | mA |
| I _{OUT} | Output current | −100 | 100 | mA |
| T _J | Maximum junction temperature | −40 | 150 | °C |
| T _{str} | Storage temperature | −65 | 150 | °C |

NOTES:

- Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification is not implied.
- The chip supply voltage must rise monotonically.

OPERATING RANGE

| PRODUCT GRADE | TEMPERATURE | VOLTAGE |
|---------------|--------------|------------|
| Commercial | 0 to +70°C | 3.3 ±10% V |
| Industrial | −40 to +85°C | 3.3 ±10% V |

64 macrocell CPLD

PZ3064

DC ELECTRICAL CHARACTERISTICS FOR COMMERCIAL GRADE DEVICESCommercial: $0^{\circ}\text{C} \leq T_{\text{amb}} \leq +70^{\circ}\text{C}$; $3.0\text{V} \leq V_{\text{DD}} \leq 3.6\text{V}$

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN. | MAX. | UNIT |
|-----------------------|---|--|------|------|---------------|
| V_{IL} | Input voltage low | $V_{\text{DD}} = 3.0\text{V}$ | | 0.8 | V |
| V_{IH} | Input voltage high | $V_{\text{DD}} = 3.6\text{V}$ | 2.0 | | V |
| V_{I} | Input clamp voltage | $V_{\text{DD}} = 3.0\text{V}$, $I_{\text{IN}} = -18\text{mA}$ | | -1.2 | V |
| V_{OL} | Output voltage low | $V_{\text{DD}} = 3.0\text{V}$, $I_{\text{OL}} = 8\text{mA}$ | | 0.5 | V |
| V_{OH} | Output voltage high | $V_{\text{DD}} = 3.0\text{V}$, $I_{\text{OH}} = -8\text{mA}$ | 2.4 | | V |
| I_{I} | Input leakage current | $V_{\text{IN}} = 0$ to V_{DD} | -10 | 10 | μA |
| I_{OZ} | 3-States output leakage current | $V_{\text{IN}} = 0$ to V_{DD} | -10 | 10 | μA |
| I_{DDQ}^1 | Standby current | $V_{\text{DD}} = 3.6\text{V}$, $T_{\text{amb}} = 0^{\circ}\text{C}$ | | 50 | μA |
| $I_{\text{DD}}^{1,2}$ | Dynamic current | $V_{\text{DD}} = 3.6\text{V}$, $T_{\text{amb}} = 0^{\circ}\text{C}$ @ 1MHz | | 1 | mA |
| | | $V_{\text{DD}} = 3.6\text{V}$, $T_{\text{amb}} = 0^{\circ}\text{C}$ @ 50MHz | | 40 | mA |
| I_{OS} | Short circuit output current ³ | 1 pin at a time for no longer than 1 second | -5 | -100 | mA |
| C_{IN} | Input pin capacitance ³ | $T_{\text{amb}} = 25^{\circ}\text{C}$, $f = 1\text{MHz}$ | | 8 | pF |
| C_{CLK} | Clock input capacitance ³ | $T_{\text{amb}} = 25^{\circ}\text{C}$, $f = 1\text{MHz}$ | 5 | 12 | pF |
| $C_{\text{I/O}}$ | I/O pin capacitance ³ | $T_{\text{amb}} = 25^{\circ}\text{C}$, $f = 1\text{MHz}$ | | 10 | pF |

NOTES:

- See Table 2, page 6 for typical value.
- This parameter measured with a 16-bit, loadable up/down counter loaded into every logic block, with all outputs enabled and unloaded. Inputs are tied to V_{DD} or ground. This parameter guaranteed by design and characterization, not testing.
- Typical values, not tested.

AC ELECTRICAL CHARACTERISTICS¹ FOR COMMERCIAL GRADE DEVICESCommercial: $0^{\circ}\text{C} \leq T_{\text{amb}} \leq +70^{\circ}\text{C}$; $3.0\text{V} \leq V_{\text{DD}} \leq 3.6\text{V}$

| SYMBOL | PARAMETER | 10 | | 12 | | UNIT |
|-----------------------|--|------|------|------|------|---------------|
| | | MIN. | MAX. | MIN. | MAX. | |
| $t_{\text{PD_PAL}}$ | Propagation delay time, input (or feedback node) to output through PAL | 2 | 10 | 2 | 12 | ns |
| $t_{\text{PD_PLA}}$ | Propagation delay time, input (or feedback node) to output through PAL & PLA | 3 | 12.5 | 3 | 14.5 | ns |
| t_{CO} | Clock to out (global synchronous clock from pin) | 2 | 7 | 2 | 8 | ns |
| $t_{\text{SU_PAL}}$ | Setup time (from input or feedback node) through PAL | 5.5 | | 7 | | ns |
| $t_{\text{SU_PLA}}$ | Setup time (from input or feedback node) through PAL + PLA | 8 | | 9.5 | | ns |
| t_{H} | Hold time | | 0 | | 0 | ns |
| t_{CH} | Clock High time | 4 | | 5 | | ns |
| t_{CL} | Clock Low time | 4 | | 5 | | ns |
| t_{R} | Input Rise time | | 20 | | 20 | ns |
| t_{F} | Input Fall time | | 20 | | 20 | ns |
| f_{MAX1} | Maximum FF toggle rate ² ($1/t_{\text{CH}} + t_{\text{CL}}$) | 125 | | 100 | | MHz |
| f_{MAX2} | Maximum internal frequency ² ($1/t_{\text{SUPAL}} + t_{\text{CF}}$) | 91 | | 74 | | MHz |
| f_{MAX3} | Maximum external frequency ² ($1/t_{\text{SUPAL}} + t_{\text{CO}}$) | 80 | | 67 | | MHz |
| t_{BUF} | Output buffer delay time | | 1.5 | | 1.5 | ns |
| $t_{\text{PDF_PAL}}$ | Input (or feedback node) to internal feedback node delay time through PAL | | 8.5 | | 10.5 | ns |
| $t_{\text{PDF_PLA}}$ | Input (or feedback node) to internal feedback node delay time through PAL+PLA | | 11 | | 13 | ns |
| t_{CF} | Clock to internal feedback node delay time | | 5.5 | | 6.5 | ns |
| t_{INIT} | Delay from valid V_{DD} to valid reset | | 50 | | 50 | μs |
| t_{ER} | Input to output disable ³ | | 12.5 | | 14 | ns |
| t_{EA} | Input to output valid | | 12.5 | | 14 | ns |
| t_{RP} | Input to register preset | | 15 | | 16 | ns |
| t_{RR} | Input to register reset | | 15 | | 16 | ns |

NOTES:

- Specifications measured with one output switching. See Figure 6 and Table 3 for derating.
- This parameter guaranteed by design and characterization, not by test.
- Output $C_{\text{L}} = 5\text{pF}$.

64 macrocell CPLD

PZ3064

DC ELECTRICAL CHARACTERISTICS FOR INDUSTRIAL GRADE DEVICESIndustrial: $-40^{\circ}\text{C} \leq T_{\text{amb}} \leq +85^{\circ}\text{C}$; $3.0\text{V} \leq V_{\text{DD}} \leq 3.6\text{V}$

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN. | MAX. | UNIT |
|------------------------|---------------------------------|--|------|------|---------------|
| V_{IL} | Input voltage low | $V_{\text{DD}} = 3.0\text{V}$ | | 0.8 | V |
| V_{IH} | Input voltage high | $V_{\text{DD}} = 3.6\text{V}$ | 2.0 | | V |
| V_{I} | Input clamp voltage | $V_{\text{DD}} = 3.0\text{V}$, $I_{\text{IN}} = -18\text{mA}$ | | -1.2 | V |
| V_{OL} | Output voltage low | $V_{\text{DD}} = 3.0\text{V}$, $I_{\text{OL}} = 8\text{mA}$ | | 0.5 | V |
| V_{OH} | Output voltage high | $V_{\text{DD}} = 3.0\text{V}$, $I_{\text{OH}} = -8\text{mA}$ | 2.4 | | V |
| I_{I} | Input leakage current | $V_{\text{IN}} = 0$ to V_{DD} | -10 | 10 | μA |
| I_{OZ} | 3-States output leakage current | $V_{\text{IN}} = 0$ to V_{DD} | -10 | 10 | μA |
| I_{DDQ}^1 | Standby current | $V_{\text{DD}} = 3.6\text{V}$, $T_{\text{amb}} = -40^{\circ}\text{C}$ | | 50 | μA |
| $I_{\text{DDQ}}^{1,2}$ | Dynamic current | $V_{\text{DD}} = 3.6\text{V}$, $T_{\text{amb}} = -40^{\circ}\text{C}$ @ 1MHz | | 1 | mA |
| | | $V_{\text{DD}} = 3.6\text{V}$, $T_{\text{amb}} = -40^{\circ}\text{C}$ @ 50MHz | | 40 | mA |
| I_{OS} | Short circuit output current | 1 pin at a time for no longer than 1 second | -5 | -130 | mA |
| C_{IN} | Input pin capacitance | $T_{\text{amb}} = 25^{\circ}\text{C}$, $f = 1\text{MHz}$ | | 8 | pF |
| C_{CLK} | Clock input capacitance | $T_{\text{amb}} = 25^{\circ}\text{C}$, $f = 1\text{MHz}$ | 5 | 12 | pF |
| $C_{\text{I/O}}$ | I/O pin capacitance | $T_{\text{amb}} = 25^{\circ}\text{C}$, $f = 1\text{MHz}$ | | 10 | pF |

NOTES:

- See Table 2, page 6 for typical values.
- This parameter measured with a 16-bit, loadable up/down counter loaded into every logic block, with all outputs enabled and unloaded. Inputs are tied to V_{DD} or ground. This parameter guaranteed by design and characterization, not testing.
- Typical values, not tested.

AC ELECTRICAL CHARACTERISTICS¹ FOR INDUSTRIAL GRADE DEVICESIndustrial: $-40^{\circ}\text{C} \leq T_{\text{amb}} \leq +85^{\circ}\text{C}$; $3.0\text{V} \leq V_{\text{DD}} \leq 3.6\text{V}$

| SYMBOL | PARAMETER | 12 | | 15 | | UNIT |
|-----------------------|--|------|------|------|------|---------------|
| | | MIN. | MAX. | MIN. | MAX. | |
| $t_{\text{PD_PAL}}$ | Propagation delay time, input (or feedback node) to output through PAL | 2 | 12 | 2 | 15 | ns |
| $t_{\text{PD_PLA}}$ | Propagation delay time, input (or feedback node) to output through PAL & PLA | 3 | 14.5 | 3 | 17.5 | ns |
| t_{CO} | Clock to out (global synchronous clock from pin) | 2 | 8 | 2 | 9 | ns |
| $t_{\text{SU_PAL}}$ | Setup time (from input or feedback node) through PAL | 7 | | 8 | | ns |
| $t_{\text{SU_PLA}}$ | Setup time (from input or feedback node) through PAL + PLA | 9.5 | | 10.5 | | ns |
| t_{H} | Hold time | | 0 | | 0 | ns |
| t_{CH} | Clock High time | 5 | | 5 | | ns |
| t_{CL} | Clock Low time | 5 | | 5 | | ns |
| t_{R} | Input Rise time | | 20 | | 20 | ns |
| t_{F} | Input Fall time | | 20 | | 20 | ns |
| f_{MAX1} | Maximum FF toggle rate ² ($1/t_{\text{CH}} + t_{\text{CL}}$) | 100 | | 100 | | MHz |
| f_{MAX2} | Maximum internal frequency ² ($1/t_{\text{SUPAL}} + t_{\text{CF}}$) | 74 | | 65 | | MHz |
| f_{MAX3} | Maximum external frequency ² ($1/t_{\text{SUPAL}} + t_{\text{CO}}$) | 67 | | 58 | | MHz |
| t_{BUF} | Output buffer delay time | | 1.5 | | 1.5 | ns |
| $t_{\text{PDF_PAL}}$ | Input (or feedback node) to internal feedback node delay time through PAL | | 10.5 | | 13.5 | ns |
| $t_{\text{PDF_PLA}}$ | Input (or feedback node) to internal feedback node delay time through PAL+PLA | | 13 | | 16 | ns |
| t_{CF} | Clock to internal feedback node delay time | | 6.5 | | 7.5 | ns |
| t_{INIT} | Delay from valid V_{DD} to valid reset | | 50 | | 50 | μs |
| t_{ER} | Input to output disable ³ | | 14 | | 15 | ns |
| t_{EA} | Input to output valid | | 14 | | 15 | ns |
| t_{RP} | Input to register preset | | 16 | | 17 | ns |
| t_{RR} | Input to register reset | | 16 | | 17 | ns |

NOTES:

- Specifications measured with one output switching. See Figure 6 and Table 3 for derating.
- This parameter guaranteed by design and characterization, not by test.
- Output $C_{\text{L}} = 5\text{pF}$.

64 macrocell CPLD

PZ3064

SWITCHING CHARACTERISTICS

The test load circuit and load values for the AC Electrical Characteristics are illustrated below.

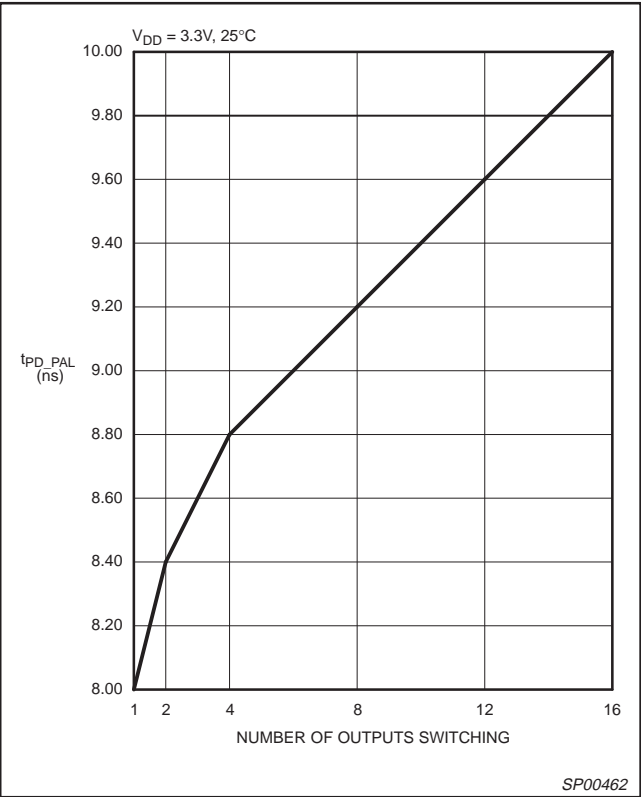
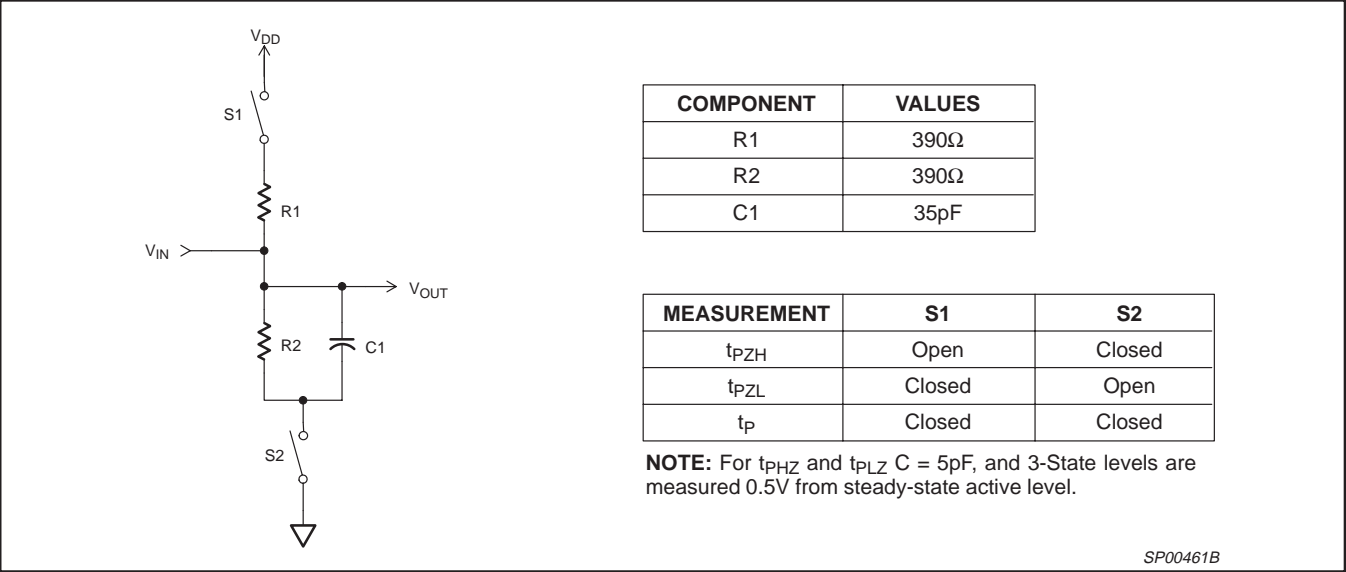
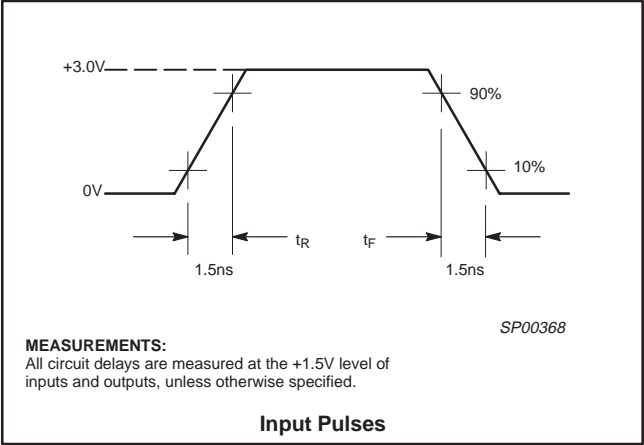


Figure 6. t_{PD_PAL} vs. Outputs Switching

Table 3. t_{PD_PAL} vs. Number of Outputs Switching
V_{DD} = 3.3V

| NUMBER OF OUTPUTS | 1 | 2 | 4 | 8 | 12 | 16 |
|-------------------|-----|-----|-----|-----|-----|------|
| Typical (ns) | 8.0 | 8.4 | 8.8 | 9.2 | 9.6 | 10.0 |

VOLTAGE WAVEFORM

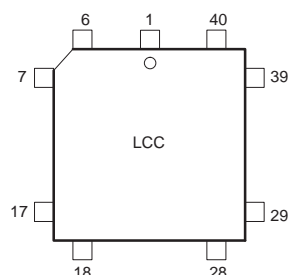


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PIN DESCRIPTIONS

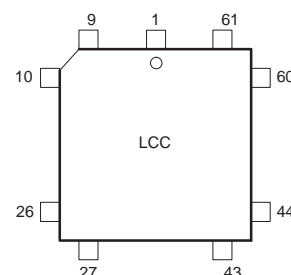
PZ3064 – 44-Pin Plastic Leaded Chip Carrier



| Pin | Function | Pin | Function | Pin | Function |
|-----|-----------------|-----|-----------------|-----|-----------------|
| 1 | IN1 | 16 | I/O-B10 | 31 | I/O-C13 |
| 2 | IN3 | 17 | I/O-B8 | 32 | I/O-C15 |
| 3 | V _{DD} | 18 | I/O-B4 | 33 | I/O-D15 |
| 4 | I/O-A0/CK3 | 19 | I/O-B3 | 34 | I/O-D13 |
| 5 | I/O-A2 | 20 | I/O-B2 | 35 | V _{DD} |
| 6 | I/O-A5 | 21 | I/O-B0/CK2 | 36 | I/O-D12 |
| 7 | I/O-A8 | 22 | GND | 37 | I/O-D11 |
| 8 | I/O-A11 | 23 | V _{DD} | 38 | I/O-D8 |
| 9 | I/O-A12 | 24 | I/O-C0/CK1 | 39 | I/O-D7 |
| 10 | GND | 25 | I/O-C2 | 40 | I/O-D2 |
| 11 | I/O-A13 | 26 | I/O-C3 | 41 | I/O-D0 |
| 12 | I/O-A15 | 27 | I/O-C4 | 42 | GND |
| 13 | I/O-B15 | 28 | I/O-C7 | 43 | IN0-CK0 |
| 14 | I/O-B13 | 29 | I/O-C8 | 44 | IN2-gtsn |
| 15 | V _{DD} | 30 | GND | | |

SP00452B

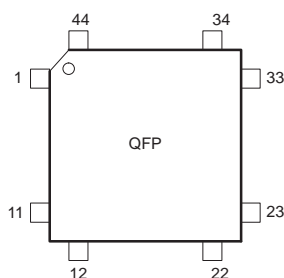
PZ3064 – 68-Pin Plastic Leaded Chip Carrier



| Pin | Function | Pin | Function | Pin | Function |
|-----|-----------------|-----|-----------------|-----|-----------------|
| 1 | IN1 | 24 | I/O-B10 | 47 | I/O-C12 |
| 2 | IN3 | 25 | I/O-B8 | 48 | GND |
| 3 | V _{DD} | 26 | GND | 49 | I/O-C13 |
| 4 | I/O-A0/CK3 | 27 | I/O-B7 | 50 | I/O-C15 |
| 5 | I/O-A2 | 28 | I/O-B5 | 51 | I/O-D15 |
| 6 | GND | 29 | I/O-B4 | 52 | I/O-D13 |
| 7 | I/O-A3 | 30 | I/O-B3 | 53 | V _{DD} |
| 8 | I/O-A4 | 31 | V _{DD} | 54 | I/O-D12 |
| 9 | I/O-A5 | 32 | I/O-B2 | 55 | I/O-D11 |
| 10 | I/O-A7 | 33 | I/O-B0/CK2 | 56 | I/O-D9 |
| 11 | V _{DD} | 34 | GND | 57 | I/O-D8 |
| 12 | I/O-A8 | 35 | V _{DD} | 58 | GND |
| 13 | I/O-A10 | 36 | I/O-C0/CK1 | 59 | I/O-D7 |
| 14 | I/O-A11 | 37 | I/O-C2 | 60 | I/O-D6 |
| 15 | I/O-A12 | 38 | GND | 61 | I/O-D4 |
| 16 | GND | 39 | I/O-C3 | 62 | I/O-D3 |
| 17 | I/O-A13 | 40 | I/O-C4 | 63 | V _{DD} |
| 18 | I/O-A15 | 41 | I/O-C5 | 64 | I/O-D2 |
| 19 | I/O-B15 | 42 | I/O-C7 | 65 | I/O-D0 |
| 20 | I/O-B13 | 43 | V _{DD} | 66 | GND |
| 21 | V _{DD} | 44 | I/O-C8 | 67 | IN0/CK0 |
| 22 | I/O-B12 | 45 | I/O-C10 | 68 | IN2-gtsn |
| 23 | I/O-B11 | 46 | I/O-C11 | | |

SP00454A

PZ3064 – 44-Pin Thin Quad Flat Package



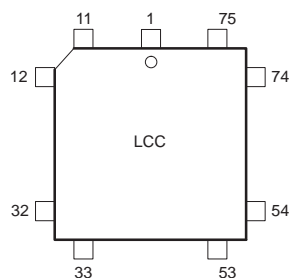
| Pin | Function | Pin | Function | Pin | Function |
|-----|-----------------|-----|-----------------|-----|-----------------|
| 1 | I/O-A8 | 16 | GND | 31 | I/O-D11 |
| 2 | I/O-A11 | 17 | V _{DD} | 32 | I/O-D8 |
| 3 | I/O-A12 | 18 | I/O-C0/CK1 | 33 | I/O-D7 |
| 4 | GND | 19 | I/O-C2 | 34 | I/O-D2 |
| 5 | I/O-A13 | 20 | I/O-C3 | 35 | I/O-D0 |
| 6 | I/O-A15 | 21 | I/O-C4 | 36 | GND |
| 7 | I/O-B15 | 22 | I/O-C7 | 37 | IN0/CK0 |
| 8 | I/O-B13 | 23 | I/O-C8 | 38 | IN2-gtsn |
| 9 | V _{DD} | 24 | GND | 39 | IN1 |
| 10 | I/O-B10 | 25 | I/O-C13 | 40 | IN3 |
| 11 | I/O-B8 | 26 | I/O-C15 | 41 | V _{DD} |
| 12 | I/O-B4 | 27 | I/O-D15 | 42 | I/O-A0/CK3 |
| 13 | I/O-B3 | 28 | I/O-D13 | 43 | I/O-A2 |
| 14 | I/O-B2 | 29 | V _{DD} | 44 | I/O-A5 |
| 15 | I/O-B0/CK2 | 30 | I/O-D12 | | |

SP00453A

64 macrocell CPLD

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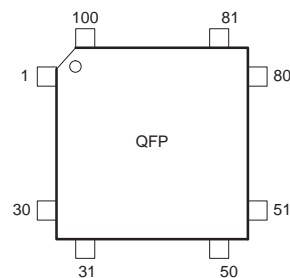
PZ3064 – 84-Pin Plastic Leaded Chip Carrier



| Pin | Function | Pin | Function | Pin | Function |
|-----|-----------------|-----|-----------------|-----|-----------------|
| 1 | IN1 | 29 | I/O-B10 | 57 | I/O-C11 |
| 2 | IN3 | 30 | I/O-B9 | 58 | I/O-C12 |
| 3 | V _{DD} | 31 | I/O-B8 | 59 | GND |
| 4 | I/O-A0/CK3 | 32 | GND | 60 | I/O-C13 |
| 5 | I/O-A1 | 33 | I/O-B7 | 61 | I/O-C14 |
| 6 | I/O-A2 | 34 | I/O-B6 | 62 | I/O-C15 |
| 7 | GND | 35 | I/O-B5 | 63 | I/O-D15 |
| 8 | I/O-A3 | 36 | I/O-B4 | 64 | I/O-D14 |
| 9 | I/O-A4 | 37 | I/O-B3 | 65 | I/O-D13 |
| 10 | I/O-A5 | 38 | V _{DD} | 66 | V _{DD} |
| 11 | I/O-A6 | 39 | I/O-B2 | 67 | I/O-D12 |
| 12 | I/O-A7 | 40 | I/O-B1 | 68 | I/O-D11 |
| 13 | V _{CC} | 41 | I/O-B0/CK2 | 69 | I/O-D10 |
| 14 | I/O-A8 | 42 | GND | 70 | I/O-D9 |
| 15 | I/O-A9 | 43 | V _{DD} | 71 | I/O-D8 |
| 16 | I/O-A10 | 44 | I/O-C0/CK1 | 72 | GND |
| 17 | I/O-A11 | 45 | I/O-C1 | 73 | I/O-D7 |
| 18 | I/O-A12 | 46 | I/O-C2 | 74 | I/O-D6 |
| 19 | GND | 47 | GND | 75 | I/O-D5 |
| 20 | I/O-A13 | 48 | I/O-C3 | 76 | I/O-D4 |
| 21 | I/O-A14 | 49 | I/O-C4 | 77 | I/O-D3 |
| 22 | I/O-A15 | 50 | I/O-C5 | 78 | V _{DD} |
| 23 | I/O-B15 | 51 | I/O-C6 | 79 | I/O-D2 |
| 24 | I/O-B14 | 52 | I/O-C7 | 80 | I/O-D1 |
| 25 | I/O-B13 | 53 | V _{DD} | 81 | I/O-D0 |
| 26 | V _{DD} | 54 | I/O-C8 | 82 | GND |
| 27 | I/O-B12 | 55 | I/O-C9 | 83 | IN0/CK0 |
| 28 | I/O-B11 | 56 | I/O-C10 | 84 | IN2-gtsn |

SP00455A

PZ3064 – 100-Pin Plastic Quad Flat Package



| Pin | Function | Pin | Function | Pin | Function |
|-----|-----------------|-----|-----------------|-----|-----------------|
| 1 | NC | 35 | I/O-B3 | 69 | I/O-D12 |
| 2 | NC | 36 | V _{DD} | 70 | I/O-D11 |
| 3 | I/O-A6 | 37 | I/O-B2 | 71 | I/O-D10 |
| 4 | I/O-A7 | 38 | I/O-B1 | 72 | NC |
| 5 | V _{DD} | 39 | I/O-B0/CK2 | 73 | I/O-D9 |
| 6 | I/O-A8 | 40 | GND | 74 | NC |
| 7 | NC | 41 | V _{DD} | 75 | I/O-D8 |
| 8 | I/O-A9 | 42 | I/O-C0/CK1 | 76 | GND |
| 9 | NC | 43 | I/O-C1 | 77 | I/O-D7 |
| 10 | I/O-A10 | 44 | I/O-C2 | 78 | I/O-D6 |
| 11 | I/O-A11 | 45 | GND | 79 | NC |
| 12 | I/O-A12 | 46 | I/O-C3 | 80 | NC |
| 13 | GND | 47 | I/O-C4 | 81 | I/O-D5 |
| 14 | I/O-A13 | 48 | I/O-C5 | 82 | I/O-D4 |
| 15 | I/O-A14 | 49 | I/O-C6 | 83 | I/O-D3 |
| 16 | I/O-A15 | 50 | I/O-C7 | 84 | V _{DD} |
| 17 | I/O-B15 | 51 | NC | 85 | I/O-D2 |
| 18 | I/O-B14 | 52 | NC | 86 | I/O-D1 |
| 19 | I/O-B13 | 53 | V _{DD} | 87 | I/O-D0 |
| 20 | V _{DD} | 54 | I/O-C8 | 88 | GND |
| 21 | I/O-B12 | 55 | NC | 89 | IN0/CK0 |
| 22 | I/O-B11 | 56 | I/O-C9 | 90 | IN2-gtsn |
| 23 | I/O-B10 | 57 | NC | 91 | IN1 |
| 24 | NC | 58 | I/O-C10 | 92 | IN3 |
| 25 | I/O-B9 | 59 | I/O-C11 | 93 | V _{DD} |
| 26 | NC | 60 | I/O-C12 | 94 | I/O-A0/CK3 |
| 27 | I/O-B8 | 61 | GND | 95 | I/O-A1 |
| 28 | GND | 62 | I/O-C13 | 96 | I/O-A2 |
| 29 | NC | 63 | I/O-C14 | 97 | GND |
| 30 | NC | 64 | I/O-C15 | 98 | I/O-A3 |
| 31 | I/O-B7 | 65 | I/O-D15 | 99 | I/O-A4 |
| 32 | I/O-B6 | 66 | I/O-D14 | 100 | I/O-A5 |
| 33 | I/O-B5 | 67 | I/O-D13 | | |
| 34 | I/O-B4 | 68 | V _{DD} | | |

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64 macrocell CPLD

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Package Thermal Characteristics

Philips Semiconductors uses the Temperature Sensitive Parameter (TSP) method to test thermal resistance. This method meets Mil-Std-883C Method 1012.1 and is described in Philips 1995 IC Package Databook. Thermal resistance varies slightly as a function of input power. As input power increases, thermal resistance changes approximately 5% for a 100% change in power.

Figure 7 is a derating curve for the change in Θ_{JA} with airflow based on wind tunnel measurements. It should be noted that the wind flow dynamics are more complex and turbulent in actual applications than in a wind tunnel. Also, the test boards used in the wind tunnel contribute significantly to forced convection heat transfer, and may not be similar to the actual circuit board, especially in size.

| Package | Θ_{JA} |
|--------------|---------------|
| 44-pin PLCC | 44.8°C/W |
| 44-pin TQFP | 60.8°C/W |
| 68-pin PLCC | 44.9°C/W |
| 84-pin PLCC | 34.7°C/W |
| 100-pin PQFP | 44.5°C/W |

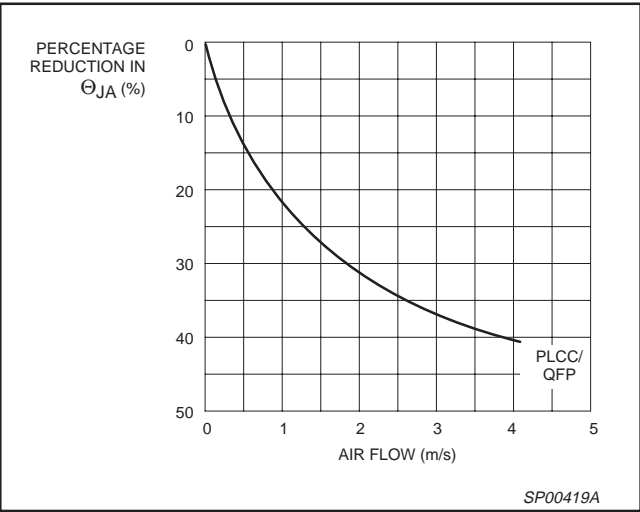


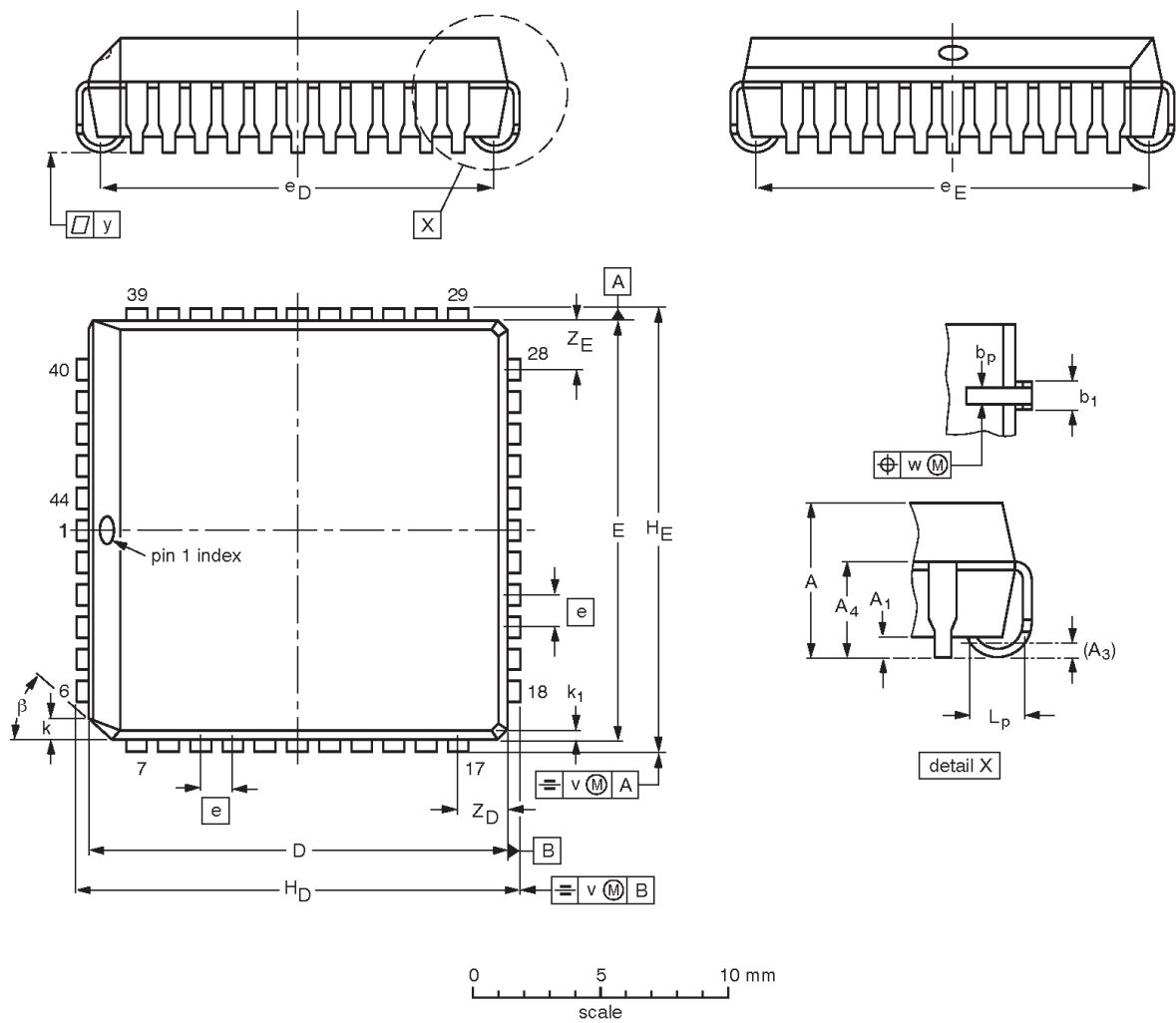
Figure 7. Average Effect of Airflow on Θ_{JA}

64 macrocell CPLD

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PLCC44: plastic leaded chip carrier; 44 leads


SOT187-2



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

| UNIT | A | A ₁ min. | A ₃ | A ₄ max. | b _p | b ₁ | D ⁽¹⁾ | E ⁽¹⁾ | e | e _D | e _E | H _D | H _E | k | k ₁ max. | L _p | v | w | y | Z _D ⁽¹⁾ max. | Z _E ⁽¹⁾ max. | β |
|--------|----------------|------------------------|----------------|------------------------|----------------|----------------|------------------|------------------|------|----------------|----------------|----------------|----------------|----------------|------------------------|----------------|-------|-------|-------|---------------------------------------|---------------------------------------|-----|
| mm | 4.57 4.19 | 0.51 | 0.25 | 3.05 | 0.53 0.33 | 0.81 0.66 | 16.66 16.51 | 16.66 16.51 | 1.27 | 16.00 14.99 | 16.00 14.99 | 17.65 17.40 | 17.65 17.40 | 1.22 1.07 | 0.51 | 1.44 1.02 | 0.18 | 0.18 | 0.10 | 2.16 | 2.16 | 45° |
| inches | 0.180 0.165 | 0.020 | 0.01 | 0.12 | 0.021 0.013 | 0.032 0.026 | 0.656 0.650 | 0.656 0.650 | 0.05 | 0.630 0.590 | 0.630 0.590 | 0.695 0.685 | 0.695 0.685 | 0.048 0.042 | 0.020 | 0.057 0.040 | 0.007 | 0.007 | 0.004 | 0.085 | 0.085 | |

Note
1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

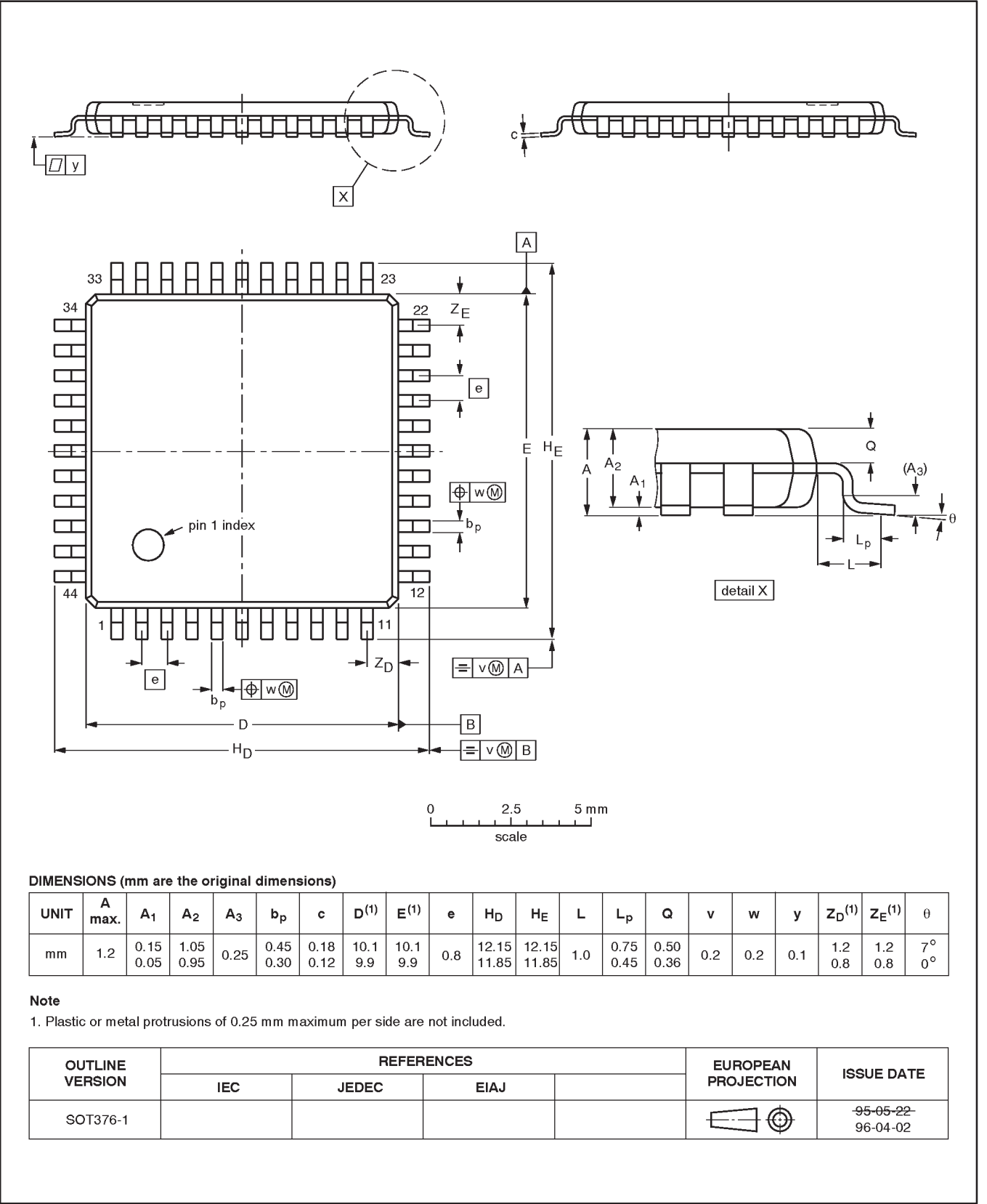
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|--------------------|------------|----------|------|--|---|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT187-2 | 112E10 | MO-047AC | | |  | 92-11-17 95-02-25 |

64 macrocell CPLD

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TQFP44: plastic thin quad flat package; 44 leads; body 10 x 10 x 1.0 mm

SOT376-1

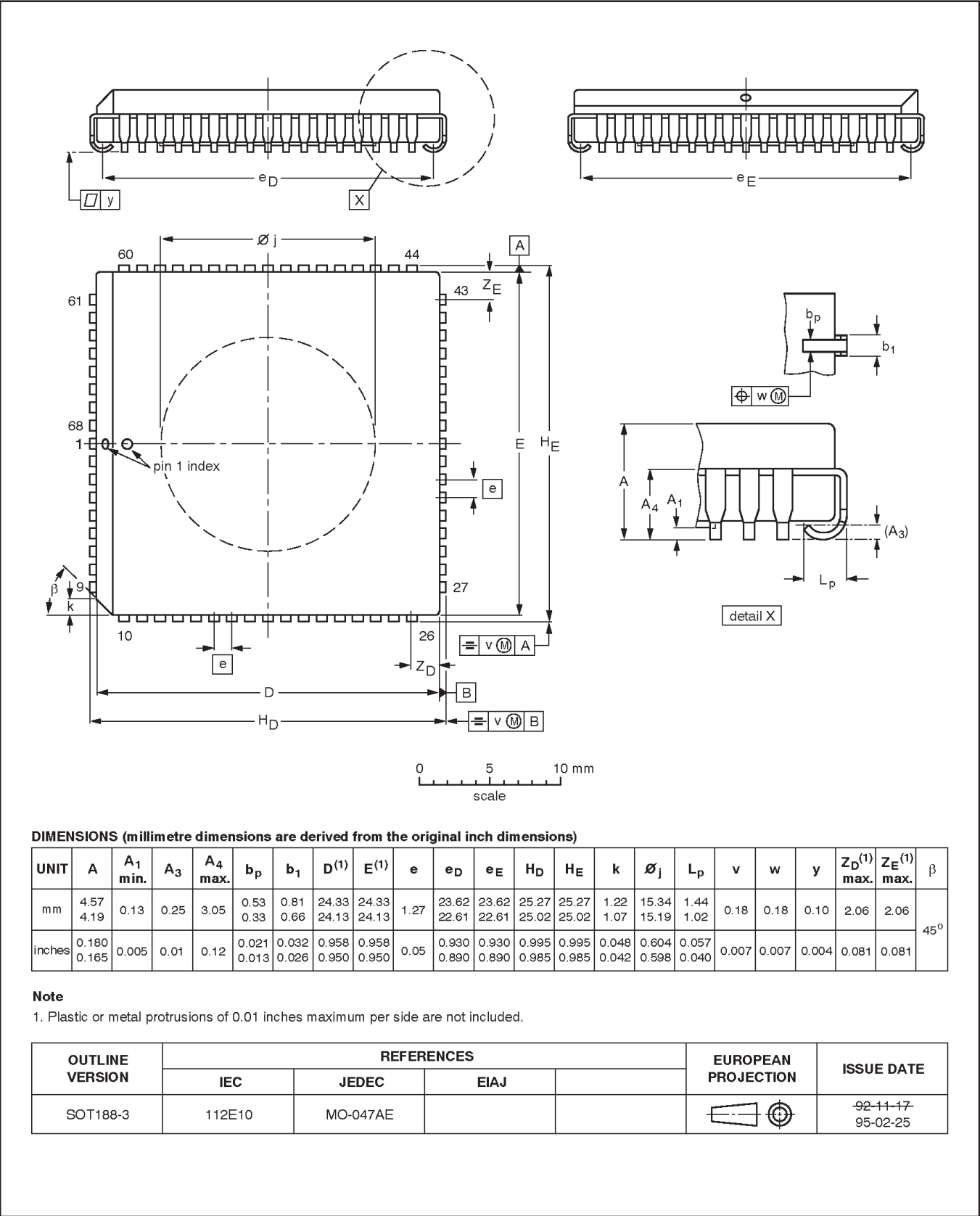


64 macrocell CPLD

PZ3064

PLCC68: plastic leaded chip carrier; 68 leads; pedestal

SOT188-3

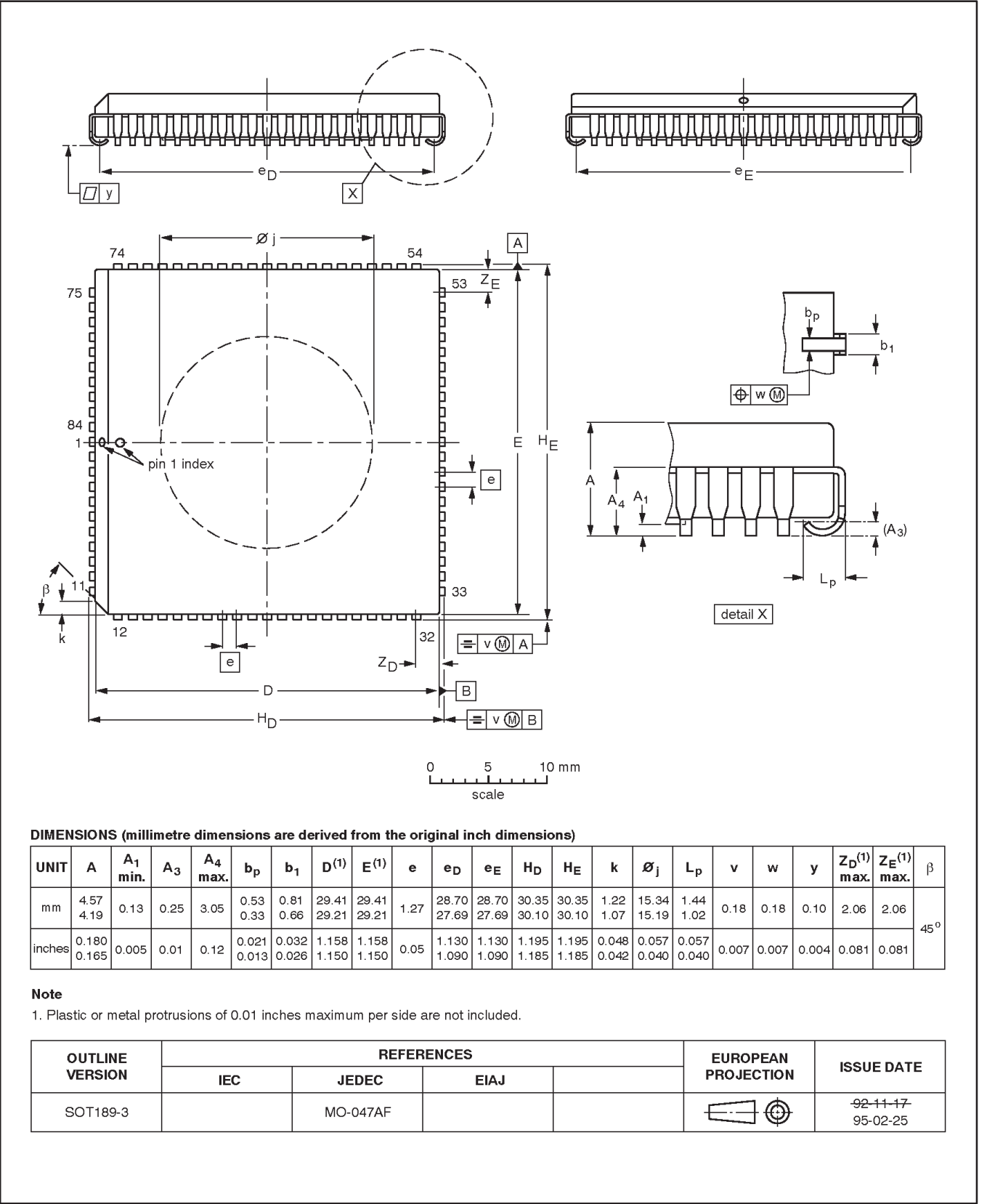


64 macrocell CPLD

PZ3064

PLCC84: plastic leaded chip carrier; 84 leads; pedestal

SOT189-3

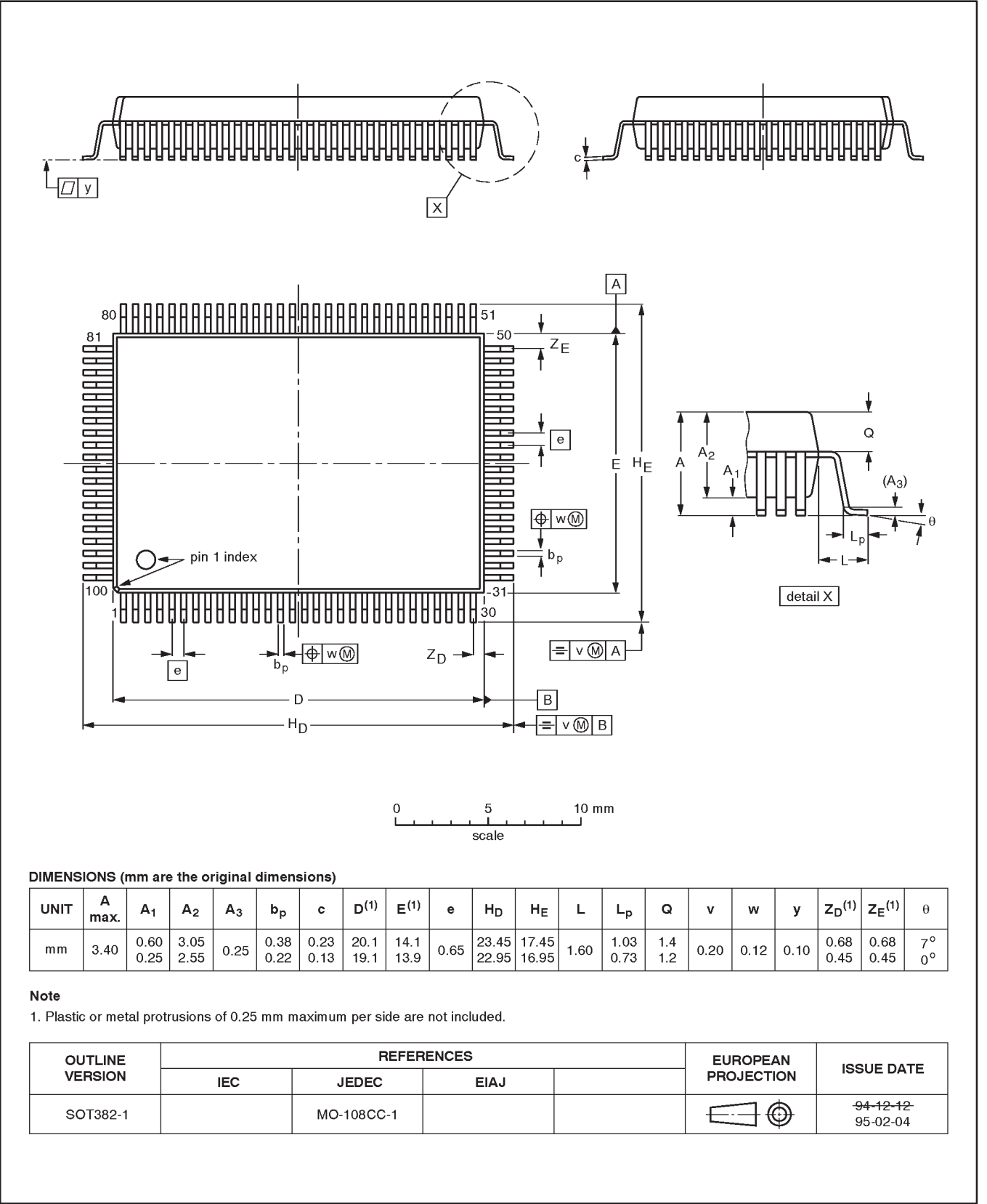


64 macrocell CPLD

PZ3064

QFP100: plastic quad flat package; 100 leads (lead length 1.6 mm); body 14 x 20 x 2.8 mm

SOT382-1



| | |
|-------------------|--------|
| 64 macrocell CPLD | PZ3064 |
|-------------------|--------|

NOTES

64 macrocell CPLD

PZ3064

Data sheet status

| Data sheet status | Product status | Definition [1] |
|---------------------------|----------------|--|
| Objective specification | Development | This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice. |
| Preliminary specification | Qualification | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
| Product specification | Production | This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Philips Semiconductors
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088-3409
Telephone 800-234-7381

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