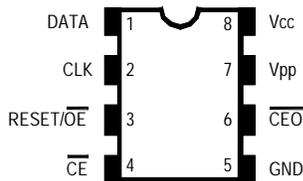


XILINX PROGRAMMER QUALIFICATION SPECIFICATION

Description

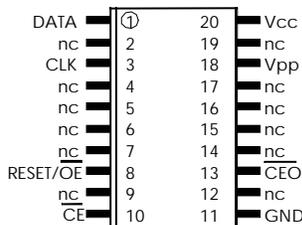
The Spartan Family of Serial Configuration PROMs provide easy-to-use, cost-effective configuration memory for Xilinx Field Programmable Gate Arrays.

These devices use a simple serial-access procedure to configure one or more LCA devices. The user can select the polarity of the reset function by programming a special bit. These devices are fully compatible and can be cascaded with other members of the XC17S00 family of devices.



8 Pin Dip/VOIC Assignments

All devices are available in the 8 pin DIP and 8 pin VOIC package except the XC17S40, XC17S40XL, XC17S50XL, XC17S100XL, and XC17S150XL which comes in the 8 pin DIP and 20 pin SOIC package (See below).



20-Pin SOIC Assignment (17S40/XL, 50XL, 100XL, 150XL Only)

The Spartan Family consists of 5 volt and 3.3 volt devices. For each 5 volt device (XC17S00), there is a 3.3 volt counterpart (XC17S00XL). All devices are one-time programmable (OTP) and are organized as follows:

XC17S05	65,536	x 1 bit
XC17S05XL	131,072	x 1 bit
XC17S10/XL	131,072	x 1 bit
XC17S20/XL	262,144	x 1 bit
XC17S30/XL	262,144	x 1 bit
XC17S40/XL	524,288	x 1 bit
XC17S50XL	1, 048,576	x 1 bit
XC17S100XL	1, 048,576	x 1 bit
XC17S150XL	1, 048,576	x 1 bit

Programming Overview

All the Spartan SPROMs are internally organized in rows, each row containing eight (8) words. The S05 device has 32 bit words and the S05XL, S10/XL, S20/XL, S30/XL and S40/XL has 64 bit words. Additional non-data rows are used to read the Manufacturer's/Device ID and set the Reset Polarity and cannot be used to store configuration data. The device programmer should prompt the user for the desired Reset Polarity.

Figure 1 shows the flow of how the SPROMs are programmed. See Figure 2 for the programming cycle overview and Figure 4 for the details of the programming cycle.

Enter Programming Mode

The programming mode is entered by holding \overline{CE} and \overline{OE} High with V_{PP} at V_{PP1} for two rising clock edges, then lowering V_{PP} to V_{PPNOM} for one more rising clock edge (See Figure 3). Once in the programming mode, the following functions are available.

Read Manufacturer's/Device ID

All of the SPROMs contain a Manufacturer's and Device identification code. Prior to attempting to program or verify the device, the device programmer should read this code and verify that it is the correct code for the device selected by the user. If not, display message "**Manufacturer or Device ID Error.**"

To read the Manufacturer's/Device identification code, first enter the programming mode. While holding \overline{CE} High and \overline{OE} Low, apply N_{IDCLK} (See Table 1) clock signals to the clock pin to access the ID row.

Table I Clock To ID (decimal)

	N_{IDCLK}	N_{RSTCLK}
S05	2,056	2,048
S05XL	4,600	4,104
S10/XL	4,600	4,104
S20/XL	4,600	4,104
S30/XL	4,600	4,104
S40/XL	19,791	16,384
S50XL	19,791	16,384
S100XL	19,791	16,384
S150XL	19,791	16,384

Then bring \overline{OE} High and \overline{CE} Low* . The first bit of the identification word is present when \overline{CE} goes Low and does not require a clock. Apply 15 additional clock signals to the CLK pin to read the complete device ID.

The Manufacturer's/Device ID

Consisting of 2 bytes of data. The first byte contains the JEDEC assigned Manufacturer's ID code for Xilinx (C9). The first four bits of the second byte define the density of the PROM (See Table II), while the last four bits of the second byte contain specific programming algorithm code (See Table III). The data is read out MSB first.

Table II Density Codes

<u>Device</u>	<u>Density Codes</u>
S05	F (1111)
S10/S10XL/S05XL	8 (1000)
S20/S20XL/S30/S30XL	A (1010)
S40/S40XL	9 (1001)
S50XL	9 (1101)
S100XL	9 (1101)
S150XL	9 (1101)

Table III Programming Algo Codes

<u>Device</u>	<u>Algorithm Code</u>
S10XL/S20XL/S40XL	9 (1001)
S05/S10/S20/S40	8 (1000)
S30XL/S05XL	7 (0111)
S30	6 (0110)
S50XL	6 (0110)
S100XL	7 (0111)
S150XL	9 (1001)

Loading and Programming a Data Word

The data word is shifted into the SPROM, one bit at a time, on the rising edge of the clock, while \overline{CE} and \overline{OE} are High. The data word counter is temporarily held in internal latches until the address is advanced to the next address, and is programmed into the memory as an entire word upon strobing the device with V_{PP} at V_{PP1} for 100 μ s.

The contents of the data word must now be verified at V_{PP2} . The data word is read while lowering \overline{CE} and capturing the data while clocking the device 31 or 63 times (See Programming Overview). The first bit of the word (LSB) is present when \overline{CE} goes low. After all bits were read, bring \overline{CE} high and compare the data to the original file data. If the data does not compare, stroke V_{PP} at V_{PP1} for 500 μ s. (Note, the original data is still contained in internal latches and does not have to be loaded into the device again.) Read the data word again (as described above) and compare it to the original data. If it still does not compare, pulse V_{PP} at V_{PP1} for another 500 μ s. Now read the data word again. If it still does not compare, power the device down and issue message: "Device Failed to Program". See Figure 4. If the word compares, increment the word counter as described below.

Increment the Address (Word) Counter

After successfully programming a data word, the address counter must be incremented. This is done on the rising edge of the clock while \overline{CE} is High and \overline{OE} is Low.*

Set RESET Polarity

The polarity of the Reset/ \overline{OE} pin may be made active Low by writing zeros into a dedicated row.(See Figure 5).

Reset/ \overline{OE} is located outside of the user data array. Enter the programming mode, then lower Reset/ \overline{OE} , hold the Data pin Low, strobe the clock N_{RSTCLK} times (See Table I), raise the Reset/ \overline{OE} pin, load the data latches with all zeros (see Load a Data Word above), and strobe V_{PP} at V_{PP1} for 5 ms.

The reset polarity has to be verified (sensed) at V_{PP2} while in programming mode. To sense the polarity bit, after strobing V_{PP} for 5ms, set \overline{CE} low and sense the $\overline{CE0}$ pin. If $\overline{CE0}$ is high, reset is active low (successfully programmed). If $\overline{CE0}$ is low, reset is active high (failed to program).

Writing ones or not writing anything maintains RESET active High.

Note:

The Reset Polarity is actually only the MSB of the data word.

* Be careful not to have \overline{CE} and \overline{OE} Low at the same time, as this causes the device to exit programming mode.

Sensing RESET Polarity

To sense or read the polarity of the Reset/ \overline{OE} pin, enter the programming mode, then lower Reset/ \overline{OE} , hold the Data pin High, then strobe the clock N_{RSTCLK} times (See Table I). Set Reset/ \overline{OE} High, set \overline{CE} Low and sense the $\overline{CE0}$ pin. If $\overline{CE0}$ is High, Reset is active Low. If $\overline{CE0}$ is Low, Reset is active High. The reset polarity bit is defaulted (unprogrammed) to active high. When the reset bit is programmed, the “reset” polarity is active low.

If the data fails to verify, display message **“Failed Margin Verify”**. If the data verifies, display message **“Device Passed”**.

Exit Programming Mode

To exit the programming mode, remove power from the device, per Figure 6.

Stand Alone Verify Of Data Bits

(Normal Mode)

The verify operation should be performed after programming. Power up the device and read the data bits out serially in normal readout mode (see Figure 7). A margin voltage (difference between V_{PP} and V_{CC}) is applied to the device to ensure charge retention on each programmed bit. Set V_{CC} to V_{CCVFY} and V_{PP} to V_{PPVFY} . When in normal mode, the Reset/ \overline{OE} signal should be driven active high if the reset polarity bit was unprogrammed (logic “1”). It should be driven active low if the reset polarity bit was programmed (logic “0”).

At the end of the verify operation the programmer must confirm that the $\overline{CE0}$ pin has gone Low one clock after the last bit is read out.

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC17S00, & XC17S00XL Family

Programming Mode Pin Assignments

DIP8 Pin	VOIC8 Pin	SOIC20 Pin	Name	I/O	Description
1	1	1	Data	I/O	The rising edge of the clock shifts a data word in or out of the SPROM one bit at a time.
2	2	3	CLK	I	Clock input. Used to increment the internal address/word counter for reading and programming.
3	3	8	RESET/ \overline{OE}	I	The rising edge of CLK shifts a data word into the PROM when \overline{CE} and \overline{OE} are High; it shifts a data word out of the PROM when \overline{CE} is Low and \overline{OE} is High. The address/word counter is incremented on the rising edge of CLK while \overline{CE} is held High and \overline{OE} is held Low. Note: Any modified polarity of the RESET/ \overline{OE} pin is ignored in the programming mode.
4	4	10	\overline{CE}	I	The rising edge of CLK shifts a data word into the PROM when \overline{CE} and \overline{OE} are High; it shifts a data word out of the PROM when \overline{CE} is Low and \overline{OE} is High. The address/word counter is incremented on the rising edge of CLK while \overline{CE} is held High and \overline{OE} is held Low.
5	5	11	GND		Ground pin
6	6	13	$\overline{CE0}$	O	The polarity of the RESET/ \overline{OE} pin can be read by sensing the $\overline{CE0}$ pin. Note: The polarity of the RESET/ \overline{OE} pin is ignored while in the programming mode. In final verification, this pin must be monitored to go Low one clock cycle after the last data bit has been read.
7	7	18	V_{PP}		Programming Voltage Supply. Programming mode is entered by holding \overline{CE} and \overline{OE} High and V_{PP} at V_{PP1} for two rising clock edges and then lowering V_{PP} to V_{PPNOM} for one more rising clock edge. A word is programmed by strobing the device with V_{PP} for the duration T_{PGM} . V_{PP} must be held at V_{CC} for normal operation.
8	8	20	V_{CC}		V_{CC} power supply input.

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC17S00, & XC17S00XL Family

DC Programming Specifications

Symbol	Description	Min	Recommended	Max	Units
V_{CCP}^*	Supply voltage during programming		5.0		V
V_{IL}	Low-level input voltage	0.0	0.0	0.5	V
V_{IH}	High-level input voltage	2.4	V_{CC}	V_{CC}	V
V_{OL}	Low-level output voltage			0.4	V
V_{OH}	High-level output voltage	2.5			V
V_{PP1}^{**}	Programming voltage	12.0	12.25	12.5	V
V_{PP2}^{***}	Margin verify voltage during programming		5.4		V
I_{PPP}	Supply current on programming pin			60	mA
V_{CCNOM}/V_{PPNOM}	Nominal Voltage		5.0		V
V_{CCVFY} (S00 Only)	Supply voltage during stand alone margin verify (5 volt devices)		5.0		V
V_{CCVFY} (S00XL Only)	Supply voltage during stand alone margin verify (3.3 volt devices)		3.3		V
V_{PPVFY} (S00 Only)	Margin voltage during stand alone margin verify (5 volt devices)		5.4		V
V_{PPVFY} (S00XL Only)	Margin voltage during stand alone margin verify (3.3 volt devices)		3.7		V

* Noise and voltage deviation allowed: $5.0V \pm 50$ mV.

** No overshoot is permitted on signal. V_{PP} must not be allowed to exceed V_{PP1} max.

*** Noise and voltage deviation allowed: $5.4V \pm 250$ mV.

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC17S00, & XC17S00XL Family

AC Programming Specifications

Symbol	Description	Min	Rec	Max	Units
1	T_{RPP}^*	10% to 90% rise time of V_{PP}	5		μs
2	T_{FPP}^*	90% to 10% fall time V_{PP}	5		μs
3	T_{PGM}	V_{PP} programming pulse width	90	100 (500 Retry)	μs
4	T_{SVC}	V_{PP} setup to CLK for entering programming	100		ns
5	T_{HVC}	V_{PP} hold from CLK for entering programming	300		ns
6	T_{SDP}	Data setup to CLK for programming	50		ns
7	T_{HDP}	Data hold from CLK for programming	0		ns
8	T_{SCC}	\overline{CE} setup from programming/verifying	100		ns
9	T_{ON}	Reset Pulse Width		5	ms
10	T_{SCV}	\overline{CE} hold from CLK for programming/verifying	100		ns
11	T_{HCV}	\overline{CE} hold from V_{PP} for programming	50		ns
12	T_{SIC}	\overline{OE} setup to CLK for incrementing address	100		ns
13	T_{HIC}	\overline{OE} hold from CLK for incrementing address	0		ns
14	T_{CAC}	CLK to data valid		400	ns
15	T_{OH}	Data hold from CLK	0		ns
16	T_{CE}	\overline{CE} low to data valid		250	ns

* Use the fastest rise and fall time (permitting no overshoot or undershoot) your hardware can support.

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC17S00, & XC17S00XL Family

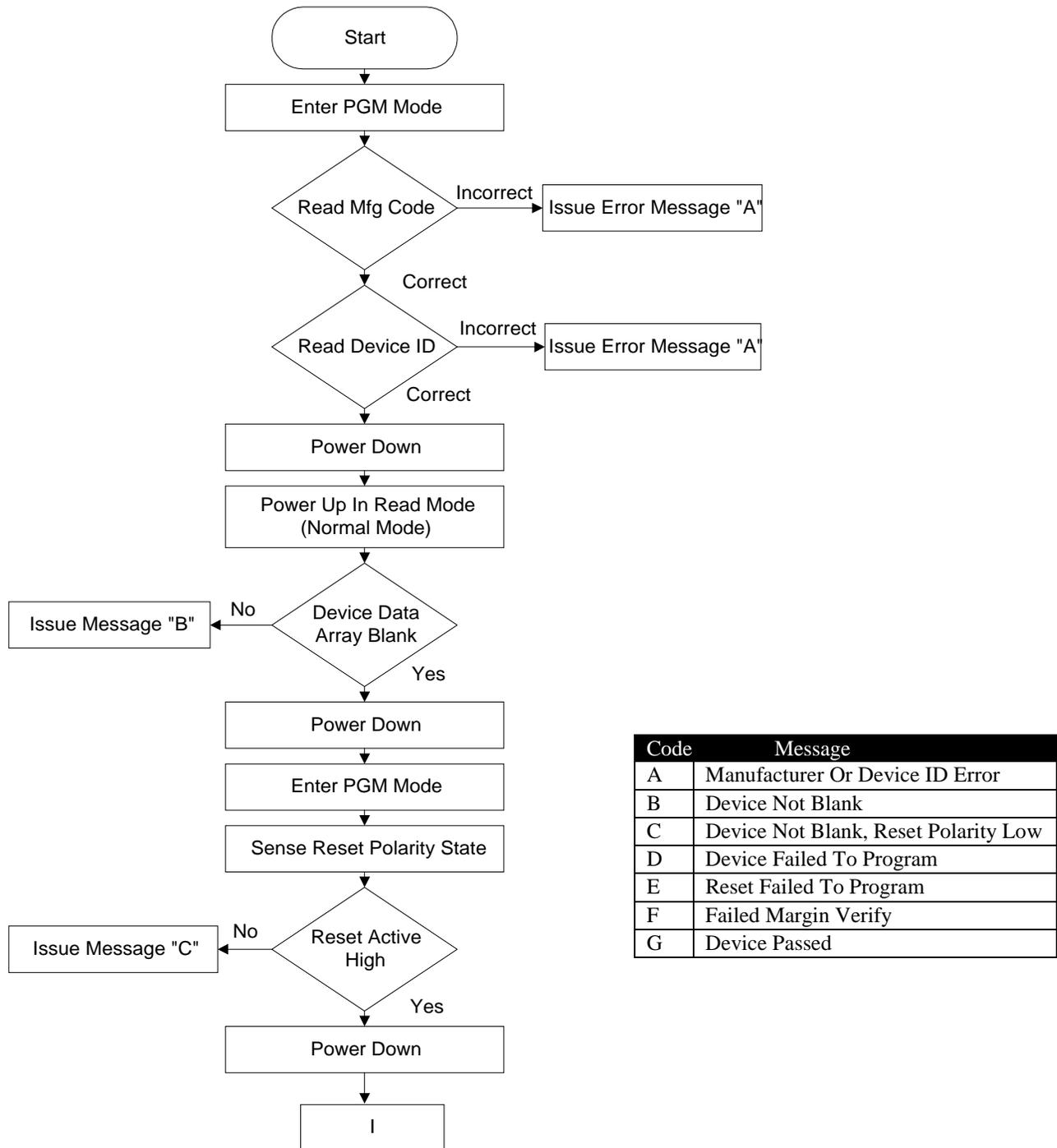
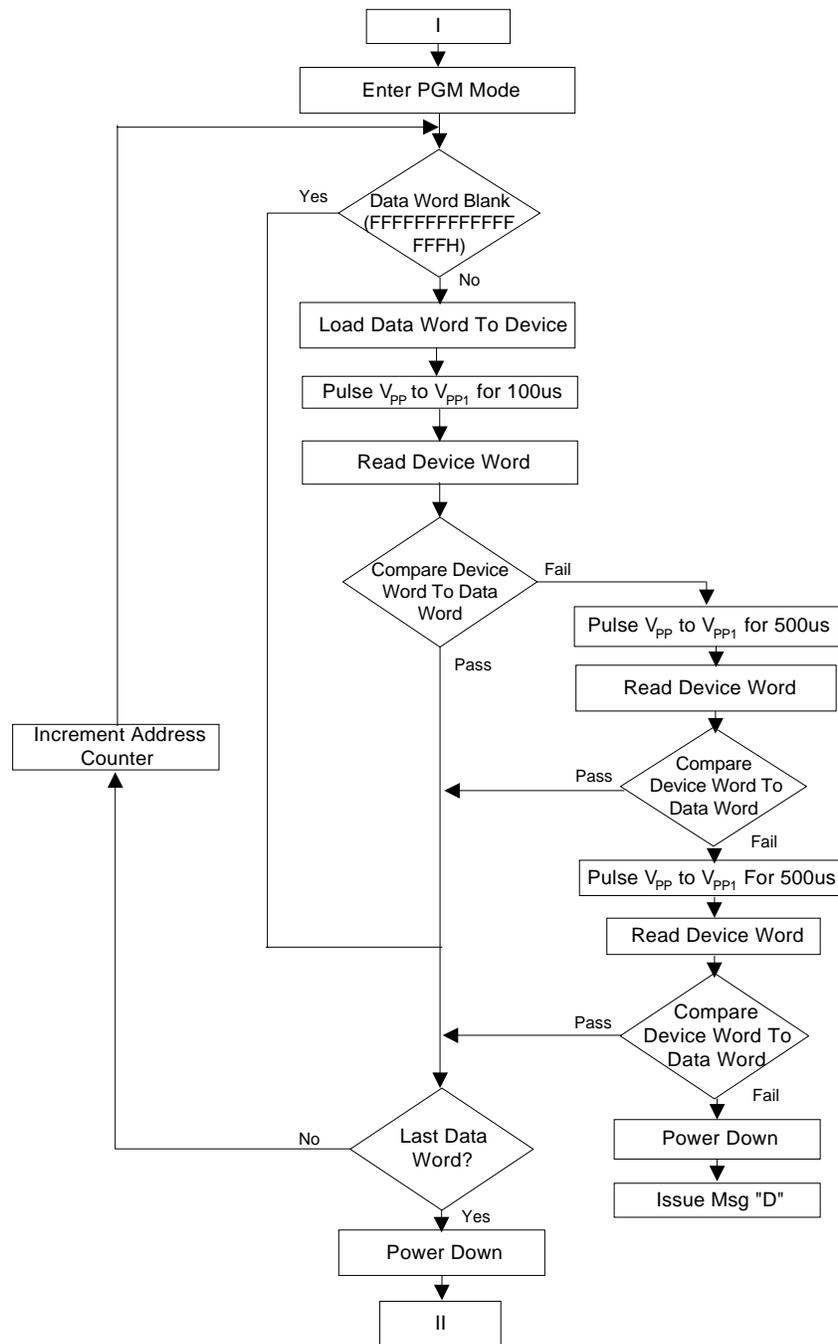


Figure 1. Programming Flow

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC17S00, & XC17S00XL Family



*32 or 64 bits, See Programming Overview

Figure 1. Programming Flow (Continued)

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC17S00, & XC17S00XL Family

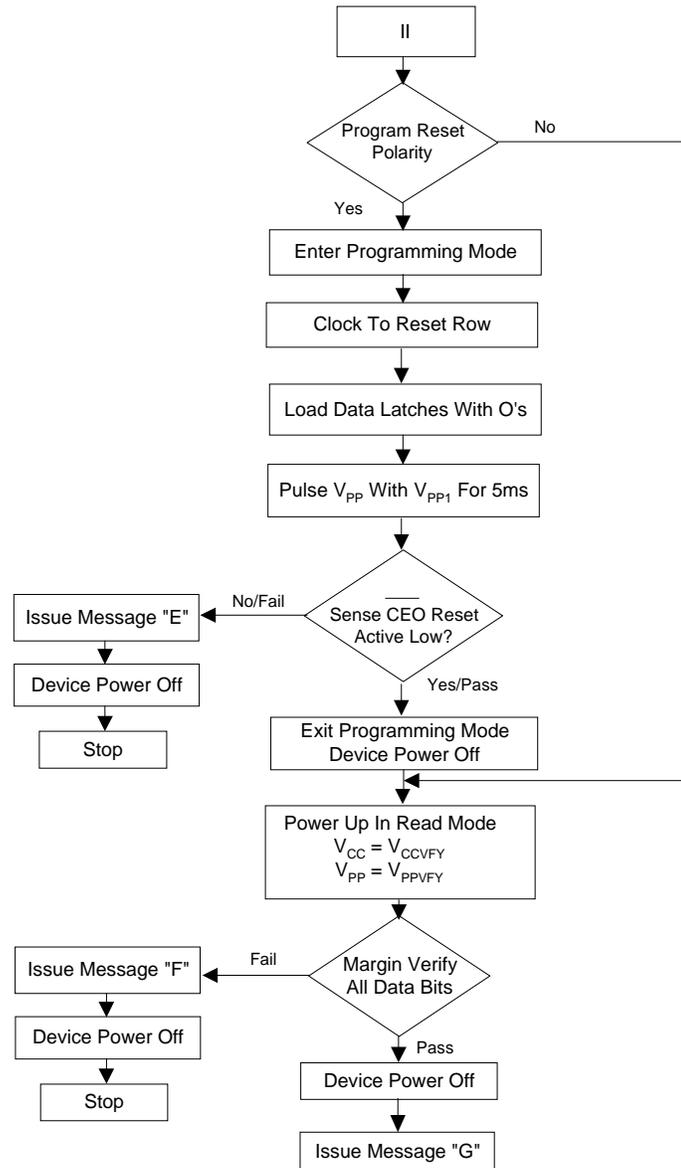


Figure 1. Programming Flow (Continued)

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC17S00, & XC17S00XL

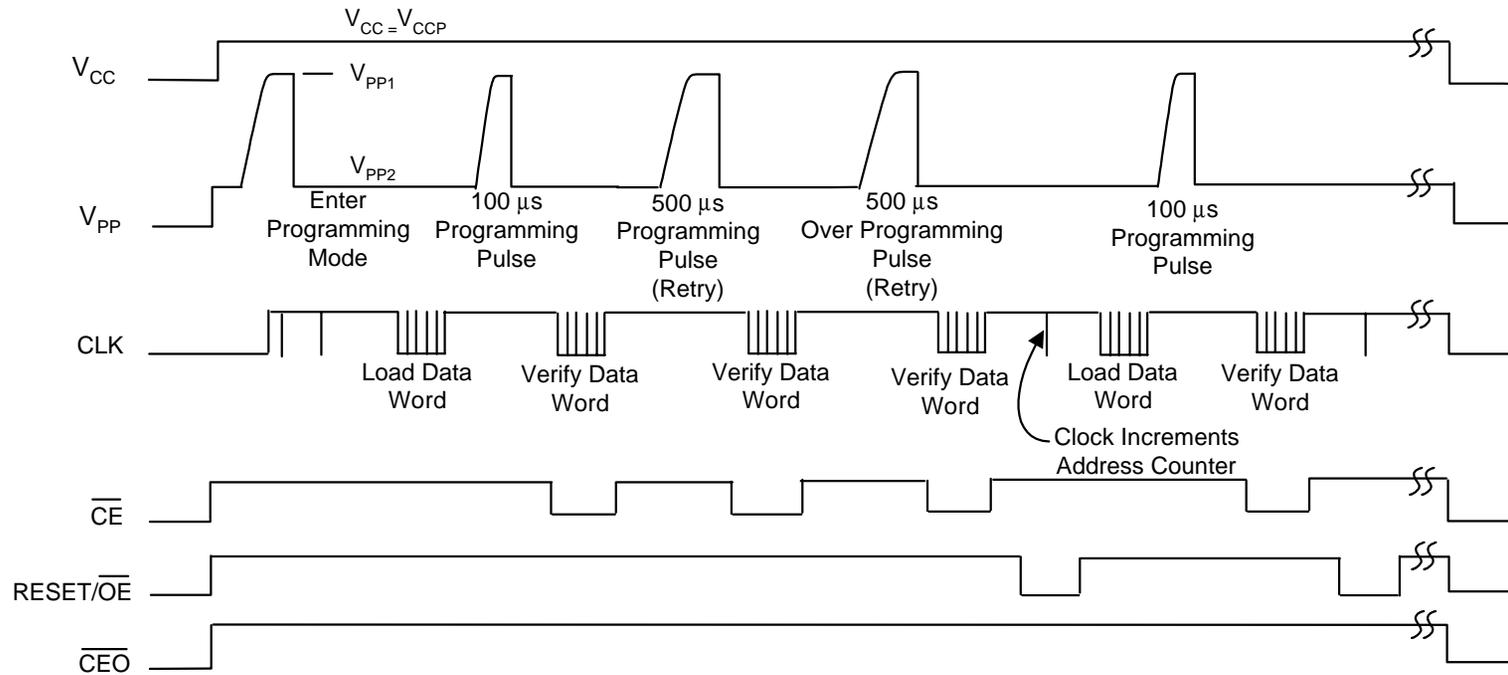


Figure 2. Programming Cycle Overview

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC17S00, & XC17S00XL

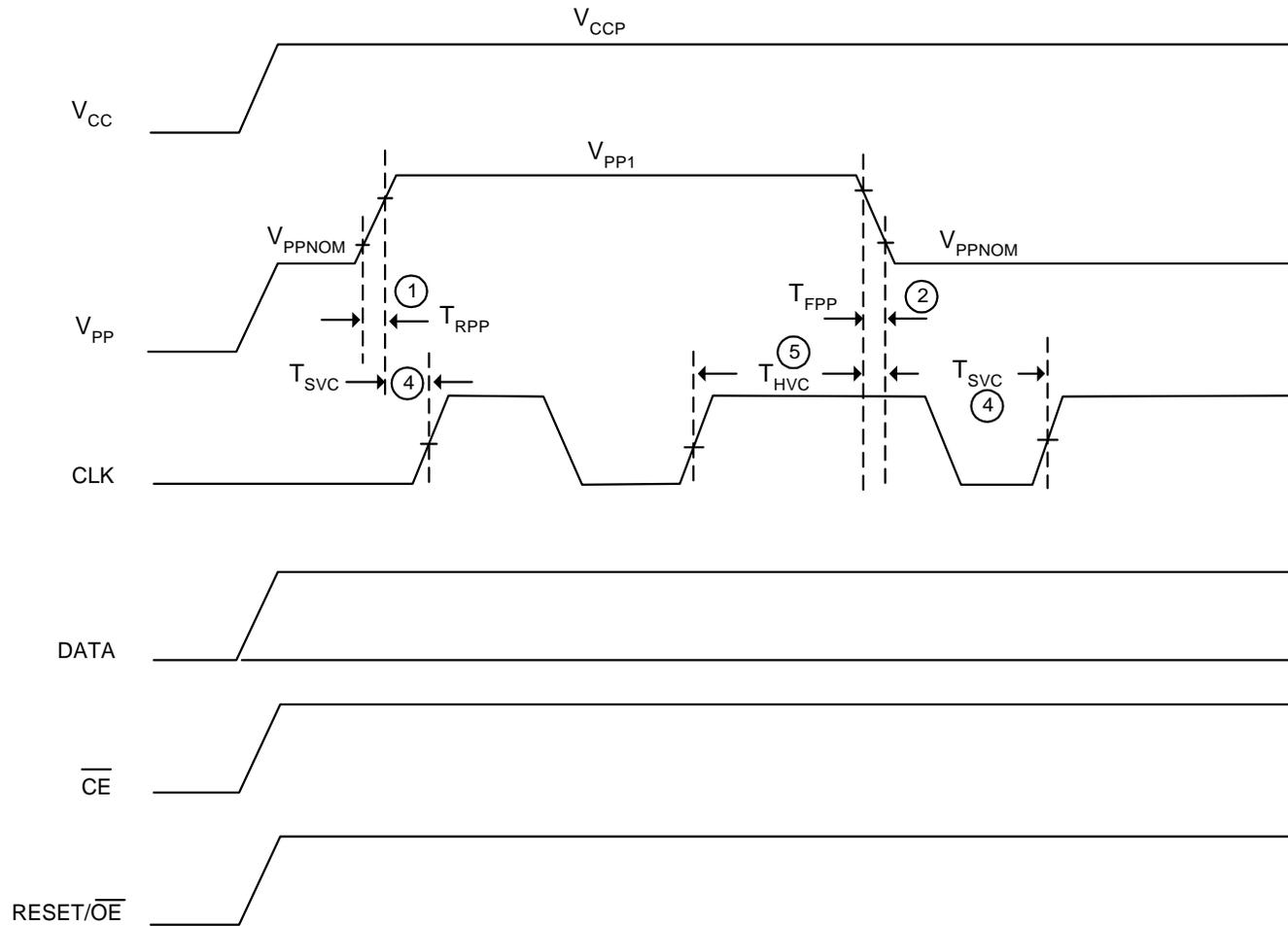


Figure 3. Enter Programming Mode

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC17S00, & XC17S00XL

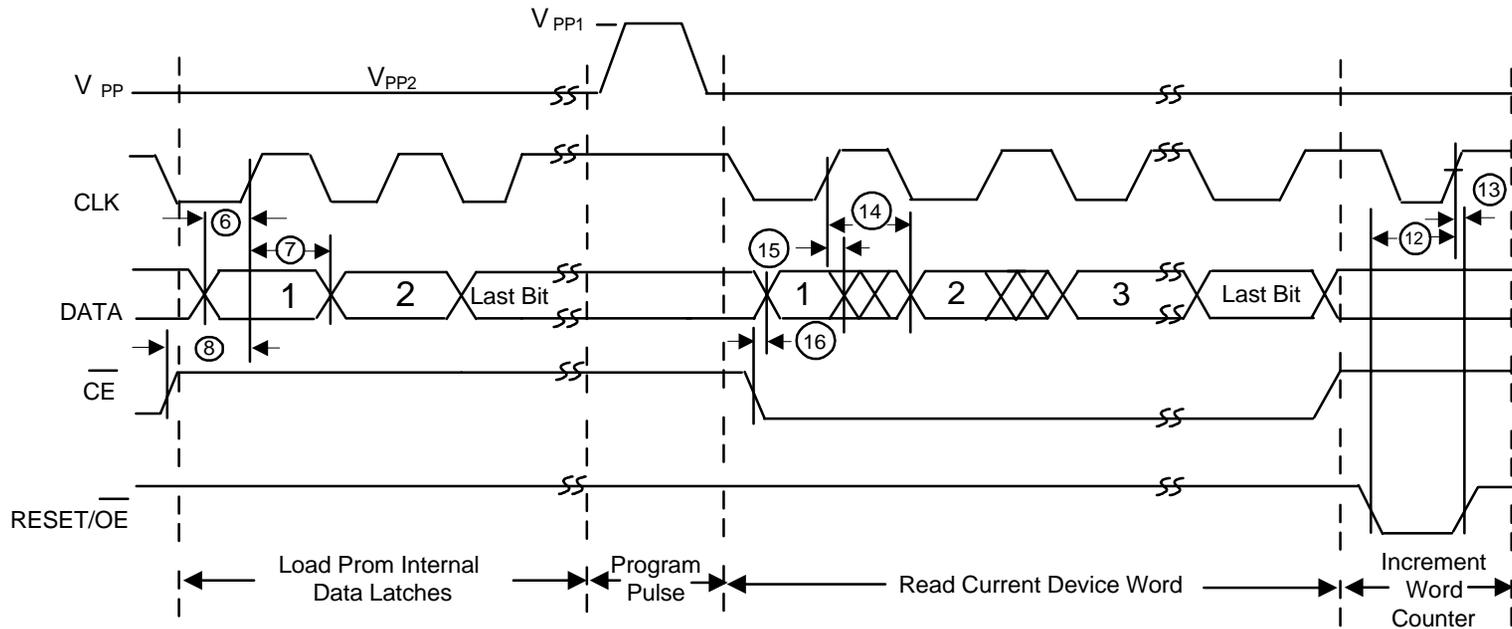


Figure 4. Details Of The Programming Cycle

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC17S00, & XC17S00XL

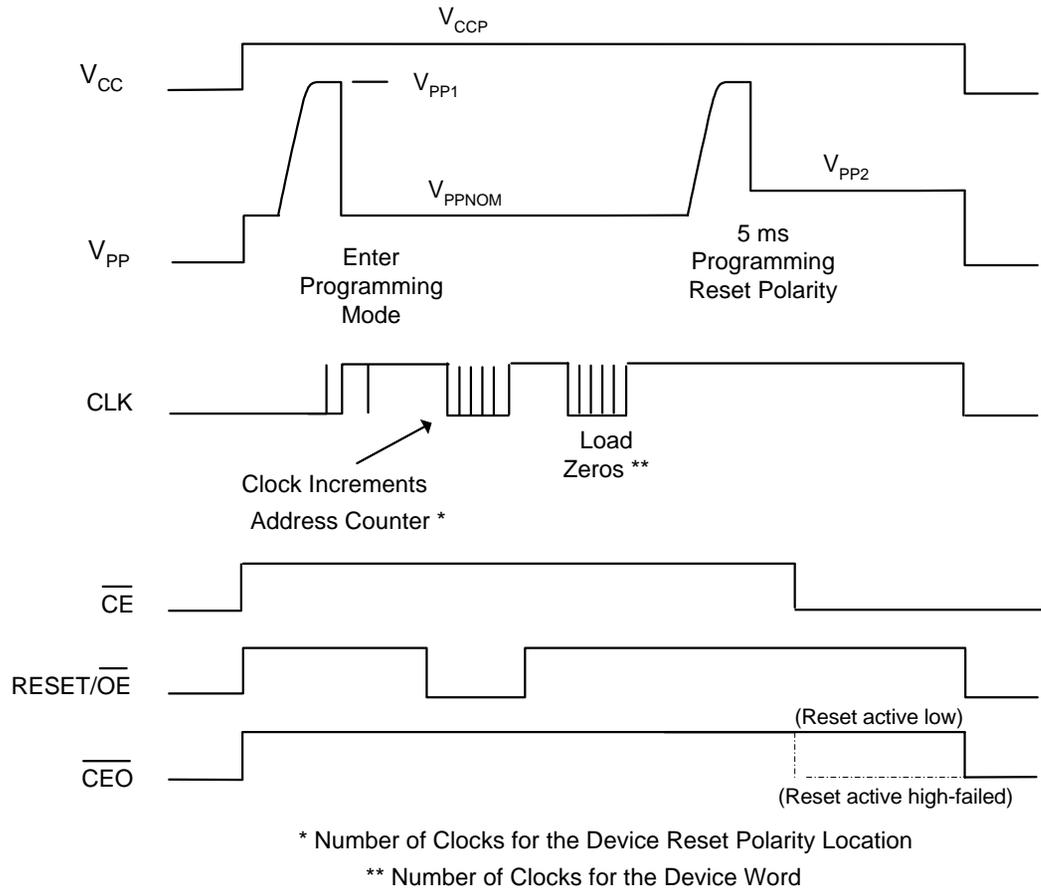
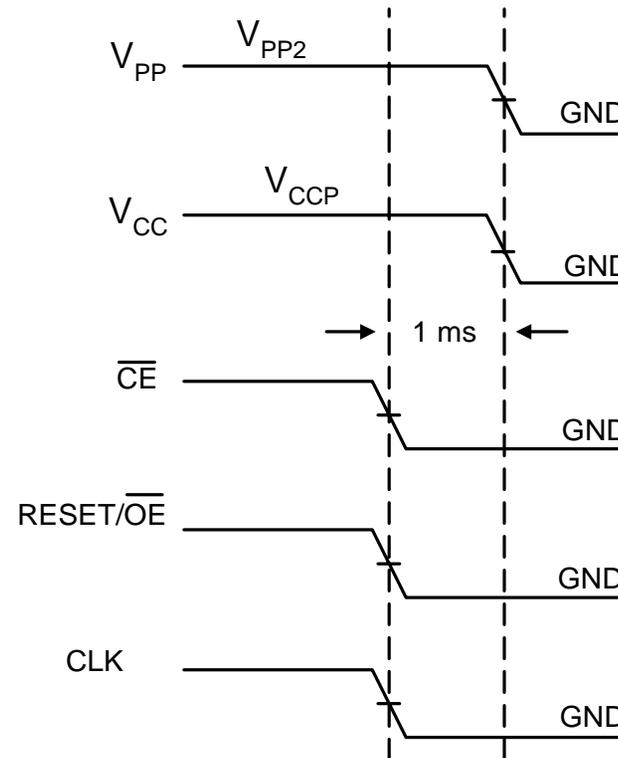


Figure 5. Programming Reset Polarity

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC17S00, & XC17S00XL



If your programming hardware does not allow V_{PP} and V_{CC} to power up and down simultaneously, make sure to first power up V_{PP} during power up and power down V_{PP} after V_{CC} during power down.

Figure 6. Exit Programming Mode

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC17S00, & XC17S00XL

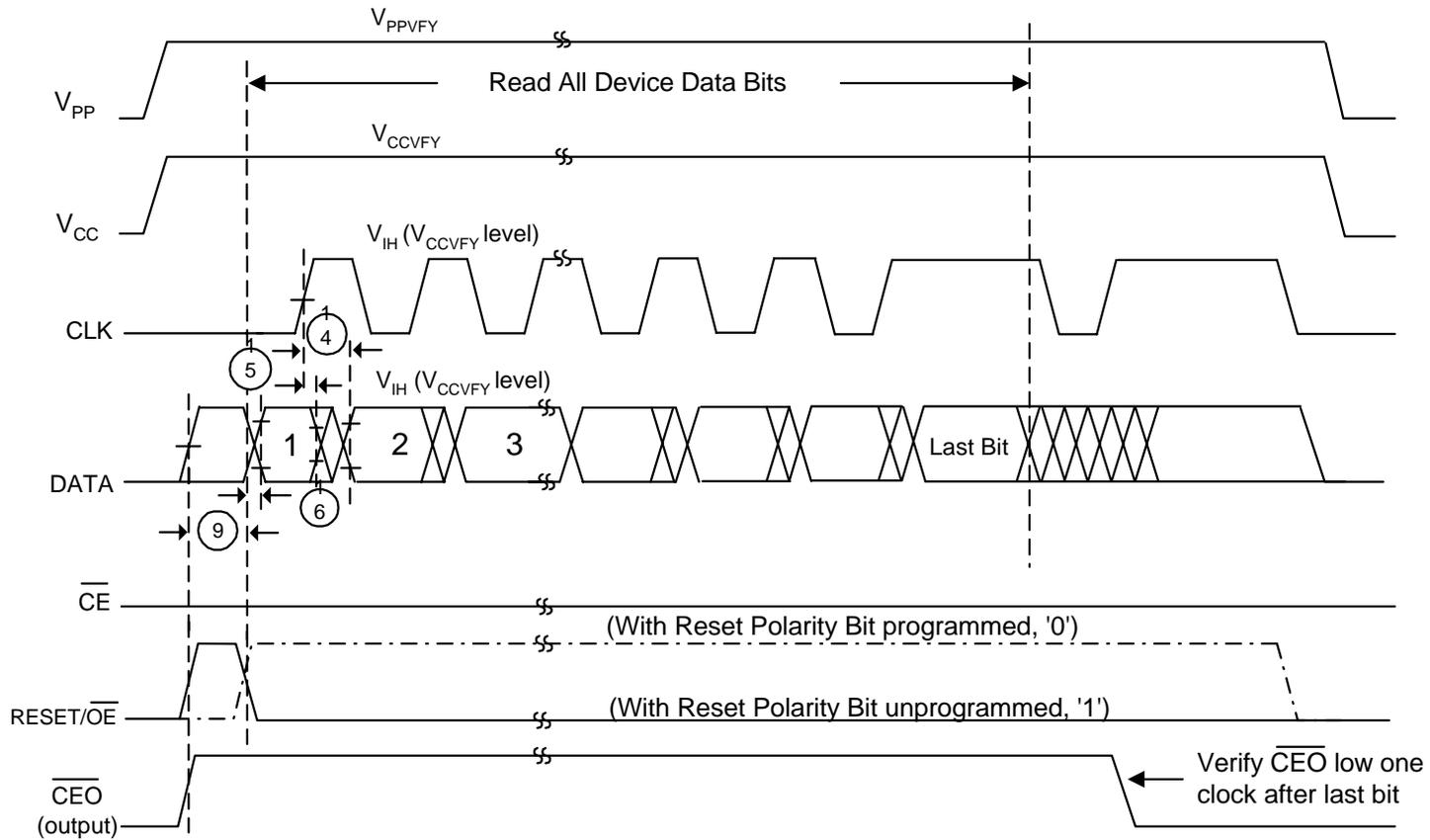


Figure 7. Details Of Verify Cycle