XRD64L14

3.3V CMOS 10-Bit, 20 MSPS, High Speed Analog-to-Digital Converter with 4:1 Input Analog Multiplexer

...the analog plus company™

March 1997–3

FEATURES

- 10-Bit Resolution
- 20MHz Sampling Rate
- 4:1 Analog Input Multiplexer
- Internal S/H Function
- Single 3.0V Power Supply
- V_{IN} DC Range: 0V to AV_{DD}
- V_{REF} DC Range: 1V to AV_{DD}
- Low Power: 80mW (typ)
- Three-State Digital Outputs
- Power Down: 1.0mW (typ) Power Dissipation
- ESD Protection: 2000V Minimum
- For 5V Operation Refer to XRD6414

APPLICATIONS

- Multiplexed Data Acquisition
- Precision Scanners
- Digital Color Copiers
- Test and Scientific Instruments
- Digital Cameras
- Medical Imaging
- IR Imaging

BENEFITS

- Complete Analog-to-Digital Converter (ADC) that Requires no External Active Components
- Small Outline Package to Reduce Board Space
- Low Power Dissipation
- Easy to Use Rugged Design

GENERAL DESCRIPTION

The XRD64L14 is a 10-bit, 20MSPS, Analog-to-Digital Converter (ADC) with a 4:1 Analog Input Multiplexer for applications that require high speed and high accuracy. Designed using an advanced CMOS process, this part offers excellent performance, low power consumption and latch-up free operation.

The XRD64L14 uses a subranging architecture to maintain low power consumption at high conversion rates. Our proprietary comparator design achieves a low analog input capacitance. The input circuitry of the XRD64L14 includes an on-chip S/H function that allows the product to digitize analog input signals between AGND and AV_{DD}. The XRD64L14 can be placed into power down (stand-by) mode, reducing the power dissipation to 1.0mW (typical) by a digitally controlled pin.

Providing external reference voltages allows easy interface to any input signal range between AGND and AV_{DD}. This also allows the system to calibrate out zero scale and full scale errors by adjusting V_{RT} and V_{RB}.

This device operates from a single 3.3V supply. Power consumption from a 3.3V supply is typically 80mW at F_S=15MHz. For 5V power supply operation refer to XRD6414.

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
XRD64L14AIQ	32 Lead Plastic TQFP (7 x 7 x 1.4 mm)	–40°C to +85°C

EXAR Corporation, 48720 Kato Road, Fremont, CA 94538 ◆ (510) 668-7000 ◆ FAX (510) 668-7017

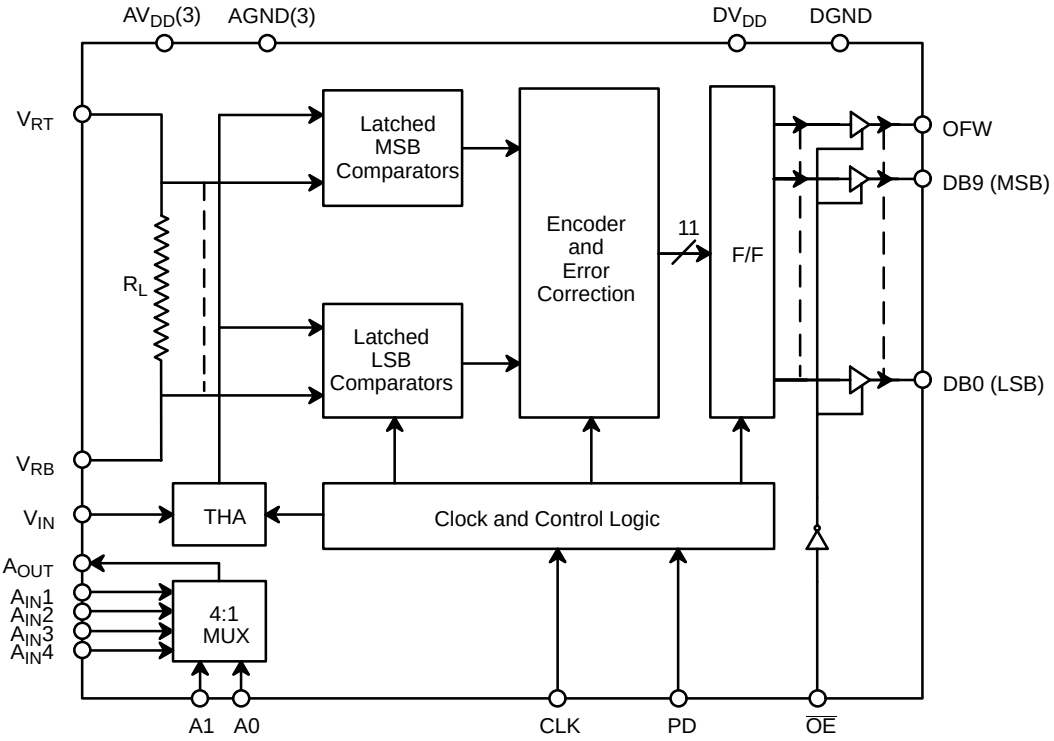
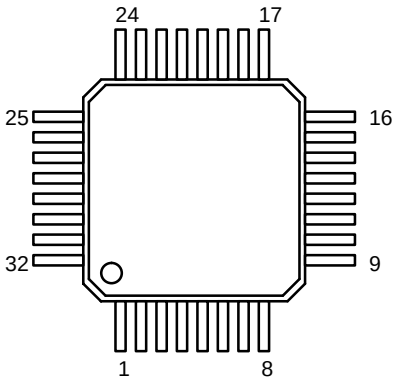


Figure 1. Simplified Block Diagram

PIN CONFIGURATION



32 Lead TQFP (7 x 7 x 1.4 mm)

PIN DESCRIPTION

Pin #	Symbol	Description
1	DB9	Data Output Bit 9 (MSB)
2	DGND	Ground (Digital Outputs)
3	AGND	Ground
4	A0	MUX Select Bit 0
5	A1	MUX Select Bit 1
6	AV_{DD}	Power Supply
7	CLK	Sampling Clock Input
8	$\overline{OE}$	Output Enable Control
9	PD	Power Down Control
10	AV_{DD}	Power Supply
11	AGND	Ground
12	V_{RT}	Top of Reference Ladder
13	V_{RB}	Bottom of Reference Ladder
14	$A_{IN}4$	MUX Analog Signal Input 4
15	$A_{IN}3$	MUX Analog Signal Input 3
16	AGND	Ground
17	$A_{IN}2$	MUX Analog Signal Input 2
18	$A_{IN}1$	MUX Analog Signal Input 1
19	A_{OUT}	MUX Analog Signal Output
20	V_{IN}	Analog Input Voltage to ADC
21	AV_{DD}	Power Supply
22	DV_{DD}	Power Supply (Digital Outputs)
23	OFW	Overflow Output
24	DB0	Data Output Bit 0 (LSB)
25	DB1	Data Output Bit 1
26	DB2	Data Output Bit 2
27	DB3	Data Output Bit 3
28	DB4	Data Output Bit 4
29	DB5	Data Output Bit 5
30	DB6	Data Output Bit 6
31	DB7	Data Output Bit 7
32	DB8	Data Output Bit 8

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified: AV_{DD} = DV_{DD} = 3.3V, F_S = 15MHz (50% Duty Cycle), V_{RT} = 2.5V, V_{RB} = 0.5V, T_A = 25°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Key Features						
n	Resolution	10			Bits	
F_S	Maximum Sample Rate		20	15	MSPS	
DC Accuracy[1]						
DNL	Differential Non-Linearity	–0.8	0.6	1.0	LSB	
INL	Integral Non-Linearity	–2.5	1.5	2.5	LSB	Best fit line (Max INL – Min INL)/2
EZS	Zero Scale Error	0	20	40	mV	
EFS	Full Scale Error	–1.0	±0.4	1.0	%	
V_{INPP}	DC Input Range	AGND		AV_{DD}	V	V_{IN} can swing from GND to AV_{DD}, actual digitized range is set by V_{RT} & V_{RB}.
Reference Voltages						
V_{RT}	Top Reference Voltage	1.0	2.5	AV_{DD}	V	
V_{RB}	Bottom Reference Voltage	AGND	0.5	AV_{DD}–1	V	
V_{REF}	Differential Ref. Voltage[2]	1.0	2	AV_{DD}	V	
R_L	Ladder Resistance	350	500	650	Ω	
Analog Input[3]						
	Input Voltage Range	V_{RB}		V_{RT}	V	V_{RB} Min. = AGND V_{RT} Max = AV_{DD}
BW	Input Bandwidth (–1 dB)[4]		50		MHz	
C_{IN}	Input Capacitance Sample[5]		20		pF	CLK = low
C_{IN}	Input Capacitance Convert[5]		7		pF	CLK = high
Analog Multiplexer						
R_{ON}	Switch Impedance		80	150	Ω	
R_{OFF}	Switch Impedance		10	5	MΩ	
T_{SW}	Switching Time		15		ns	
X_t	Crosstalk		–80		dB	f_{IN} = 6MHz
Conversion Character						
t_{AP}	Aperture Delay		6		ns	
t_{AJ}	Aperture Jitter		30		ps	
Dynamic						
SNR	Signal-to-Noise Ratio					
	F_{IN} = 1MHz		58		dB	F_S = 10MSPS
SNDR	SNR and Distortion					
	F_{IN} = 1MHz		57		dB	F_S = 10MSPS

ELECTRICAL CHARACTERISTICS (CONT'D)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Digital Inputs						
V_{IH}	Digital Input High Voltage	2.5			V	
V_{IL}	Digital Input Low Voltage			0.5	V	
I_{IN}	DC Leakage Currents[6]					
	CLK, $\overline{OE}$, PD, A0, A1		5		µA	Between GND and AV_{DD}
	Input Capacitance		5		pF	
Digital Outputs						
V_{OH}	Output High Voltage	2.5			V	
V_{OL}	Output Low Voltage			0.4	V	
I_{OZ}	High-Z Leakage	–10		10	µA	OE = high, or PD = high
t_{DL}	Data Valid Delay[2]	10	12	14	ns	
t_{DEN}	Data Enable Delay	10	12	14	ns	
t_{DHZ}	Data High-Z Delay	7	8	9	ns	
	Pipeline Delay (Latency)		3		cycles	Time delay between CLK and data output
Power Supplies						
I_{DD}(PD)	Power Down (I_{DD})		0.3	0.5	mA	PD = high, excluding current through reference ladder
AV_{DD}	Operating Voltage[7,8]	2.7	3.3	3.6	V	
DV_{DD}	Logic Power Supply[9]	2.7	3.3	3.6	V	
I_{DD}	Supply Current (I_{DD})		24	32	mA	PD = low

Notes

1 *Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width (V_{REF}/1024) is the DNL error. The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage. Accuracy is a function of the sampling rate (FS).*

2 *Specified values guarantee functionality. Refer to other parameters for accuracy.*

3 *Guaranteed. Not tested.*

4 *–1 dB bandwidth is a measure of performance of the A/D input stage (S/H + amplifier). Refer to other parameters for accuracy within the specified bandwidth.*

5 *See V_{IN} equivalent circuit. Switched capacitor analog input requires driver with low output resistance.*

6 *All inputs have diodes to AV_{DD} and AGND. Input DC currents will not exceed specified limits for any input voltage between AGND and AV_{DD}.*

7 *The AGND pins are connected through the silicon substrate. Connect all AGND pins together at the package and to the analog ground plane. DGND and AGND are connected through junction diodes. See logic output interface section.*

8 *The AV_{DD} pins should be tied together at the package.*

9 *See logic output interface section.*

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND	+7.0V
V_{RT} & V_{RB}	V_{DD} +0.5 to GND –0.5V
V_{IN}	V_{DD} +0.5 to GND –0.5V
All Inputs	V_{DD} +0.5 to GND –0.5V
All Outputs	V_{DD} +0.5 to GND –0.5V
Storage Temperature	–65 to +150°C
Package Power Dissipation Rating to 75°C	
TQFP	1000mW
Derates above 75°C	14mW/°C
Lead Temperature (Soldering 10 seconds)	+300°C

Notes:

1 *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.*

2 *Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies.* All inputs have protection diodes *which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.*

3 *V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.*

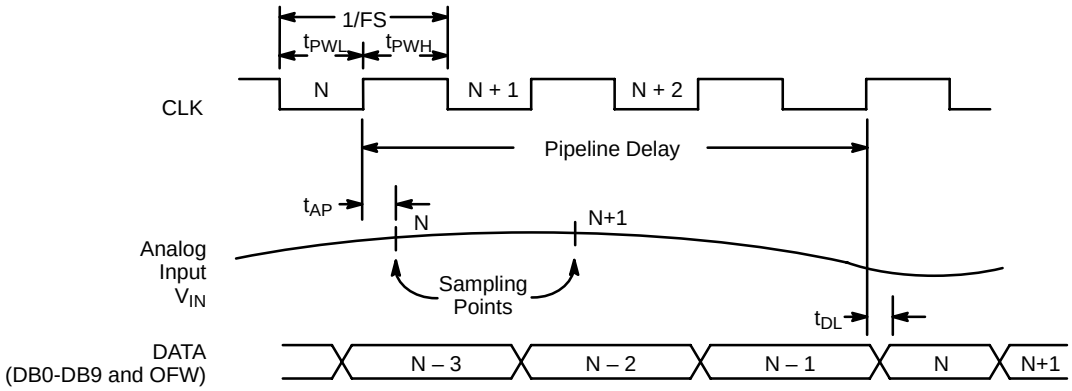


Figure 2. XRD64L14 Timing Diagram

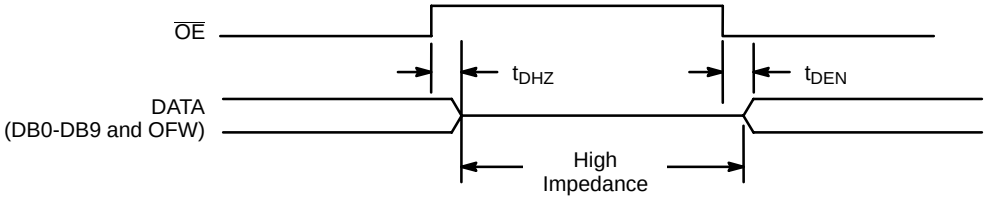


Figure 3. 3-State Timing Diagram

THEORY OF OPERATION

V_{IN} Analog Input

This part has a switched capacitor type input circuit. The input impedance changes with the phase of the input clock. V_{IN} is sampled at the low to high clock transition and the digital data changes at the low to high clock transition. The diagram *Figure 4.* shows an equivalent input circuit.

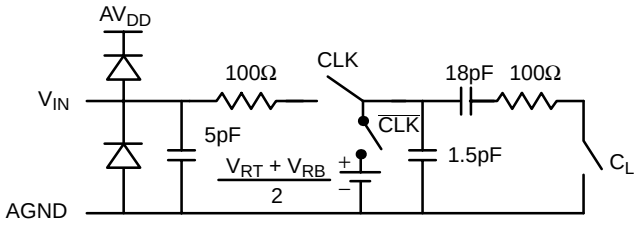


Figure 4. Equivalent Input Circuit

OFW Overflow (Output)

This signal indicates when the Analog Input (V_{IN}) goes above V_{RT}. The pin is normally at a low logic level. When $V_{IN} > V_{RT}$, OFW will go high and the data bits (DB0 – DB9) will show full scale (i.e. all 1s).

$\overline{OE}$ Output Enable (Input)

This signal controls the 3-state drivers on the digital outputs DB0 – DB9 and OFW. During normal operation $\overline{OE}$ should be held low so that all outputs are enabled. When $\overline{OE}$ is driven high DB0 – DB9 and OFW go into high impedance mode. This control operates asynchronous to the clock and will only control the output drivers. The internal output register will get updated if the clock is running while the outputs are in three-state mode.

$\overline{OE}$	DBO-DB9	OFW
0	Enabled	Enabled
1	Three-Stated	Three-Stated

Table 1. Output Enable

Power Supply Sequencing

There are no power supply sequencing issues if DV_{DD} and AV_{DD} of the XRD64L14 are driven from the same supply. Best parametric results, however, are obtained when DV_{DD} and AV_{DD} are driven from separate supplies. When DV_{DD} and AV_{DD} are driven separately, AV_{DD} must come up at the same time or before DV_{DD}, and go down at the same time or after DV_{DD}. If the power supply sequencing in this case is not followed, then damage may occur to the product due to current flow through the source-body junction diodes between DV_{DD} and AV_{DD}.

Logic Output Interface

The digital output drive circuitry of the XRD64L14 was designed to operate separately from the analog supplies. The DV_{DD} pin of the XRD64L14 is a separate power supply dedicated to the logic output drivers. DV_{DD} is not connected internally with any of the other power supplies. *Figure 5.* illustrates the power supply circuity of the XRD64L14.

DV_{DD} and DGND connect directly to the digital logic power of the user's system isolating the analog and digital power supplies and grounds. DGND is not common to the XRD64L14 substrate. The XRD64L14 substrate is common only to the packages' GND pins. See the power supply sequencing section if AV_{DD} and DV_{DD} are powered separately.

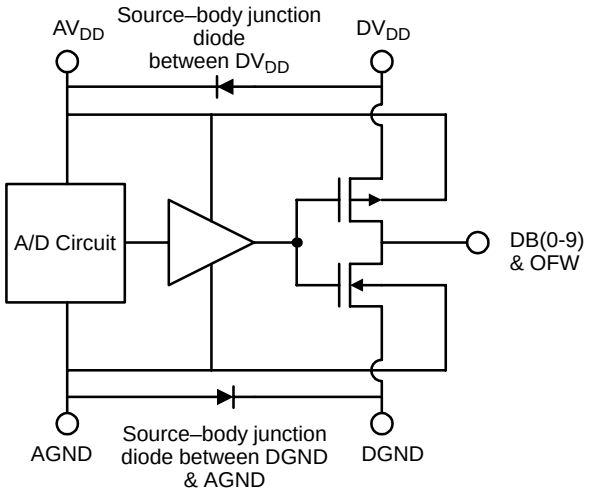


Figure 5. XRD64L14 ADC Power Supply Circuit Allows Separate AV_{DD} & DV_{DD} and Separate AGND & DGND

FINAL DESIGN CONSIDERATIONS

The XRD64L14 can be evaluated with the XRD6414AB application board. Contact your distributor or sales person for delivery. Using the XRD64L14AB the following final design considerations can be made.

1. Be generous with analog and digital ground planes. Mirror the ground plane with the supply planes. Use a 5 mil power / ground plane separation if a four layer board can be used. The XRD64L14 substrate is common to the packages' AGND pins only. DGND and DV_{DD} are separate supplies dedicated to the output logic drivers of the XRD64L14. Connect DGND and DV_{DD} to the power planes of the system's digital logic.
2. Keep high frequency decoupling capacitors very close to the A/D pins and minimize the loop area included so less flux will induce less noise. Use decoupling capacitors in the same locations as on the XRD6414AB.
3. Coupling between logic signals and analog circuitry can easily change a 10-bit system into an 8-bit system or worse. Completely separate them. Watch for coupling opportunities from other sources not immediately associated with the A/D. Don't use switching power supplies in adjacent locations, for example.
4. The DC performance of the XRD64L14 is optimized with rise and fall times of CLK edges limited to greater than or equal to 10ns. A resistor in series with the CLK input pin can combine with parasitic capacitance to limit rise and fall times. Select a low jitter clock with a 50% duty cycle for best spectral results.
5. Use support devices equivalent to those used on the evaluation board. Use the application board to verify these devices up front, i.e. use very linear passive components in the signal path.
6. Select a driving op amp whose noise, speed, and linearity fits the application. Use a resistor to decouple the output of the driving op amp from the switching input capacitance of the XRD64L14.
7. DNL and INL performance is optimized when the V_{RB} input of the XRD64L14 is buffered. If V_{RB} is connected to the PCB ground plane it is subject to the noise and ground bounce in that plane. For example V_{RB} could be buffered to 50mV above ground and still have a wide reference voltage range set by connecting V_{RT} to a voltage near AV_{DD}.
8. Use 50 or 100Ω resistors to isolate the XRD64L14 digital output pins from a latch or bus connection. This protects the output drivers and reduces the effects of high speed switching logic signals from degrading the ADC performance. Layout the latch or digital buffers as close to the ADC as possible to minimize trace length.

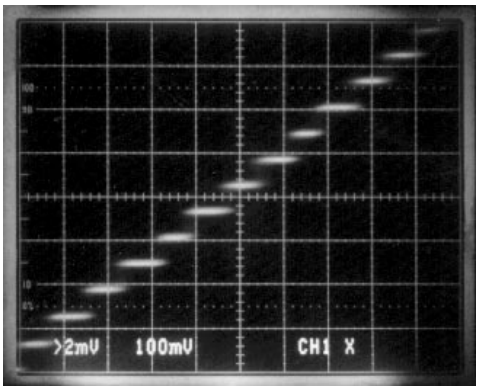


Figure 6. Crossplot Staircase Output
CLK = (15MSPS, t_{rf} = 15 ns), AV_{DD} = 3V,
V_{REF} = 2V

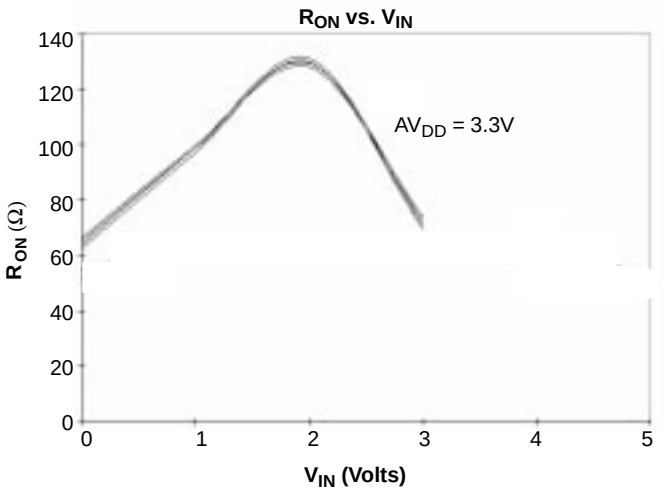


Figure 7. Analog MUX R_{ON} vs. Input Voltage

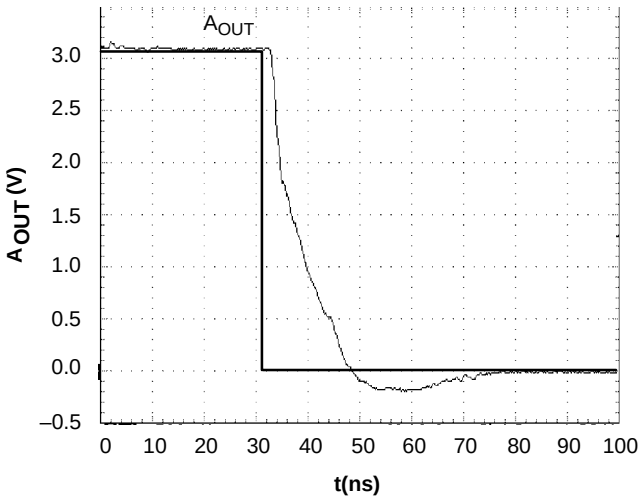


Figure 8. MUX Switching Time Waveform,
AV_{DD} = 3V

A1	A0	Selected Analog Input
0	0	$A_{IN}1$
0	1	$A_{IN}2$
1	0	$A_{IN}3$
1	1	$A_{IN}4$

Table 2. Truth Table for Analog Input Selection

PD	Device Status
1	Off (Not Operating)
0	On (Operating)

Table 3. Power Down

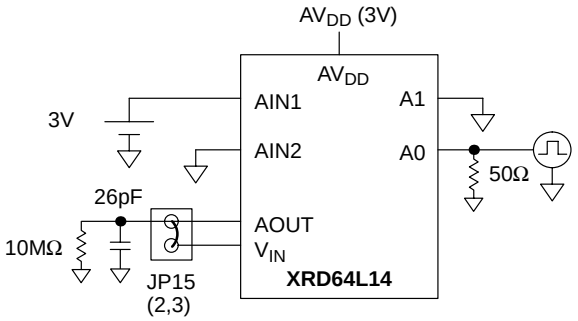


Figure 9. MUX Switching Time Test Circuit

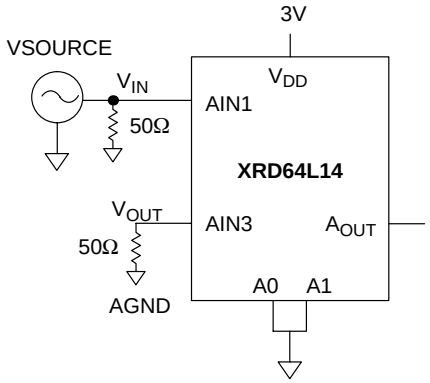


Figure 10. Crosstalk Test Circuit

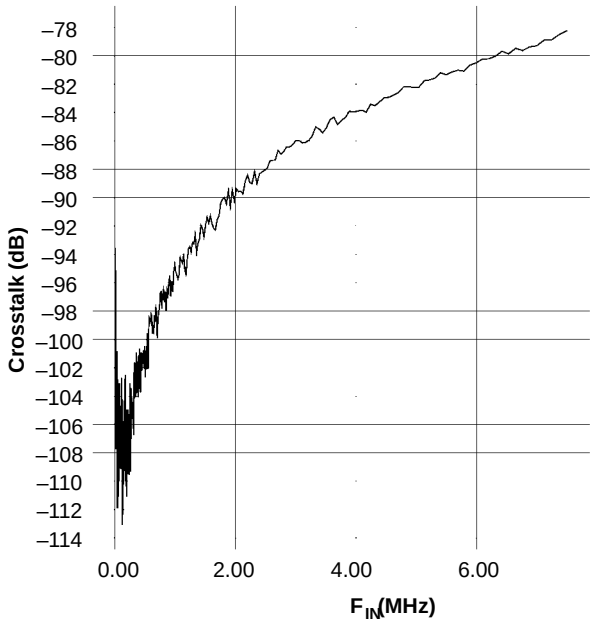


Figure 11. XRD64L14 Crosstalk, AV_{DD} = 3V and V_{IN} = 8dBm

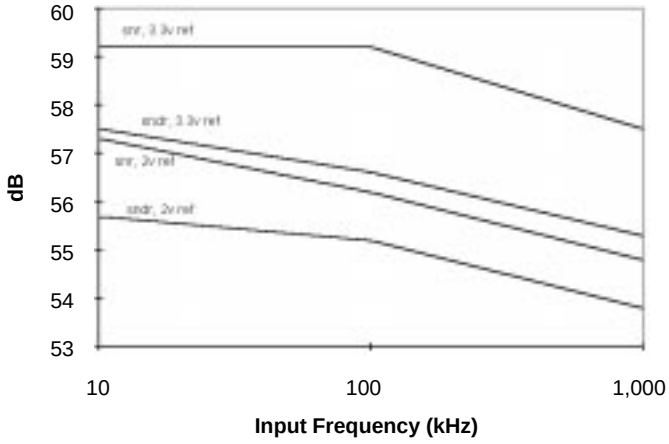


Figure 12. XRD64L14 SNR & SNDR vs. F_{IN}, AV_{DD} = 3.3V, DV_{DD} = 3.3V, V_{REF} =3.3V & 2V, F_S = 10MSPS, C_{IN} = 100pF

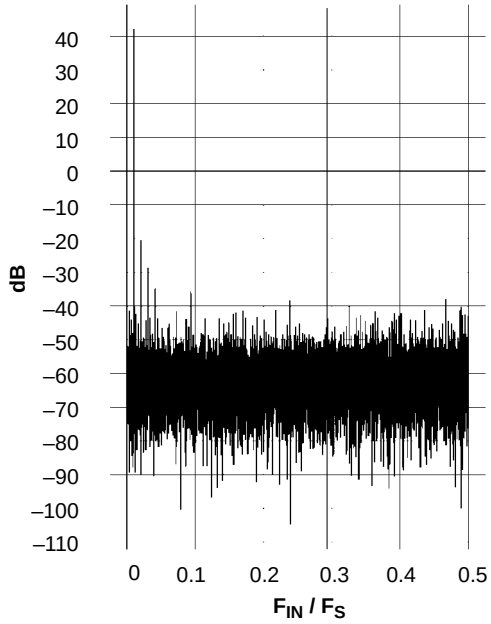


Figure 13. XRD64L14 FFT VREF = V_{DD} = 3V, DV_{DD} = 3.3V, F_{IN} = 100kHz, F_S = 10MSPS, C_{IN} = 100pF

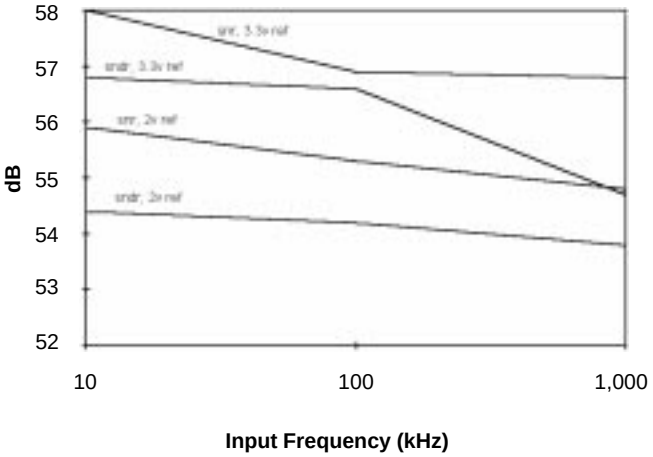


Figure 14. XRD64L14 SNR & SNDR vs. F_{IN}, AV_{DD} = 3.3V, DV_{DD} = 3.3V, V_{REF} = 3.3V & 2V, F_S = 15MSPS, C_{IN} = 100pF

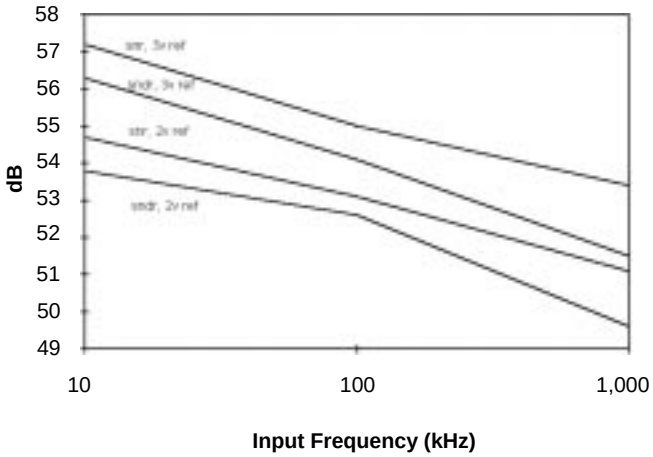


Figure 15. XRD64L14 SNR & SNDR vs. F_{IN}, AV_{DD} = 3.3V, DV_{DD} = 3.3V, V_{REF} = 3.3V & 2V, F_S = 20MSPS, C_{IN} = 100pF

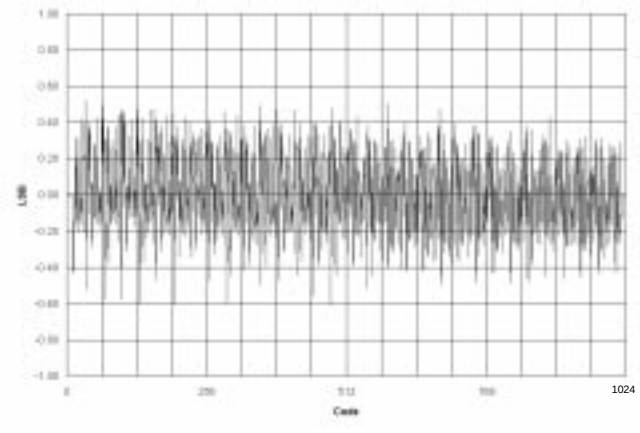


Figure 16. XRD64L14 DNL @ 15MSPS, AV_{DD} = 3V, V_{RT}=2.5V, V_{RB} = 0.5V

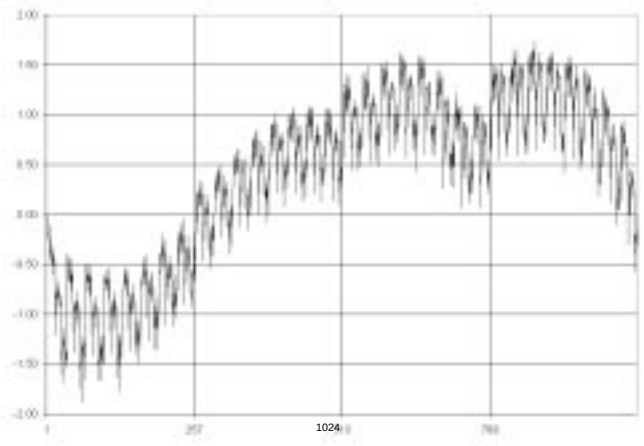
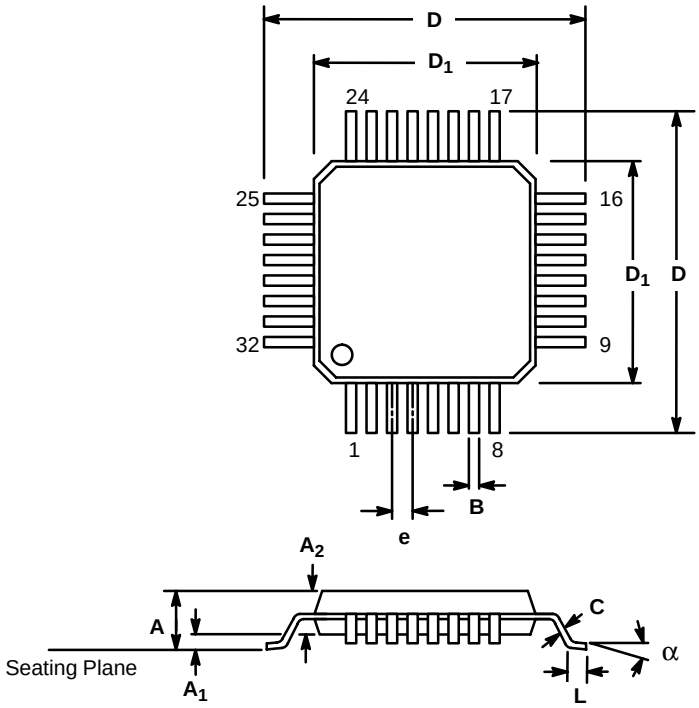


Figure 17. XRD64L14 INL @ 15MSPS, AV_{DD} = 3V, V_{RT}=2.5V, V_{RB} = 0.5V

32 LEAD THIN QUAD FLAT PACK
(7 x 7 x 1.4 mm TQFP)

Rev. 2.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.055	0.063	1.40	1.60
A_1	0.002	0.006	0.05	0.15
A_2	0.053	0.057	1.35	1.45
B	0.012	0.018	0.30	0.45
C	0.004	0.008	0.09	0.20
D	0.346	0.362	8.80	9.20
D_1	0.272	0.280	6.90	7.10
e	0.0315 BSC		0.80 BSC	
L	0.018	0.030	0.45	0.75
α	0°	7°	0°	7°

Note: The control dimension is the millimeter column

Notes

Notes

NOTICE

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