WM8171

3.3V Integrated Signal Processor for Area Array CCDs

Product Preview Rev 1.0 August 1998

DESCRIPTION

The WM8171 is a 10-bit, 21 MSPS data acquisition system which is designed to digitise signals from area array CCDs.

The device contains input blanking, correlated double sampling (CDS), programmable gain amplifier, black level clamp, on-board voltage reference and a 10-bit, 21 MSPS ADC. Two auxiliary 8 bit DACs are provided which may be used for bias voltage control or camera functions such as auto-focus.

The WM8171 is designed to interface to a wide range of area array CCDs and can operate at sample rates up to 21 MSPS by setting the reference bias current via an external resistor connected to the ISET pin.

The user is able to control the device functions and monitor on-chip register settings via the easy-to-use digital management interface.

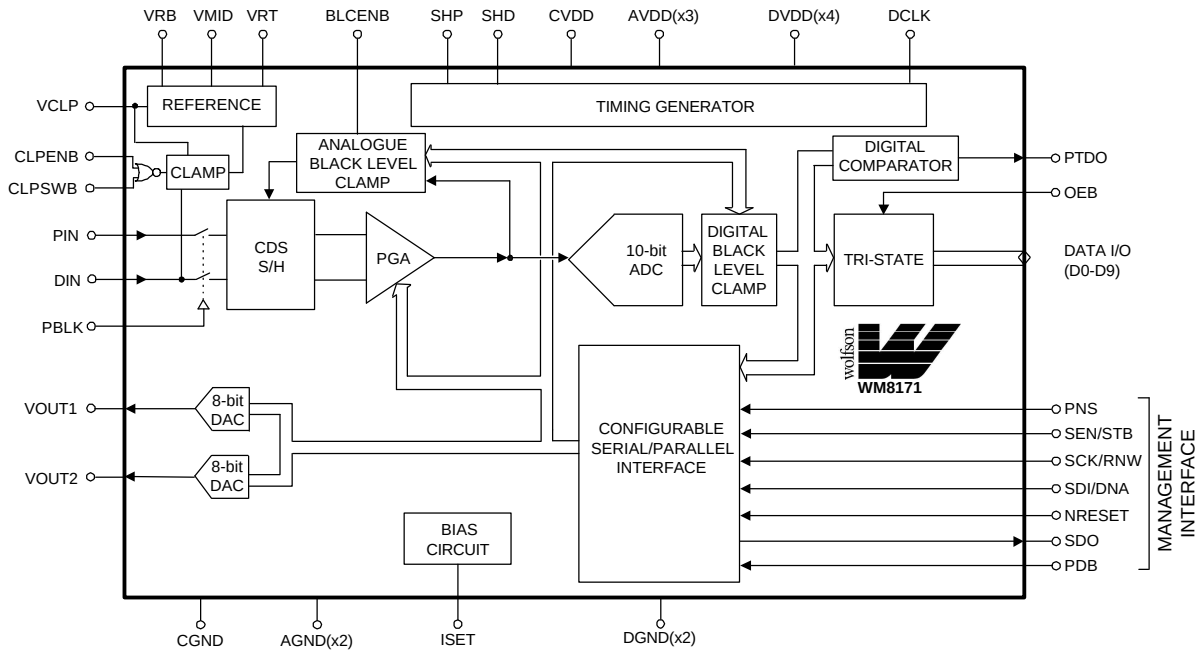
FEATURES

- **Correlated double sampling**
- **Programmable gain amplifier**
- **10-bit, 21 MSPS ADC**
- **Black level clamp**
- **Input blanking**
- **Two auxiliary 8-bit DACs**
- **Power save mode**
- **Serial or parallel control bus**
- **Adjustable sample rate**
- **User selectable sampling on rising or falling edge of clocks**
- **Single 3.3V power supply (3V minimum)**
- **48 pin TQFP package**
- **Power consumption typically 190mW at 12MHz, 270mW at 21MHz**

APPLICATIONS

- **Digital still cameras**
- **PC cameras**
- **Progressive scan CCDs**
- **NTSC, PAL interline CCDs**

BLOCK DIAGRAM



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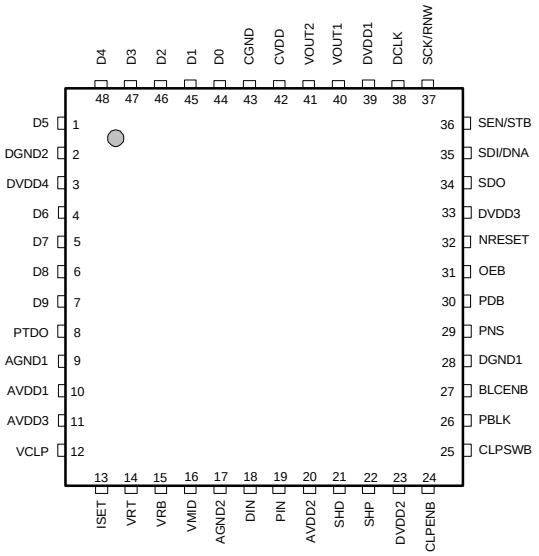
PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMP. RANGE	PACKAGE
XWM8171CFT/V	0 to 70°C	48-PIN TQFP

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

As per JEDEC specifications A112-A and A113-A this product requires specific storage conditions prior to surface mount assembly and as such will be supplied in vacuum sealed moisture barrier bags.

CONDITION	MIN	MAX
Analogue supply voltages (AVDD1 to AVDD3)	AGND -0.3V	AGND +7V
Digital supply voltages (DVDD1 to DVDD4)	DGND -0.3V	DGND +7V
Clock supply voltage, CVDD	CGND -0.3V	CGND +7V
Digital inputs BLCENB, CLPENB, CLPSWB, PBLK, SHD, SHP pins	DGND -0.3V	DVDD2 +0.3V
Digital inputs PDB, NRESET, SCK/RNW, SEN/STB, PNS, SDI/DNA, OEB, DCLK, SDO pins	DGND -0.3V	DVDD3 +0.3V
Digital outputs, D0 to D9, PTDO	DGND -0.3V	DVDD4 +0.3V
Analogue inputs and analogue outputs	AGND -0.3V	AVDD +0.3V
Maximum difference between AGND, DGND and CGND	- 0.1V	+0.1V
Maximum difference between DVDD1, AVDD and CVDD	- 0.1V	+0.1V
Operating temperature range, T_A	0°C	+70°C
Storage temperature	-65°C	+150°C
Lead temperature (soldering, 10 seconds)		+260°C

Note 1: AGND denotes the voltage on any analogue ground pin.
DGND denotes the voltage on any digital ground pin.
CGND denotes the voltage on the clock ground pin.
For this device all GND pins should be star connected as close as possible to the device.

Note 2: AVDD denotes the voltage on any AVDD pin.
For this device all AVDD supplies should be connected together.

RECOMMENDED OPERATING CONDITIONS

SHD/SHP = 21MHz RISET=15kΩ

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply voltage			2.97		3.63	V
Analogue supply current - active	I_{AACT}			68		mA
Digital supply current - active (Note 1)	I_{DACT}			8		mA
Clock supply current - active	I_{CACT}			6		mA
Supply current - standby (Total)	I_{SDBY}	SHD/SHP = 0MHz			10	µA

SHD/SHP = 12MHz RISET=22kΩ

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply voltage			2.97		3.63	V
Analogue supply current - active	I_{AACT}			50		mA
Digital supply current - active (Note 1)	I_{DACT}			4		mA
Clock supply current - active	I_{CACT}			4		mA
Supply current – standby (Total)	I_{SDBY}	SHD/SHP = 0MHz			10	µA

Note 1: Digital supply current - active includes DVDD4 current, which is dependent on the D[9:0] capacitive load.

PIN DESCRIPTION

PIN NO	NAME	TYPE	DESCRIPTION
1	D5	Digital IO	Data output 5/parallel data IO3
2	DGND2	Supply	Digital ground for D0 to D9, PTDO pins
3	DVDD4	Supply	Digital supply for D0 to D9, PTDO pins
4	D6	Digital IO	Data output 6/parallel data IO4
5	D7	Digital IO	Data output 7/parallel data IO5
6	D8	Digital IO	Data output 8/parallel data IO6
7	D9	Digital IO	Data output 9 (MSB)/parallel data IO7
8	PTDO	Digital output	Programmable threshold detect output
9	AGND1	Supply	Analogue ground and device substrate
10	AVDD1	Supply	Analogue supply for ADC
11	AVDD3	Supply	Analogue supply for references, bias voltage
12	VCLP	Analogue output	Reset level clamping voltage output
13	ISET	Analogue output	External resistor for bias current control
14	VRT	Analogue output	Upper ADC reference voltage output
15	VRB	Analogue output	Lower ADC reference voltage output
16	VMID	Analogue output	Midrail reference voltage output
17	AGND2	Supply	Analogue ground and device substrate
18	DIN	Analogue input	Video data input
19	PIN	Analogue input	Video preset input
20	AVDD2	Supply	Analogue supply for S/H, PGA, analogue DC correction loop and auxiliary DACs
21	SHD	Digital input	Sample and Hold data control
22	SHP	Digital input	Sample and Hold preset control
23	DVDD2	Supply	Digital supply BLCENB, CLPENB, CLPSWB, PBLK, SHD, SHP pins
24	CLPENB	Digital input	Reset level clamp enable input, active low
25	CLPSWB	Digital input	Reset level clamp enable switch, active low
26	PBLK	Digital input	Input blocking control, active low
27	BLCENB	Digital input	Black level clamp control, active low
28	DGND1	Supply	Digital ground for DVDD1, DVDD2, DVDD3 supplies
29	PNS	Digital input	Parallel not serial control
30	PDB	Digital input	External power down, active low
31	OEB	Digital input	Output enable bar, active low
32	NRESET	Digital input	Master chip reset, active low
33	DVDD3	Supply	Digital supply for PDB, NRESET, SCK/RNW, SEN/STB, PNS, SDI/DNA, OEB, DCLK, SDO pins
34	SDO	Digital tri-stateable output	Serial data output, tri-stateable
35	SDI/DNA	Digital input	Serial data in/parallel data not address (management interface)
36	SEN/STB	Digital input	Serial enable/parallel strobe (management interface)
37	SCK/RNW	Digital input	Serial clock/parallel read not write (management interface)
38	DCLK	Digital input	Output data retiming clock input
39	DVDD1	Supply	Digital supply for internal logic
40	VOUT1	Analogue output	Auxiliary DAC1 output
41	VOUT2	Analogue output	Auxiliary DAC2 output
42	CVDD	Supply	Positive supply for internal clock generation circuitry
43	CGND	Supply	Ground for internal clock generation circuitry
44	D0	Digital output	Data output 0 (LSB), tri-stateable
45	D1	Digital output	Data output 1, tri-stateable
46	D2	Digital IO	Data output 2/parallel data IO0
47	D3	Digital IO	Data output 3/parallel data IO1
48	D4	Digital IO	Data output 4/parallel data IO2

ELECTRICAL CHARACTERISTICS

Test Characteristics

CVDD = AVDD = DVDD = 3.3V, AGND = DGND = CGND = 0V, RISET=15kΩ, TA = 0°C to +70°C, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Digital Inputs							
High level input voltage	V_{IH}			0.8*DVDD			V
Low level input voltage	V_{IL}					0.2*DVDD	V
High level input current	I_{IH}					1	µA
Low level input current	I_{IL}					1	µA
Input capacitance	C_{IN}				5		pF
Digital Outputs							
High level output voltage	V_{OH}	I_{OH} = 1mA		DVDD-0.75			V
Low level output voltage	V_{OL}	I_{OL} = 1mA				0.75	V
High impedance O/P current	I_{OZ}					1	
Analogue Inputs							
Input common mode range	V_{CMR}			0.3		AVDD-0.3	V
10-bit ADC Performance Including CDS and PGA Functions NO MISSING CODES GUARANTEED							
Resolution				10			Bits
Maximum differential non-linearity	DNL	PGA at minimum gain				+/-1	LSB
Maximum integral non-linearity	INL	PGA at minimum gain			+/-2		LSB
Maximum sampling rate	S_{MAX}			21.5			MSPS
CDS S/H							
Maximum input voltage for full scale ADC output	V_{INMAX}	PGA = 00hex					
		V375	TIMES2				
		0	0		1		V
		0	1		0.5		V
		1	0		1.5		V
		1	1		0.75		V
Minimum input voltage for full scale ADC output	V_{INMIN}	PGA = FFhex					
		V375	TIMES2				
		0	0		40		mV
		0	1		20		mV
		1	0		60		mV
		1	1		30		mV
PGA							
Minimum gain	G_{NTMIN}	TIMES2=0			0		dB
Minimum gain	G_{TMIN}	TIMES2=1			6		dB
Maximum gain	G_{NTMAX}	TIMES2=0			28		dB
Maximum gain	G_{TMAX}	TIMES2=1			34		dB
LSB step size	G_{LSB}				0.11		dB
Resolution				8			Bits
PGA maximum differential non-linearity	P_{DNL}						LSB
PGA maximum integral non-linearity	P_{INL}						LSB

Test Characteristics

CVDD = AVDD = DVDD = 3.3V, AGND = DGND = CGND = 0V, RISET=15kΩ, TA = 0°C to +70°C, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Reset Level Clamp Switch/AC Coupling Resistance							
AC coupling resistance, ON	R_{CON}	ACINP=1			53		kΩ
AC coupling resistance, OFF	R_{COFF}	ACINP=0		2			MΩ
Reset level clamp switch resistance	R_{ON}	ACINP=0, CLPENB=0 CLPSWB=0			150		Ω
Black Level Clamp							
DC offset correction range	V_{BLCR}			80			mV
References							
VMID voltage	VMID				AVDD/2		V
VRT - VRB, Note 1	V_{REFL}	V375=0			0.6		V
VRT - VRB, Note 1	V_{REFH}	V375=1			0.875		V
VCLP voltage referenced to VMID		VCLP[1.0]	V375				
	V_{COOO}	0 0	0		-0.3		V
	V_{CO1O}	0 1	0		0		V
	V_{C1OO}	1 0	0		+0.3		V
	V_{COO1}	0 0	1		-0.437		V
	V_{CO11}	0 1	1		0		V
	V_{C1O1}	1 0	1		+0.437		V
Voltage on ISET pin	V_{ISET}				1.24		V
V_{ISET} temperature coefficient	V_{ITEMP}						mV/°C
Auxiliary DACs							
Resolution				8			Bits
Maximum integral non-linearity	INL					±1	LSB
Maximum differential non-linearity	DNL					±1	LSB
Zero scale error	D_{ZCE}						LSB
Full scale output, TIMES 2	D_{FSO}	AUX1X1, AUX2X1 = 0			AVDD		V
Full scale output, TIMES 1	D_{FSOH}	AUX1X1, AUX2X1 = 1			AVDD/2		V
Output slew rate	D_{SR}						V/µsec
Output settling time	D_{TS}						µsec
Load regulation	D_{LR}						mV/mA

Note 1: ADC input voltage is twice VRT- VRB voltage.

DETAILED TIMING DIAGRAMS

INPUT VIDEO SAMPLING

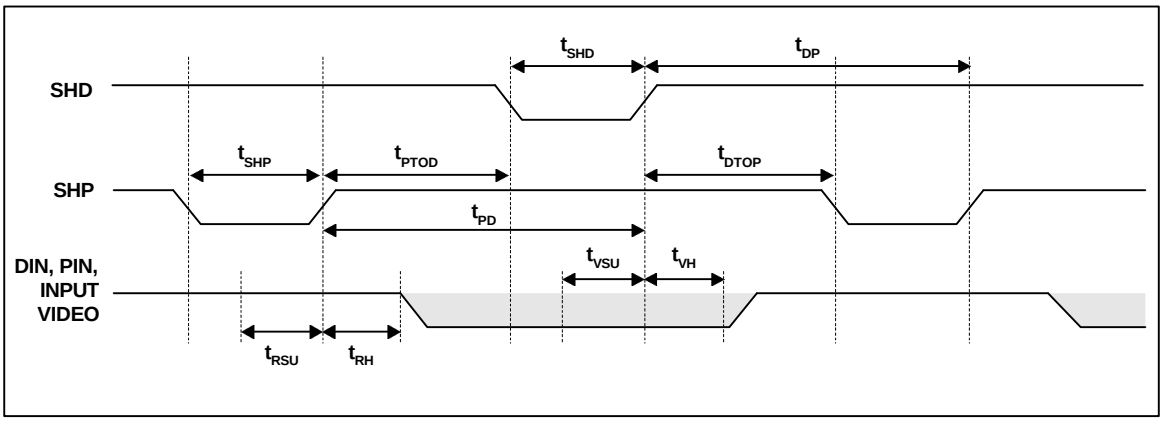


Figure 1 Input Video Sampling Diagram

Test Characteristics

CVDD = AVDD = DVDD = 3.3V, AGND = DGND = CGND = 0V, RISET=15kΩ, TA = 0°C to +70°C, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input video (DIN) set-up time with reference to SHD trailing edge	t_{VSU}		5			ns
Input video (DIN) hold time with reference to SHD trailing edge	t_{VH}		5			ns
Reset video (PIN) set-up time with reference to SHP trailing edge	t_{RSU}		5			ns
Reset video (PIN) hold time with reference to SHP trailing edge	t_{RH}		5			ns
SHD active low time	t_{SHD}		7.5			ns
SHP active low time	t_{SHP}		7.5			ns
SHP high to SHD low time	t_{PTOD}		10			ns
SHD high to SHP low time	t_{DTOP}		10			ns
SHD trailing edge to SHP trailing edge	t_{DP}		21.4			ns
SHP trailing edge to SHD trailing edge	t_{PD}		21.4			ns

OUTPUT DATA

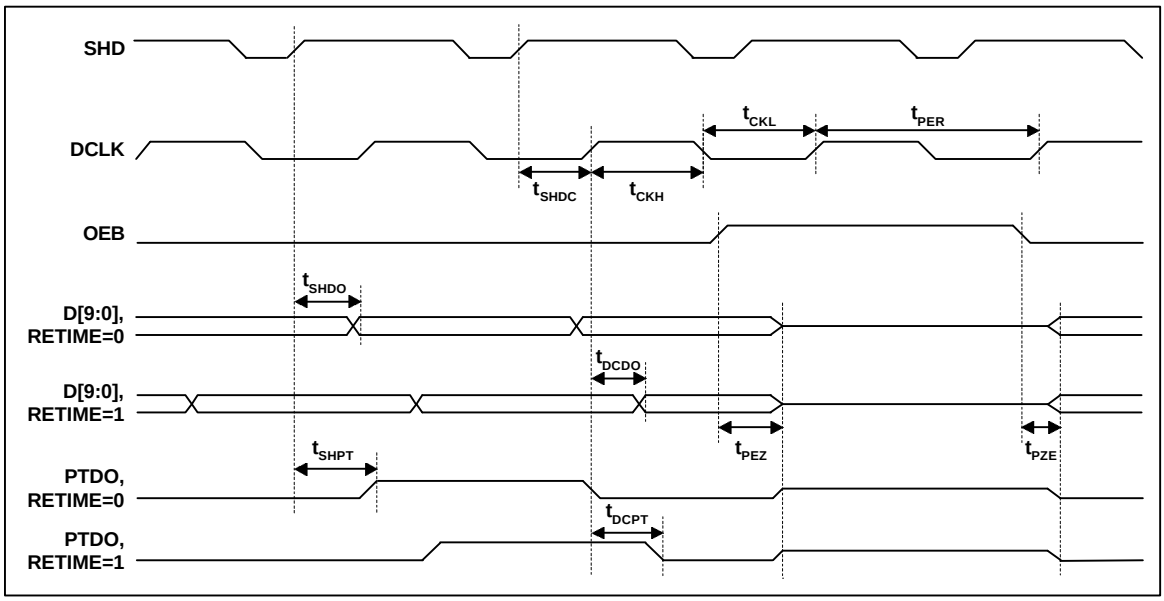


Figure 2 Output Data Timing Diagram

Test Characteristics

CVDD = AVDD = DVDD = 3.3V, AGND = DGND = CGND = 0V, RISET=15kΩ, TA = 0°C to +70°C, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DCLK period	t_{PER}		47.6			ns
DCLK high	t_{CKH}		19			ns
DCLK low	t_{CKL}		19			ns
Output propagation delay, RETIME = 0, SHD trailing edge to D[9:0] out	t_{SHDO}					ns
Output propagation delay, RETIME = 1, DCLK leading edge to D[9:0] out	t_{DCDO}					ns
Trailing edge of SHD to leading edge of DCLK	t_{SHDC}					ns
Output disable time, OEB rising to D[9:0] and PTDO tristate	t_{PEZ}					ns
Output enable time, OEB falling to D[9:0] and PTDO out	t_{PZE}					ns
PTDO propagation delay, RETIME = 0, SHD trailing edge to PTDO out	t_{SHPT}					ns
PTDO propagation delay, RETIME=1, DCLK leading edge to PTDO out	t_{DCPT}					ns

CLAMPING CONTROLS

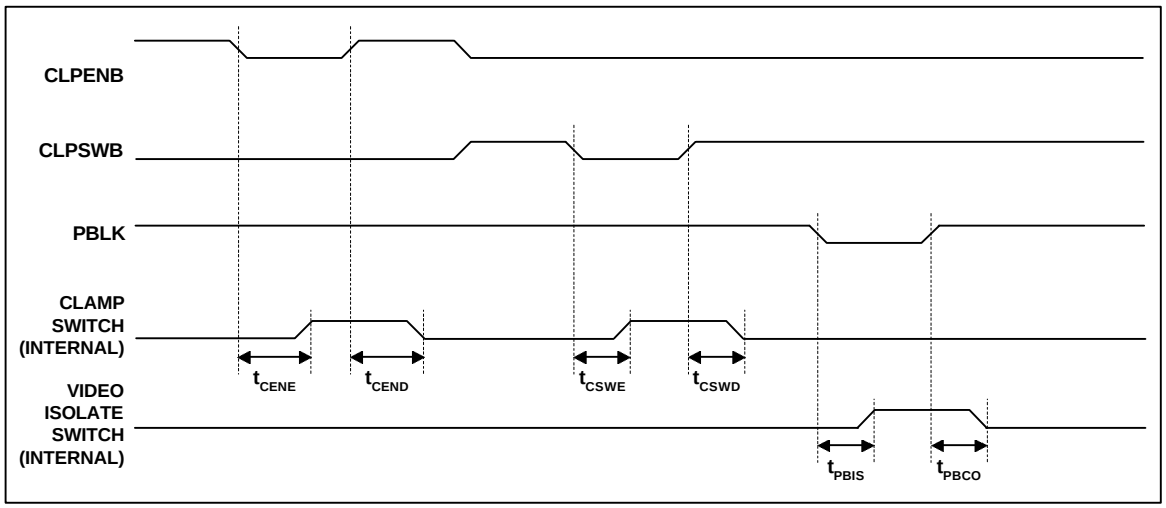


Figure 3 Clamping Controls Timing Diagram

Test Characteristics

CVDD = AVDD = DVDD = 3.3V, AGND = DGND = CGND = 0V, RISET=15kΩ, TA = 0°C to +70°C, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CLPENB enable time	t_{CENE}					ns
CLPENB disable time	t_{CEND}					ns
CLPSWB enable time	t_{CSWE}					ns
CLPSWB disable time	t_{CSWD}					ns
PBLK isolate time	t_{PBIS}					ns
PBLK connect time	t_{PBCO}					ns

BLCENB INPUT

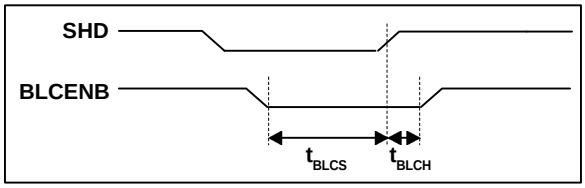


Figure 4 BLCENB Input Timing Diagram

Test Characteristics

CVDD = AVDD = DVDD = 3.3V, AGND = DGND = CGND = 0V, RISET=15kΩ, TA = 0°C to +70°C, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
BLCENB setup time to SHD trailing edge	t_{BLCS}					ns
BLCENB hold time from SHD trailing edge	t_{BLCH}					ns

SERIAL INTERFACE

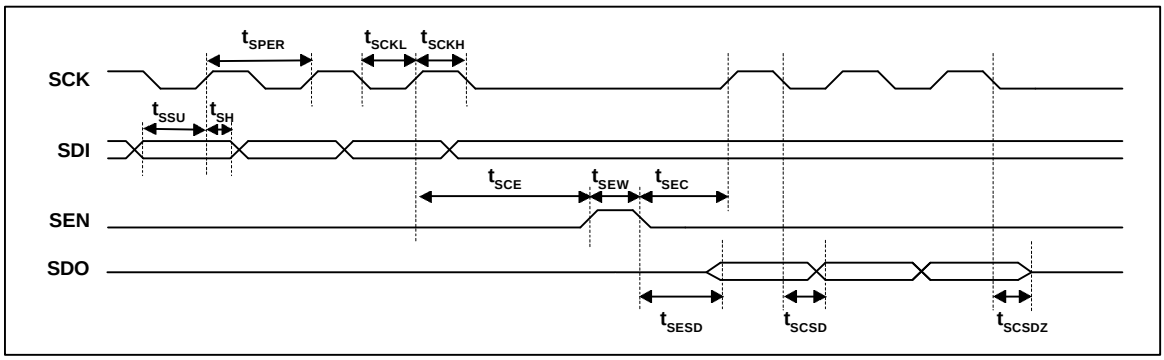


Figure 5 Serial Interface Timing Diagram

Test Characteristics

CVDD = AVDD = DVDD = 3.3V, AGND = DGND = CGND = 0V, RISET=15kΩ, TA = 0°C to +70°C, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SCK period	t_{SPER}		83.3			ns
SCK high	t_{SCKH}		37.5			ns
SCK low	t_{SCKL}		37.5			ns
SDI set up time	t_{SSU}		10			ns
SDI hold time	t_{SH}		10			ns
SCK high to SEN high	t_{SCE}		20			ns
SEN low to SCK high	t_{SEC}		20			ns
SEN pulse width	t_{SEW}		50			ns
SEN low to SDO out	t_{SESD}					ns
SCK low to SDO out	t_{SCSD}					ns
SCK low to SDO high impedance	t_{SCSDZ}					ns

PARALLEL INTERFACE

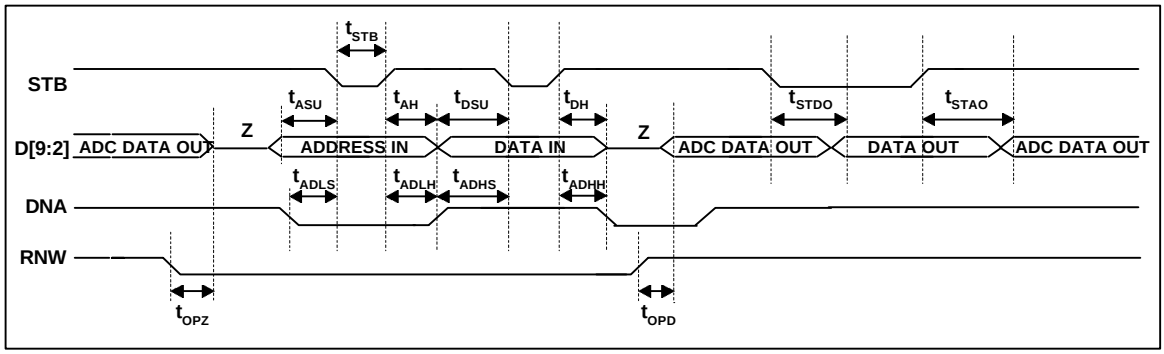


Figure 6 Parallel Interface Timing Diagram

Test Characteristics

CVDD = AVDD = DVDD = 3.3V, AGND = DGND = CGND = 0V, RISET=15kΩ, TA = 0°C to +70°C, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
RNW low to OP[9:2] Tri-state	t_{OPZ}				20	ns
Address setup time to STB low	t_{ASU}		0			ns
DNA low setup time to STB low	t_{ADLS}		10			ns
STB low time	t_{STB}		50			ns
Address hold time from STB high	t_{AH}		10			ns
DNA low hold time from STB high	t_{ADLH}		10			ns
Data setup time to STB low	t_{DSU}		0			ns
DNA high setup time to STB low	t_{ADHS}		10			ns
Data hold time from STB high	t_{DH}		10			ns
DNA high hold time from STB high	t_{ADHH}		10			ns
RNW high to OP[9:2] output	t_{OPD}		0			ns
Data output propagation delay from STB low	t_{STDO}					ns
ADC data out propagation delay from STB high	t_{STAO}					ns

SYSTEM INFORMATION

The WM8171 is a complete signal processing and data acquisition system which is designed to interface directly to the analogue output of area array CCDs. The device digitises the video signals from the CCD for subsequent digital processing of the data. The WM8171 can be used in a wide range of CCD-based video applications such as digital still cameras, as shown in Figure 7.

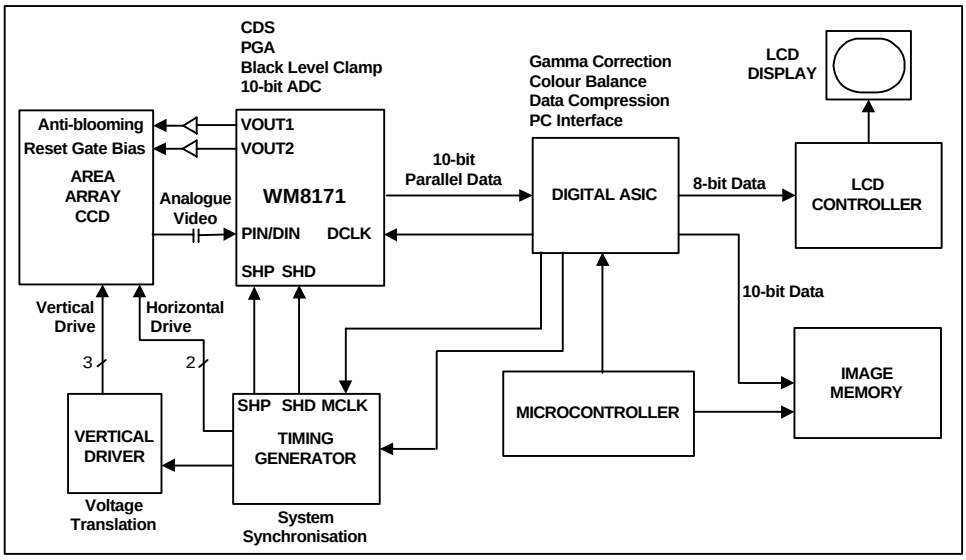


Figure 7 Digital Still Camera System Block Diagram

TYPICAL PERFORMANCE

SHD, SHP = 21MHz, PGA gain = 0dB, VRT-VRB = 875mV, RISET = 15KΩ

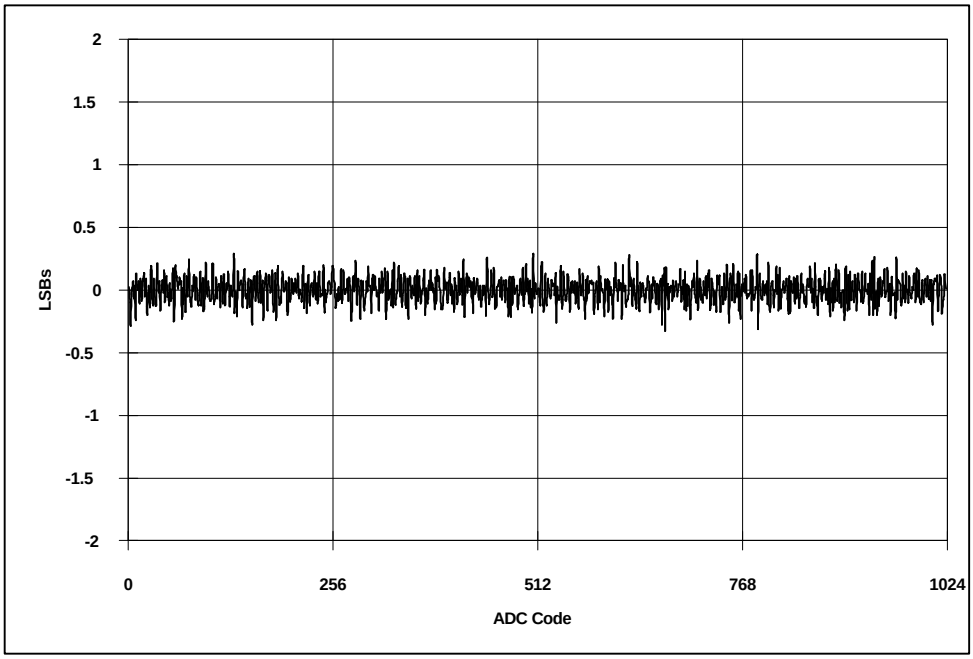


Figure 8 WM8171 10-bit DNL Plot

DEVICE DESCRIPTION

GENERAL OPERATION

The analogue circuitry within the WM8171 consists of a Sample/Hold (S/H) block, a Programmable Gain Amplifier (PGA), a DC Offset Correction loop, and a 10-bit 21MSPS Analogue to Digital Converter (ADC). The Sample/Hold block takes a Correlated Double Sample (CDS) of the incoming video. The CDS video sample is transferred differentially into the PGA block, which is used to gain the signal to the full dynamic range of the ADC. The PGA is controlled digitally via the management interface. The 10-bit pipeline ADC takes the output from the PGA and converts the analogue voltage into a digital representation of the signal.

To correct for DC offsets in the input video, the Sample/Hold block and the PGA, DC offset correction circuitry is provided under the control of an external input. An analogue correction loop using mixed mode circuitry removes the majority of the DC offset by summing the output of a DAC into the main signal path. An up/down counter controlled from the output of a comparator updates the DAC. The comparator checks the output from the PGA against a voltage representing the target black level. As the analogue correction loop does not correct for DC offsets in either the ADC or the comparator in the feedback loop, a further digital offset is automatically calculated within the digital section following the ADC, which forces the digital output to the previously programmed value.

Two auxiliary 8-bit DACs are provided, which can be used within the camera system to control bias voltages to the area CCD, or to provide DC voltages for peripheral camera functions, such as auto-focus control.

To allow the registers within the WM8171 to be programmed a management interface is provided which allows either serial or parallel control. The interface allows the user to both write to, and read from the internal registers, which eases system debug as values previously programmed can be checked.

INPUT SAMPLE AND HOLD, AND VIDEO TIMING

The WM8171 includes a Sample/Hold section at its input, which is used to acquire samples from the analogue output of the area array CCD. The Sample/Hold is configured as shown in Figure 9, and can be operated in a basic Sample and Hold mode or in Correlated Double Sampling (CDS) mode.

In CDS, the input video reset level is sampled under the control of the signal applied to the SHP digital input and the input video signal level is sampled under the control of the signal applied to the SHD digital input.

The Sample/Hold produces a differential voltage output signal, which is passed to the following PGA.

Detailed input timing of the Sample/Hold is shown in Figures 10 and 11. Note that there should be no overlap between the SHP and SHD pulses. Any overlap will cause the WM8171 to operate incorrectly. The WM8171 can be programmed via the management interface to accept SHP and SHD inputs as either both positive, or both negative pulses. Control of this function is via the control bit INVSHX.

INPUT BLANKING

In some cases the output signals from the CCD can be larger than the input stage of WM8171 could normally handle without overload and saturation. To avoid this situation the Sample/Hold stage is preceded by a pair of analogue switches, which can be used to block the analogue input signals at PIN and DIN from passing to the Sample/Hold stage. These switches are turned on or off by placing a high or low level on the PBLK pin respectively.

RESET LEVEL CLAMP OR AC COUPLING

The input video can be interfaced via a capacitor to the WM8171 by two methods. A Reset Level Clamp facility is provided which can be used in both Sample and Hold and in CDS modes of operation. The clamp switch is closed if a low level is applied to both CLPENB and CLPSWB digital inputs. The clamp voltage, VCLP, can be programmed via the management interface to be equal to VRB, VMID, or VRT. A typical use of the Reset Level Clamp facility using CDS is shown in Figure 12.

Alternatively, the CLPENB and CLPSWB digital inputs can be tied high, which will disable the Reset Level Clamp switch, and the control bit ACINP set. This control bit connects an internal AC coupling resistor to the DIN input, which allows the user to simply AC couple the analogue video signal into the WM8171. If CDS is also used, then any drift on the WM8171 side of the coupling capacitor due to input video DC content will be removed.

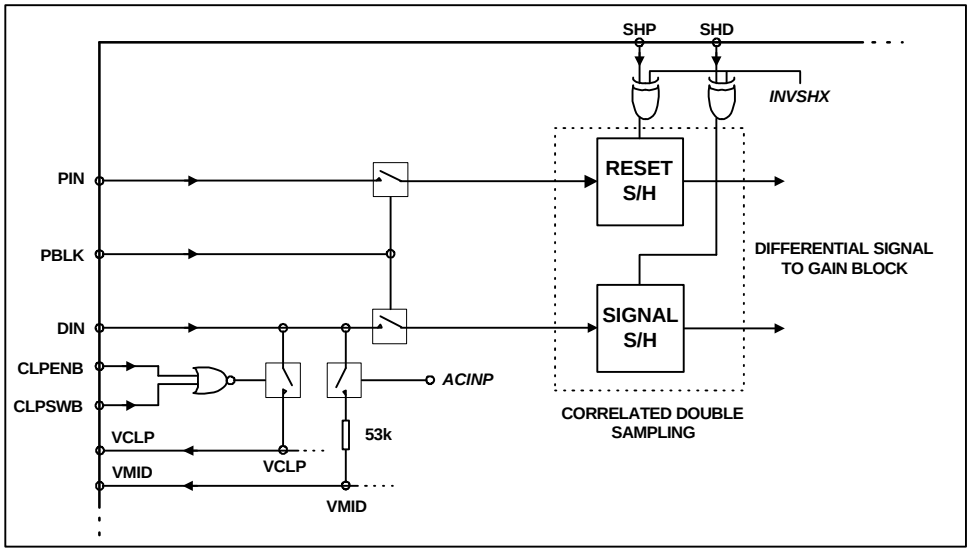


Figure 9 Input Sample/Hold and Reset Level Clamp Block Diagram

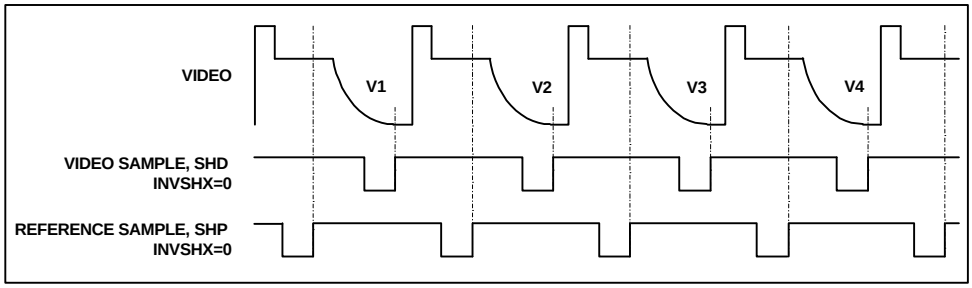


Figure 10 Input Sample/Hold Timing, INVSHX = 0

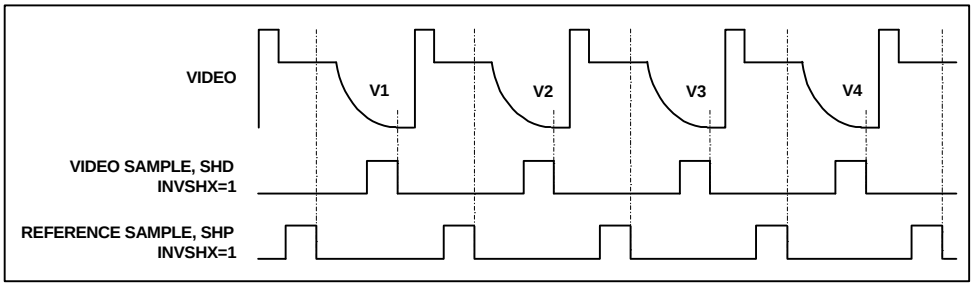


Figure 11 Input Sample/Hold Timing, INVSHX = 1

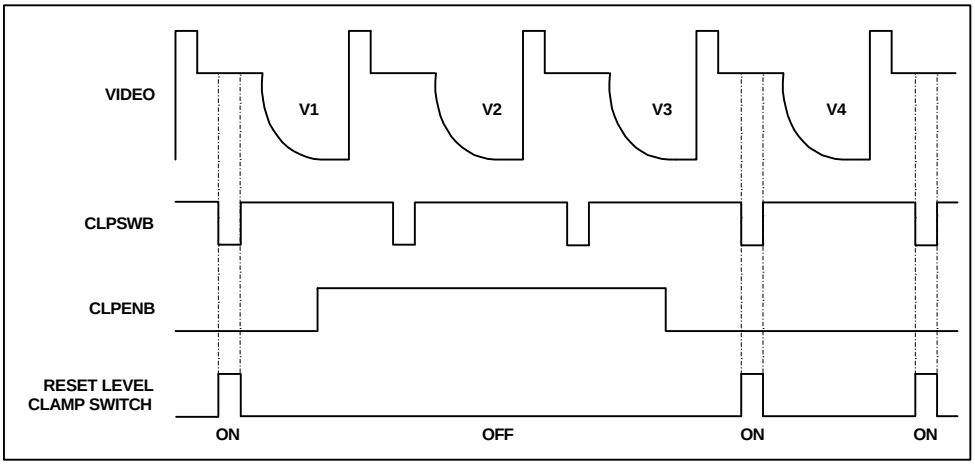


Figure 12 Reset Level Clamp Timing

PROGRAMMABLE GAIN AMPLIFIER

The WM8171 contains a Programmable Gain Amplifier (PGA), which precedes the analogue-to-digital converter (ADC). The gain of the PGA is set digitally via the management interface to a level which delivers the maximum signal to the input of the ADC without it over ranging, and thus obtaining the maximum dynamic range from the ADC.

The gain control on the WM8171 is separated into two sections, a programmable gain section, and a fixed gain section. The programmable gain section is controlled via an 8-bit word written by the management interface, and has a typical range of between 0dB and 28dB. The gain response of the programmable gain section is linear on a logarithmic scale. This means that each LSB increase (or decrease) of digital gain setting represents an equal fraction of a dB (typically 0.11dB) of actual gain increase (or decrease).

There is also a fixed gain section, which is programmable to be either 0dB or 6dB. Setting the TIMES2 control bit via the management interface enables this additional gain.

Figure 13 shows the typical WM8171 gain response with and without the additional 6dB.

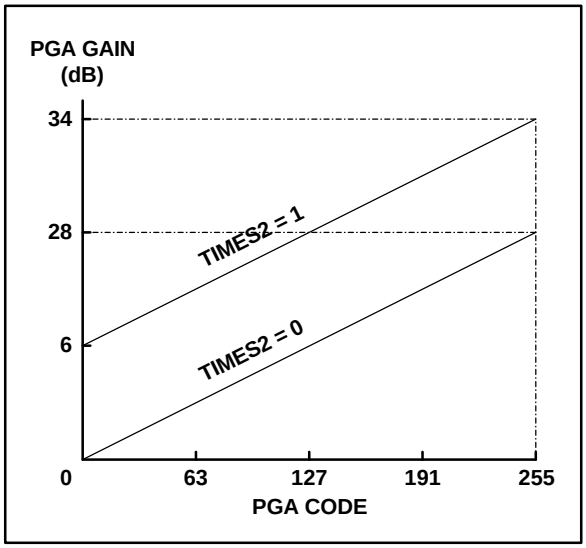


Figure 13 Graph of typical WM8171 Gain Response

REFERENCE VOLTAGES

All references used on the WM8171 are derived from an internal bandgap reference voltage. The ADC uses two reference voltages, VRT and VRB. The Sample/Hold and PGA use a midrail voltage reference, VMID. The voltage for Reset Level Clamp, VCLP, can be selected to be equal to VRT, VRB or VMID. These four voltages are buffered on-chip and are each available at output pins. Each of these pins should be carefully decoupled with capacitors of the type and size detailed in the Recommended External Components section.

The voltage difference between VRT and VRB can be programmed, in order to accommodate different input signal ranges, to two values via the management interface. The WM8171 default condition is VRT-VRB typically 0.6V but can be increased to 0.875V by setting the V375 control bit. Due to the nature of the ADC design, the difference between VRT and VRB is typically half the maximum input signal which the ADC can convert successfully, i.e. if VRT-VRB is 0.875V, then the ADC can accommodate an input signal after the PGA of greater than 1.5V.

INPUT SIGNAL AMPLITUDE

The PGA gain setting allows the WM8171 to amplify the input video signal to be equal to the full-scale input of the ADC. The minimum input video signal that can be scaled to the full-scale input of the ADC is defined when the PGA is at the maximum gain. The maximum input video signal that can be scaled to the full-scale input of the ADC is defined when the PGA is at minimum gain.

The minimum and maximum video input signal, which the WM8171 can accommodate, is set by a combination of the TIMES2 and the V375 control bits. The input video conditions are summarized in Table 1

TIMES2	V375	MAXIMUM VIN FOR FULL SCALE ADC INPUT PGA GAIN = 00(HEX)	MINIMUM VIN FOR FULL SCALE ADC INPUT PGA GAIN = FF(HEX)
0	0	1.0V	40mV
0	1	1.5V	60mV
1	0	0.5V	20mV
1	1	0.75V	30mV

Table 1 Input Signal Amplitude Conditions

ANALOGUE TO DIGITAL CONVERTER, DEVICE LATENCY AND OUTPUT TIMING

The 10-bit resolution ADC uses a pipelined architecture. The latency is the time delay between the video sample (SHD) occurring and the corresponding valid output data being available. There are two possible inputs that control the detailed timing of data output from the WM8171. These are SHD and DCLK. The selection between SHD and DCLK is dependant on the control bit RETIME. If RETIME is set low, then the output data on the D[9:0] pins is referenced to the rising edge of the SHD control input. If RETIME is set high, the output data on the D[9:0] pins is reference to the rising edge of the DCLK clock input. The use of RETIME allows the user to accurately control the output data timing, which can ease the design of the interface between the WM8171 and following digital ASIC, especially for high pixel rate systems.

With RETIME set low, the WM8171 latency is equal to eight pixel periods. With RETIME set high, the WM8171 latency is equal to eight pixel periods plus the difference in timing between SHD and DCLK. These two conditions are shown in Figure 14.

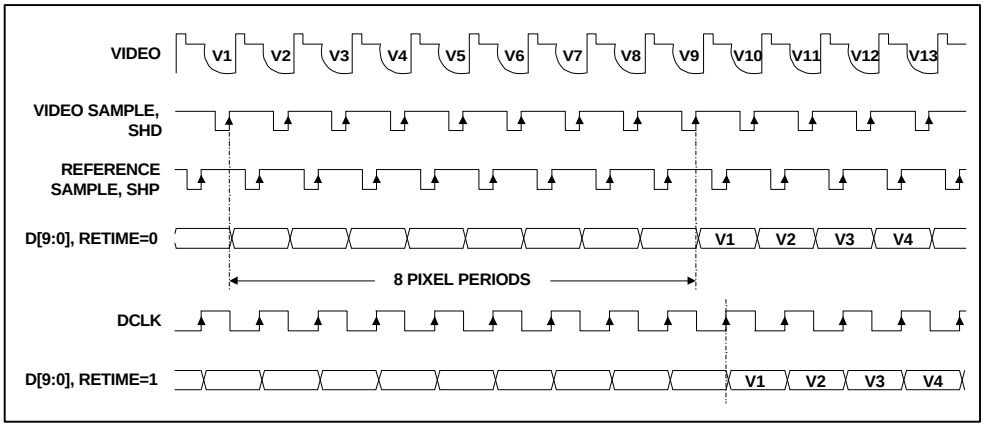


Figure 14 WM8171 Latency

SETTING THE MAXIMUM CONVERSION RATE

The maximum conversion rate of the ADC, S/H and PGA stages within the WM8171 are directly related to the value of bias current at which the signal path operates. Within limits an increase in bias current allows an increase in maximum conversion rate to be achieved. Inserting a resistor between the ISET pin and AGND sets the value of bias current.

The value should be set to that recommended in Table 2 corresponding to the maximum conversion rate at which the device is required to operate.

Note that the higher the value of RISET the lower the power consumption of the device will be.

RISET	MAX. CONVERSION RATE (MSPS)
22kΩ	12
20kΩ	15
17kΩ	18
15kΩ	21

Table 2 RISET vs Maximum Conversion Rate

BLACK LEVEL OFFSET CORRECTION CIRCUITRY

Unless compensated for, the analogue signal applied to the input of the ADC would contain unacceptably high and variable DC offsets. The offsets consist of the sum of two principal components. These are black level offsets in the output video from the CCD, which can be monitored during optically black pixel phases, and offsets from the amplifiers in the analogue signal path of the WM8171. These offsets would reduce the maximum dynamic range that the ADC can achieve and can vary significantly with time and temperature. Additionally, any DC offsets in the signal path are multiplied by the PGA gain, which can cause the internal amplifiers to limit, particularly if the gain is at a high setting.

The DC offset correction is performed in two stages. There is an analogue DC correction loop that removes the majority of the offset, and a digital clamp that removes the rest. Applying a falling edge to the BLCENB digital input pin enables firstly the analogue correction loop and then the digital correction circuitry. This correction circuitry is to be used during periods when optically black pixels are being output from the CCD. The block diagram of the offset correction circuitry is shown in Figure 15.

ANALOGUE CORRECTION LOOP

The Analogue Correction Loop functions by comparing the output from the PGA during the optically black video period with a DAC output voltage, derived from the ADC reference voltages, which corresponds to a 10-bit code which is programmable between 0 and 255 (dec). This code is the required TARGET for the WM8171 to output for optically black pixels. The output of the comparator, sampled ANDUR times per analogue enable, controls an up/down counter, the contents of which provide the input data to an 8-bit bipolar DAC. The output of this DAC is subtracted from the input of the PGA such that the PGA output becomes closer to the TARGET value programmed. Using this method the majority of any DC offset from either the input video signal, or the signal chain amplifiers is removed.

The Analogue Correction Loop does not correct for DC offsets in the ADC or the comparator in the feedback path, and is quantised, in terms of ADC codes, to the resolution of the 8-bit DAC, which changes depending on the actual PGA gain set. Therefore the resulting output code from the ADC during these optically black pixels will not be exactly equal to the TARGET value. The residual error in the black level is corrected in the digital correction circuitry.

DIGITAL CORRECTION CIRCUITRY

The Digital Correction Circuitry that follows the ADC corrects for any difference between the actual ADC output code and the programmed TARGET value.

During the period when the Digital Correction Circuitry is enabled, the circuit calculates the average digital error between the programmed TARGET value and the ADC output code, over a certain number of ADC conversions. This average digital error is subsequently subtracted from all ADC conversions until the Digital Correction Circuitry is enabled again.

The number of ADC conversions that the Digital Correction Circuitry calculates the average over is programmable via the management interface. This number is set in the DIGDUR register, and is equal to $2^{[DIGDUR]}$ pixel periods.

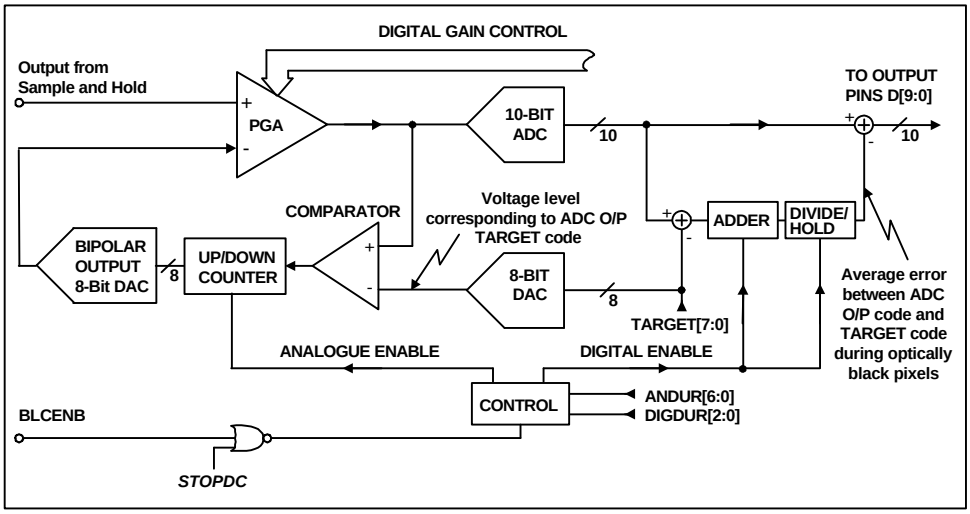


Figure 15 DC Offset - Analogue Correction Block Diagram

DC OFFSET CORRECTION INITIATION AND TIMING

The overall timing of the DC correction algorithm is shown in Figure 16. The duration of the analogue and digital correction loops are independent. The user must ensure that the overall correction period, which is equal to the analogue loop enable time plus the Digital Correction Circuitry enable time, is no longer than the duration of the optically black pixels output from the CCD. This will prevent the potential error of active video being included in the digital average calculated within the WM8171, which would cause an incorrect error value to be stored.

Applying a falling edge to the BLCENB digital input pin enables the Analogue loop and the Digital Correction Circuitry. Once the correction has been initiated, the internal WM8171 control circuitry runs until both the analogue and digital correction enables are complete. All issues associated with latency through the WM8171 have been considered in the internal controller design.

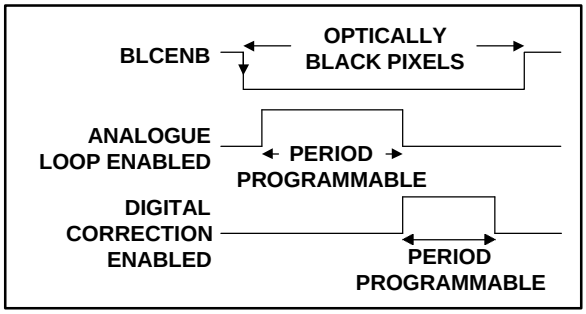


Figure 16 DC Correction Algorithm Timing

The total period (P) of the combined Analogue Correction Loop and Digital Correction Circuitry, measured in Pixel Periods, is given by the following formula:

$P = ([ANDUR] \times 4 + 2^{[DIGDUR]})$ Pixel Periods

Where:

[ANDUR] is the contents of the Analogue Duration register ANDUR[6:0].

[DIGDUR] is the contents of the Digital Duration register DIGDUR[2:0].

The selection of ANDUR and DIGDUR values is at the discretion of the user, but the following considerations should be made. The internal up/down counter is 8-bit, which covers 256 steps. The counter is incremented/decremented ANDUR times per BLCENB falling edge, which implies that the minimum number of falling edges on BLCENB to guarantee that the analogue loop has reached its final value is 256/ANDUR. In actual use however, the change in DC conditions through the WM8171 will be relatively small, which will mean that the analogue loop will settle to the new value quicker. The value chosen for DIGDUR depends on the number of black pixels available, but a larger value means that any

black pixel noise is averaged over a greater number, which will result in a more accurate error value being stored.

The analogue DC correction loop error voltage within the WM8171 is not subject to drift because it is derived from a digitally controlled DAC, which implies that once the DC correction circuitry has settled, the correction circuitry can be turned off. This can be achieved by setting the control bit STOPDC via the Management Interface. The correction circuitry should be re-enabled after any write to the PGA register so that DC change due to the different gain is accommodated for.

There are two main ways that the DC correction circuitry can be used. The BLCENB can be activated either during the optically black lines at the beginning or end of the CCD output field, or during the optically black pixels at the beginning or end of each video line. Using the first option results in the DC conditions being established before any active video is present, and since completely optically black lines are present large values can be programmed to ANDUR and DIGDUR respectfully. With the second option, smaller values for ANDUR and DIGDUR would have to be used, as the number of black pixels in each line is limited. With both options, it is recommended that the correction circuitry be enabled for one frame of video, and then turned off again.

Although the WM8171 only requires a falling edge on BLCENB to initiate the correction circuitry users may input BLCENB signals which are low for the complete duration of the optically black pixels if preferred (this signal format is generally available from CCD timing generator devices). In this case the WM8171 can be programmed to output an error flag on the PTDO pin if the BLCENB input returns to a high state before both the Analogue and Digital Enables are complete. This allows checking that the ANDUR and DIGDUR values programmed to the device will not cause a potential error in the correction circuitry because active video has been included in the internal calculations. See the Programmable Threshold Detect Output section for details of all error flags available.

PROGRAMMABLE THRESHOLD DETECT OUTPUT

The Programmable Threshold Detect Output, (PTDO), primary function is to indicate to the user when the ADC output has exceeded a value programmed into the THRES[9:0] registers via the Management Interface. The PTDO output will output a high state, which is aligned to the output data, if the ADC output exceeds the programmed value. Typically this pin would be used in conjunction with external gain calibration algorithms to set the PGA gain.

The PTDO output can also be used to indicate a number of system error flags which are available to the user. These flags are multiplexed onto the PTDO pin under control of the Management Interface.

An error can be flagged if the pixel data during the black pixels is outside the correction range of the logic within the WM8171, or if the BLCENB pin has returned high before both the analogue and digital DC correction circuitry has completed their tasks. An error can also be flagged if the output from the ADC is out of range, i.e. the ADC output code is trying to exceed 3FF(hex), or be less than 0(hex).

The error flag can be programmed to be output on the PTDO pin under control of the register bits PTDO[1:0].

AUXILIARY DIGITAL TO ANALOGUE CONVERTERS

The WM8171 includes two independent 8-Bit Digital to Analogue Converters. Their analogue outputs are available at pins VOUT1 and VOUT2 respectively. Their output voltages are controlled in two ways. The maximum output voltage from the DACs can be independently set to be either AVDD or AVDD/2 under control of the AUX1X1 and AUX2X1 control bits. Each DAC can then be programmed to one of 256 codes by the 8-bit contents of the Auxiliary DAC registers defined in the register map shown in Table 6.

These DACs can be used to trim CCD control voltages such as the anti-blooming or reset gate bias voltages, or used within the camera system for features such as auto-focus.

MANAGEMENT INTERFACE

The WM8171 includes an easy-to-use and comprehensive Management Interface that allows the user to write to and read from on-board registers and thus control all the digitally programmable features of the device. The Management Interface can be configured to operate in either Parallel or Serial Mode by setting the Parallel Not Serial (PNS) pin high or low respectively. Serial Mode is recommended for real time video applications because writing and reading from the device can be carried out at any time. If Parallel Mode is used, writing and reading must be performed within areas of inactive video to prevent valid ADC output data from being replaced with the Management Interface data.

MANAGEMENT INTERFACE CONFIGURATION

The pins used to control the Management Interface are described in Table 3.

The timing for writing in Serial and Parallel Mode is shown in Figures 17 and 19 respectively.

Selected registers can also be read via the interface thus allowing stored values to be checked by the user. The timing for reading in Serial and Parallel Mode is shown in Figures 18 and 20 respectively.

PIN NAME	SERIAL MODE FUNCTION	PARALLEL MODE FUNCTION
PNS	Set Low to indicate Serial Mode	Set High to indicate Parallel Mode
SEN/STB	Serial interface ENable, active High	Parallel interface STrobe, active Low
SDI/DNA	Serial Data Interface	Data Not Address input
SCK/RNW	Serial interface Clock	Read Not Write input
SDO	Serial Data Out	Not Used
D2-D9	Not Used	Parallel data I/O pins

Table 3 Management Interface Pins and Functions

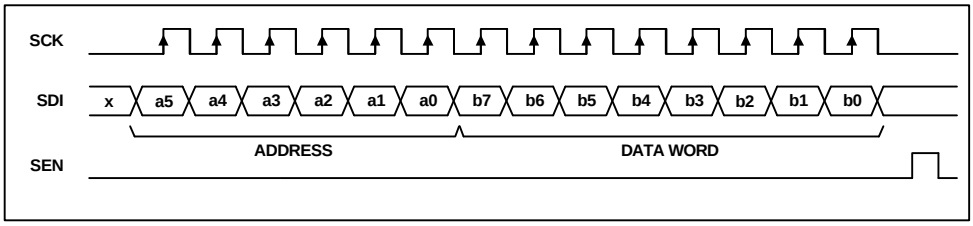


Figure 17 Writing in Serial Mode

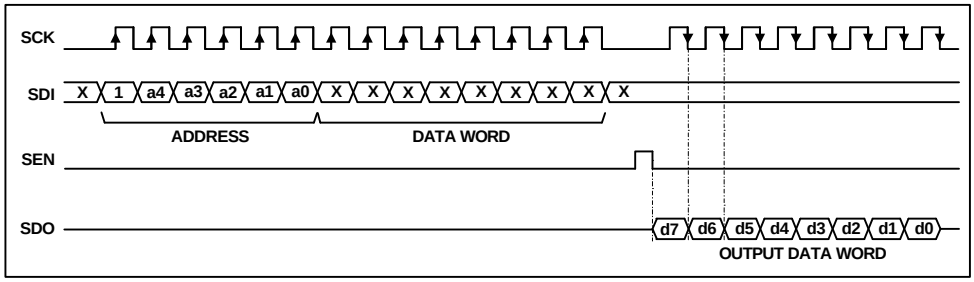


Figure 18 Reading in Serial Mode

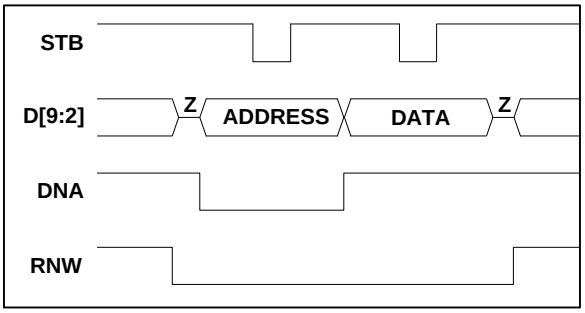


Figure19 Writing in Parallel Mode

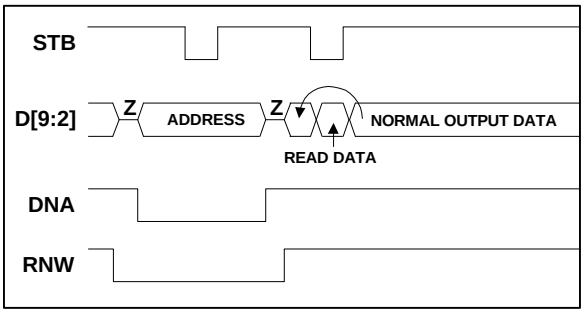


Figure 20 Reading in Parallel Mode

POWER DOWN CONTROL

The WM8171 includes a separate power down pin, PDB. When this pin is taken low the whole device is powered down and all internal registers maintain their currently programmed value. Setting the PD0 bit in the Power Down 1 register can perform a similar power down operation. These two global power downs are logically OR'd.

In addition to the above power down facilities the WM8171 contains seven other selective power downs of individual sections of the device. Setting the appropriate bit in the Power Down 2 register, as described in the Device Configuration section of this data sheet, will power down the particular part of the circuit. These bits are logically ANDed so that any combination of the available device sections can be powered down simultaneously

POWER SUPPLIES

This datasheet describes the WM8171 for use in a complete 3.3V system. The performance and characteristics will differ for the WM8171 if a 5V supply is required. If 5V supplies are required, contact Wolfson Microelectronics Ltd. for further detailed parametric information.

The WM8171 includes several power supply pins, each of which routes power to particular parts of the device circuitry. It is important to note the circuit sections of the device, which are connected to the various supply pins. This is summarized in Table 4.

The WM8171 can operate with all supply pins connected to 5V or with all supply pins connected to 3.3V. It can also operate with all analogue supply pins at 5V and the individual digital supply pins connected to a combination of 5V and 3.3V.

The set of allowable combinations of supply pin connections is shown in Table 5. All AVDD, CVDD and DVDD1 pins should be maintained at the same supply voltage. The other supplies can be at any combination of either 5V or 3.3V.

SUPPLY NAME	CIRCUIT SECTIONS CONNECTED TO
AVDD1	ADC
AVDD2	Main analogue signal path
AVDD3	Reference and bias generator
CVDD	Clock generator circuitry
DVDD1	Internal logic and level shifters
DVDD2	BLCENB, CLPENB, CLPSWB, PBLK, SHD, SHP
DVDD3	PDB, NRESET, SCK/RNW, SEN/STB, PNS, SDI/DNA, OEB, DCLK, SDO
DVDD4	D0-D9, PTDO

Table 4 Supply Pins Vs Device Circuit Sections Connected

NO.	AVDD1, AVDD2, AVDD3, CVDD, DVDD1	DVDD2	DVDD3	DVDD4
1	3.3V	3.3V	3.3V	3.3V
2	3.3V	3.3V	3.3V	5V
3	3.3V	3.3V	5V	3.3V
4	3.3V	3.3V	5V	5V
5	3.3V	5V	3.3V	3.3V
6	3.3V	5V	3.3V	5V
7	3.3V	5V	5V	3.3V
8	3.3V	5V	5V	5V
9	5V	3.3V	3.3V	3.3V
10	5V	3.3V	3.3V	5V
11	5V	3.3V	5V	3.3V
12	5V	3.3V	5V	5V
13	5V	5V	3.3V	3.3V
14	5V	5V	3.3V	5V
15	5V	5V	5V	3.3V
16	5V	5V	5V	5V

Table 5 Supply Pins vs Supply Voltages – Allowable Combinations

GROUND AND POWER SUPPLY PIN CONNECTIONS

As detailed above, each of the power supply and ground pins of the WM8171 is allocated to a particular section of the overall device circuitry. It is important that the use of ground and power planes on any printed circuit board layout should take account of this fact. See Figure 20 for Recommended Device Decoupling.

DEVICE CONFIGURATION

REGISTER MAP

The register map is shown in Table 6. In Serial Mode the contents of address location <a5> determines whether the address location defined by <a[4:0]> is to be read from or written to. For a read operation <a5> is set to 1. To write to a register <a5> should be cleared to 0.

In Parallel Mode a 0 in <a5> forces a write operation. A high level on RNW, irrespective of the contents of <a5>, however, determines a parallel read operation.

Address <a5:a0>	Description	Def'lt (Hex)	RW	BIT							
				b7	b6	b5	b4	b3	b2	b1	b0
000000	Not Used										
000001	Software Reset		W	0	0	0	0	0	0	0	0
000010	Set Up Register 1	02	RW	STOPDC	0	POSVID	TIMES2	INVSHX	ACINP	VCLP1	VCLP0
000011	Set Up Register 2	00	RW	0	PTDO1	PTDO0	INVDIG	RETIME	0	0	0
000100	Black Level Target	40	RW	TARGET7	TARGET6	TARGET5	TARGET4	TARGET3	TARGET2	TARGET1	TARGET0
000101	PGA Gain	00	RW	GAIN7	GAIN6	GAIN5	GAIN4	GAIN3	GAIN2	GAIN1	GAIN0
000110	Digital Duration	02	RW	0	0	0	0	0	DIGDUR2	DIGDUR1	DIGDUR0
000111	Analogue Duration	05	RW	0	ANDUR6	ANDUR5	ANDUR4	ANDUR3	ANDUR2	ANDUR1	ANDUR0
001000	Reserved										
001001	Threshold Detect LSB	00	RW	THRES7	THRES6	THRES5	THRES4	THRES3	THRES2	THRES1	THRES0
001010	Threshold Detect MSB	00	RW	0	0	0	0	0	0	THRES9	THRES8
001011	Power Down 1	00	RW	0	0	0	0	0	0	0	PD0
001100	Power Down 2	00	RW	0	PD7	PD6	PD5	PD4	PD3	PD2	PD1
001101	Auxiliary DAC1	00	RW	AUX1 DAC7	AUX1 DAC6	AUX1 DAC5	AUX1 DAC4	AUX1 DAC3	AUX1 DAC2	AUX1 DAC1	AUX1 DAC0
001110	Auxiliary DAC2	00	RW	AUX2 DAC7	AUX2 DAC6	AUX2 DAC4	AUX2 DAC4	AUX2 DAC3	AUX2 DAC2	AUX2 DAC1	AUX2 DAC0
001111	Reserved										
010000	AUX DAC Control	00	RW	0	0	0	0	0	0	AUX2X1	AUX1X1
010001	Reserved										
010010	Reserved										
010011	Reserved										
010100	Reserved										
010101	Reserved										
010110	Reserved										
010111	Reference Select	00	RW	0	0	0	0	0	0	0	V375
011000	Reserved										
011001	Reserved										
011010	Reserved										
011011	Reserved										
011100	Reserved										
011101	Reserved										
011110	Reserved										
011111	Revision Number		R	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0

Table 6 Register Table

CONTROL BIT TABLE

CONTROL BITS	DESCRIPTION
SOFTWARE RESET (000001)	
	A write to this register will force all registers to return to their default state.
SET UP REGISTER 1 (000010)	
VCLP[1:0]	Controls the VCLP voltage output. VCLP1 / VCLP0 / VCLP PIN 0 / 0 / VRB 0 / 1 / VMID 1 / 0 / VRT 1 / 1 / Reserved
ACINP	Enables the AC coupling resistor between **DIN** and **VMID**. ACINP 0 No AC coupling resistor 1 AC coupling resistor
INVSHX	Enables the invert on **SHD**/**SHP**. INVSHX 0 No invert, SHD / SHP active low 1 Invert, SHD / SHP active high
TIMES2	Enables additional 6dB gain in PGA. TIMES2 0 No additional 6dB gain 1 Additional 6dB gain
POSVID	Allows the WM8171 to accept positive going video. Default input video is negative. POSVID 0 Input video negative going (Default) 1 Input video positive going
STOPDC	Enables or disables both the analogue and digital DC correction circuitry. STOPDC 0 DC offset correction circuitry enabled 1 DC offset correction circuitry disabled
SET UP REGISTER 2 (000011)	
RETIME	Enables the retiming of the digital outputs with DCLK. RETIME 0 No retiming 1 Output data retimed
INVDIG	Digitally inverts the D[9:0] outputs. INVDIG 0 No invert 1 Outputs inverted
PTDO[2:0]	Selects the signal output onto the PTDO Pin. PTDO1 / PTDO0 / PTDO PIN 0 / 0 / Threshold detect output 0 / 1 / Out of range signal 1 / 0 / Clip1 error - digital correction error (ADC output is outside the digital correction range). 1 / 1 / BLCENB error - caused by BLCENB going high before the internal DC offset correction circuitry has finished.
BLACK LEVEL TARGET (000100)	
TARGET[7:0]	Target value for the black level.

CONTROL BITS	DESCRIPTION
PGA GAIN (000101)	
GAIN[7:0]	Controls the PGA gain. 00hex is minimum gain FFhex is maximum gain
DIGITAL DURATION (000110)	
DIGDUR[2:0]	Digital correction duration: number of ADC conversion which are used to calculate the average. DIGDUR2 DIGDUR1 DIGDUR0 Durations 0 0 0 1 ADC conversion 0 0 1 2 ADC conversions 0 1 0 4 ADC conversions 0 1 1 8 ADC conversions 1 0 0 16 ADC conversions 1 0 1 32 ADC conversions 1 1 0 64 ADC conversions 1 1 1 128 ADC conversions
ANALOGUE DURATION (000111)	
ANDUR[6:0]	Controls the duration of the analogue loop enable - i.e. it represents the number of times that the up-down counter will be clocked per falling edge of the BLCENB input.
THRESHOLD DETECT LSB / MSB (001001/10)	
THRES[9:0]	Threshold detect value. If the corrected ADC output data is greater than the THRES[9:0] then PTDO will be high. (Note PTDO[1:0] must be 00bin). Note THRES[9:0] is split into two registers, THRES[9:8] and THRES[7:0].
POWER DOWN 1 & 2 (001011/1100)	
PD[7:0]	Controls the analogue power downs. Note this is split over 2 registers (0 - block enabled, 1 - block powered down). PD0 Global power down, OR'd with PDB pin PD1 S/H, PGA and the analogue correction loop power down PD2 VMID and VCLP power down. PD3 VRT and VRB power down. PD4 ADC only power down. PD5 AUX2DAC power down PD6 AUX1DAC power down
AUXILIARY DAC 1 (001101)	
AUX1DAC[7:0]	Auxiliary 1 DAC value
AUXILIARY DAC 2 (001110)	
AUX2DAC[7:0]	Auxiliary 2 DAC value.
AUX DAC CONTROL (010000)	
AUX1X1	Auxiliary DAC1 scaling factor. AUX1X1 0 TIMES2 1 TIMES1
AUX2X1	Auxiliary DAC2 scaling factor. AUX2X1 0 TIMES2 1 TIMES1
REFERENCE SELECT (010111)	
V375	Selects ADC reference voltage V375 VRT-VRB 0 0.6V 1 0.875V
REVISION NUMBER (011111)	
REV[7:0]	The device revision number. This is ASCII representation of the device revision number i.e. 'A, B, C etc', as a seven bit number, e.g.: ' 41' = A, '42' = B, etc.

RECOMMENDED EXTERNAL COMPONENTS

DEVICE DECOUPLING

The WM8171 contains a high speed 10-bit ADC and wide bandwidth signal amplifiers that are sensitive to noise on supply pins, reference pins and elsewhere. Therefore particular attention should be paid to the decoupling of the WM8171 to prevent unwanted noise from entering the signal path.

Figure 20 and Table 7 show the recommended decoupling capacitors and ground connections. Note that the analogue and digital ground pins are each connected to their respective separate analogue and digital ground return paths. Each analogue supply pin is decoupled to the analogue ground with a parallel combination of tantalum and ceramic capacitors. Each digital supply pin is decoupled to the digital ground with the same parallel capacitor combination.

For optimum performance each parallel capacitor combination should be connected as close to the particular supply pin as is physically possible.

The careful use of separate analogue and digital ground planes can help to prevent coupling of digital noise into the sensitive analogue sections of the internal device circuitry. The AGND and DGND connections should be star-pointed as close to the WM8171 as possible.

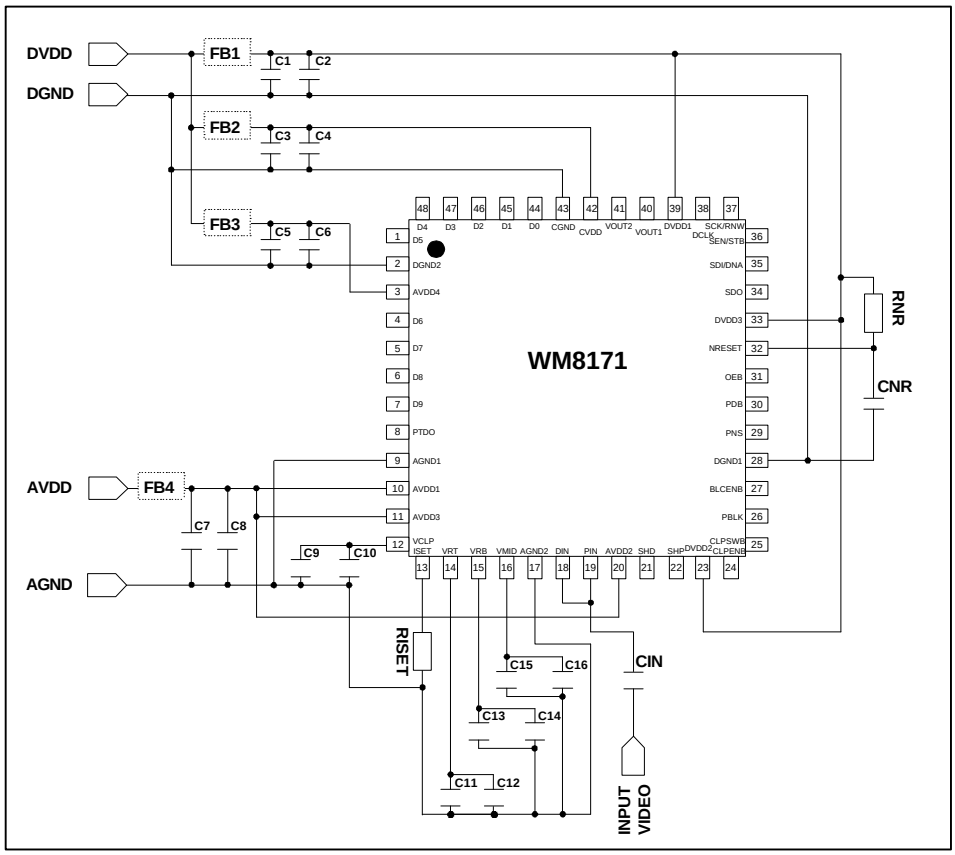


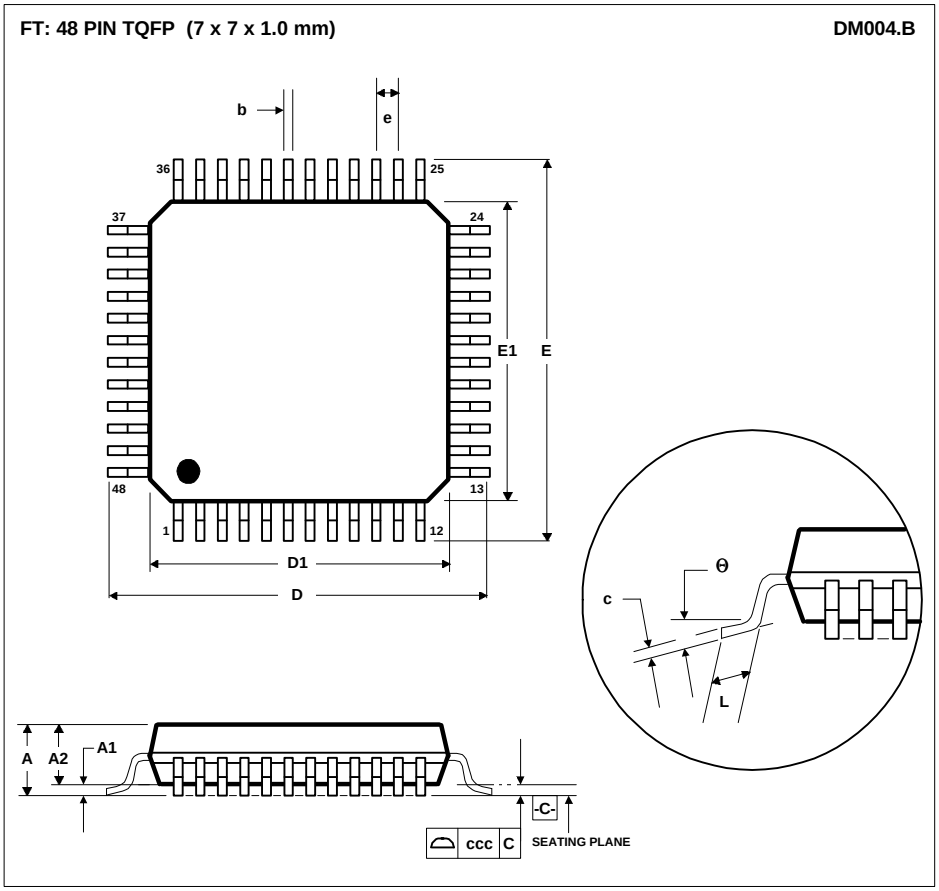
Figure 20 WM8171 External Components

COMPONENT REFERENCE	SUGGESTED VALUE	DESCRIPTION
FB1		Optional ferrite bead
FB2		Optional ferrite bead
FB3		Optional ferrite bead
FB4		Optional ferrite bead
C1	10µF	Decoupling to DGND for pin 39(DVDD1), pin 33(DVDD3) and pin 23(DVDD2)
C2	0.1µF	Decoupling to DGND for pin 39(DVDD1), pin 33(DVDD3) and pin 23(DVDD2)
C3	10µF	Decoupling to DGND for pin 42(CVDD)
C4	0.1µF	Decoupling to DGND for pin 42(CVDD)
C5	10µF	Decoupling to DGND for pin 3(DVDD4)
C6	0.1µF	Decoupling to DGND for pin 3(DVDD4)
C7	10µF	Decoupling to AGND for pin 10(AVDD1), pin 11(AVDD3) and pin 20(AVDD2)
C8	0.1µF	Decoupling to AGND for pin 10(AVDD1), pin 11(AVDD3) and pin 20(AVDD2)
C9	10µF	Decoupling to AGND for pin 12(VCLP)
C10	0.1µF	Decoupling to AGND for pin 12(VCLP)
C11	1µF	Decoupling to AGND for pin 14(VRT)
C12	0.1µF	Decoupling to AGND for pin 14(VRT)
C13	1µF	Decoupling to AGND for pin 15(VRB)
C14	0.1µF	Decoupling to AGND for pin 15(VRB)
C15	1µF	Decoupling to AGND for pin 16(VMID)
C16	0.1µF	Decoupling to AGND for pin 16(VMID)
CIN		Video input coupling capacitor to pin 18(DIN) and pin 19(PIN)
CNR		Capacitor between pin 32(NRESET) and DGND
RNR		Pull-up resistor between pin 32(NRESET) and pin 33(DVDD3)
RISET		Internal bias setting resistor between pin 13(ISET) and AGND

Table 7 Device Decoupling Components

PACKAGE DIMENSIONS

FT: 48 PIN TQFP (7 x 7 x 1.0 mm) **DM004.B**



Symbols	Dimensions (Millimeters)		
	MIN	NOM	MAX
A	-----	-----	1.20
A_1	0.05	-----	0.15
A_2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.09	-----	0.20
D	9.00 BSC		
D_1	7.00 BSC		
E	9.00 BSC		
E_1	7.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
Θ	0^o	3.5^o	7^o
Tolerances of Form and Position			
ccc	0.08		
REF:	JEDEC.95, MS-026		

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.25MM.
D. MEETS JEDEC.95 MS-026, VARIATION = ABC. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.