Winbond Electronics Corp.

8-BIT VERIFICATION MICROCONTROLLER

GENERAL DESCRIPTION

The W78V58B product corresponds to the W78C51/52/58 and W78C154*, except that an external 4, 8, 32, or 16 KB EPROM replaces the mask ROM in this product. This microcontroller can be used to verify mask ROM codes before the fabrication of a mask ROM. For detailed specifications concerning the W78V58B, refer to the data sheet for the W78C51/52/58/154* and WHC8302.

FEATURES

- 8-bit CMOS microcontroller
- Fully static design
- 0 to 40 MHz operation
- 256-byte on-chip scratchpad RAM
- 64 KB program memory address space
- 64 KB data memory address space
- Boolean processor
- Six-source, two-level interrupt capability
- Three 16-bit timer/counters
- One full duplex serial channel
- Built-in power management
- Four 8-bit bidirectional I/O ports
- Substitutes external EPROM for the "internal" 4, 8, 32, or 16 KB mask ROM of the W78C51/52/58/154* and supports signal to indicate which ROM is active, "internal" or "external"
- Packaged in 100-pin PQFP

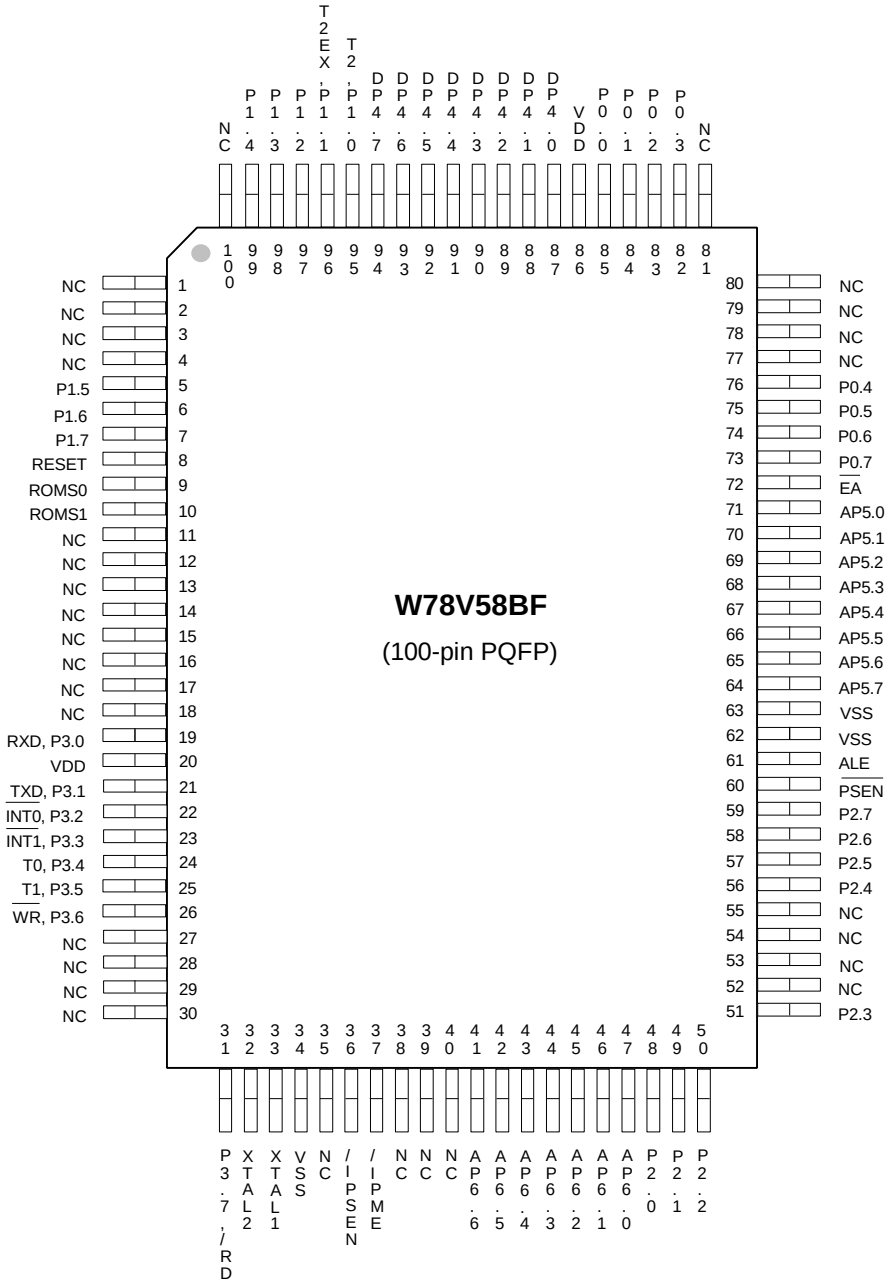
Notes for all W78C154*:

1. W78V58B will verify W78C154 except port1.6 & port1.7 as output mode:

W78V58B	port1.6 & port1.7	pull-ups
W78C154	port1.6 & port1.7	open drain

2. The specification of W78C154 is exclusive, therefore, the DC characteristics is not fully compatible with W78V58B, however the function is still the same as W78V58B.

PIN CONFIGURATION



PIN DESCRIPTION

P0.0- P0.7 I/O Port0

Function depends on ROMS1 and ROMS0. For details see Table D1.

P1.0- P1.7 I/O Port1

Function is the same as in the W78C51/52/58/154*.

P2.0- P2.7 I/O Port2

Function depends on ROMS1 and ROMS0. For details see Table D1.

P3.0- P3.7 I/O Port3

Function is the same as in the W78C51/52/58/154*.

DP4.0- DP4.7 Address/Data Bus

Pins ROMS1 and ROMS0 determine functions of DP4. For details, see Table D2.

AP5.0 - AP5.7 Address Bus

Pins ROMS1 and ROMS0 determine functions of AP5. For details, see Table D3.

AP6.0- AP6.6 Address Bus

Pins ROMS1 and ROMS0 determine functions of AP6. For details, see Table D4.

$\overline{\text{IPME}}$

Internal Program Memory Enable Output, active low.

This is the "internal" program memory enable signal. It outputs "0" to indicate that the access buses are DP4, AP5 and AP6. It outputs "1" to indicate that the access buses are Port 0 and Port 2.

ROMS1, ROMS0

ROM Size Select Input.

This is input pins to determine verification of 4 different ROM sizes including 4K, 8K, 16K and 32K bytes. Default status is pulled high by an internal pull-high resistor (approx. 30K). For details, see tables D1–D4.

$\overline{\text{IPSEN}}$

Internal Program Store Enable Output, active low.

Pins ROMS1 and ROMS0 determine function of $\overline{\text{IPSEN}}$, which is an active low output.

$\overline{\text{IPSEN}}$ enable "internal" program memory output to the DP4 bus during fetch and MOVC operation. For details, see table D5.

$\overline{\text{EA}}$, $\overline{\text{PSEN}}$, ALE, RST, XTAL1, XTAL2

Functions same as in W78C58.

ROMS1	ROMS0	FUNCTION OF $\overline{\text{PSEN}}$, PORT 0, AND PORT 2
0	0	Same as in the W78C51. (Verify 4K ROM.)
0	1	Same as in the W78C52. (Verify 8K ROM.)
1	0	Same as in the W78C154* (Verify 16K ROM.)
1	1	Same as in the W78C58. (Verify 32K ROM.)

Table D1.

ROMS1	ROMS0	FUNCTIONS OF DP4
0	0	Provides a multiplexed low-byte address/data bus during accesses to external 4 KB EPROM.
0	1	Provides a multiplexed low-byte address/data bus during accesses to external 8 KB EPROM.
1	0	Provides a multiplexed low-byte address/data bus during accesses to external 16 KB EPROM.
1	1	Provides a multiplexed low-byte address/data bus during accesses to external 32 KB EPROM.

Table D2.

ROMS1	ROMS0	FUNCTIONS OF AP5
0	0	AP5 output the <7:0> address of the external 4K EPROM.
0	1	AP5 output the <7:0> address of the external 8K EPROM.
1	0	AP5 output the <7:0> address of the external 16K EPROM.
1	1	AP5 output the <7:0> address of the external 32K EPROM.

Table D3.

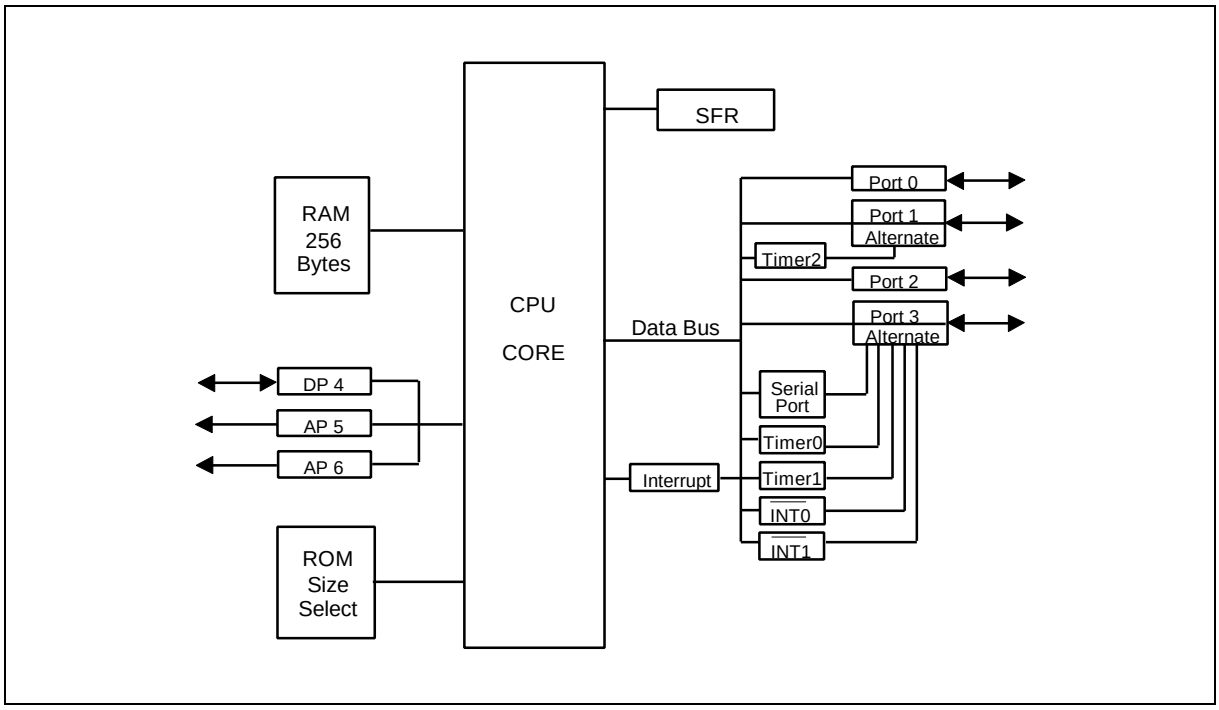
ROMS1	ROMS0	FUNCTIONS OF AP6
0	0	AP6<3:0> output the <11:8> address of the external 4K EPROM.
0	1	AP6<4:0> output the <12:8> address of the external 8K EPROM.
1	0	AP6<5:0> output the <13:8> address of the external 16K EPROM.
1	1	AP6<6:0> output the <14:8> address of the external 32K EPROM.

Table D4.

ROMS1	ROMS0	FUNCTIONS OF $\overline{\text{IPSEN}}$
0	0	Outputs low to enable the lowest 4KB program memory output.
0	1	Outputs low to enable the lowest 8KB program memory output.
1	0	Outputs low to enable the lowest 16KB program memory output.
1	1	Outputs low to enable the lowest 32KB program memory output.

Table D5.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Pins ROMS1 and ROMS0 are input pins used to select one of four different ROM sizes: 4, 8, 16, or 32 K bytes. When $\overline{EA}$ is set to high, an internal program code is fetched from the external 4, 8, 16, or 32 KB EPROM. The interface pins needed are DP4<7:0>, as the data bus, and AP5<7:0> and AP6<3:0>, AP6<4:0>, AP6<5:0> or AP6<6:0>, as the address bus, depending on the states of ROMS1 and ROMS0. When $\overline{EA}$ is set to low, the device is compatible with W78C32 operations.

For example, when pins ROMS1 and ROMS0 are held in the "L" and "H" states, respectively, the W78V58B's functions are fully compatible with those of the W78C52, except that the internal 8 KB ROM is replaced by an external EPROM. To reduce the size occupied by the EPROM, one can use the W78T064, which is a 20-pin and 300-mil 8 KB EPROM with internal address latch. When the W78T064 is used as the EPROM, DP4<7:0> are used as the low-byte address and data bus and $\overline{IPSEN}$ is used to enable the output of W78T064.

The $\overline{IPME}$ pin indicates the access buses for the program memory. It outputs "0" to indicate that the access buses are DP4, AP5, and AP6, that is, the "internal" program memory is being accessed. It outputs "1" to indicate that the access buses are Port 0 and Port 2, that is, the "external" program memory is being accessed.

Power Reduction Function

The W78V58B supports power reduction but is not guaranteed to duplicate the current specifications of the W78C32.

The status of the external pins during the idle and power-down modes for the W78V58B is shown in the following table.

MODE \ PIN		ALE	$\overline{PSEN}$	PT0- PT3	DP4	AP5, AP6
Idle	Internal	1	1	Same as W78C52	Floating	Address
	External	1	1	Same as W78C52	Floating	Address
Power Down	Internal	0	0	Same as W78C52	Floating	Address
	External	0	0	Same as W78C52	Floating	Address

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
DC Power Supply	V_{DD}–V_{SS}	-0.3	+7.0	V
Input Voltage	V_{IN}	V_{SS} -0.3	V_{DD} +0.3	V
Operating Temperature	T_{OPR}	0	70	°C
Storage Temperature	T_{STG}	-55	+150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

DC CHARACTERISTICS

(V_{DD}–V_{SS} = 5V ±10%, T_{OPR} = 25° C, F_{OSC} = 40 MHz, unless otherwise specified.)

PARAMETER	SYM.	TEST CONDITIONS	SPEC.			UNIT
			MIN.	TYP.	MAX.	
Oper. Voltage	V_{DD}		4.5	5	5.5	V
Oper. Current	I_{DD}	* No Load	-	-	40	mA
Idle Current	I_{IDLE}	Program Idle Mode	-	-	10	mA
Pwdn Current	I_{PWDN}	Program Power-down Mode	-	-	50	µA
Input Leakage Current	I_{LK1}	RESET Internal Pull-low Notes 1, 2	-10	-	+300	µA
	I_{LK2}	Port 0, DP4, $\overline{EA}$ Note 1	-10	-	+10	µA
	I_{LK3}	P1, P2, P3 Note 1	-50	-	+10	µA
O/P Low Voltage	V_{OL1}	I_{OL1} = 2 mA (Port 1, 2, 3)	-	-	0.45	V
O/P High Voltage	V_{OH1}	I_{OH1} = -100 µA (Port 1, 2, 3)	2.4	-	-	V
O/P Low Voltage	V_{OL2}	I_{OL2} = 4 mA Note 3 (ALE, $\overline{PSEN}$, P0, DP4)	-	-	0.45	V
O/P High Voltage	V_{OH2}	I_{OH2} = -400 µA Note 3 (ALE, $\overline{PSEN}$, P0, DP4)	2.4	-	-	V
O/P Low Voltage	V_{OL3}	I_{OL2} = 2 mA (AP5, AP6, $\overline{IPME}$, $\overline{IPSEN}$)	-	-	0.45	V

DC Characteristics, continued

PARAMETER	SYM.	TEST CONDITIONS	SPEC.			UNIT
			MIN.	TYP.	MAX.	
O/P High Voltage	V_{OH3}	I_{OH2} = -100 µA (AP5, AP6, $\overline{IPME}$, $\overline{IPSEN}$)	2.4	-	-	V
Input Voltage	V_{ILT}	V_{DD} = 5V ±10%	0	-	0.8	V
Input Voltage	V_{IHT}	V_{DD} = 5V ±10%	2.4	-	Note 4	V
Input Voltage	V_{ILC}	V_{DD} = 5V ±10%, XTAL1 Note 5	0	-	0.8	V
Input Voltage	V_{IHC}	V_{DD} = 5V ±10%, XTAL1 Note 5	3.5	-	Note 4	V
Input Voltage	V_{ILR}	V_{DD} = 5V ±10%, RESET Note 5	0	-	0.8	V
Input Voltage	V_{IHR}	V_{DD} = 5V ±10%, RESET Note 5	2.4	-	Note 4	V

Notes:

1. $0<V_{IN}<V_{DD}$, for RESET, $\overline{EA}$, Port 0, DP4, P1, P2 and P3 inputs in leakage.
2. Using an internal pull low/high resistor (approx. 30K).
3. ALE, $\overline{PSEN}$, P0 and DP4 in external program or data access mode.
4. The maximum input voltage is V_{DD} +0.2V.
5. XTAL1 is a CMOS input and RESET is a Schmitt trigger input.

AC CHARACTERISTICS

AC specifications are a function of the particular process used to manufacture the product, the ratings of the I/O buffers, the capacitive load, and the internal routing capacitance. Most of the specifications can be expressed in terms of multiple input clock periods (T_{CP}), and actual parts will usually experience less than a ±20 nS variation.

Refer to the W78C52 data sheet for further AC specifications besides those listed below.

Clock Input Waveform

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTE
Operating Speed	F_{OP}	0	-	40	MHz	1
Clock Period	T_{CP}	25	-	-	nS	2
Clock High	T_{CH}	10	-	-	nS	3
Clock Low	T_{CL}	10	-	-	nS	3

Notes:

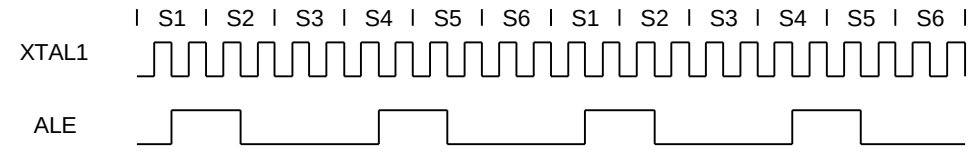
1. The clock may be stopped indefinitely in either state.
2. The T_{CP} specification is used as a reference in other specifications.
3. There are no duty cycle requirements on the XTAL1 input.

Program Fetch Cycle

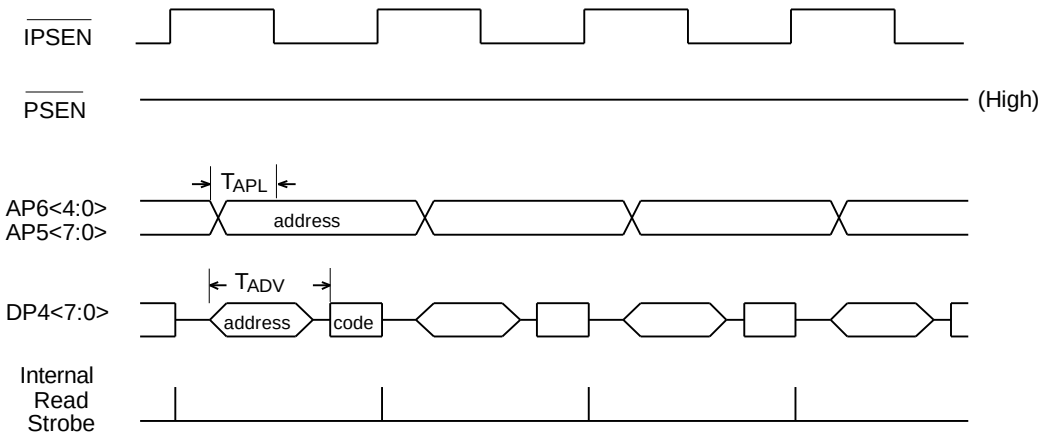
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Address Valid to $\overline{PSEN}$ Low	T_{APL}	2 T_{CP}	-	-	nS
Address Valid to Data Valid	T_{ADV}	-	-	4 T_{CP}	nS

TIMING WAVEFORMS

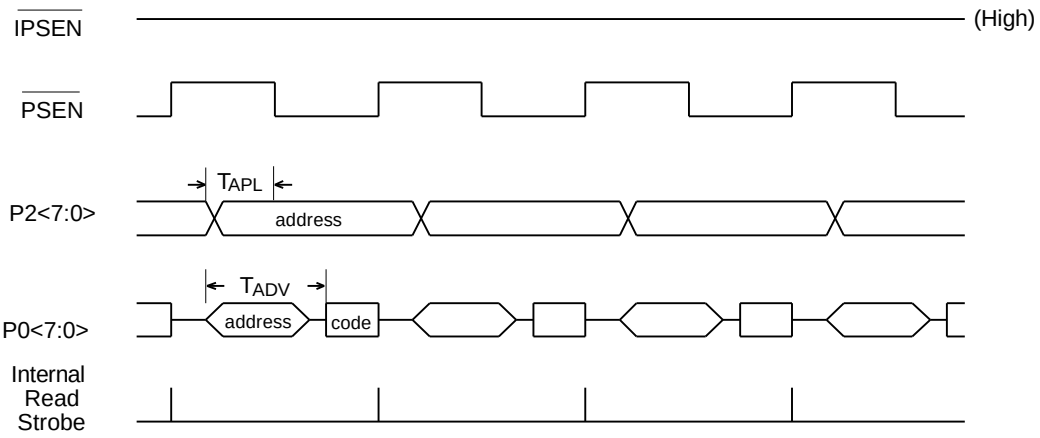
PROGRAM FETCH CYCLE (W78C52 as example)



Internal (address: 0 to 1FFFH) program fetch:



External (address: 2000H to 0FFFFH) program fetch:



TYPICAL APPLICATION CIRCUIT

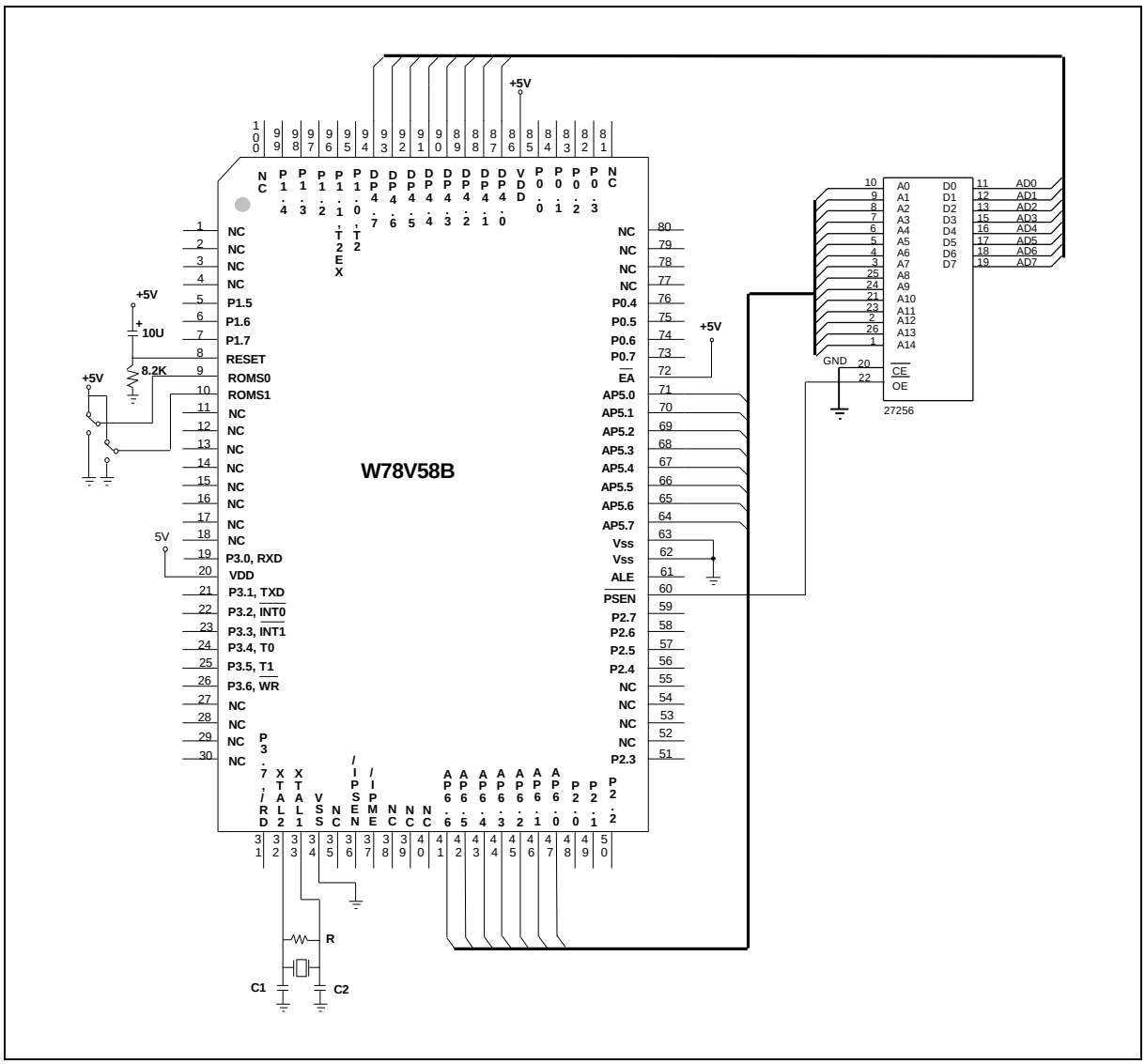


Figure A

CRYSTAL	C1	C2	R
16 MHz	30P	30P	–
24 MHz	15P	15P	–
33 MHz	10P	10P	6.8K
40 MHz	5P	5P	6.8K

Above table shows the reference values for crystal applications.

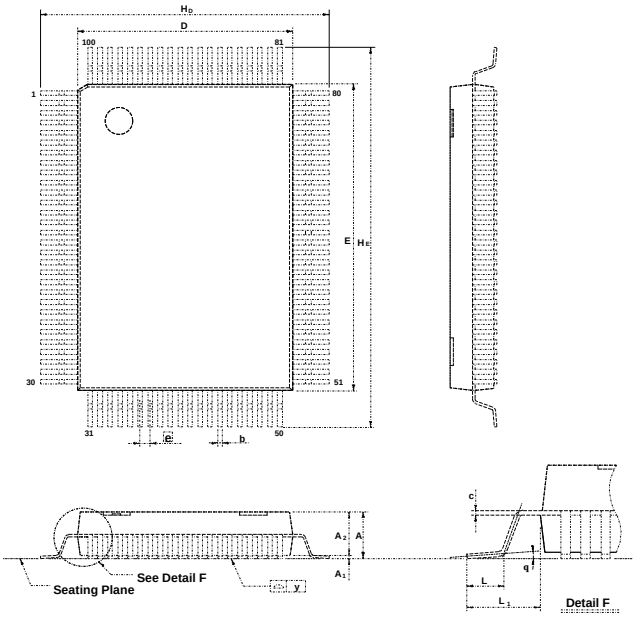
Notes:

1. For C1, C2, and R components refer to Figure A.
2. It is recommended that the crystals be replaced with oscillators for applications above 35 MHz.
3. ROMS0, ROMS1 select type:

ROMS1	ROMS0	VERIFY TYPE
0	0	(Verify 4K ROM)
0	1	(Verify 8K ROM)
1	0	(Verify 16K ROM)
1	1	(Verify 32K ROM)

PACKAGE DIMENSIONS

100-pin QFP



Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	----	----	0.130	----	----	3.30
A_1	0.004	----	----	0.10	----	----
A_2	0.107	0.112	0.117	2.718	2.845	2.972
b	0.010	0.012	0.016	0.254	0.305	0.407
c	0.004	0.006	0.010	0.101	0.152	0.254
D	0.546	0.551	0.556	13.87	14.00	14.13
E	0.782	0.787	0.792	19.87	20.00	20.13
e	0.020	0.026	0.032	0.498	0.65	0.802
H_D	0.728	0.740	0.752	18.49	18.80	19.10
H_E	0.964	0.976	0.988	24.49	24.80	25.10
L	0.039	0.047	0.055	0.991	1.194	1.397
L_1	0.087	0.095	0.103	2.21	2.413	2.616
y	----	----	0.004	----	----	0.102
q	0°	----	12°	0°	----	12°

Notes:

1. **Dimension D & E do not include interlead flash.**
2. **Dimension b does not include dambar protrusion/intrusion.**
3. **Controlling dimension: Millimeters**
4. **General appearance spec. should be based on final visual inspection spec.**

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