A. General Description:

The USB micro-controller is the best choice for MP3 player, MMC/CompactFlash™/SmartMedia™ card reader/writer, voice recorder and devices with USB port as an interface to transfer information. It is a multi-function chip with excellent performance and low cost. Because all the devices designed by this controller that do not need to have the mechanical parts, which have the properties of fully anti vibration and extremely low power consumption. By using this one chip solution, all the efforts from R/D to production will reduce a lot and this will simplify the RMA problems also

B. Features:

1. Support Transfer Interfaces:
   - USB Interface
   - ATA/IDE Interface
2. Support **ICE Mode** for ICE Emulation during Product Design R/D Period
3. Support Flash ROM (Flash EPROM) for **In-System Programming** through USB Port or RS232 Port:
   - 0x0000h~0xFFFFh: 64KB
4. 8051 RAM Mode:
   - Internal RAM 256 Bytes.

     RAM 0H–127H can be addressed directly and indirectly as the same as in 8051. Address pointers are R0 and R1 of the selected register bank.

     RAM 128H–255H can only be addressed indirectly as the same as in 8051. Address pointers are R0, R1 of the selected registers bank.
   - Internal MOVX RAM:

     0x0000h~0x0FFFh: 4KB (Internal and USB Registers)

     0x1000h~0x27FFh: 6KB (On Chip)
   - External MOVX RAM:

     0x2800h~0xFFFFh: 54KB
5. Support SRAM Buffer (Dual Buffer Mode):
   - A Buffer (256+8 = 264 Words)
   - B Buffer (256+8 = 264 Words)
6. Support MP3 Decoder Chips:

- MICRONAS MAS3507D
- ST Microelectronics STA013
- TLI TL7230MD (Samsung)

7. Support Solid State Storage Cards:
   - SmartMedia™ Card (Capacity up to 128MB)
   - CompactFlash™ Card
   - MultiMedia Card (Capacity up to 32MB/Card)
8. Support Specification Versions:
   - SmartMedia™ Electrical Specification Version 1.10

     SmartMedia™ Physical Format Specification Version 1.10

     SmartMedia™ Format Specification Version 1.10
   - USB Specification Reversion 1.1

     Support one CONTROL transfer, one interrupt transfer and two BULK transfer

     Support MP3 USB uC interface.

     Endpoint:

     Endpoint 0: 16 bytes control transfer.

     Endpoint 1: 64*2 bytes bulk transfer for IN transaction.

     Endpoint 2: 64*2 bytes bulk transfer for OUT transaction.

     Endpoint 3: 8byte interrupt transfer for IN transaction.

     Data Payload:

     Endpoint 0: max 16 bytes
     Endpoint 1: max 64 bytes

     Endpoint 2: max 64 bytes

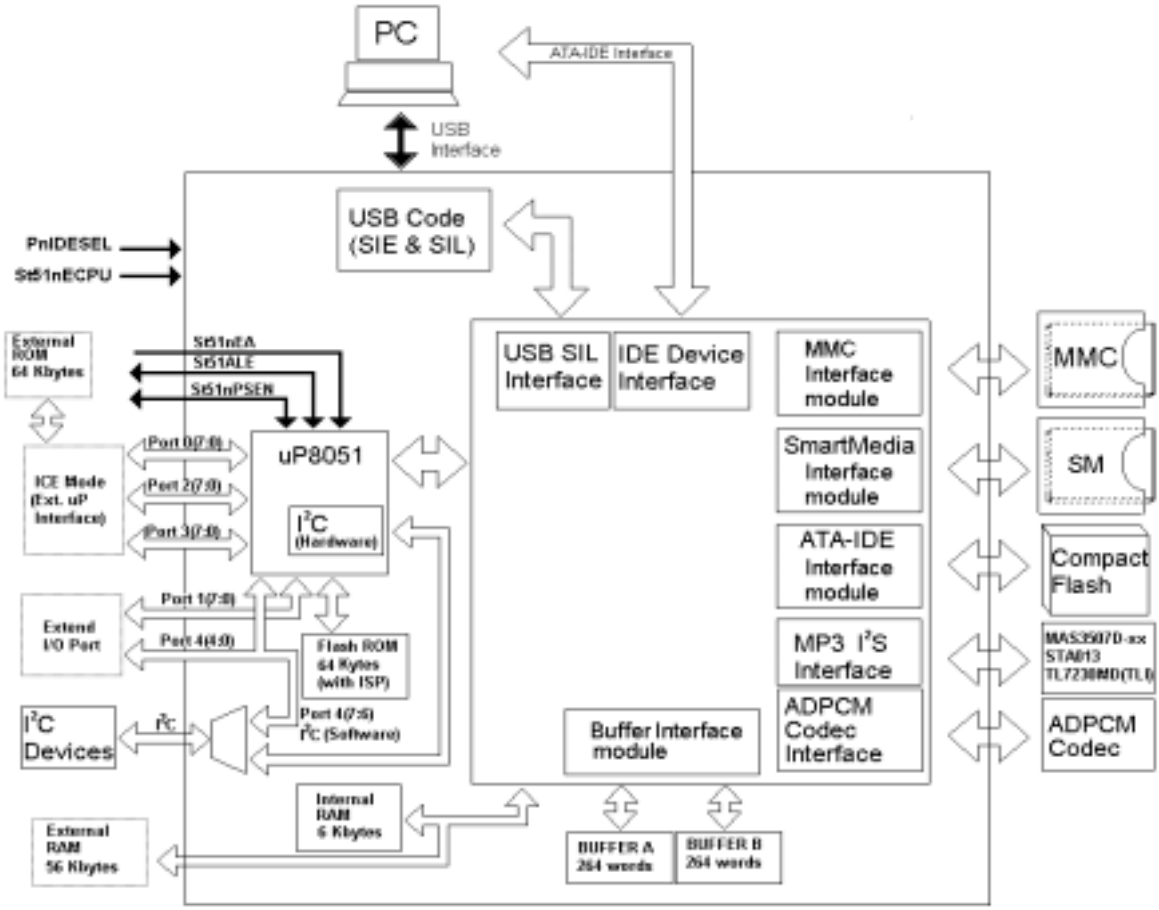
Endpoint 3: max 8 bytes

- MultiMediaCard System Specification 1.4
- CompactFlash™ Specification Version 1.4
- PC Card Standard Release 7.0

9. Host Transfer Rate for SmartMedia™/CompactFlash™: 16.6MB/s (PIO4)
10. Transfer Rate for USB Interface: “Full speed” Up to12Mbits/sec
11. Support ADPCM CODEC for Voice Recorder
12. Support I^2C Interface for LCD Controller Chip
13. 128-Pin or 100-Pin QFP Package
14. Operating Voltage: 3.0V~5.5V **(* Note 1**)
15. USB bus-powered capability
16. Power Saving implemented:
    - Power-down mode
    - Idle mode
17. Working Frequency: 12MHz

***Note 1: For USB system, operating voltage is 3.0V~3.6V.**

C. FUNCTION BLOCK DIAGRAM:



USB Micro-Controller Block Diagram

FUNCTIONAL DESCRIPTION

The W78E717E architecture consists of a core controller surrounded by various registers, four general purpose I/O ports, one special purpose programmable 4-bits I/O port, 256 bytes of RAM, three timer/counters, a serial port. The processor supports 111 different opcodes and references both a 64K program address space and a 64K data storage space.

Timers 0, 1, and 2

Timers 0, 1, and 2 each consist of two 8-bit data registers. These are called TL0 and TH0 for Timer 0, TL1 and TH1 for Timer 1, and TL2 and TH2 for Timer 2. The TCON and TMOD registers provide control functions for timers 0, 1. The T2CON register provides control functions for Timer 2. RCAP2H and RCAP2L are used as reload/capture registers for Timer 2. The operations of Timer 0 and Timer 1 are the same as in the W78C51. Timer 2 is a 16-bit timer/counter that is configured and controlled by the T2CON register. Like Timers 0 and 1, Timer 2 can operate as either an external event counter or as an internal timer, depending on the setting of bit C/T2 in T2CON. Timer 2 has three operating modes: capture, auto-reload, and baud rate generator. The clock speed in capture or auto-reload mode is the same as that of Timers 0 and 1.

External Interrupts

The W78E717E has four external interrupts, which are called /INT0, /INT1, /INT2, /INT3. The IT0 and IT1 bits in the TCON register determine if these interrupts are level triggered (ITn=0) or falling edge triggered (ITn=1). The interrupt bit will be reset by the interrupt hardware if it was an edge triggered interrupt. It is the programmer's responsibility to ensure that the external event that generates a level triggered interrupt is satisfied and that the input is removed before the end of the interrupt service routine. The /INT0 will be used if Card (Smart Media Card, CompactFlash Card and MutiMedia Card) transfer data interrupt was enabled. The /INT1 will be used if USB transfer interrupt was enabled The /INT2 will be used when I2C was enable

$\overline{\text{INT2}}$ / $\overline{\text{INT3}}$

Two additional external interrupts, $\overline{\text{INT2}}$ and $\overline{\text{INT3}}$, whose functions are similar to those of external interrupt 0 and 1 in the standard 80C52. The functions/status of these interrupts are determined/shown by the bits in the XICON (External Interrupt Control) register. The XICON register is bit-addressable but is not a standard register in the standard 80C52. Its address is at 0C0H. To set/clear bits in the XICON register, one can use the "SETB ($\overline{\text{CLR}}$) bit" instruction. For example, "SETB 0C2H" sets the EX2 bit of XICON.

Clock

The W78E717E is designed to use either a crystal oscillator or an external clock. Internally, the clock is divided with two before it is used by default. This makes the W78E717E relatively insensitive to duty cycle variations in the clock.

Crystal Oscillator

The W78E717E incorporates a built-in crystal oscillator. To make the oscillator work, a crystal must be connected across pins XTAL1 and XTAL2. In addition, a load capacitor must be connected from each pin to ground, and a resistor must also be connected from XTAL1 to XTAL2 to provide a DC bias when the crystal frequency is above 12 MHz.

External Clock

An external clock should be connected to pin XTAL1. Pin XTAL2 should be left unconnected. The XTAL1 input is a CMOS-type input, as required by the crystal oscillator. As a result, the external clock signal should have an input one level of greater than 3.5 volts.

Power Management

Idle Mode

The idle mode is entered by setting the IDL bit in the PCON register. In the idle mode, the internal clock to the processor is stopped. The peripherals and the interrupt logic continue to be clocked. The processor will exit idle mode when either an interrupt or a reset occurs.

Power-down Mode

When the PD bit in the PCON register is set, the processor enters the power-down mode. In this mode all of the clocks are stopped, including the oscillator. To exit from power-down mode is by a hardware reset or external interrupts $\overline{INT0}$ to $\overline{INT1}$ when enabled and set to level triggered.

Reset

The external RESET signal is sampled at S5P2. To take effect, it must be held high for at least two machine cycles while the oscillator is running. An internal trigger circuit in the reset line is used to deglitch the reset line when the W78E717E is used with an external RC network. The reset logic also has a special glitch removal circuit that ignores glitches on the reset line. During reset, the ports are initialized to FFH, the stack pointer to 07H, PCON (with the exception of bit 4) to 00H, and all of the other SFR registers except SBUF to 00H. SBUF is not reset.

W78E717E Special Function Registers (SFRs) and Reset Values

F8									FF
F0	+B 00000000						**CHPENR 00000000**		F7
E8									EF
E0	+ACC 00000000								E7
D8	**+P4 xxxx1111**								DF
D0	+PSW 00000000								D7
C8	+T2CON 00000000		RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000			CF
C0	XICON 00000000				**SFRAL 00000000**	**SFRAH 00000000**	**SFRFD 00000000**	**SFRCN 00000000**	C7
B8	+IP 00000000							**CHPCON 0xx00000**	BF
B0	+P3 00000000								B7
A8	+IE 00000000								AF
A0	+P2 11111111								A7
98	+SCON 00000000	SBUF xxxxxxxx							9F
90	+P1 11111111								97
88	+TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000			8F

80	+P0 11111111	SP 00000111	DPL 00000000	DPH 00000000				PCON 00110000	87

Notes:

1.The SFRs marked with a plus sign (+) are both byte- and bit-addressable.

2. The text of SFR with bold type characters is extension function registers.

Winbond Electronics Corp.

Port 4 (D8H)

BIT	NAME	FUNCTION
7	P47	I2C used
6	P46	I2C used
5	P45	Default Read/Write internal MOVX register, Read/Write signal of P36 and P37 will output at set to low.
4	P44	Port 4 General purpose I/O
3	P43	Port 4 General purpose I/O with interrupt 2.
2	P42	Port 4 General purpose I/O
1	P41	Port 4 General purpose I/O
0	P40	Port 4 General purpose I/O

Port 4, SFR P4 at address D8H, is a 4-bit multipurpose programmable I/O port. Each bit can be configured individually by software. P4.0–P4.3 is a bi-directional I/O port which is same as port 1, P4.2 and P4.3 also serve as external interrupt $\overline{INT3}$ and $\overline{INT2}$ if enabled.

XICON - external interrupt control (C0H)

PX3	EX3	IE3	IT3	PX2	EX2	IE2	IT2

PX3: External interrupt 3 priority high if set

EX3: External interrupt 3 enable if set

IE3: If IT3 = 1, IE3 is set/cleared automatically by hardware when interrupt is detected/serviced

IT3: External interrupt 3 is falling-edge/low-level triggered when this bit is set/cleared by software

PX2: External interrupt 2 priority high if set

EX2: External interrupt 2 enable if set

IE2: If IT2 = 1, IE2 is set/cleared automatically by hardware when interrupt is detected/serviced

IT2: External interrupt 2 is falling-edge/low-level triggered when this bit is set/cleared by software

Eight-source interrupt information:

INTERRUPT SOURCE	VECTOR ADDRESS	POLLING SEQUENCE WITHIN PRIORITY LEVEL	ENABLE REQUIRED SETTINGS	INTERRUPT TYPE EDGE/LEVEL
External Interrupt 0	03H	0 (highest)	IE.0	TCON.0
Timer/Counter 0	0BH	1	IE.1	-
External Interrupt 1	13H	2	IE.2	TCON.2
Timer/Counter 1	1BH	3	IE.3	-
Serial Port	23H	4	IE.4	-
Timer/Counter 2	2BH	5	IE.5	-
External Interrupt 2	33H	6	XICON.2	XICON.0
External Interrupt 3	3BH	7 (lowest)	XICON.6	XICON.3

In-System Programming (ISP) Mode

The W78E717E equips one 64K byte of main MTP-ROM bank for application program (called APROM) and one 4K byte of auxiliary MTP-ROM bank for loader program (called LDROM). In the normal operation, the microcontroller executes the code in the APROM. If the content of APROM needs to be modified, the W78E717E allows user to activate the In-System Programming (ISP) mode by setting the CHPCON register. **The CHPCON is read-only by default, software must write two specific values 87H, then 59H sequentially to the CHPENR register to enable the CHPCON write attribute. Writing CHPENR register with the values except 87H and 59H will close CHPCON register write attribute.** The W78E717E achieves all in-system programming operations including enter/exit ISP Mode, program, erase, read ... etc, during device in the idle mode. Setting the bit CHPCON.0 the device will enter in-system programming mode after a wake-up from idle mode. Because device needs proper time to complete the ISP operations before awaken from idle mode, software may use timer interrupt to control the duration for device wake-up from idle mode. To perform ISP operation for revising contents of APROM, software located at APROM setting the CHPCON register then enter idle mode, after awaken from idle mode the device executes the corresponding interrupt service routine in LDROM. Because the device will clear the program counter while switching from APROM to LDROM, the first execution of RETI instruction in interrupt service routine will jump to 00H at LDROM area. The device offers software reset for switching back to APROM while the content of APROM has been updated completely. **Setting CHPCON register bit 0, 1 and 7 to logic-1 will result software reset to reset the CPU**. The software reset serves as a external reset. This in-system programming feature makes the job easy and efficient in which the application needs to update firmware frequently. In some applications, the in-system programming feature makes it possible to easily update the system firmware without opening the chassis.

SFRAH, SFRAL: The objective address of on-chip MTP-ROM in the in-system programming mode. SFRFAH contains the high-order byte of address, SFRFAL contains the low-order byte of address.

SFRFD: The programming data for on-chip MTP-ROM in programming mode.

SFRCN: The control byte of on-chip MTP-ROM programming mode.

SFRCN (C7)

BIT	NAME	FUNCTION
7	-	Reserve.
6	WFWIN	On-chip MTP-ROM bank select for in-system programming. = 0: 64K bytes MTP-ROM bank is selected as destination for re-programming. = 1: 4K bytes MTP-ROM bank is selected as destination for re-programming.
5	OEN	MTP-ROM output enable.
4	CEN	MTP-ROM chip enable.
3, 2, 1, 0	CTRL[3:0]	The flash control signals

MODE	WFWIN	CTRL<3:0>	OEN	CEN	SFRAH, SFRAL	SFRFD

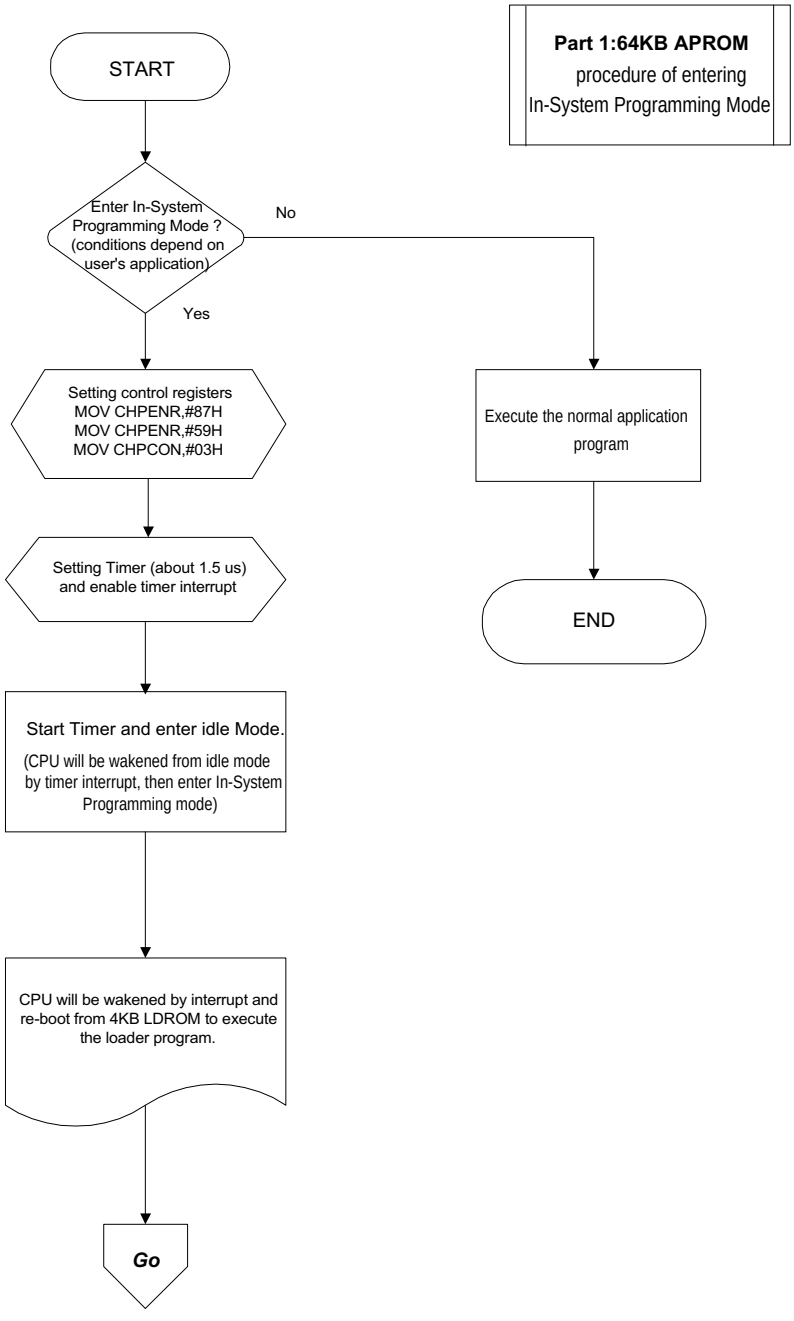
Erase 64KB APROM	0	0010	1	0	X	X
Program 64KB APROM	0	0001	1	0	Address in	Data in
Read 64KB APROM	0	0000	0	0	Address in	Data out
Erase 4KB LDROM	1	0010	1	0	X	X
Program 4KB LDROM	1	0001	1	0	Address in	Data in
Read 4KB LDROM	1	0000	0	0	Address in	Data out

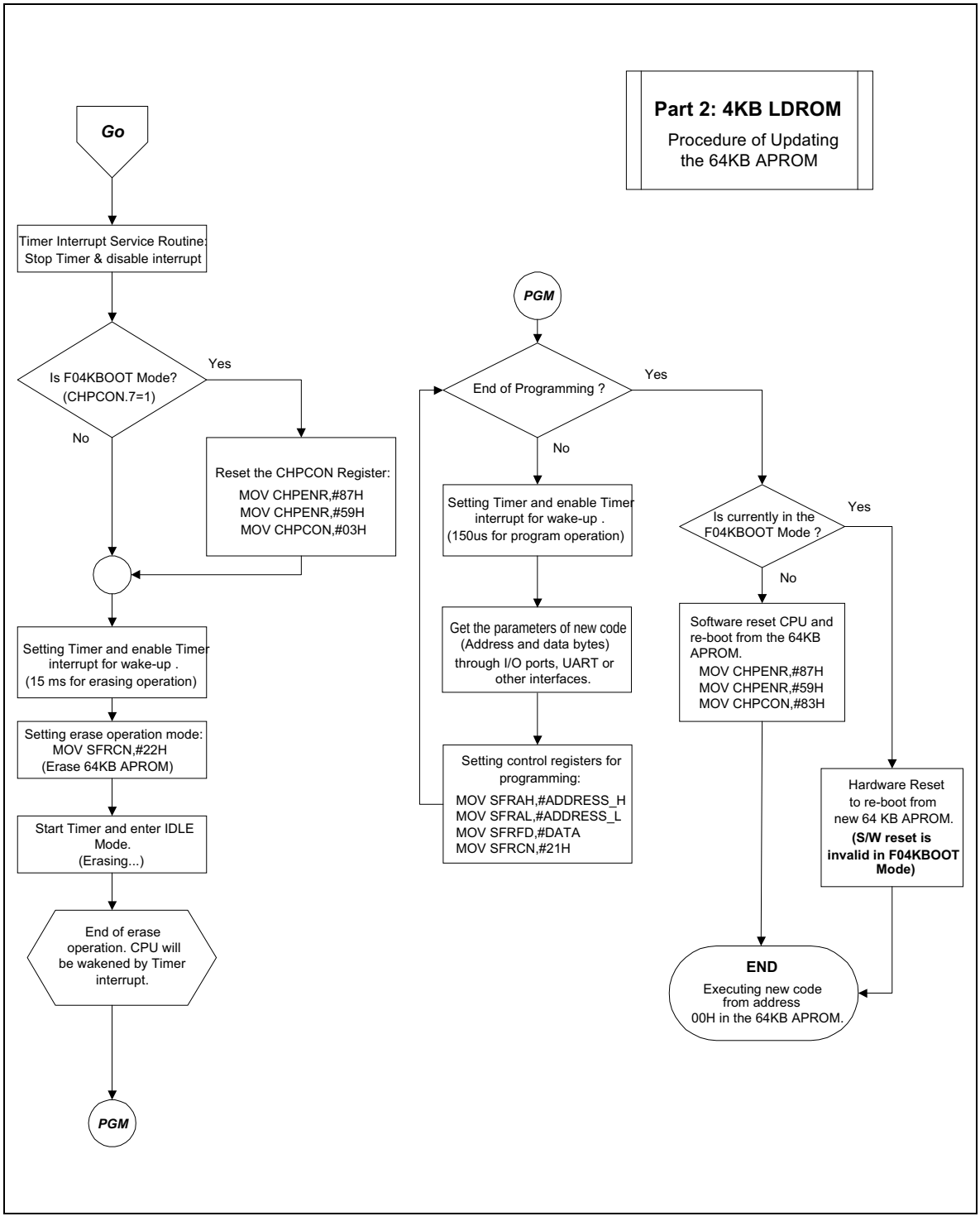
In-System Programming Control Register (CHPCON)

CHPCON (BFH)

BIT	NAME	FUNCTION
7	SWRESET (F04KMODE)	When this bit is set to 1, and both FBOOTSL and FPROGEN are set to 1. It will enforce microcontroller reset to initial condition just like power on reset. This action will re-boot the microcontroller and start to normal operation. To read this bit in logic-1 can determine that the F04KBOOT mode is running.

The Algorithm of In-System Programming

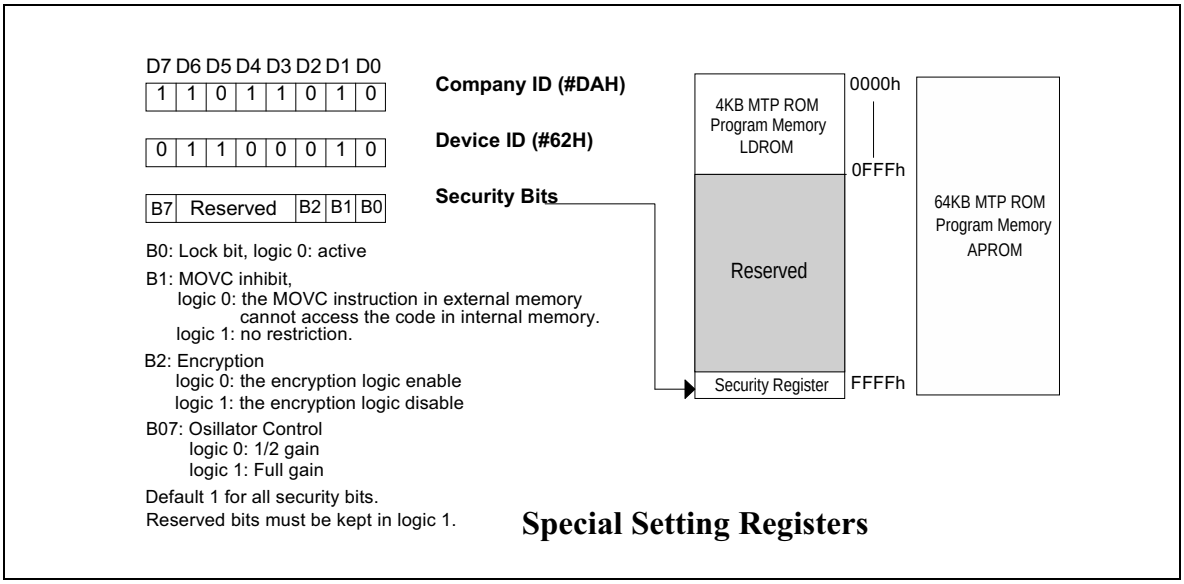




SECURITY

During the on-chip MTP-ROM programming mode, the MTP-ROM can be programmed and verified repeatedly. Until the code inside the MTP-ROM is confirmed OK, the code can be protected. The protection of MTP-ROM and those operations on it are described below.

The W78E717E has several Special Setting Registers, including the Security Register and Company/Device ID Registers, which can not be accessed in programming mode. Those bits of the Security Registers can not be changed once they have been programmed from high to low. They can only be reset through erase-all operation. The contents of the Company ID and Device ID registers have been set in factory. The Security Register is located at the 0FFFFH of the LDROM space.



Special Setting Registers

Lock bit

This bit is used to protect the customer's program code in the W78E717E. It may be set after the programmer finishes the programming and verifies sequence. Once this bit is set to logic 0, both the MTP ROM data and Special Setting Registers can not be accessed again.

MOVC Inhibit

This bit is used to restrict the accessible region of the MOVC instruction. It can prevent the MOVC instruction in external program memory from reading the internal program code. When this bit is set to logic 0, a MOVC instruction in external program memory space will be able to access code only in the external memory, not in the internal memory. A MOVC instruction in internal program memory space will always be able to access the ROM data in both internal and external memory. If this bit is logic 1, there are no restrictions on the MOVC instruction.

Encryption

This bit is used to enable/disable the encryption logic for code protection. Once encryption feature is enabled, the data presented on port 0 will be encoded via encryption logic. Only whole chip erase will reset this bit.

D. PIN ASSIGNMENT:

USB Interface Pins: 5

ITEM	Symbols	Pin #	Pin Type	Description
		LQFP128		
1	DP	94	I/O	USB Port.
2	DM	95	I/O	USB Port.
3	VDDA	93	I	Analog power supply.
4	GNDA	96	I	Analog power ground.
5	PVBUS	97	I	USB Port.

SRAM and External ROM Interface Pins: 27

ITEM	Symbols	Pin #	Pin Type	Description
		LQFP128		
1	PORAMnCS	55	O	St51 External RAM Chip selects Strobe. Low active
2	PORAMnWR	54	O	St51 External RAM Write Strobe. Low active
3	PORAMnRD	52	O	St51 External RAM Read Strobe. Low active
4	PRAMA[15:0]	51,50,49,48,47,46,45,44,43,42,40,39, 38,37,36,35	O	St51 External ROM/RAM Address Bus.
5	PMEMDAT[7:0]	64,65,66,67,68,69,70,71	I/O	St51 External ROM/RAM DATA I/O Port.

MP3 (I^2S Interface Pins): 3

ITEM	Symbols	Pin #	Pin Type	Description
		LQFP128		
1	PM P3DRQ	110	I	MP3 Data Request Pin (connect to MP3 decoder DRQ pin)
2	PMP3DCLK	111	O	MP3 Data Clock Pin (connect to MP3 decoder CLK pin), the frequency is about 128K ~ 2MHz.
3	PMP3DAT	113	O	MP3 Data Output Pin (connect to MP3 decoder DAT pin)

I^2C Interface Pins (within interrupt Pin): 3

ITEM	Symbols	Pin #	Pin Type	Description
		LQFP128		
1	PBSCL St51P4.7	106	I/O	General purpose I/O, DDC port serial clock I/O **Schmitt trigger input** V_{IH}/V_{IL}=0.7V_{DD}/0.3V_{DD}, V+/V-=~0.6V_{DD}/0.4V_{DD} **Open-drain output**, sink current: 8mA
2	PBSDA St51P4.6	107	I/O	General purpose I/O, DDC port serial data I/O **Schmitt trigger input** V_{IH}/V_{IL}=0.7V_{DD}/0.3V_{DD}, V+/V-=~0.6V_{DD}/0.4V_{DD} **Open-drain output**, sink current: 8mA
3	PuP4BITnINT	109	I	4bit microprocessor interrupt in by this pin.

IDE Device Interface and SmartMedia™ Interface Pins: 28

ITEM	Symbols	Pin #	Pin Type	Description
		LQFP128		
1	POCFnRD	3	O	IDE Read Enable (connect to IDE Interface Storage Device nRD pin)
	POSMnRD			SmartMedia™/Flash Read Enable. (connect to Flash Memory RE/WE pin)
2	POCFnWR	2	O	IDE Write Enable (connect to IDE Interface Storage Device nWR pin)
	POSMnWR			SmartMedia™/Flash Write Enable (connect to Flash Memory RE/WE pin)
3	POCFnCE1	116	O	IDE Device Chip Enable (connect to IDE Interface Storage Device CE1 pin)
4	POCFnCE2	119	O	IDE Device Chip Enable (connect to IDE Interface Storage Device CE2 pin).
5	PICFINTRQ	114	I	IDE Device interrupt request. (connect to IDE Interface Storage Device INT pin).
6	PISMFRDY	26	I	SmartMedia™/Flash Ready/BSY signal. Connect to flash memory pin Ready/nBusy.

	POCFA[2:0]	16,15,14	O	PBIDEAddr[15:0] pins connect directly to IDE Interface Storage Device Address Bus[15:0].
7	POSMnFWP POSMFCLE POSMFALE	16 15 14	O	PSMnFWP- SmartMedia™/Flash Write Protect. Connect to Flash Memory WP pin. PSMFCLE- SmartMedia™/Flash Command Latch Enable. Connect to Flash Memory CLE pin. PSMFALE- SmartMedia™/Flash Address Latch Enable. Connect to Flash Memory ALE pin.
8	PBCFDAT[7:0]	128,127,126,125, 124,123,122,121	I/O	PBIDEDat[7:0] pins are direct connect to Storage Device (with IDE interface) Data Bus[7~0].
	PBSMDAT[7:0]			PBSMDat[7:0] pins connect directly to SmartMedia™/Flash Data Bus[0:7].
9	PBCFDAT[15:8]	25,24,23,22,20,19,18,17	I/O	PBIDEDat[15:8] pins are direct connect to Storage Device (with IDE interface) Data Bus[15~8].
10	PICFnCD	4	I	This pin is a Card Detect Pin. Connect to the IDE Interface Storage Device Card Detect pin. It is internal pull high
11	PISMnFCD	28	I	SmartMedia™/Flash Card Detect. Connect to the SmartMedia™ pin 11. It is internal pull high
12	POSMnFCE	1	O	SmartMedia™/Flash Chip Enable. Connect to Flash Memory CE pin. It is internal pull high

MultiMediaCard Interface Pins: 3

ITEM	Symbols	Pin #	Pin Type	Description
		LQFP128		
1	PMMCCLK	115	O	MultiMediaCard Clock Pin. The frequency is about 200K ~ 12.5MHz.
2	PBMMCCMD	118	I/O	MultiMediaCard Command/Response Pin.
3	PBMMCDAT	120	I/O	MultiMediaCard Data Input/Output Pin.

ADPCM Codec (Winbond W6620) Interface Pins: 4

ITEM	Symbols	Pin #	Pin Type	Description
		LQFP128		

1	PADPCMDRx	27	I	This pin is used to receive input data, controlled by PADPCMClk and PADPCMSync. Connect directly to ADPCMCodec DT pin.
2	PADPCMDTx	29	O	This pin is used to transmission output data controlled by PADPCMClk and PADPCMSync. Connect directly to ADPCMCodec DR pin.
3	PADPCMClk	31	O	This pin is to receive bit clock or clock for transmission. The frequency varies from 128KHz to 2MHz. Connect directly to ADPCMCodec BCLKT&BCLKR pin.
4	PADPCMSync	32	O	This pin is to output 8KHz pulse train to receive / transmit frame syncs, Connect directly to ADPCMCodec FST&FSR pin.

IDE Host Interface/External St51 Microprocessor Pins: 42

ITEM	Symbols	Pin #	Pin Type	Description
		LQFP128		
1	St51P3.7 (St51nRD)	88	I/O	Bi-directional I/O with internal pull-ups. It is also used for St51 microprocessor External Data Memory Read Strobe.
	PHnIOR			Host I/O Read signals. It's active low and includes the internal pull-up resistors.
2	St51P3.6 (St51nWR)	87	I/O	Bi-directional I/O with internal pull-ups. It is also used for St51 microprocessor External Data Memory Write Strobe.
	PHnIOW			Host I/O Write signals. It's active low and includes the internal pull-up resistors.
3	St51P3.5 (St51T1)	100	I/O	Bi-directional I/O with internal pull-ups. It is also used for St51 microprocessor Timer 1 External input.
	PnCS1		I	Card enable 1(When True IDE mode transfer is set).
4	St51P3.4 (St51T0)	102	I/O	Bi-directional I/O with internal pull-ups. It is also used for St51 microprocessor Timer 0 External input.
	PnCS2		I	Card enable 2(When True IDE mode transfer is set).
5	St51P3.3 (St51INT1)	90	O	The St51 microprocessor Ext.Int1 source output when ICE Mode is setting.

	PIOCS16			In True IDE mode this output signal is asserted low when this device is expecting a word data transfer cycle
6	St51P3.2 (St51INT0)	89	O	The St51 microprocessor Ext.Int0 source output when ICE Mode is setting.
	PHnINTRQ			Host interrupt request (When True IDE mode transfer is set)
7	St51P3.1 (St51TXD)	103	I/O	Bi-directional I/O with internal pull-ups. It is also used for St51 microprocessor Serial Port 0 Output.
	PBnDASP			Drive Active or Slave Present (When True IDE mode transfer is set)
8	St51P3.0 (St51RXD)	92	I/O	Bi-directional I/O with internal pull-ups. It is also used for St51 microprocessor Serial Port 0 input.
	PBnPDIAG			Status changed or pass diagnostic (When True IDE mode transfer is set)
9	St51P4.4	30	I/O	St51 microprocessor Port4 (Extra port, general purpose I/O).
	PHnRST		I	Host reset signal. When active, it initiates the control registers and resets St51 microprocessor. This signal is active low.
10	St51P4.3	108	I/O	St51 microprocessor Port4 (Extra port, general purpose I/O).
	St51MRST		I	For external St51 microprocessor reset when ICE Mode.
11	St51P4[2:0]	99,91,98	I/O	St51 microprocessor Port4 (Extra port, general purpose I/O).
	PHADDR[2:0]		I	Host address bus 0~2(True IDE Interface)
13	St51P1[7:0]	13,12,11,10,8,7,6,5	I/O	St51 microprocessor Port1 (General purpose I/O).
14	St51P0[7:0]	63,62,61,60,59,58,57,56	I/O	St51 microprocessor Port0 (General purpose I/O). This port also provides a multiplexed low order address/data bus during accesses to external memory.
	PBHD[7:0]			Host data bus 0~7. Support 8-bit or 16-bit data transfer.

15	St51P2[7:0] PBHD[15:8]	84,83,82,81,80,78,77,76	I/O	St51 microprocessor Port2 (General purpose I/O). This port also provides the upper address for accesses to external memory. Host data bus 8~15. Support 8-bit or 16-bit data transfer
16	St51nEA	79	I	This pin force St51 microprocessor to execute out of external ROM. '0' External ROM Select. It is no pull up resistor.
17	St51ALE	74	O	It is used to enable the address latch that separates the address from the data on St51 Port0[7:0].
18	St51nPSEN	75	O	Enable the external ROM data onto the St51Port0 address/data bus during fetch and MOVC operation. When internal ROM access is performed, no strobe signal outputs from this pin
19	St51nECPU	72	I	This pin is used to enable the internal('1') St51 or External('0') St51 microprocessor. It is no pull up resistor.
20	PnIDESEL	86	I	Select IDE interface('1') or St51 Microprocessor interface('0'). It is no pull up resistor.

Global Signal Pins: 13

ITEM	Symbols	Pin #	Pin Type	Description
		LQFP128		
1	PSYSnRST	101	I	System Reset Signal, active low.
2	PIXTAL	34	I	Crystal input pad.
3	POXTAL	33	O	Crystal Output pad.
5	PCLKOUT	104	O	Clock output. The clock frequency can be modifying by the Firm Ware, it can divide the main clock by CLK/(2*n+2) and output to the system, which needs the clock, ex PIXTAL=12MHz, the frequency is about 24MHz.
6	VDD	9,41,73,105	I	+5V / + 3.3 Power Supply
7	GND	21,53,85,117	I	Ground
8	TESTPIN	112	I	Test Mode, PLL enable('0') or PLL disable('1'), internal strong pull low.

E. USB and Card Interface Register Definition:

Use MOVX @DPTR in 8051 to read/write the register. The addresses are shown as below,

NO.	ADDRESS (HEX)	Description	Reset Value (Hex)
Host IDE I/O Interface Register			
E.1	0x0100h	Data Register (CF_DATA)	00h
E.2	0x0101h	Feature Register (Write Only) (CF_FEATURE)	-
E.3	0x0101h	Error Register (Read Only) (CF_ERR_REG)	00h
E.4	0x0102h	Sector Count Register (CF_SEC_CNT)	00h
E.5	0x0103h	Sector Number Register (CF_SEC_NUM)	00h
E.6	0x0104h	Cylinder Low Register (CF_CYL_L)	00h
E.7	0x0105h	Cylinder High Register (CF_CYL_H)	00h
E.8	0x0106h	Device Header Register (CF_DRV_HD)	00h
E.9	0x0107h	Command Register (Write Only) (CF_CMD_REG)	-
E.10	0x0107h	Status Register (Read Only) (CF_STAT)	00h
E.11	0x010Eh	Device Control Register (Write Only) (CF_DEVICE_CTL)	-
E.12	0x010Eh	Alternate Status Register (Read Only) (CF_ALSTAT)	00h
E.13	0x010Fh	Drive Address Register (Read Only)	00h
Top Register			
E.14	0x0120h	Disk Interrupt Control Register (DINCTCL)	00h
E.15	0x0121h	Disk Interrupt Reason Register (DINTRSN)	00h
E.16	0x0122h	System Control Register (SYS_CTL)	00h
E.17	0x0123h	Storage & Host to Buffer Direction / FLASH ECC Status Register (BD_ECCTL)	00h
E.18	0x0124h	MMCIO Control Register (MMCIO_CTL)	F5h
E.19	0x0125h	Buffers Direction/Status Register (BD_ST)	08h

E.20	0x0126h	IDE Control Register (STO_CTL)	E0h
E.21	0x0127h	USB Control Register (USBIDE_CTL)	C8h
E.22	0x0128h	XTALOUT Frequency Control Register (XTALOUT_CTL)	80h
E.23	0x0129h	MP3/ADPCM Control Register (DEBUG_REG)	14h
E.24	0x012Ah	MP3/ADPCM Control Register (MP3_ADPCM_CTL)	14h
E.25	0x012Bh	MP3 Frequency Control \ ADPCM Data Bit Rate Control Register (MP3ADPCMCLK)	01h
E.26	0x012Ch	ADPCM Synchronize Register (Frame syncs 8Khz) (ADPCMCLK2)	FFh
E.27	0x012Dh	ADPCM Data Register (ADPCM_DAT_REG)	00h
E.28	0x012Eh	Card Detect Direct Register (CARDDETECT)	27h
E.29	0x012Fh	CPU Clock Wake Up Counter Register (WAKE_CNT)	41h
A Buffer Register			
E.30	0x0130h	Sector A Buffer Access Low Byte Register (ABUFL)	FFh
E.31	0x0131h	Sector A Buffer Access High Byte Register (ABUFH)	FFh
E.32	0x0132h	A Buffer Device Address Pointer Register (DAP Low 8 Bits) (ADAPL)	01h
E.33	0x0133h	A Buffer Device Address Pointer Register (DAP High 3 Bits) (ADAPH)	00h
E.34	0x0134h	A Buffer Host Address Pointer Register (HAP Low 8 Bits) (AHAPL)	00h
E.35	0x0135h	A Buffer Host Address Pointer (HAP High 3 Bits) (AHAPH)	00h
E.36	0x0136h	A Buffer Host Stop Pointer Register (HSP Low 8 Bits) (AHSPL)	FFh
E.37	0x0137h	A Buffer Host Stop Pointer Register (HSP High 3 Bits) (AHSPH)	00h
E.38	0x0138h	A Buffer Control Register (ABUF_CTL)	04h
Flash -- SmartMedia Register			
E.39	0x0140h	Flash Manufacturer Code Register (Read Only)	00h
E.40	0x0141h	Flash Device ID code Register (Read Only)	00h
E.41	0x0142h	Flash Command Register (Write Only)	-
E.42	0x0143h	Flash Start Address 0 Register (Write Only)	-

E.43	0x0144h	Flash Start Address 1 Register (Write Only)	-
E.44	0x0145h	Flash Start Address 2 Register (Write Only)	-
E.45	0x0146h	Flash Start Address 3 Register for 64,128 MB (Write Only)	-
E.46	0x0147h	Flash Sequencer Control Register	29h
E.47	0x0148h	Flash Control Register	1fh
E.48	0x0149h	Flash Direct Buffer Access Control Register	00h
E.49	0x014Ah	Flash Data Read/Write Count Low Byte Register	00h
E.50	0x014Bh	Flash Data Read/Write Count High Byte Register	20h
E.51	0x014Ch	Flash Memory Status Register (Read Only)	00h
E.52	0x014Dh	Flash CLK/MMC Clock Frequency Control Register	00h
E.53	0x014Eh	Flash LBA_L Register	00h
E.54	0x014Fh	Flash LBA_H Register	00h
MMC Register, Address is the Same as Flash Address			
E.55	0x0140h	CRCCode Res.ARG Register	unknown
E.56	0x0141h	CRCCode Encode Register	unknown
E.57	0x0142h	MMC Res.CMN ARG Register	00h
E.58	0x0143h	MMC Res ARG.0 Register	00h
E.59	0x0144h	MMC Res ARG.1 Register	00h
E.60	0x0145h	MMC Res ARG.2 Register	00h
E.61	0x0146h	MMC Res ARG.3 Register	00h
E.62	0x0148h	MMC Control Register1 (MMC_CTL1)	1f h
E.63	0x0149h	MMC Control Register2 (MMC_CTL2)	00h
E.64	0x014Bh	MMC Control Register3 (MMC_CTL3)	00h
E.65	0x014Eh	DAT CRCCode Low Byte Register (Read Only)	00h
E.66	0x014Fh	DAT CRCCode High Byte Register (Read Only)	00h

External RAM/Buffer Register			
E.67	0x0150h	Sector Buffer Data (Byte) Access Register (RAMBUF)	FFh
E.68	0x0152h	Device Address Pointer Register (DAP Low 8 Bits) (RAMDAPL)	00h
E.69	0x0153h	Device Address Pointer Register (DAP High 8 Bits) (RAMDAPH)	00h
E.70	0x0154h	Buffer Control Register (RAM_CTL)	00h
B Buffer Register			
E.71	0x0160h	Sector B Buffer Access Low Byte Register (BBUFL)	FFh
E.72	0x0161h	Sector B Buffer Access High Byte Register (BBUFH)	FFh
E.73	0x0162h	B Buffer Device Address Pointer Register (DAP Low 8 Bits) (BDAPL)	00h
E.74	0x0163h	B Buffer Device Address Pointer Register (DAP High 1 Bits) (BDAPH)	00h
E.75	0x0164h	B Buffer Host Address Pointer Register (HAP Low 8 Bits) (BHAPL)	00h
E.76	0x0165h	B Buffer Host Address Pointer Register (HAP High 2 Bits) (BHAPH)	00h
E.77	0x0166h	B Buffer Host Stop Pointer Register (HSP Low 8 Bits) (BHSPL)	FFh
E.78	0x0167h	B Buffer Host Stop Pointer Register (HSP High 2 Bits (BHSPH)	00h
E.79	0x0168h	B Buffer Control Register (BBUF_CTL)	04h
USB Interface Register			
E.80	0x0180h	USB Control Register (UCR)	08h
E.81	0x0181h	USB Pulse Control Register (UPCR)	00h
E.82	0x0182h	Endpoint 0 Received Packet Size Register (Read Only) (EP0PSR)	00h
E.83	0x0183h	Endpoint 0 Data Output Register (Write Only) (EP0DOR)	-
E.84	0x0183h	Endpoint 0 Data Input Register (Read Only) (EP0DIR)	24h
E.85	0x0184h	Endpoint 3 Data Output Register (Write Only) (EP3DOR)	-
E.86	0x0185h	USB Return Trigger Register (URTR)	00h
E.87	0x0186h	USB Address Register (UAR)	00h
E.88	0x0187h	Interrupt Enable Register (IER)	00h

E.89	0x0188h	Interrupt Source Register (Read Only) (ISR)	00h
E.90	0x0189h	Extended Interrupt Enable Register (EIER)	00h
E.91	0x018Ah	Extended Interrupt Source Register (Read Only) (EISR)	00h
E.92	0x018Bh	FIFO Clear Register (FCR) (Write Only)	-
E.93	0x018Ch	FIFO Status Register (Read Only) (FSR)	FBh
E.94	0x018Dh	Mode Select Register (MSR)	00h
E.95	0x018Eh	Draft/Memory Data Register (DMDR)	FFh
E.96	0x018Fh	End Point Address Register 1 (EPAR1)	21h
E.97	0x0190h	End Point Address Register 2 (EPAR2)	03h
E.98	0x0191h	FIFO Address Register (FAR)	00h
Internal MOVX RAM Address (6K Bytes)			
E.99	0x1000h- 0x27FFh	Internal MOVX RAM	00h

E.a REGISTER DESCRIPTION:

◆HOST IDE I/O INTERFACE (0x010Xh)

E.1: Data Register (CF_DATA), Address: 0x0100h, Access: R/W

DIRECTION - This register is bi-directional for the drive and host.

ACCESS RESTRUCTIONS - This register can be written or the contents is valid on read when DRQ is set to one.

FUNCTIONAL DESCRIPTION - The data register is 16-bit wide.

BIT DESCRIPTION -

15	14	13	12	11	10	9	8
Data (15:8)							

7	6	5	4	3	2	1	0
Data (7:0)							

E.2: Feature Register (CF_FEATURE), Address: 0x0101h, Access: Write Only

DIRECTION - This register is write-only by host.

ACCESS RESTRICTION - This register is write-only when BSY and DRQ are both equal to zero.

FUNCTIONAL DESCRIPTION - This register is command specific.

BIT DESCRIPTION -

7	6	5	4	3	2	1	0
Command specific							

E.3: Error Register (CF_ERR_REG), Address: 0x0101h, Access: Read Only

DIRECTION - This register is read-only by host.

ACCESS RESTRICTION - The contents of this register shall be valid when BSY and DRQ are equal to zero and ERR is asserted.

FUNCTIONAL DESCRIPTION - This register contains the operation status for the current command.

BIT DESCRIPTION -

7	6	5	4	3	2	1	0

Reserves	UNC	MC	IDNF	MCR	ABRT	TKONF	AMNF

Bit 7 Reserved.

Bit 6 UNC (Uncorrectable Data Error) indicate an uncorrectable data error has been encountered;

Bit 5 MC (Media Change) is used by removable media devices.

Bit 4 IDNF (ID Not Found) indicates the requested sector's ID field could not be found;

Bit 3 MCR (Media Change Requested) is used by removable media devices.

Bit 2 ABRT (Aborted Command) indicates the requested command has been aborted because the command code or a command parameter is invalid or some other error has occurred.

Bit 1 TKONF (Track 0 Not Found) indicates the track 0 has not been found during a RECALIBRATE command;

Bit 0 AMNF (Address Mark Not Found) indicates the data address mark has not been

E.4: Sector Count Register (CF_SEC_CNT), Address: 0x0102h, Access: R/W

DIRECTION - This register is bi-directional for the drive and host.

ACCESS RESTRICTION - This register is write-only when BSY and DRQ are both equal to zero.

FUNCTIONAL DESCRIPTION - This register contains the number of sector of data requested to be transferred on a read or write operation between the host and the device. If the value in this register is zero, a count of 256 sectors is specified.

BIT DESCRIPTION -

7	6	5	4	3	2	1	0
Sector Count							

E.5: Sector Number Register (CF_SEC_NUM), Address: 0x0103h, Access: R/W

DIRECTION - This register is bi-directional for the drive and host.

ACCESS RESTRICTION - This register is write-only when BSY and DRQ are both equal to zero.

FUNCTIONAL DESCRIPTION - If the LBA bit is cleared to zero in the Device/Head register, this register contains the starting sector number for any media access. If the LBA bit is set to one in the Device/Head register, this register contains Bits 7-0 of the LBA for any media access.

BIT DESCRIPTION -

CHS

7	6	5	4	3	2	1	0

Sector (7:0)

LBA

7	6	5	4	3	2	1	0
LBA (7:0)							

E.6: Cylinder Low Register (CF_CYL_L), Address: 0x0104h, Access: R/W

DIRECTION - This register is bi -directional for the drive and host.

ACCESS RESTRICTION - This register is write-only when BSY and DRQ are both equal to zero.

FUNCTIONAL DESCRIPTION – If the LBA bit is cleared to zero in the Device/Head register, this register contains the low order bits of the starting cylinder address for any media access. If the LBA bit is set to one in the Device/Head register, this register contains Bits 15-8 of the LBA for any media access.

BIT DESCRIPTION -

CHS

7	6	5	4	3	2	1	0
Cylinder (7:0)							

LBA

7	6	5	4	3	2	1	0
LBA (15:8)							

E.7: Cylinder High Register (CF_CYL_H), Address: 0x0105h, Access: R/W

DIRECTION - This register is bi-directional for the drive and host.

ACCESS RESTRICTION - This register is write-only when BSY and DRQ are both equal to zero.

FUNCTIONAL DESCRIPTION - If the LBA bit is cleared to zero in the Device/Head register, this register contains the low order bits of the starting cylinder address for any media access. If the LBA bit is set to one in the Device/Head register, this register contains Bits 23-16 of the LBA for any media access.

BIT DESCRIPTION -

CHS

7	6	5	4	3	2	1	0

Cylinder (7:0)

LBA

7	6	5	4	3	2	1	0
LBA (15:8)							

E.8: Device/Head Register (CF_DRV_HD), Address: 0x0106h, Access: R/W

DIRECTION - This register is bi-directional for the drive and host.

ACCESS RESTRICTION - This register is write-only when BSY and DRQ are both equal to zero.

FUNCTIONAL DESCRIPTION - This register selects the device, defines address translation as CHS or LBA, and provides the head address if CHS mode or LBA (27:24) if LBA mode.

BIT DESCRIPTION -

CHS (cylinder-head-sector)

7	6	5	4	3	2	1	0
1	LBA	1	DEV	HS3	HS2	HS1	HS0

LBA (logic block address)

7	6	5	4	3	2	1	0
1	LBA	1	DEV	LBA (27:24)			

Bit 7 Set to one for backward compatibility;

Bit 6 LBA mode if this bit is set to one, otherwise, CHS mode.

Bit 5 Set to one for backward compatibility;

Bit 4 DEV is the device address. When the DEV bit is equal to zero, Device 0 is selected. When the DEV bit is equal to one, Device 1 is selected.

Bit 3-0 If LBA is equal to zero (CHS), these contain the head address of the starting CHS address. The HS3 bit is the most significant bit. If LBA is equal to one(LBA), these bits represent bits 27 through 24 of the LBA.

E.9: Command Register (CF_CMD_REG), Address: 0x0107h

DIRECTION - This register is write-only by host.

ACCESS RESTRICTION - This register is write-only when BSY and DRQ are both equal to zero. The contents of this register and all other Command Block registers are not valid while a device is in the Sleep mode.

FUNCTIONAL DESTRIPTION - This register contains the command code being sent to the device. Command execution begins immediately after this register is written.

BIT DESCRIPTION

7	6	5	4	3	2	1	0
Command Code							

E.10: Status Register (CF_STAT), Address: 0x0107h, Access: Read Only

DIRECTION -This register is read-only by host.

ACCESS RESTRICTION - The contents of this register, except for BSY, will be ignored when BSY is set to one. BSY is valid at all time. The contents of the register and all other Command Block registers are not valid while a device is in the Sleep mode.

FUNCTIONAL DESCRIPTION - This register contains the device status. The contents of this register are updated to reflect the current state of the device and the progress of any command being executed by the device.

BIT DESCRIPTION

7	6	5	4	3	2	1	0
BSY	DRDY	DF	DSC	DRQ	CORR	IDX	ERR

Bit 7 BSY (Busy) is set whenever the device has control of the command Block Registers. When the BSY bit is equal to one, writing commands to this register will be ignored

Bit 6 DRDY (Device Ready) is set to indicate that the device is capable of accepting all command codes. This bit shall be cleared at power on.

Bit 5 DF (Device Fault) indicates a device fault error has been detected. The internal status or internal conditions that causes this error to be indicated is vendor specific.

Bit 4 DSC (Device Seek Complete) indicates that the device heads are settled over a track.

Bit 3 DRQ (Data Request) indicates that the device is ready to transfer a word or byte between the host and the device.

Bit 2 CORR (Corrected Data) is used to indicate a correctable data error. The definition of what constitutes a correctable error is vendor specific.

Bit 1 IDX (Index) is vendor specific.

Bit 0 ERR (Error) indicates that an error occurred during execution of the previous command. The bits in the Error register have additional information regarding the cause of the error.

E.11: Device Control Register (CF_DEVICE_CTL), Address: 0x010Eh

This register is used to control the CompactFlash Memory Card interrupt request and to issue an ATA soft reset to

the card. The bits are defined as follows:

7	6	5	4	3	2	1	0
X	X	X	X	1	SW Rst	-IEn	0

Bit 7 This bit is an X (don't care).

Bit 6 This bit is an X (don't care).

Bit 5 This bit is an X (don't care).

Bit 4 This bit is an X (don't care).

Bit 3 This bit is ignored by the CompactFlash Memory Card.

Bit 2 (SW Rst) This bit is set to 1 in order to force the CompactFlash Memory Card to perform an AT Disk controller Soft Reset operation. This does not change the PCMCIA Card Configuration Registers (4.3.2 to 4.3.5) as hardware Reset does. The Card remains in Reset until this bit is reset to '0'.

Bit 1 (-IEn) The Interrupt Enable bit enables interrupts when the bit is 0. When the bit is 1, interrupts from the CompactFlash Memory Card are disabled. This bit also controls the Int bit in the Configuration and Status Register. This bit is set to 1 at power on and Reset.

Bit 0 This bit is ignored by the CompactFlash Memory Card.

E.12: Alternate Status Register (CF_ALSTAT), Address: 0x010Eh, Access: Read Only

This register description are same as Status Register.

E.13: Drive Address Register (Read Only), Address: 0x010Fh, Access: Read Only

◆TOP REGISTER (0x012Xh)

E.14: Disk Interrupt Control Register (DINTCTL), Address: 0x0120h, Access: R/W

Bit 7 0: Host Write Command Enable.

1: Host Write Command Disable.

Bit 6 0: Host SRST Enable.

1: Host SRST Disable.

Bit 5 0: USB Interrupt Enable.

1: USB Interrupt Disable.

BIT4 0: MP3Data Request/ ADPCM Data Full Interrupt Enable.

1: MP3Data Request/ ADPCM Data Full Interrupt Disable.

Bit 3 0: External uP4BITINT Input Enable.

1: External uP4BITINT Input Disable.

Bit 2 0: Direct CF/IDE Interrupt Pin Enable.

1: Direct CF/IDE Interrupt Pin Disable.

Bit 1 0: ADPCM Data Require Interrupt Enable.

1: ADPCM Data Require Interrupt Disable.

Bit 0 0: SM/CF/MMC Card Insert/Remove Interrupt Enable.

1: SM/CF/MMC Card Insert/Remove Interrupt Disable.

E.15: Disk Interrupt Reason Register (DINTRSN), Address: 0x0121h, Access: R/W

Bit 7 1: Host Write Command Interrupt Flag.

Bit 6 1: HOST SRST Interrupt Flag.

Bit 5 1: USB Interrupt Flag.

BIT4 1: MP3Data Request/ ADPCM Data Full Interrupt Flag.

Bit 3 1: EXTERNAL uP4BIT Interrupt Input Flag.

Bit 2 1: DIRECT CF/IDE Interrupt PIN Flag.

Bit 1 1: ADPCM DATA Require Interrupt Flag.

Bit 0 1: SM/CF/MMC Card Insert/Remove Interrupt Flag.

E.16: System Control Register (SYS_CTL), Address: 0X0122h, Access: R/W

Bit 7 0: PLL Disable (When USB disable, system run on 12MHz clock).

1: PLL Enable.

Bit 6 CPU Clock Select,

0: CLK48MHz.

1: XTAL_12MHz.

Bit 5 0: Else No Divide.

1: Input Clock Source Divide 2.

Bit 4 CLK48MHz for External USB (SIE & SIL) Circuit:.

0: Enable.

1: Disable.

Bit 3 Clock to Circuit Host.

0: Enable.

1: Disable.

Bit 2 Clock to Circuit USB.

0: Enable.

1: Disable.

Bit 1 Clock to Circuit Buffer.

0: Enable.

1: Disable.

Bit 0 Standby Mode Set.

1: Enable. All circuit clock source will be disable.

0: Disable.

E.17: Storage &Host to Buffer Direction / FLASH ECC Status Register (BD_ECCTL), Address: 0x0123h Access: Read Only

Bit 7 (Read Only) 0 Storage (CF, SM, MMC) Direct To Buffer A.

1 Storage (CF, SM, MMC) Direct To Buffer B.

Bit 6 (Read Only) 0 Device (USB, PP) Direct To Buffer A.

1 Device (USB, PP) Direct To Buffer B.

Bit 5 (Read Only) 0 Device (MP3) Direct To Buffer A.

1 Device (MP3) Direct To Buffer B.

Bit 4 (Read Only) SM ECC Done.

1: SM ECC Error.

0: SM ECC No Error.

Bit 3 (Read Only) SM Error Correct 2

Bit 1 (Read Only) SM Double Error 1.

1: With Error.

Bit 0 (Read) SM Error Correct 1.

(Write) Set the BUFFER(A/B) Valid with Bit(0)

E.18: MMC Control Register (MMCIO_CTL), Address: 0x0124h, Access: R/W

Bit 7(R) MMCCMDIn Pin Status.

Bit 6(R) MMCDATIn Status.

Bit 5 1: CF_nRD, CF_nWE, CF_nCS1, CF_nCS2 to High-Z.

Bit 4 Direct Out MMC Data Pin.

1: MMC Data Pin will be Output H.

0: MMC Data Pin will be Output L.

Bit 3 MMC Data Pin Output Gate Control.

1: Enable Output.

0: Disable Output.

Bit 2 Direct Out MMC Command Pin.

1: MMC Command Pin will be Output H.

0: MMC Command Pin will be Output L.

Bit 1 MMC Command Pin Output Gate Control.

1: Enable Output.

0: Disable Output.

Bit 0 Direct Out MMC Clock Pin.

1: MMC Clock Pin will be Output H.

0: MMC Clock Pin will be Output L.

E.19: Buffers Direction/Status Register (BD_ST), Address: 0x0125h, Access: R/W

Bit 7 0: uP External RAM.

1: Direct to FLASH/CF/MMC.

Bit 6 Reserved.

Bit 5 0: Flash Direct To Buffer A.

1: Flash Direct To Buffer B.

Bit 4 0: Host (USB/IDE) Direct To Buffer A.

1: Host (USB/IDE) Direct To Buffer B.

Bit 3 1: Force MP3_DAT & Buffer A/B Direction.

Bit 2 0: MP3_DAT Direct To Buffer A.

1: MP3_DAT Direct To Buffer B.

Bit 1 1: B Buffer Data Valid/Ready.

Bit 0 1: A Buffer Data Valid/Ready.

E.20: IDE Control Register (STO_CTL), Address: 0x0126h, Access: R/W

Bit 7 0: Extend 1 (ADPCM) Card Detect Pin Enable.

1: Extend 1 (ADPCM) Card Detect Pin Disable.

Bit 6 0: Extend 2 (ADPCM) Card Detect Pin Enable.

1: Extend 2 (ADPCM) Card Detect Pin Disable.

Bit 5 0: Extend 3 (ADPCM) Card Detect Pin Enable.

1: Extend 3 (ADPCM) Card Detect Pin Disable.

Bit 4 0: IDE 8Bits Transfer Mode Select.

1: Else 16Bits.

Bit 3~2

"11" CPU Interface Select;

"10" MMC Interface Select;

"01" IDE Interface Select;

"00" SM Interface Select;

Bit 1 IDE Read'1'/Write'0' Direction.

Bit 0 Set IDE Direct Buffer Transfer '1'.

E.21: USB Control Register (USBIDE_CTL), Address: 0x0127h, Access: R/W

Bit 7 HnDASP_I.

Bit 6 HnPDIAG_I.

Bit 5 HnDASP_noe.

Bit 4 HnPDIAG_noe.

Bit 3 USB_RST

1: Reset USB (SIE & SIL).

0: Enable USB (SIE & SIL).

Bit 2 Host either USB or IDE select

1: IDE Interface Select.

0: USB Interface Select.

Bit 1 Device IDE/USB R/W Direction.

1: Read.

0: Write.

Bit 0 1: Set IDE Direct Buffer Transfer

0: Set USB Direct Buffer Transfer

E.22: XTALOut Frequency Control (XTALOUT_CTL), Address: 0x0128h, Access: R/W

BIT 7 Clock Out Enable.

0: Enable.

1: Disable.

BIT 6 System Clock Select.

1: Select system clock.

0: Setting by bit (6~0).

BIT 5~0 Base Of 25 MHz:

"0000000": 12.500 MHz -- 80ns

"0000001": 06.250 MHz --160ns

"0000011": 03.125 MHz --320ns

E.23: MP3/ADPCM Control Register (DEBUG_REG), Address: 0x0129h, Access: R/W

Bit (7~5) MMC CMD/DAT I/O Bus Select:

0XX -> Default MMC Bus.

100 -> CF_DIO(1):MMC_CMD; CF_DIO(0):MMC_DAT;

101 -> CF_DIO(3):MMC_CMD; CF_DIO(2):MMC_DAT;

110 -> CF_DIO(5):MMC_CMD; CF_DIO(4):MMC_DAT;

111 -> CF_DIO(7):MMC_CMD; CF_DIO(6):MMC_DAT;

Bit 4 Reserved.

Bit 3 Reserved.

Bit 2 PADPCMDTx Signal out (use as I/O pin).

Bit 1 PADPCMSync Signal out (use as I/O pin).

Bit 0 PADPCMCLK Signal out (use as I/O pin).

E.24: MP3/ADPCM Control Register (MP3_ADPCM_CTL), Address: 0x012Ah, Access: R/W

Bit 7 MP3_StartPlay

1: Enable,

0: Disable.

Bit 6 Reserved.

Bit 5 1: MP3 I2S Falling Edge output,

0: MP3 I2S Rising Edge output,

Bit 4 1: MP3 DRQ High Active.

0: Low Active.

Bit 3 1: MP3 Data Byte Unit.

0: MP3 Data Bit Unit.

Bit 2 MP3 Data Output Gate.

1: Enable Output.

0: Disable Output.

Bit 1 1: TL7230MD HIP Select.

0: ADPCM Interface.

Bit 0 MMC Card Detect PIN Enable.

0: Enable.

1: Disable.

E.25: MP3 Frequency Control \ ADPCM Data Bit Rate Control Register (MP3ADPCMCLK)

Address: 0x012Bh, Access: R/W

Bit 7 ADPCM Enable.

1: Enable,

0: Disable.

Bit 6~4 ADPCM Sample Bit Number (1~8)

Bit 3~0 Base Of CLK MHz:

"0000": (CLK/2)/2 MHz

"0001": (CLK/4)/2 MHz

"0011": (CLK/6)/2 MHz

"XXXX": (CLK/(2*n+2))/2 MHz

For ADPCM: 128KHz ~ 2MHz Clock Gen

E.26: ADPCM Synchronizes Register (ADPCMCLK2) (frame syncs 8Khz)

Address: 0x012Ch, Access: R/W

BIT 7~0 Base Of ADPCM Data Bit Rate Frequency:

"000": CLK/2 MHz

"001": CLK/4 MHz

"011": CLK/6 MHz

"XXX": CLK/(2*n+2) MHz

E.27: ADPCM Data Register (ADPCM_DAT_REG), Address: 0x012Dh, Access: R/W

E.28: Card Detect Direct Register (CARDDETECT), Address: 0x012Eh, Access: R/W

Bit 7 TLI_nGTB:

1: PADPCMDTx Input.

0: Output Mode.

Bit 6 TLI_nGTA:

1: PADPCMSync, PADPCMCLK Input.

0: Output Mode.

Bit 5 PADPCMCLK. Use As I/O When ADPCM _Disable In ADPCM Mode.

Bit 4 PADPCMSync. Use As I/O When ADPCM _Disable In ADPCM Mode.

Bit 3 PADPCMDTx. Use As I/O When ADPCM_Disable In ADPCM Mode.

Bit 2(R) PADPCMDRx.

Bit 1(R) CF_nCD, set to “Hi” when Compact Flash Card is inserted.

Bit 0(R) SMnFCD set to “Hi” when Smart Media Card is inserted.

E.29: CPU Clock Wake Up Counter Register (WAKE_CNT), Address: 0x012Fh, Access: R/W,

Bit 7~0 De-glitch Counter When Crystal Start.

Bit 1 Disable "CUT CLK" Function '1'.

Bit 0 Disable CLK input Gate '0'.

◆ **A Buffer Register (0x013Xh)**

E.30: Sector A Buffer Access Low Byte (ABUFL), Address: 0x0130h, Access: R/W

E.31: Sector A Buffer Access High Byte (ABUFH), Address: 0x0131h, Access: R/W

E.32: A Buffer Device Address Pointer (DAP Low 8 Bits) Register (ADAPL)

Address: 0x0132h, Access: R/W

E.33: A Buffer Device Address Pointer (DAP High 3 Bits) Register (ADAPH)

Address: 0x0133h, Access: R/W

Bit 7~3(R) Reserved

Bit 2~0 Bit [2..0] Map To The Bit [10..8].

E.34: A Buffer Host Address Pointer (HAP Low 8 Bits) Register (AHAPL)

Address: 0x0134h, Access: R/W

E.35: A Buffer Host Address Pointer (HAP High 3 Bits) Register (AHAPH)

Address: 0x0135h, Access: R/W

Bit 7~3(R) Reserved

Bit 2~0 Bit [2..0] Map To The Bit [10..8].

E.36: A Buffer Host Stop Pointer (HSP Low 8 Bits) Register (AHSPL)

Address: 0x0136h, Access: R/W

E.37: A Buffer Host Stop Pointer (HSP High 3 Bits) Register (AHSPH)

Address: 0x0137h, Access: R/W

Bit 7~3(R) Reserved

Bit 2~0 Bit [2..0] Map To The Bit [10..8].

E.38: A Buffer Control Register (ABUF_CTL), Address: 0x0138h, Access: R/W

Bit 7~4 Reserved

Bit 3 1: Enable RAM A Buffer (nBCS);

0: Disable RAM A Buffer.

Bit 2 1: Enable AUTO_DAP (Disk Address Pointer)

0: Disable

Bit 1 1: Enable Auto Preset HAP (Host Address Pointer).

0: Disable

Bit 0 1: Enable AUTO_HAP

0: Disable

◆Flash -- SmartMedia Register (0x014Xh)

E.39: Flash Manufacturer Code Register, Address: 0x0140h, Access: Read Only

E.40: Flash Device ID code Register, Address: 0x0141h, Access: Read Only

E.41: Flash Command Register, Address: 0x0142h, Access: Write Only

E.42: Flash Start Address 0 Register, Address: 0x0143h, Access: Write Only

E.43: Flash Start Address 1 Register, Address: 0x0144h, Access: Write Only

E.44: Flash Start Address 2 Register, Address: 0x0145h, Access: Write Only

E.45: Flash Start Address 3 Register for 64,128 Mbyte, Address: 0x0146h, Access: Write Only

E.46: Flash Sequencer Control Register, Address: 0x0147h, Access: R/W

Bit 7(R/W 1) FSEQ(7) : SDATA 8 Bytes Address When Do_ECC GET BUFFER DATA.

Bit 6(R/W 0) FSEQ(6) : SEL_AC(FCMD)=> ADDRESS "1",COMMAND "0".

Bit 5(R/W 1) FSEQ(5) : Direct map SM'PIN nFCE

Bit 4(R/W 0) FSEQ(4) : MMCnRFSlt : “0” MMC ROM TYPE SELECT

“1” MMC FLASH TYPE SELECT

Bit 3(R/W 0) FSEQ(3) : SoftReset MMC_TOP '0'.

Bit 2(R 1) FSEQ(2) : Reserved.

Bit 1(R 1) FSEQ(1) : Reserved.

Bit 0(R 0) FSEQ(0) : FRDY Status.

E.47: Flash Control Register, Address: 0x0148h, Access: R/W

Bit 7(R/W 0) FCTL(7): nFRST

Bit 6(R/W 0) FCTL(6): nWP

Bit 5(R/W 0) FCTL(5): ADD_SET,MORE THEN 32MBYTE "1", OTHER ELSE "0";

Bit 4(R/W 1) FCTL(4): SPR_MOV "1" ENABLE / "0" DISABLE

Bit 3(R/W 1) FCTL(3): ECC_Ena

Bit 2(R/W 1) FCTL(2): AUTO_ECC_CLR

Bit 1(R/W 1) FCTL(1): P512D

Bit 0(R/W 1) FCTL(0): DATA_SEL "1" ENABLE / "0" DISABLE (512 BYTE/PAGE)

E.48: Flash Direct Buffer Access Control Register, Address: 0x0149h, Access: R/W

Bit 7(R/W 0) FDBACTL(7): FERASE "1" ENABLE / "0" DISABLE

Bit 6(R/W 1) FDBACTL(6): FW_RDIR "0" write / "1"read

Bit 5(R/W 0) FDBACTL(5): PAGE_256. READ FLASH 256 ODD PAGE: SET "1" TO ENABLE SIGNAL DO_ECC

Bit 4(R/W 0) FDBACTL(4): SET_RID

Bit 3(R/W 0) FDBACTL(3): SET_RSTATE

Bit 2(R/W 0) FDBACTL(2): SET_FCMD

Bit 1(R/W 0) FDBACTL(1): SET_FACMD

Bit 0(R/W 0) FDBACTL(0): SET_FDBA

E.49: Flash Data Read/Write Count Low Byte Register, Address: 0x014Ah, Access: R/W

E.50: Flash Data Read/Write Count High Byte Register, Address: 0x014Bh, Access: R/W

Bit 1,0(R/W) BIT 1~0(00) : Bit[1..0] Map To The Bit[9..8] Of Flash Read/Write Count High Register

E.51: Flash Memory Status Register, Address: 0x014Ch, Access: Read Only

E.52: Flash CLK/MMC Clock Frequency Control Register, Address: 0x014Dh, Access: R/W

Bit 7 BIT 7 (1) : "0" SYS_CLK, "1" setting by bit(6~0);

Bit 6~0 BIT 6~0 “1111111”: BASE OF 25 MHz:

"0000000": 12.500 MHz -- 80ns

"0000001": 06.250 MHz --160ns

"0000011": 03.125 MHz --320ns

E.53: Flash LBA_L Register, Address: 0x014Eh, Access: R/W

E.54: Flash LBA_H Register, Address: 0x014Fh, Access: R/W

◆MMC Register, Address is the Same as Flash Address

E.55: CRCCode Res.ARG Register, Address: 0x0140h, Access: R/W

E.56: CRCCode Encode Register, Address: 0x0141h, Access: R/W

E.57: MMC Res.CMN ARG Register, Address: 0x0142h, Access: R/W

E.58: MMC Res ARG.0 Register, Address: 0x0143h, Access: R/W

E.59: MMC Res ARG.1 Register, Address: 0x0144h, Access: R/W

E.60: MMC Res ARG.2 Register, Address: 0x0145h, Access: R/W

E.61: MMC Res ARG.3 Register, Address: 0x0146h, Access: R/W

E.62: MMC Control Register1 (MMC_CTL1), Address: 0x0148h, Access: R/W

Bit 5(R/W 0) ‘1' MMC CMDFSM output 8 CLK after CMD finish transfer (CMDNoResFlag)

Bit 4(R/W 0) '1' MMC CMDFSM Get Response Enable ELSE '0' DISABLE Get Response

Bit 3(R/W 0) '1' MMC CMDFSM Will be Start when DAT_FSM Set

Bit 2(R/W 0)' '1' MMC DATFSM Get Response Only.

Bit 1(R/W 0) '1' MMC DATFSM CRC Check Enable '1' ELSE '0' Disable;

Bit 0(R/W 0) '1' MMC DATFSM Read/'0'Write DIRECTION;

E.63: MMC Control Register2 (MMC_CTL2), Address: 0x0149h, Access: R/W

Bit 7(R/W 0) STREAM MODE ACCESS '1' ELSE '0';

DAT_FSM DO NOT OUTPUT StartAck'0' when Write.

DAT_FSM DO NOT WAIT MMC OUTPUT StartAck'0' when Read

Bit 6(R/W 0) '1' MMC CMDFSM Get SPRegister, CID, CSD

Bit 5(R/W 0) '1' MMC CMDFSM Get Response Only

E.64: MMC Control Register3 (MMC_CTL3), Address: 0x014Bh, Access: R/W

Bit 7(R/W) BIT 7(1) : CLK to circuit flh_top.vhd/ecc_top.vhd: ENA(0)\DIS(1);

Bit 6(R/W) BIT 6(1) : CLK to circuit mmc.vhd : ENA(0)\DIS(1);

Bit 5(R/W) BIT 5(0) : TRIGGER MMC CMDFSM Data Transfer START '1'.

Bit 4(R) BIT 4(0) : CMD CRC Check, '1' Error, '0' Data O.K.

Bit 3(R/W) BIT 3(0) : TRIGGER MMC DATFSM Data Transfer START '1'.

Bit 2(R) BIT 2(0) : DAT CRC Check, '1' Error, '0' Data O.K.

E.65: DAT CRCCode Low Byte Register, Address: 0x014Eh, Access: Read Only

E.66: DAT CRCCode High Byte Register, Address: 0x014Fh, Access: Read Only

◆Buffer Related Register (0x15Xh)

E.67: Sector Buffer Data (Byte) Access (RAMBUF), Address: 0x0150h, Access: R/W

E.68: Device Address Pointer (DAP Low 8 Bits) Register (RAMDAPL)

Address: 0x0152h, Access: R/W, Default: 00H

E.69: Device Address Pointer (DAP High 8 Bits) Register (RAMDAPH)

Address: 0x0153h, Access: R/W, Default: 00H

E.70: Buffer Control Register (RAM_CTL)

Address: 0x0154h, Access: R/W, Default: 00H

Bit 7~4 Reserved

Bit 3 1: Enable RAM Buffer (nBCS);

0: Disable

Bit 2 1: Enable AUTO_DAP

0: Disable

Bit 1 Reserved

Bit 0 Reserved

◆B Buffer Register (0x016Xh)

E.71: Sector B Buffer Access Low Byte (BBUFL), Address: 0x0160h, Access: R/W

E.72: B Buffer Sector Buffer Access High Byte (BBUFH)

Address: 0x0161h, Access: R/W

E.73: B Buffer Device Address Pointer (DAP Low 8 Bits) Register (BDAPL)

Address: 0x0162h, Access: R/W

E.74: B Buffer Device Address Pointer (DAP High 1 Bits) Register (BDAPH)

Address: 0x0163h, Access: R/W

Bit 7~1(R) Reserved

Bit 0 Bit [0] Map To The Bit [8].

E.75: B Buffer Host Address Pointer (HAP Low 8 Bits) Register (BHAPL)

Address: 0x0164h, Access: R/W

E.76: B Buffer Host Address Pointer (HAP High 2 Bits) Register (BHAPH)

Address: 0x0165h, Access: R/W

Bit 7~2(R) Reserved

Bit 1~0 Bit [1..0] Map To The Bit [9..8].

E.77: B Buffer Host Stop Pointer (HSP Low 8 Bits) Register (BHSPL)

Address: 0x0166h, Access: R/W

E.78: B Buffer Host Stop Pointer (HSP High 2 Bits) Register (BHSPH)

Address: 0x0167h, Access: R/W

Bit 7~2(R) Reserved

Bit 1~0 Bit [2..0] Map To The Bit [9..8].

E.79: B Buffer Control Register (BBUF_CTL), Address: 0x0168h, Access: R/W

Bit 7~4 Reserved

Bit 3 1: Enable RAM B Buffer (nBCS).

0: Disable B Buffer.

Bit 2 1: Enable AUTO_DAP (Disk Address Pointer)

0: Disable

Bit 1 1: Enable Auto Preset HAP (Host Address Pointer).

0: Disable

Bit 0 1: Enable AUTO_HAP.

0: Disable

When set to high, relative function is enable. All of the bits are auto-clear. So it does not need to write low to previous programming bit. The following are the definitions of each bit in this register.

◆USB Interface Register (0x018Xh)

E.80: USB Control Register (UCR), Address: 0x0180h, Access: R/W

Bit 7 Endpoint 2 return STALL

1: Return STALL for OUT transaction of Endpoint 2.

0: Back to normal operation.

Bit 6 Endpoint 1 return STALL

1: Return STALL for IN transaction of Endpoint 1.

0: Back to normal operation.

Bit 5 Endpoint 0 return STALL

1: Return STALL for IN/OUT transaction of Endpoint 0.

0: Back to normal operation.

Bit 4 Set Vbus transition polarity

1: If Vbus transition is from low to high, it will generate interrupt.

0: If Vbus transition is from high to low, it will generate interrupt.

Bit 3 Force SE0 (Single End 0) on D+ and D-

1: Force SE0 on D+ and D-, D+ and D- will be force to “Low”

0: D+ and D- back to normal tri-state.

Bit 2 Chip suspend enable

1: Force the chip to enter suspend mode.

0: Disable suspend mode.

Bit 1 Endpoint 2 DMA enable

1: Enable Endpoint 2 DMA transfer.

0: Disable Endpoint 2 DMA transfer.

Bit 0 Endpoint 1 DMA Enable

1: Enable Endpoint 1 DMA transfer.

0: Disable Endpoint 1 DMA transfer.

E.81: USB Pulse Control Register (UPCR), Address: 0x0181h, Access: R/W

Bit 7 Reserved

Bit 6 Reserved

Bit 5 Reserved

Bit 4 Reserved

Bit 3 Clear Endpoint 2 sequence bit

1: It will clear the sequence bit of Endpoint 2 to be DATA0.

0: No operation

Bit 2 Clear Endpoint 1 sequence bit

1: It will clear the sequence bit of Endpoint 1 to be DATA0.

0: No operation

Bit 1 Remote wakeup trigger

1: The chip will assert a resume signal on USB bus.

0: No operation.

Bit 0 Software reset

1: This chip will generate a self-reset. The function is same as RESET pin active except uc interface. But the USB address register will be cleared. The other functions of this chip will return initial state

0: No operation.

E.82: Endpoint 0 Received Packet Size Register (EP0PSR), Address: 0x0182h, Access: Read only,

uC read this register to get Endpoint 0 data packet size when host issues a OUT transaction only.

E.83: Endpoint 0 Data Output Register (EP0DOR), Address: 0x0183h, Access: Write only

uC write Endpoint 0 data to respond the data packet to host. Bit 7 is MSB.

E.84: Endpoint 0 Data Input Register (EP0DIR), Address: 0x0183h, Access: Read only

uC read Endpoint 0 data packet from USB through this register.

E.85: Endpoint 3 Data Output Register (EP3DOR), Address: 0x0184h, Access: Write only

uC write Endpoint 3 data to respond the data packet to host. Bit 7 is MSB.

E.86: USB Return Trigger Register (URTR), Address: 0x0185h, Access: R/W

Bit 7 Endpoint 3 return STALL

1: Return STALL for IN transaction of Endpoint 3.

0: No operation

Bit 6 Endpoint 3 return DATA

1: Return DATA packet for IN transaction of Endpoint 3.

0: No operation

Bit 5 Select DATA0/DATA1 PID of Endpoint 3

1: Select DATA1 PID of Endpoint 3. This bit is not auto-cleared.

0: Select DATA0 PID of Endpoint 3

Bit 4 Reserved

Bit 3 Select DATA0/DATA1 PID of Endpoint 0

1: Select DATA1 PID of Endpoint 0. This bit is not auto-cleared.

0: Select DATA0 PID of Endpoint 0

Bit 2 Endpoint 0 return DATA

1: Return DATA packet for IN transaction of Endpoint 0.

0: No operation

Bit 1 Endpoint 0 return STALL

1: Return STALL for IN or OUT transaction of Endpoint 0.

0: No operation

Bit 0 Endpoint 0 return ACK

1: Return ACK for OUT transaction of Endpoint 0.

0: No operation

E.87: USB Address Register (UAR), Address: 0x0186h, Access: R/W

When the chip operates under normal mode, the register is USB address register. If the transfer of Set_Address request is complete, uC will write the new device address to bit 6~0 of this register. The chip will recognize the following transactions by the new address value. Bit 6 is MSB.

Bit 7 Not use.

Bit 0~6 USB address.

E.88: Interrupt Enable Register (IER), Address: 0x0187h, Access: R/W

Bit 7 Endpoint 2 enable

1: Device can receive Endpoint 2 packet.

0: Device will ignore Endpoint 2 packet.

Bit 6 Endpoint 1 enable

1: Device can receive Endpoint 1 packet.

0: Device will ignore Endpoint 1 packet.

Bit 5 Endpoint 3 enable

1: Device can receive Endpoint 3 packet.

0: Device will ignore Endpoint 3 packet.

Bit 4 Reserved

Bit 3 Endpoint 1 EOP (End Of Process) interrupt enable

1: When the EOP of DMA is active, the chip will end the DMA request and assert the NINT after the last byte on EOP has been transmitted. If the interrupt of this function has been serviced in autoDMA mode, the chip will start the DMA transfer automatically to request the next block data.

0: Disable the interrupt. Default setting is 0.

Bit 2 Endpoint 3 interrupt enable

1: The chip will assert NINT to uC after host issues a IN token or ACK packet.

0: Disable the interrupt. Default setting is 0.

Bit 1 Vbus transition interrupt enable

1: The chip will assert NINT to uC if the Vbus transition meet the setting.

0: Disable the interrupt. Default setting is zero.

Bit 0 Endpoint 0 interrupt enable

1: The chip will assert NINT to uC after host issues packet to Endpoint 0.

0: Disable the interrupt. Default setting is 0

E.89: Interrupt Source Register (ISR), Address: 0x0188h, Access: Read only

Bit 7 Extended interrupt

1: An extended interrupt exists. uC must read the extended interrupt source register to get the interrupt event.

0: No extended interrupt.

Bit 6 Endpoint 3 IN interrupt

1: Interrupt of Endpoint 3 received IN-token exists. The bit will be set to low after uC read this register.

0: No Endpoint 3 IN interrupt.

Bit 5 Endpoint 3 ACK interrupt

1: Interrupt of Endpoint 3 received ACK-packet exists. The bit will be set to low after uC read this register.

0: No Endpoint 3 ACK interrupt.

Bit 4 Vbus transition interrupt

1: Interrupt of the specified transition of Vbus exits. The bit will be set to low after uC read this register.

0: No transition on Vbus.

Bit 3 Endpoint 0 OUT interrupt

1: Interrupt of Endpoint 0 received OUT-transaction exists. The bit will be set to low after uC read this register.

0: No Endpoint 0 OUT interrupt.

Bit 2 Endpoint 0 IN interrupt

1: Interrupt of Endpoint 0 received IN-token exist. The bit will be set to low after uC read this register.

0: No Endpoint 0 IN interrupt.

Bit 1 Endpoint 0 SETUP interrupt

1: Interrupt of Endpoint 0 received SETUP-transaction exist. The bit will be set to low after uC read this register.

0: No Endpoint 0 SETUP interrupt.

Bit 0 Endpoint 0 ACK interrupt.

1: Interrupt of Endpoint 0 received ACK-packet exists. The bit will be set to low after uC read this register.

0: No Endpoint 0 ACK interrupt.

If the chip is selected for normal operation, the register is the Interrupt Source Register. NINT and the content of the register will be cleared after uC read this register. But it can not clear the content of extended interrupt source register.

Event, otherwise, new extended interrupt will not assert the NINT signal to be active.

E.90: Extended Interrupt Enable Register (EIER), Address: 0x0189h, Access: R/W

Bit 7 Reserved

Bit 6 Reserved

Bit 5 Reserved

Bit 4 Reserved

Bit 3 USB package error interrupt enable

1: This chip will assert NINT to uC after host issues a packet with some error (CRC error, bit stuffing error, EOP error)

0: Disable the interrupt. The default setting is 0.

Bit 2 USB resume interrupt enable

1: This chip will assert NINT to uC when host issues a valid resume signal on USB bus.

0: Disable the interrupt. The default setting is 0.

Bit 1 USB suspend interrupt enable

1: This chip will assert NINT to uC when host issues a valid suspend signal on USB bus.

0: Disable the interrupt. The default setting is 0.

Bit 0 USB reset interrupt enable

1: This chip will assert NINT to uC when host issues a valid reset signal on USB bus.

0: Disable the interrupt. The default setting is 0.

E.91: Extended Interrupt Source Register (EISR), Address: 0x018Ah, Access: Read only

Bit 7 Reserved

Bit 6 DMA EOP interrupt.

1: The chip has transferred the last byte of one block data on EOP(End Of Process) signal of DMA interface. The bit will be set to 0 after uC read this register.

0: No DMA EOP interrupt.

Bit 5 Reserved

Bit 4 DATA0 / DATA1 of Endpoint 0 DATA PID

1: Indicate the received data packet is DATA1.

0: Indicate the received data packet is DATA0

Bit 3 USB error interrupt.

1: The chip has received a packet with some error and will be set to 0 after uC read this register.

0: No USB error interrupt.

Bit 2 Resume interrupt

1: The chip has received a valid resume signal and will be set to 0 after uC read this register.

0: No resume interrupt.

Bit 1 Suspend interrupt

1: The chip has received a valid suspend signal and will be set to 0 after uC read this register.

0: No suspend interrupt

Bit 0 Reset interrupt

1: The chip has received a valid reset signal and will be set to 0 after uC read this register.

0: No reset interrupt.

If the chip is selected for normal operation, the register is the Extended Interrupt Source Register.

The following are the bit definitions of EISR.

E.92: FIFO Clear Register (FCR), Address: 0x018Bh

Bit 7 Reserved

Bit 6 Reserved

Bit 5 Endpoint 2 FIFO clear

1: The FIFO of Endpoint 2 will be cleared. And the bit1 of UCR will be cleared too.

0: No operation.

Bit 4 Endpoint 1 FIFO clear

1: The FIFO of Endpoint 1 will be cleared. And the bit0 of UCR will be cleared too.

0: No operation.

Bit 3 Endpoint 3 FIFO clear

1: The FIFO of Endpoint 3 will be cleared.

0: No operation.

Bit 2 Reserved

Bit 1 Endpoint 0 IN FIFO clear

1: The FIFO of Endpoint 0 input will be cleared.

0: No operation.

Bit 0 Endpoint 0 OUT FIFO clear

1: The FIFO of Endpoint 0 output will be cleared.

0: No operation.

When set to high, relative FIFO is cleared. All of the bits are auto-clear. So it does not need to write low to previous programming bit. The following are the definitions of each bit in this register.

E.93: FIFO Status Register (FSR), Address: 0x018Ch, Access: Read only

Bit 7 Endpoint 2 FIFO2 empty

1: The FIFO2 of Endpoint 2 is empty.

0: It indicates the FIFO with data.

Bit 6 Endpoint 2 FIFO1 empty

1: The FIFO1 of Endpoint 2 is empty.

0: It indicates the FIFO with data.

Bit 5 Endpoint 1 FIFO2 empty

1: The FIFO2 of Endpoint 1 is empty.

0: It indicates the FIFO with data.

Bit 4 Endpoint 1 FIFO1 empty

1: The FIFO1 of Endpoint 1 is empty.

0: It indicates the FIFO with data.

Bit 3 Endpoint 3 FIFO empty

1: The FIFO of Endpoint 3 is empty.

0: It indicates the FIFO with data.

Bit 2 USB VCC

1: connecting to USB hub.

0: No connection to USB hub.

Bit 1 Endpoint 0 IN FIFO empty

1: The FIFO of Endpoint 0 input is empty.

0: It indicates the FIFO with data.

Bit 0 Endpoint 0 OUT FIFO empty

1: The FIFO of Endpoint 0 output is empty.

0: It indicates the FIFO with data.

E.94: Mode Select Register (MSR), Address: 0x018Dh, Access: R/W

Bit 7 Reserved

Bit 6 Reserved

Bit 5, 4 The two bits indicate the operation mode of this chip. The following is the definition of their combination.

Bit 5	Bit 4	
0	0	normal operation
0	1	memory test

Bit 3 Non_autoDMA enable

1: Enable the DMA mode to be Non_autoDMA mode. The chip will response zero length data for the IN packet of Endpoint 1 when the bit0 of UCR is disable. And the bit0 of UCR will be cleared after EOP has been active.

0: Disable the DMA mode to be Non_autoDMA mode. The chip will response NAK for the IN packet of Endpoint 1 when the bit0 of UCR is disable. The bit0 of UCR will not be cleared by EOP and DRQEP1 will automatically assert after the EOP interrupt has been serviced.

Bit 2 Reserved

Bit 1 Reserved

Bit 0 Select memory test mode bank

1: Select bank 1

0: Select bank 0

E.95: Draft/Memory Data Register (DMDR), Address: 0x018Eh, Access: R/W

Bit 7~0 In normal operation, uC can access this register to verify the interface between uC and the chip. When the chip is set in memory test mode, this register is the data window to access the FIFO`s data. The data of the FIFO that has been address by FAR will be written or read through the register.

E.96: Endpoint Address Register 1 (EPAR1), Address: 0x018Fh, Access: R/W

Bit 7~4 The Endpoint address of Endpoint 2 OUT can be programmed to any value except 0. Bit 4 is LSB. The default setting is 2.

Bit 3~0 The Endpoint address of Endpoint 1 IN can be programmed to any value except 0. Bit 0 is LSB. The default setting is 1.

E.97: Endpoint Address Register 2 (EPAR2), Address: 0x0190h, Access: R/W

Bit 7~4 Reserved.

Bit 3~0 The Endpoint address of Endpoint 3 IN can be programmed to any value except 0. Bit 0 is LSB. The default setting is 3.

E.98: FIFO Address Register (FAR), Address: 0x0191h, Access: R/W

When the chip operates under memory test mode, the access of the register is switched to FIFO address register. Bit 7 is MSB. The value of the register can address all FIFOs in the chip. The address is described below.

Address range: **Bank1**

00h ~ 3Fh: FIFO1 of Endpoint 1

40h ~ 7Fh: FIFO2 of Endpoint 1

80h ~ BFh: FIFO1 of Endpoint 2

C0h ~ FFh: FIFO2 of Endpoint 2

Address range: **Bank0**

00h ~ 0Fh: FIFO of Endpoint 0 output

10h ~ 1Fh: FIFO of Endpoint 0 input

20h ~ 2Fh: FIFO of Endpoint 3 output

CONTROL TRANSFERS OF EP0

FROM HOST FROM MP3 R/W

CONTROL READ TRANSFER:

	TOKEN PHASE	DATA PHASE	HANDSHAKE PHASE
SETUP STAGE	SETUP PID, ADDR', CRC	DATA0 PID, DATA..., CRC, CRC	ACK OR NOTHING
DATA STAGE	IN PID, ADDR', CRC	DATA1 PID, DATA..., CRC, CRC	ACK
STATUS STAGE	OUT PID, ADDR', CRC	DATA1 PID, CRC, CRC	ACK

CONTROL WRITE TRANSFER WITH DATA STAGE:

	TOKEN PHASE	DATA PHASE	HANDSHAKE PHASE
SETUP STAGE	SETUP PID, ADDR', CRC	DATA0 PID, DATA..., CRC, CRC	ACK OR NOTHING
DATA STAGE	OUT PID, ADDR', CRC	DATA1 PID, DATA..., CRC, CRC	ACK
STATUS STAGE	IN PID, ADDR', CRC	DATA1 PID, CRC, CRC	ACK

CONTROL WRITE TRANSFER WITH NO-DATA STAGE:

	TOKEN PHASE	DATA PHASE	HANDSHAKE PHASE
SETUP STAGE	SETUP PID, ADDR', CRC	DATA0 PID, DATA..., CRC, CRC	ACK OR NOTHING
STATUS STAGE	IN PID, ADDR', CRC	DATA1 PID, CRC, CRC	ACK

F. ABSOLUTE MAXIMUM RATINGS:

Item	Symbol	Parameter	Min.	Max.	Unit
1	V_{DD}-V_{SS}	DC Power Supply	-0.3	+7.0	V
2	V_{IN}	Input Voltage	V_{SS}-0.3	V_{DD}+0.3	V
3	Ta	Operating Temperature	0	+70	°C
4	Tst	Storage Temperature	-55	+150	°C

G. D.C. CHARACTERISTICS:

(V_{DD}-V_{SS}= 5V±10%, T_A= 25°C, Fosc = 20MHz, unless otherwise specified.)

G.1. Input Leakage Current

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
I_{LK}	Input Leakage Current	V_{IH} = V_{DD} / V_{IL} = GND	-10	-	+10	µA
R_{PU}	Pull Up Resistor	V_{DD} = 5.0V	50K	-	500K	Ohm

G.2. Input Characteristics

Symbol	Parameter	Specification						Unit
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{DD}	Operating Voltage	4.5	5	5.5	3.0	3.3	3.6	V
$USBV_{DD}$	USB Operating Voltage	-	-	-	3.0	3.3	3.6	V
I_{DD}	Operating Current	-	-	50	-	-	35	mA
I_{PWDN}	Power Down Current	-	-	50	-	-	40	µA

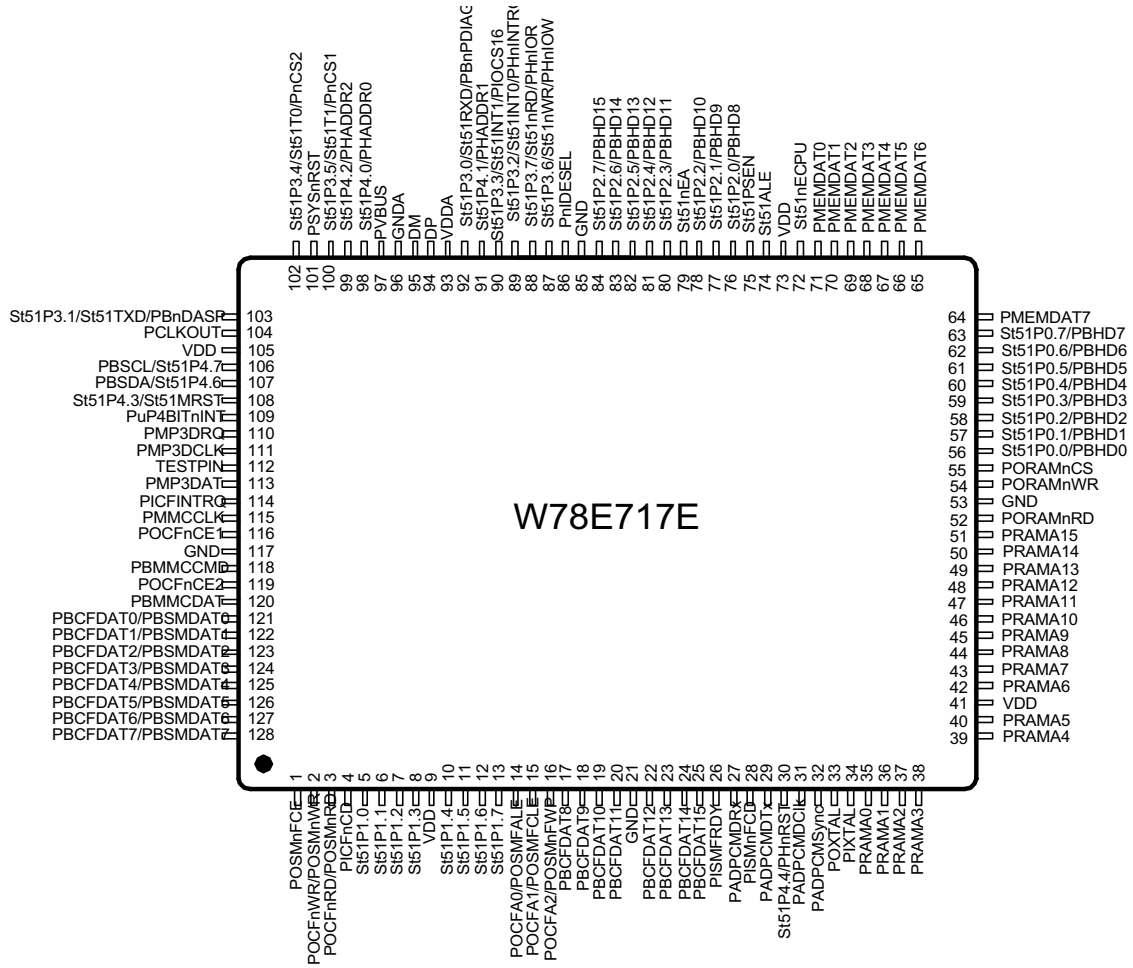
V_{IH}	Input High Voltage	2.4	-	V_{DD} +0.2	2.0	-	V_{DD}+0.2	V
V_{IL}	Input Low Voltage	0	-	0.8	0	-	0.6	V
V_{IH}	Input High Voltage Schmitt Trigger	-	2.8	-	-	1.8	-	V
V_{IL}	Input Low Voltage Schmitt Trigger	-	2.0	-	-	1.0	-	V

G.3. Output Characteristics

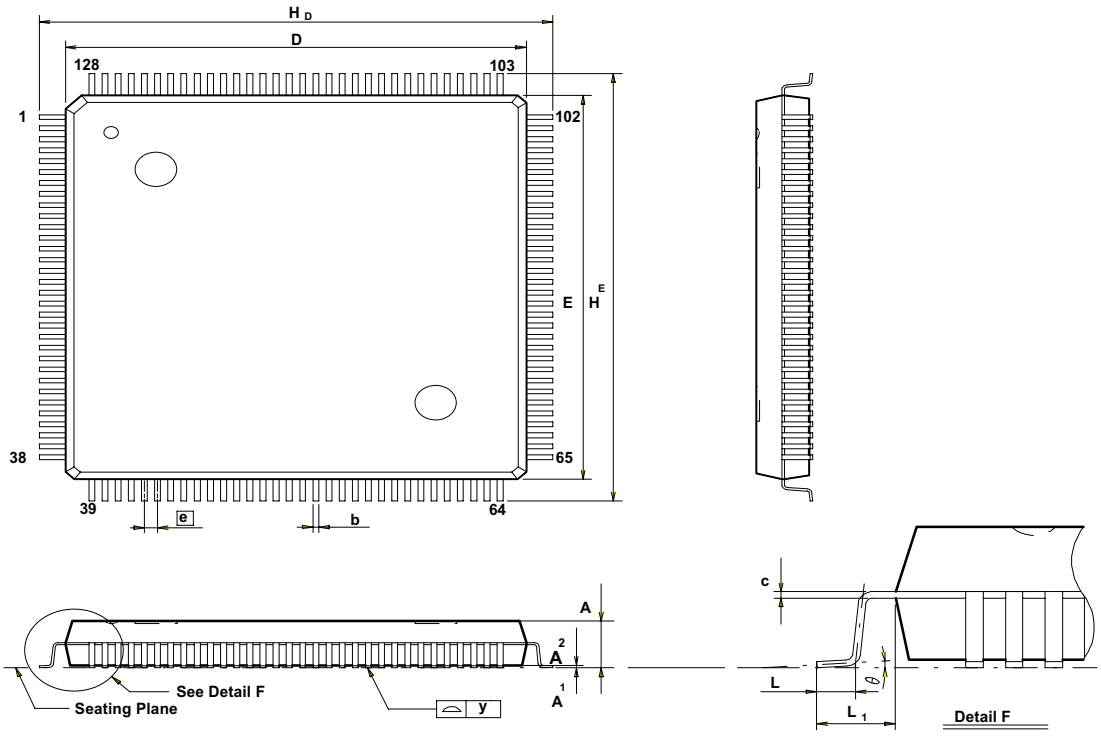
Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
V_{OL1}	Output Low Voltage / VDD = 5.5V	I_{OL} = +12mA	-	-	0.45	V
V_{OH1}	Output High Voltage / VDD = 4.5V	I_{OH} = -12mA	2.4	-	-	V
V_{OL2}	Output Low Voltage / VDD = 5.5V	I_{OL} = +8mA	-	-	0.45	V
V_{OH2}	Output High Voltage / VDD = 4.5V	I_{OL} = -8mA	2.4	-	-	V
V_{OL3}	Output Low Voltage / VDD = 5.5V	I_{OL} = +6mA	-	-	0.45	V
V_{OH3}	Output High Voltage / VDD = 4.5V	I_{OL} = -6mA	2.4	-	-	V
I_{OZ}	TRI-State Leakage Current	V_{OL} = V_{DD} V_{OH} = GND	-10	-	+10	UA

H. PACKAGE SPECIFICATION:

H1.1 128 PIN ASSIGNMENT:



H1.2 PACKAGE: 128L LQFP (14x20x1.4mm footprint 2.0mm)



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.063	—	—	1.60
A_1	0.002	—	—	0.05	—	—
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.011	0.15	0.20	0.27
c	0.004	0.006	0.010	0.10	0.15	0.25
D	0.547	0.551	0.555	13.90	14.00	14.10
E	0.783	0.787	0.791	19.90	20.00	20.10
e	—	0.020	—	—	0.50	—
H_D	0.626	0.630	0.634	15.90	16.00	16.10
H_E	0.862	0.866	0.870	21.90	22.00	22.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	
y	—	—	0.004	—	—	0.10
θ	0°	—	12°	0°	—	12°

Application Note: In-system Programming Software Examples

This application note illustrates the in-system programmability of the Winbond W78E717E MTP-ROM microcontroller. In this example, microcontroller will boot from 64KB APROM bank and waiting for a key to enter in-system programming mode for re-programming the contents of 64KB APROM. While entering in-system programming mode, microcontroller executes the loader program in 4KB LDROM bank. The loader program erases the 64KB APROM then reads the new code data from external SRAM buffer (or through other interfaces) to update the 64KB APROM.

EXAMPLE 1:

```
;*****************************************************************************************************************
;* Example of 64K APROM program: Program will scan the P1.0. if P1.0 = 0, enters in-system
;* programming mode for updating the contents of APROM code else executes the current ROM code.
;* XTAL = 40 MHz
;*****************************************************************************************************************
                .chip 8052
                .RAMCHK OFF
                .symbols

CHPCON          EQU     BFH
CHPENR          EQU     F6H
SFRAL           EQU     C4H
SFRAH           EQU     C5H
SFRFD           EQU     C6H
SFRCN           EQU     C7H

                ORG     0H
LJMP            100H                                    ; JUMP TO MAIN PROGRAM
;*************************************************************************
;*  TIMER0 SERVICE VECTOR ORG = 000BH
;*************************************************************************
                ORG     00BH
                CLR     TR0                     ; TR0 = 0, STOP TIMER0
                MOV     TL0,R6
                MOV     TH0,R7
                RETI
;*************************************************************************
;*  64K APROM MAIN PROGRAM
;*************************************************************************
                ORG     100H
MAIN_64K:
                MOV     A,P1                    ; SCAN P1.0
                ANL     A,#01H
                CJNE    A,#01H,PROGRAM_64K      ; IF P1.0 = 0, ENTER IN-SYSTEM PROGRAMMING MODE
                                                JMP NORMAL_MODE
PROGRAM_64K:
                MOV     CHPENR,#87H     ; CHPENR = 87H, CHPCON REGISTER WRTE ENABLE
                MOV     CHPENR,#59H     ; CHPENR = 59H, CHPCON REGISTER WRITE ENABLE
                MOV     CHPCON,#03H     ; CHPCON = 03H, ENTER IN-SYSTEM PROGRAMMING MODE
                MOV     TCON,#00H       ; TR = 0 TIMER0 STOP
                MOV     IP,#00H         ; IP = 00H
                MOV     IE,#82H         ; TIMER0 INTERRUPT ENABLE FOR WAKE-UP FROM IDLE MODE
                MOV     R6,#FEH         ; TL0 = FEH
                MOV     R7,#FFH         ; TH0 = FFH
                MOV     TL0,R6
                MOV     TH0,R7
                MOV     TMOD,#01H       ; TMOD = 01H, SET TIMER0 A 16-BIT TIMER
```

```
                MOV     TCON,#10H       ; TCON = 10H, TR0 = 1,GO
                MOV     PCON,#01H       ; ENTER IDLE MODE FOR LAUNCHING THE IN-SYSTEM

                                        ; PROGRAMMABILITY
;*****************************************************************************
;* Normal mode 64KB APROM program: depending user's application
;*****************************************************************************
NORMAL_MODE:

                                        .
                                        ; User's application program

                                                .
                                                .
                                                .
```

EXAMPLE 2:

```
;*************************************************************************************************************************  ;*
Example of 4KB LDROM program: This loader program will erase the 64KB APROM first, then reads the new ;*
code from external SRAM and program them into 64KB APROM bank. XTAL = 40 MHz
;*************************************************************************************************************************
                .chip 8052
                .RAMCHK OFF
                .symbols

CHPCON          EQU     BFH
CHPENR          EQU     F6H
SFRAL           EQU     C4H
SFRAH           EQU     C5H
SFRFD           EQU     C6H
SFRCN           EQU     C7H

                ORG     000H
                LJMP    100H            ; JUMP TO MAIN PROGRAM
   ;*********************************************************************
   ;* 1. TIMER0 SERVICE VECTOR ORG = 0BH
   ;*********************************************************************
                ORG     000BH
                CLR     TR0             ; TR0 = 0, STOP TIMER0
                MOV     TL0,R6
                MOV     TH0,R7
                RETI
;*********************************************************************
   ;*  4KB LDROM MAIN PROGRAM
   ;*********************************************************************
                ORG     100H

MAIN_4K:

                MOV     CHPENR,#87H             ; CHPENR = 87H, CHPCON WRITE ENABLE.
                MOV     CHPENR,#59H             ; CHPENR = 59H, CHPCON WRITE ENABLE.
                MOV     A,CHPCON
                ANL     A,#80H
```

```
                CJNE    A,#80H,UPDATE_64K       ; CHECK  F04KBOOT MODE ?

                MOV     CHPCON,#03H             ; CHPCON = 03H, ENABLE IN-SYSTEM

                PROGRAMMING.
                MOV     CHPENR,#00H             ; DISABLE CHPCON WRITE ATTRIBUTE
                MOV     TCON,#00H               ; TCON = 00H, TR = 0 TIMER0 STOP
                MOV     TMOD,#01H               ; TMOD = 01H, SET TIMER0 A 16BIT TIMER
                MOV     IP,#00H                 ; IP = 00H
                MOV     IE,#82H                 ; IE = 82H, TIMER0 INTERRUPT ENABLED
                MOV     R6,#FEH
                MOV     R7,#FFH
                MOV     TL0,R6
                MOV     TH0,R7
                MOV     TCON,#10H               ; TCON = 10H, TR0 = 1, GO
                MOV     PCON,#01H               ; ENTER IDLE MODE

 UPDATE_64K:
                MOV     CHPENR,#00H             ; DISABLE CHPCON WRITE-ATTRIBUTE
                MOV     TCON,#00H               ; TCON = 00H , TR = 0 TIM0 STOP
                MOV     IP,#00H                 ; IP = 00H
                MOV     IE,#82H                 ; IE = 82H, TIMER0 INTERRUPT ENABLED
                MOV     TMOD,#01H               ; TMOD = 01H, MODE1
                MOV      R6,#3CH
                ; SET WAKE-UP TIME FOR ERASE OPERATION, ABOUT 15mS.DEPENDING

                ; ON USER'S SYSTEM CLOCK RATE.
                MOV     R7,#B0H
                MOV     TL0,R6
                MOV     TH0,R7

ERASE_P_4K:

                MOV     SFRCN,#22H              ; SFRCN(C7H) = 22H  ERASE 64K
                MOV     TCON,#10H               ; TCON = 10H, TR0 = 1,GO
                MOV     PCON,#01H               ; ENTER IDLE MODE (FOR ERASE OPERATION)

;*********************************************************************
;
;* BLANK CHECK
;*********************************************************************
;
                MOV     SFRCN,#0H               ; READ 64KB APROM MODE
                MOV     SFRAH,#0H               ; START ADDRESS = 0H
                MOV     SFRAL,#0H
                MOV     R6,#FBH                 ; SET TIMER FOR READ OPERATION, ABOUT 1.5 μS.
                MOV     R7,#FFH
                MOV     TL0,R6
                MOV     TH0,R7
BLANK_CHECK_LOOP:

                SETB    TR0                     ; ENABLE TIMER 0
                MOV     PCON,#01H               ; ENTER IDLE MODE
                MOV     A,SFRFD                 ; READ ONE BYTE

                CJNE    A,#FFH,BLANK_CHECK_ERROR
                INC     SFRAL                   ; NEXT ADDRESS
                MOV     A,SFRAL
                JNZ     BLANK_CHECK_LOOP
```

```
                INC     SFRAH
                MOV     A,SFRAH
                CJNE    A,#0H,BLANK_CHECK_LOOP   ; END ADDRESS = FFFFH
                JMP     PROGRAM_64KROM

BLANK_CHECK_ERROR:

                MOV     P1,#F0H
                MOV     P3,#F0H
                JMP $

;*****************************************************************************
;
;* RE-PROGRAMMING 64KB APROM BANK
;*****************************************************************************
;
PROGRAM_64KROM:

                MOV     DPTR,#0H                ; THE ADDRESS OF NEW ROM CODE
                MOV     R2,#00H                 ; TARGET LOW BYTE ADDRESS
                MOV     R1,#00H                 ; TARGET HIGH BYTE ADDRESS
                MOV     DPTR,#0H                ; EXTERNAL SRAM BUFFER ADDRESS
                MOV     SFRAH,R1                ; SFRAH, TARGET  HIGH ADDRESS
                MOV     SFRCN,#21H              ; SFRCN(C7H) = 21 (PROGRAM 64K)
                MOV     R6,#0CH                 ; SET TIMER FOR PROGRAMMING, ABOUT 150 µS.
                MOV     R7,#FEH
                MOV     TL0,R6
                MOV     TH0,R7

PROG_D_64K:
                MOV     SFRAL,R2                ; SFRAL(C4H) = LOW BYTE ADDRESS
                MOVX    A,@DPTR                 ; READ DATA FROM EXTERNAL SRAM BUFFER
                MOV     SFRFD,A                 ; SFRFD(C6H) = DATA IN
                MOV     TCON,#10H               ; TCON = 10H, TR0 = 1,GO
                MOV     PCON,#01H               ; ENTER IDLE MODE (PRORGAMMING)
                INC     DPTR
                INC     R2
                CJNE    R2,#0H,PROG_D_64K
                INC      R1
                MOV     SFRAH,R1
                CJNE    R1,#0H,PROG_D_64K

;*****************************************************************************
;
; * VERIFY 64KB APROM BANK
;*****************************************************************************
;
                MOV     R4,#03H                 ; ERROR COUNTER
                MOV     R6,#FBH                 ; SET TIMER FOR READ VERIFY, ABOUT 1.5 µS.
                MOV     R7,#FFH
                MOV     TL0,R6
                MOV     TH0,R7
                MOV     DPTR,#0H                ; The start address of sample code
                MOV     R2,#0H                  ; Target  low byte address
                MOV     R1,#0H                  ; Target  high byte address
                MOV     SFRAH,R1                ; SFRAH, Target high address
                MOV     SFRCN,#00H              ; SFRCN = 00 (Read ROM CODE)

 READ_VERIFY_64K:
                MOV     SFRAL,R2                ; SFRAL(C4H) = LOW ADDRESS
                MOV     TCON,#10H               ; TCON = 10H, TR0 = 1,GO
```

```
                MOV     PCON,#01H
                INC     R2
                MOVX    A,@DPTR
                INC     DPTR
                CJNE    A,SFRFD,ERROR_64K
                CJNE    R2,#0H,READ_VERIFY_64K
                INC     R1
                MOV     SFRAH,R1
                CJNE    R1,#0H,READ_VERIFY_64K

;*******************************************************************************
;* PROGRAMMING COMPLETLY, SOFTWARE RESET CPU
;*******************************************************************************
                MOV     CHPENR,#87H             ; CHPENR = 87H
                MOV     CHPENR,#59H             ; CHPENR = 59H
                MOV     CHPCON,#83H             ; CHPCON = 83H, SOFTWARE RESET.

ERROR_64K:
                DJNZ    R4,UPDATE_64K           ; IF ERROR OCCURS, REPEAT 3 TIMES.
        .
          ; IN-SYSTEM PROGRAMMING FAIL, USER'S PROCESS TO DEAL WITH IT.
                        .
                        .
                        .
```