



8-BIT MICROCONTROLLER

GENERAL DESCRIPTION

The W78C51C microcontroller supplies a wider frequency range than most 8-bit microcontrollers on the market. It is compatible with the industry standard 80C51 microcontroller series.

The W78C51C contains four 8-bit bidirectional parallel ports, two 16-bit timer/counters, and a serial port. These peripherals are supported by a five-source, two-level interrupt capability. There are 128 bytes of RAM and an 4K byte mask ROM for application programs.

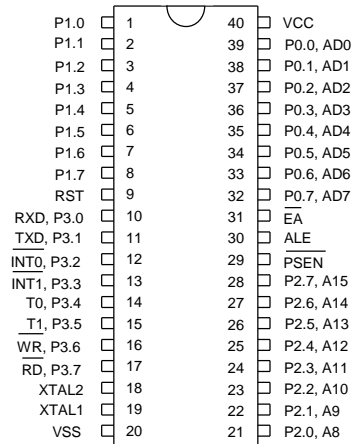
The W78C51C microcontroller has two power reduction modes, idle mode and power-down mode, both of which are software selectable. The idle mode turns off the processor clock but allows for continued peripheral operation. The power-down mode stops the crystal oscillator for minimum power consumption. The external clock can be stopped at any time and in any state without affecting the processor.

FEATURES

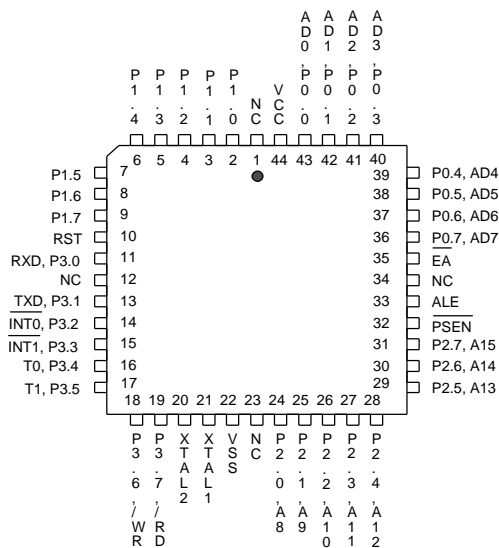
- 8-bit CMOS microcontroller
- Fully static design
- Low standby current at full supply voltage
- DC-40 MHz operation
- 128 bytes of on-chip scratchpad RAM
- 4K bytes of on-chip mask ROM
- 64K bytes program memory address space
- 64K bytes data memory address space
- Four 8-bit bidirectional ports
- Two 16-bit timer/counters
- One full duplex serial port
- Boolean processor
- Five-source, two-level interrupt capability
- Built-in power management
- Code protection
- Packages:
 - DIP 40: W78C51C-16/24/40
 - PLCC 44: W78C51CP-16/24/40
 - QFP 44: W78C51CF-16/24/40
 - TQFP 44: W78C51CM-16/24/40

PIN CONFIGURATIONS

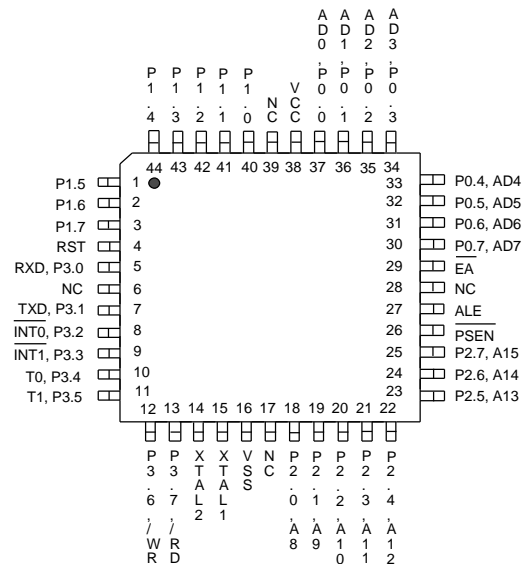
40-Pin DIP (W78C51C)



44-Pin PLCC (W78C51CP)



44-Pin QFP/TQFP (W78C51CF/W78C51CM)





PIN DESCRIPTION

P0.0- P0.7

Port 0, Bits 0 through 7. Port 0 is a bidirectional I/O port. This port also provides a multiplexed low order address/data bus during accesses to external memory.

P1.0- P1.7

Port 1, Bits 0 through 7. Port 1 is a bidirectional I/O port with internal pull-ups.

P2.0- P2.7

Port 2, Bits 0 through 7. Port 2 is a bidirectional I/O port with internal pull-ups. This port also provides the upper address bits for accesses to external memory.

P3.0- P3.7

Port 3, Bits 0 through 7. Port 3 is a bidirectional I/O port with internal pull-ups. All bits have alternate functions, which are described below:

PIN	ALTERNATE FUNCTION
P3.0	RXD Serial Receive Data
P3.1	TXD Serial Transmit Data
P3.2	$\overline{\text{INT0}}$ External Interrupt 0
P3.3	$\overline{\text{INT1}}$ External Interrupt 1
P3.4	T0 Timer 0 Input
P3.5	T1 Timer 1 Input
P3.6	$\overline{\text{WR}}$ Data Write Strobe
P3.7	$\overline{\text{RD}}$ Data Read Strobe

$\overline{\text{EA}}$

External Address Input, active low. This pin forces the processor to execute out of external ROM. This pin should be kept low for all W78C31 operations.

RST

Reset Input, active high. This pin resets the processor. It must be kept high for at least two machine cycles in order to be recognized by the processor.

ALE

Address Latch Enable Output, active high. ALE is used to enable the address latch that separates the address from the data on Port 0. ALE runs at 1/6th of the oscillator frequency. A single ALE pulse is skipped during external data memory accesses. ALE goes to a high impedance state during reset with a weak pull-up.



PSEN

Program Store Enable Output, active low. $\overline{\text{PSEN}}$ enables the external ROM onto the Port 0 address/data bus during fetch and MOV_C operations. $\overline{\text{PSEN}}$ goes to a high impedance state during reset with a weak pull-up.

XTAL1

Crystal 1. This is the crystal oscillator input. This pin may be driven by an external clock.

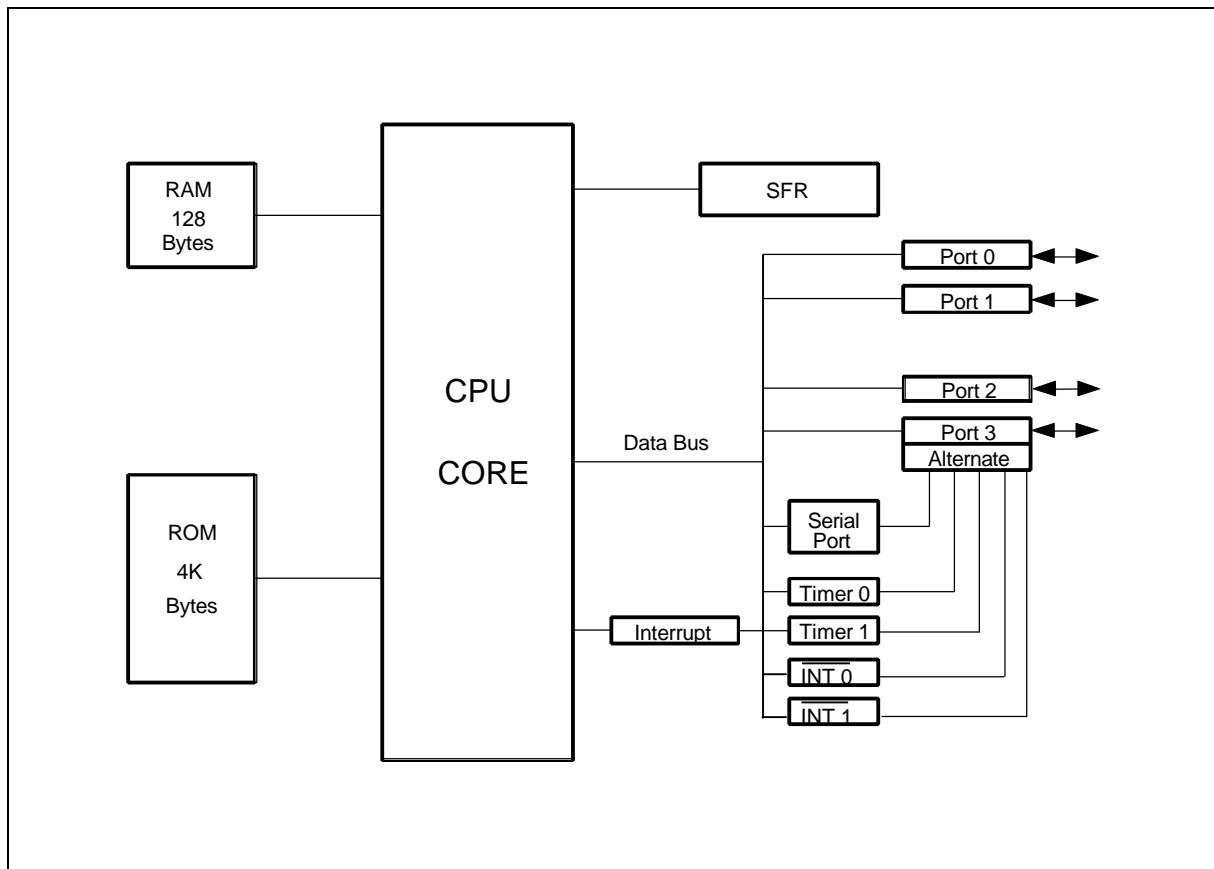
XTAL2

Crystal 2. This is the crystal oscillator output. It is the inversion of XTAL1.

Vss, Vcc

Power Supplies. These are the chip ground and positive supplies.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The W78C51C architecture consists of a core controller surrounded by various registers, four general purpose I/O ports, 128 bytes of RAM, two timer/counters, and a serial port. The processor supports 111 different opcodes and references both a 64K program address space and a 64 K data storage space.

Timers 0, 1

Timers 0, 1 each consist of two 8-bit data registers. These are called TL0 and TH0 for Timer 0, TL1 and TH1 for Timer 1. The TCON and TMOD registers provide control functions for timers 0, 1.

Clock

The W78C51C is designed to be used with either a crystal oscillator or an external clock. Internally, the clock is divided by two before it is used. This makes the W78C51C relatively insensitive to duty cycle variations in the clock.

Crystal Oscillator

The W78C51C incorporates a built-in crystal oscillator. To make the oscillator work, a crystal must be connected across pins XTAL1 and XTAL2. In addition, a load capacitor must be connected from each pin to ground, and a resistor must also be connected from XTAL1 to XTAL2 to provide a DC bias when the crystal frequency is above 24 MHz.

External Clock

An external clock should be connected to pin XTAL1. Pin XTAL2 should be left unconnected. The XTAL1 input is a CMOS-type input, as required by the crystal oscillator. As a result, the external clock signal should have an input one level of greater than 3.5 volts.

Power Management

Idle Mode

The idle mode is entered by setting the IDL bit in the PCON register. In the idle mode, the internal clock to the processor is stopped. The peripherals and the interrupt logic continue to be clocked. The processor will exit idle mode when either an interrupt or a reset occurs.

Power-down Mode

When the PD bit of the PCON register is set, the processor enters the power-down mode. In this mode all of the clocks, including the oscillator are stopped. The only way to exit power-down mode is by a reset.

Reset

The external RESET signal is sampled at S5P2. To take effect, it must be held high for at least two machine cycles while the oscillator is running.

An internal trigger circuit in the reset line is used to deglitch the reset line when the W78C51C is used with an external RC network. The reset logic also has a special glitch removal circuit that ignores glitches on the reset line.

During reset, the ports are initialized to FFH, the stack pointer to 07H, PCON (with the exception of bit 4) to 00H, and all of the other SFR registers except SBUF to 00H. SBUF is not reset.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
DC Power Supply	V _{CC} -V _{SS}	-0.3	+7.0	V
Input Voltage	V _{IN}	V _{SS} -0.3	V _{CC} +0.3	V
Operating Temperature	T _A	0	70	°C
Storage Temperature	T _{ST}	-55	+150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

DC CHARACTERISTICS

V_{CC}-V_{SS} = 5V ; $\pm 10\%$, T_A = 25° C, F_{OSC} = 20 MHz unless otherwise specified.

PARAMETER	SYMBOL	TEST CONDITIONS	SPECIFICATION		UNIT
			MIN.	MAX.	
Operating Voltage	V _{DD}		4.5	5.5	V
Operating Current	I _{DD}	No load V _{DD} = 5.5V	-	30	mA
Idle Current	I _{IDLE}	Idle mode V _{DD} = 5.5V	-	6	mA
Power Down Current	I _{PWDN}	Power-down mode V _{DD} = 5.5V	-	50	μA
Input Current P1, P2, P3	I _{IN1}	V _{DD} = 5.5V V _{IN} = 0V or V _{DD}	-50	+10	μA
Logical 1-to-0 Transition Current P1, P2, P3 ^{(*)1}	I _{TL}	V _{DD} = 5.5V V _{IN} = 2.0V ^{(*)1}	-650	-	μA
Input Current RST ^{(*)2}	I _{IN2}	V _{DD} = 5.5V, V _{IN} = V _{DD}	-	+300	μA
Input Leakage Current P0, $\overline{\text{EA}}$	I _{LK}	V _{DD} = 5.5V 0V < V _{IN} < V _{DD}	-10	+10	μA
Output Low Voltage P1, P2, P3	V _{OL1}	V _{DD} = 4.5V I _{OL1} = +2 mA	-	0.45	V
Output Low Voltage ALE, $\overline{\text{PSEN}}$, P0 ^{(*)3}	V _{OL2}	V _{DD} = 4.5V I _{OL2} = +4 mA	-	0.45	V
Output High Voltage P1, P2, P3	V _{OH1}	V _{DD} = 4.5V I _{OH1} = -100 μA	2.4	-	V
Output High Voltage ALE, $\overline{\text{PSEN}}$, P0 ^{(*)3}	V _{OH2}	V _{DD} = 4.5V I _{OH2} = -400 μA	2.4	-	V
Input Low Voltage (Except RST)	V _{IL1}	V _{DD} = 4.5V	0	0.8	V
Input Low Voltage RST ^{(*)4}	V _{IL2}	V _{DD} = 4.5V	0	0.8	V
Input Low Voltage XTAL1 ^{(*)4}	V _{IL3}	V _{DD} = 5.0V	0	0.8	V



DC Characteristics, continued

PARAMETER	SYMBOL	TEST CONDITIONS	SPECIFICATION		UNIT
			MIN.	MAX.	
Input High Voltage (Except RST)	V _{IH1}	V _{DD} = 5.5V	2.4	V _{DD} +0.2	V
Input High Voltage RST ^(*4)	V _{IH2}	V _{DD} = 5.5V	3.5	V _{DD} +0.2	V
Input High Voltage XTAL1 ^(*4)	V _{IH3}	V _{DD} = 5.0V	3.5	V _{DD} +0.2	V

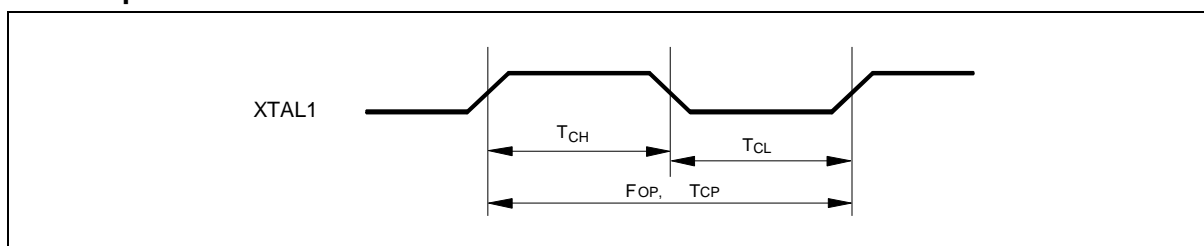
Notes:

1. Pins of P1, P2 and P3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2V.
2. RST pin has an internal pull-down resistor.
3. P0, ALE, $\overline{\text{PSEN}}$ are in the external access mode.
4. XTAL1 is a CMOS input and RST is a Schmitt trigger input.

AC CHARACTERISTICS

The AC specifications are a function of the particular process used to manufacture the part, the ratings of the I/O buffers, the capacitive load, and the internal routing capacitance. Most of the specifications can be expressed in terms of multiple input clock periods (TCP), and actual parts will usually experience less than a ± 20 nS variation. The numbers below represent the performance expected from a 1.2 micron CMOS process when using 2 and 4 mA output buffers.

Clock Input Waveform



PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Operating Speed	F _{OP}	0	-	40	MHz	1
Clock Period	T _{CP}	25	-	-	nS	2
Clock High	T _{CH}	10	-	-	nS	3
Clock Low	T _{CL}	10	-	-	nS	3

Notes:

1. The clock may be stopped indefinitely in either state.
2. The T_{CP} specification is used as a reference in other specifications.
3. There are no duty cycle requirements on the XTAL1 input.

Program Fetch Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Address Valid to ALE Low	TAAS	1 TCP-Δ	-	-	nS	4
Address Hold from ALE Low	TAAH	1 TCP-Δ	-	-	nS	1, 4
ALE Low to $\overline{\text{PSEN}}$ Low	TAPL	1 TCP-Δ	-	-	nS	4
$\overline{\text{PSEN}}$ Low to Data Valid	TPDA	-	-	2 TCP	nS	2
Data Hold after $\overline{\text{PSEN}}$ High	TPDH	0	-	1 TCP	nS	3
Data Float after $\overline{\text{PSEN}}$ High	TPDZ	0	-	1 TCP	nS	
ALE Pulse Width	TALW	2 TCP-Δ	2 TCP	-	nS	4
$\overline{\text{PSEN}}$ Pulse Width	TPSW	3 TCP-Δ	3 TCP	-	nS	4

Notes:

1. P0.0–P0.7, P2.0–P2.7 remain stable throughout entire memory cycle.
2. Memory access time is 3 TCP.
3. Data have been latched internally prior to $\overline{\text{PSEN}}$ going high.
4. "Δ" (due to buffer driving delay and wire loading) is 20 nS.

Data Read Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
ALE Low to $\overline{\text{RD}}$ Low	TDAR	3 TCP-Δ	-	3 TCP+Δ	nS	1, 2
$\overline{\text{RD}}$ Low to Data Valid	TDDA	-	-	4 TCP	nS	1
Data Hold from $\overline{\text{RD}}$ High	TDDH	0	-	2 TCP	nS	
Data Float from $\overline{\text{RD}}$ High	TDDZ	0	-	2 TCP	nS	
$\overline{\text{RD}}$ Pulse Width	TDRD	6 TCP-Δ	6 TCP	-	nS	2

Notes:

1. Data memory access time is 8 TCP.
2. "Δ" (due to buffer driving delay and wire loading) is 20 nS.

Data Write Cycle

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
ALE Low to $\overline{\text{WR}}$ Low	TDAW	3 TCP-Δ	-	3 TCP+Δ	nS
Data Valid to $\overline{\text{WR}}$ Low	TDAD	1 TCP-Δ	-	-	nS
Data Hold from $\overline{\text{WR}}$ High	TDWD	1 TCP-Δ	-	-	nS
$\overline{\text{WR}}$ Pulse Width	TDWR	6 TCP-Δ	6 TCP	-	nS

Note: "Δ" (due to buffer driving delay and wire loading) is 20 nS.

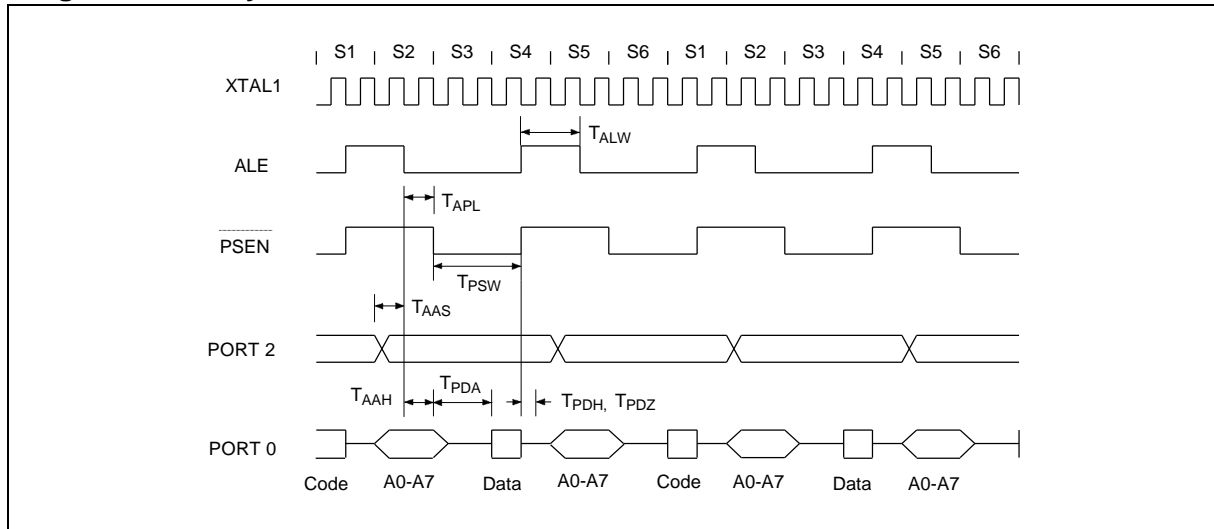
Port Access Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Port Input Setup to ALE Low	TPDS	1 TCP	-	-	nS
Port Input Hold from ALE Low	TPDH	0	-	-	nS
Port Output to ALE	TPDA	1 TCP	-	-	nS

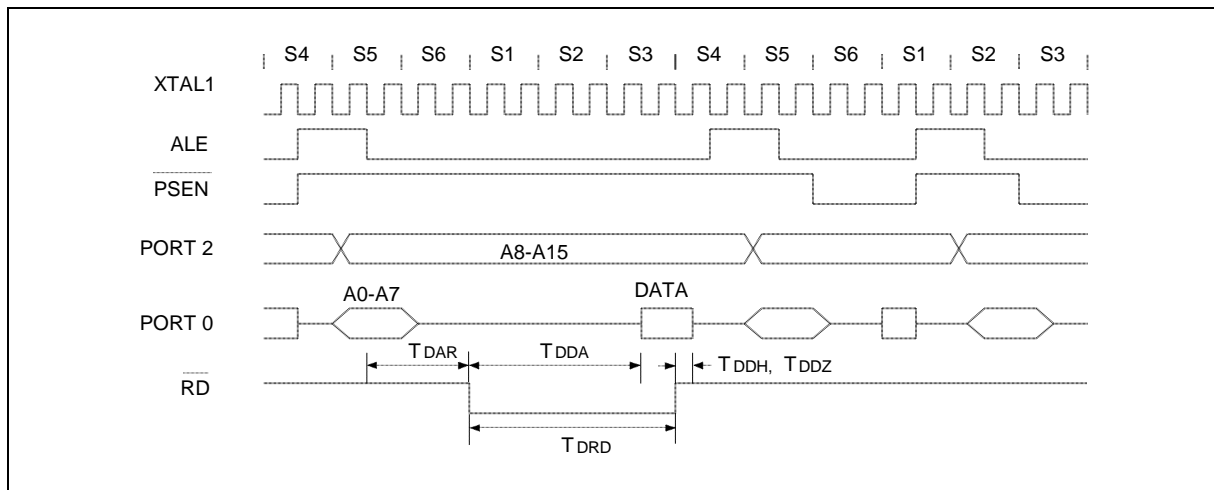
Note: Ports are read during S5P2, and output data becomes available at the end of S6P2. The timing data are referenced to ALE, since it provides a convenient reference.

TIMING WAVEFORMS

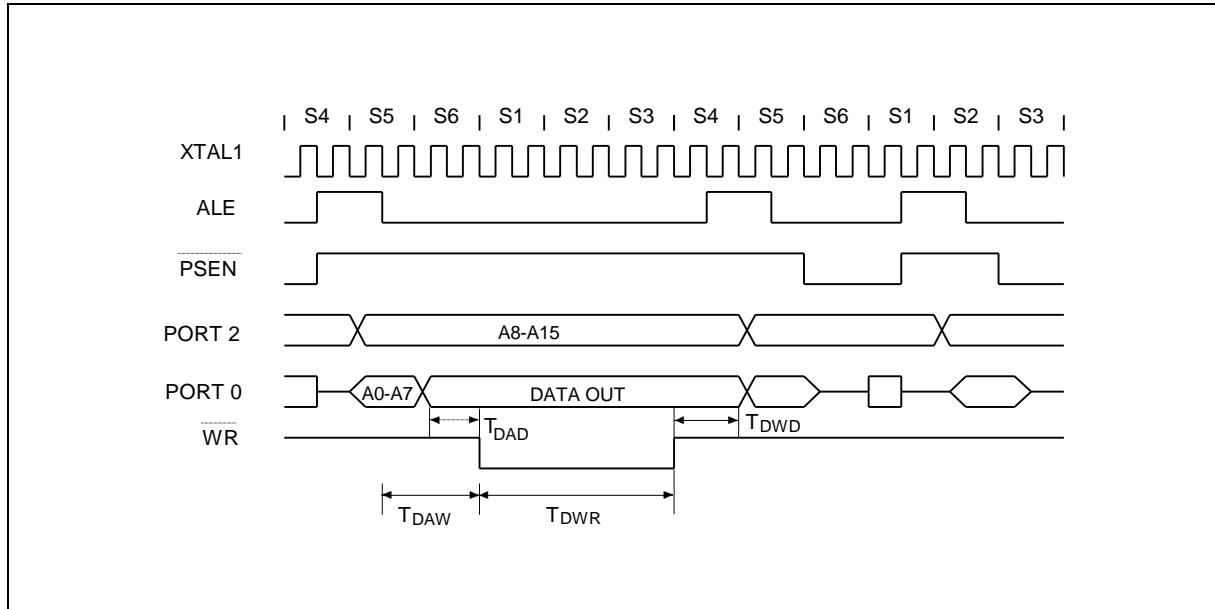
Program Fetch Cycle



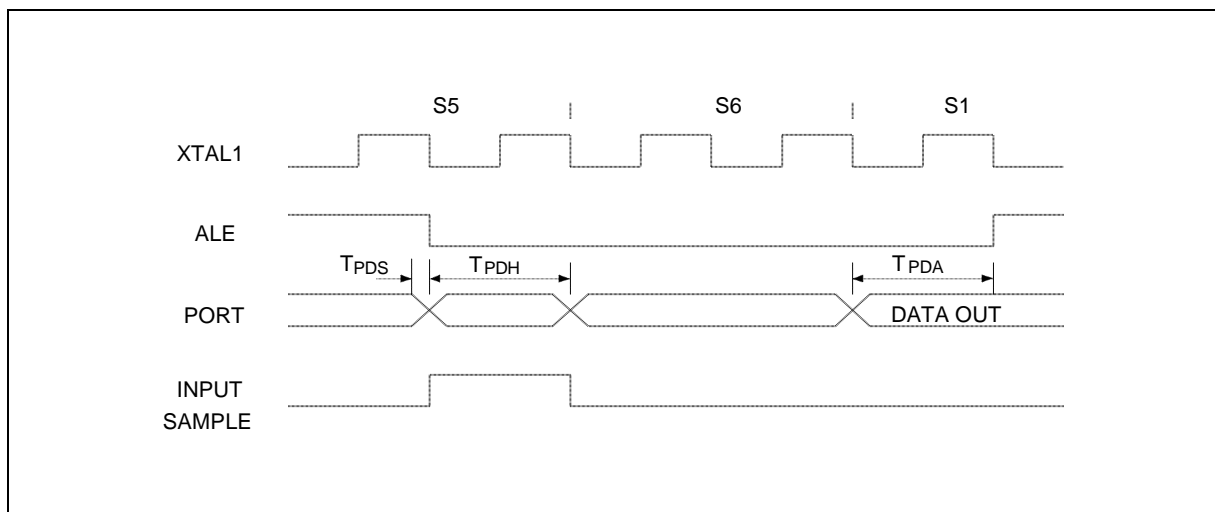
Data Read Cycle



Data Write Cycle



Port Access Cycle



APPLICATION CIRCUIT

Expanded External Program Memory and Crystal

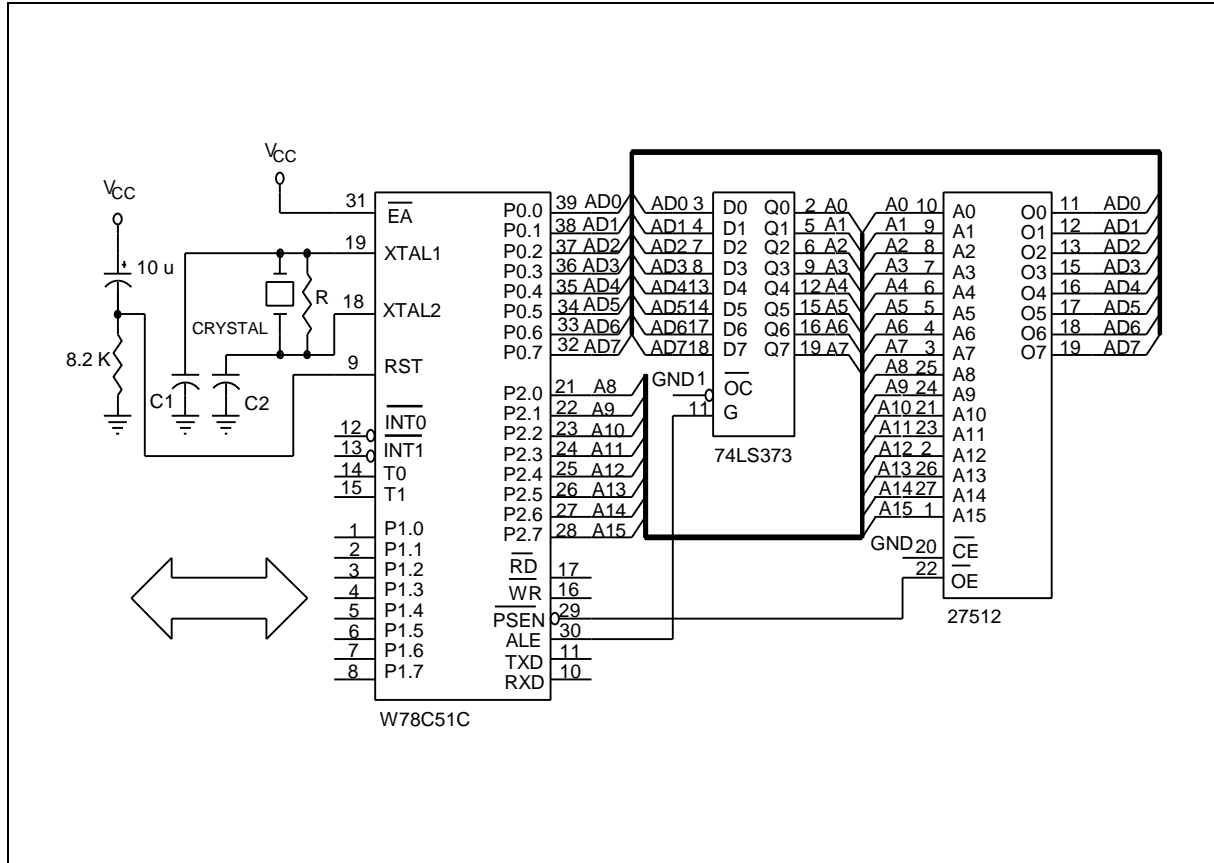


Figure A

CRYSTAL	C1	C2	R
16 MHz	30P	30P	—
24 MHz	15P	15P	—
33 MHz	10P	10P	6.8K
40 MHz	5P	5P	4.7K

Above table shows the reference values for crystal applications.

Note: C1, C2, R components refer to Figure A.

Expanded External Data Memory and Oscillator

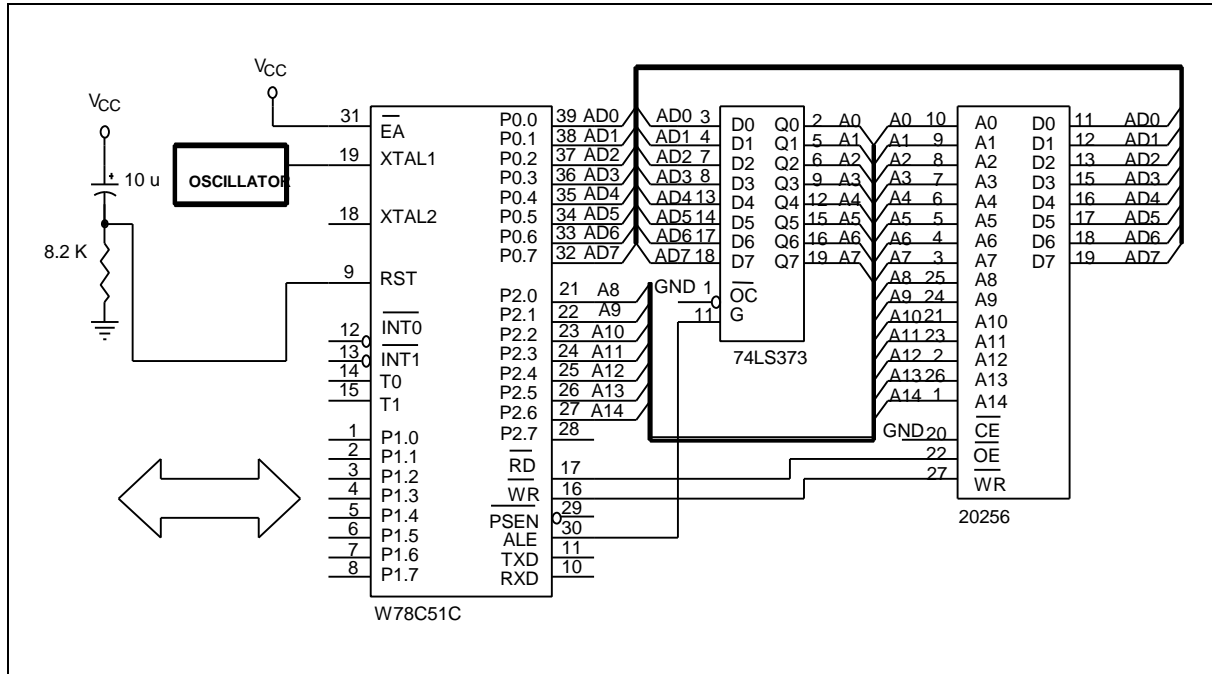
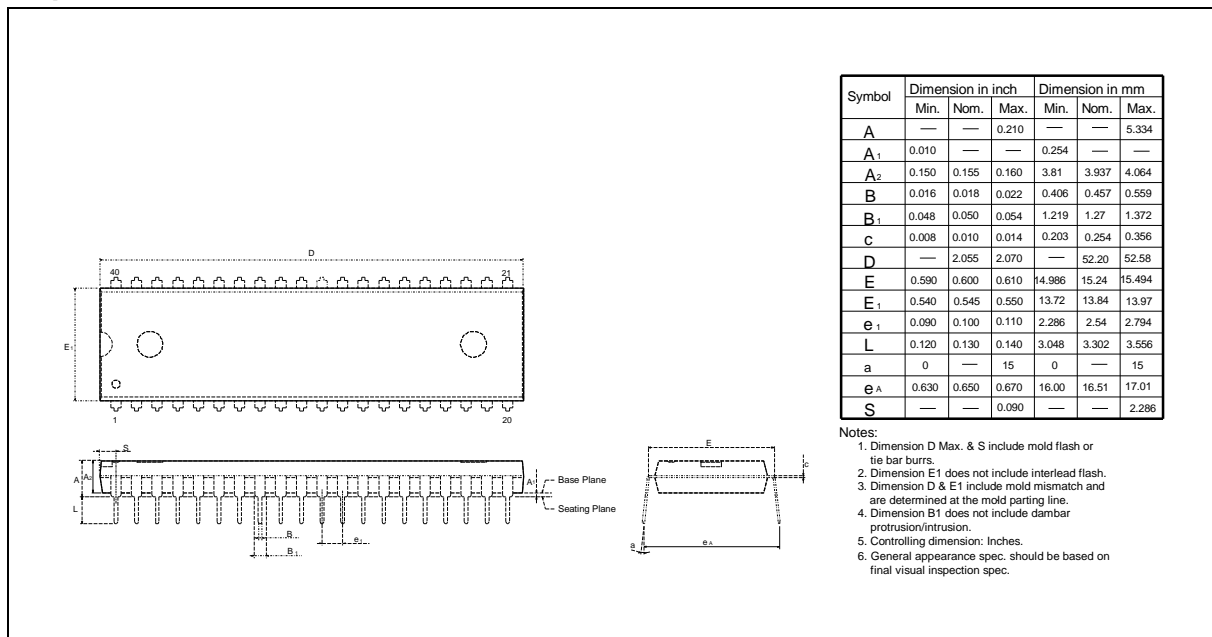


Figure B

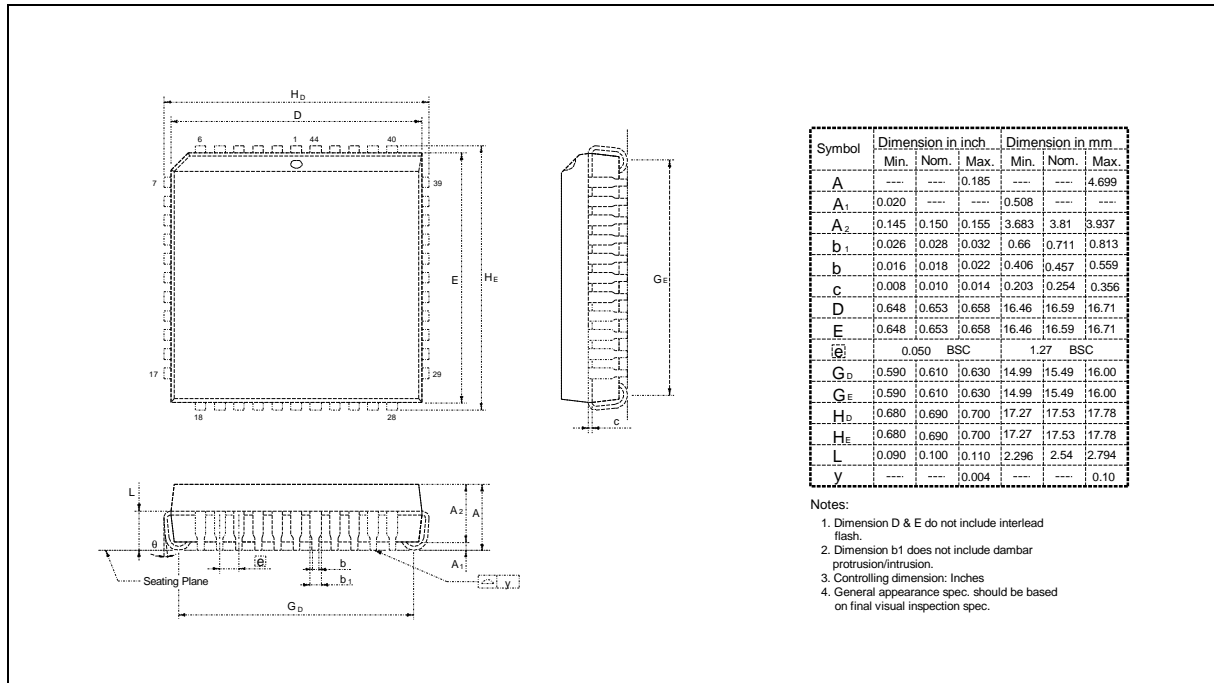
PACKAGE DIMENSIONS

40-pin DIP

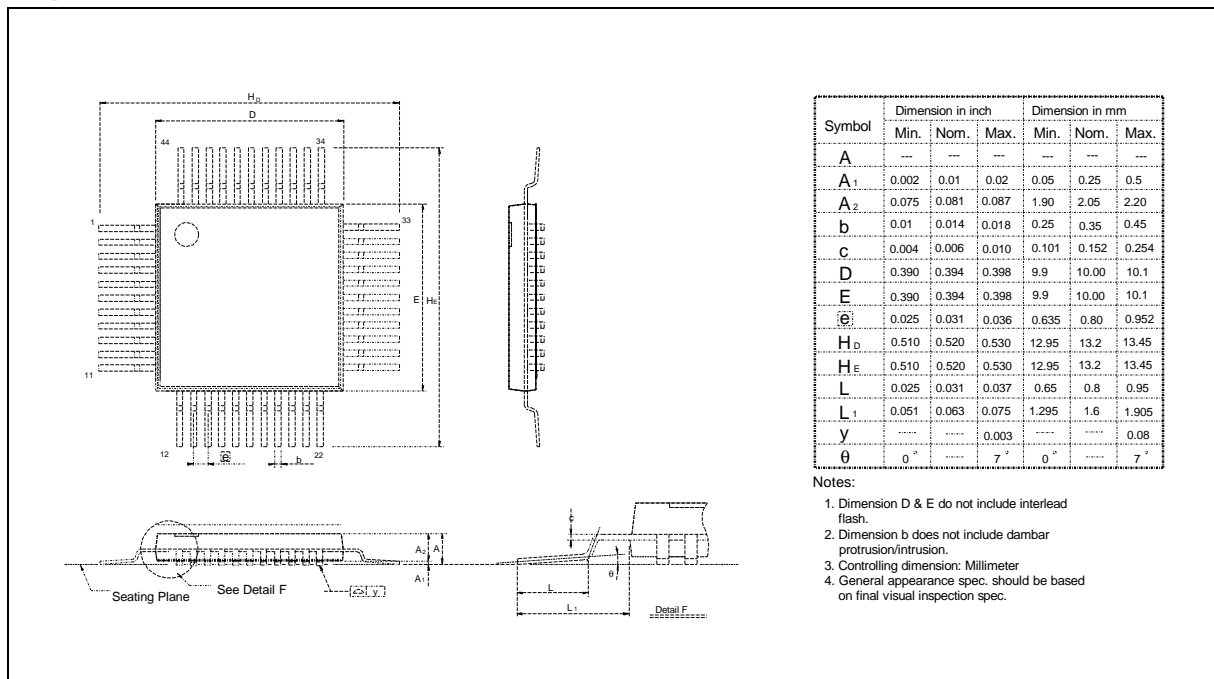


Package Dimensions, continued

44-pin PLCC



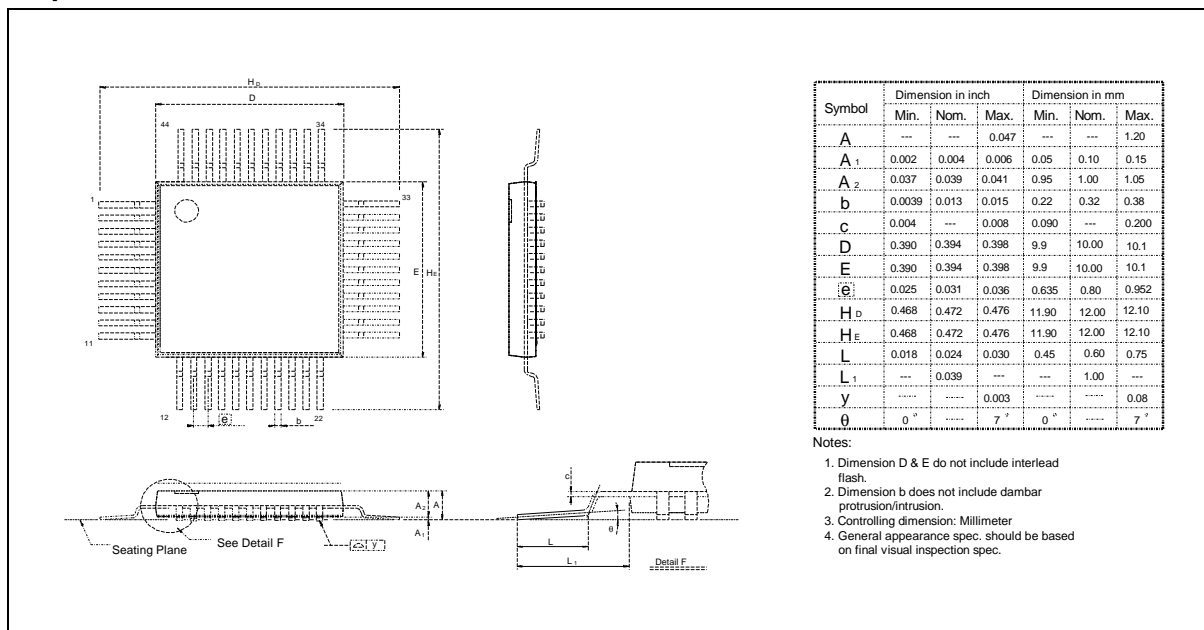
44-pin QFP





Package Dimensions, continued

44-pin TQFP



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Note: All data and specifications are subject to change without notice.