1. PRODUCT DESCRIPTION

The WFP6852A is a 6-bit, 300-channel signal driver designed for low power SVGA TFT-LCD panel applications. The WFP6852A's form factor has been optimized for low-cost, bending TCP applications. **The input pin order and timing are compatible with drivers from TI and NEC.**

The WFP6852A's internal architecture includes a resistor-string DAC with the value of the individual resistor segments weighted to reduce signal driver power dissipation by as much as 20% to 60% when compared to non-weighted resistor string DAC architectures.

The input pin order and timing of the WFP6852A allows the panel maker to get the benefits of the Winbond architecture (such as superior uniformity, low power dissipation, and 2.5V interface for reduced EMI and power) while maintaining multi-source compatibility.

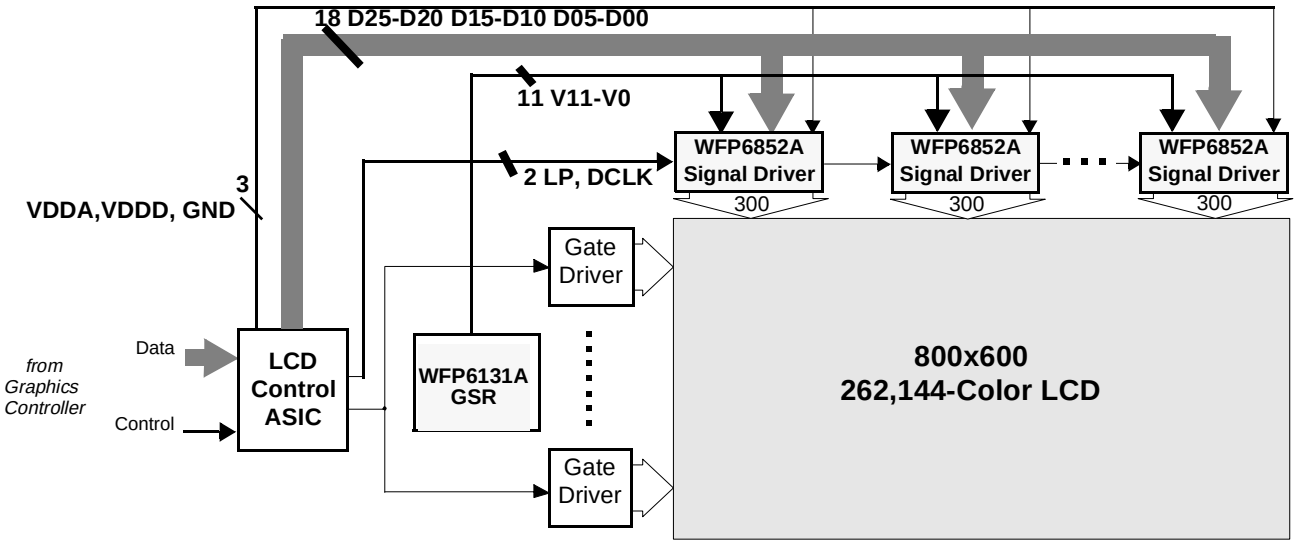
The WFP6852A also provides input selectable double edge clocking and data inversion features. These may be employed in applications that don't need TI/NEC compatibility.

Signal Driver

300-Channel, 6-Bit Signal Driver for TFT-LCD Applications

Features:

- Weighted Rstring architecture
- High speed data transfer of up to 65MHz at VDDD = 3.3V
- Data Inversion and Double Clock feature
- Extremely low output error of 8mV (max) at VDDA = 3.3V
- Input pin compatible with uPD16640x family and TMS57485
- Logic Power Supply Range: 2.3V-2.7V
  3.0V-3.6V
- Analog Power Supply Range: 3.0V-5.5V

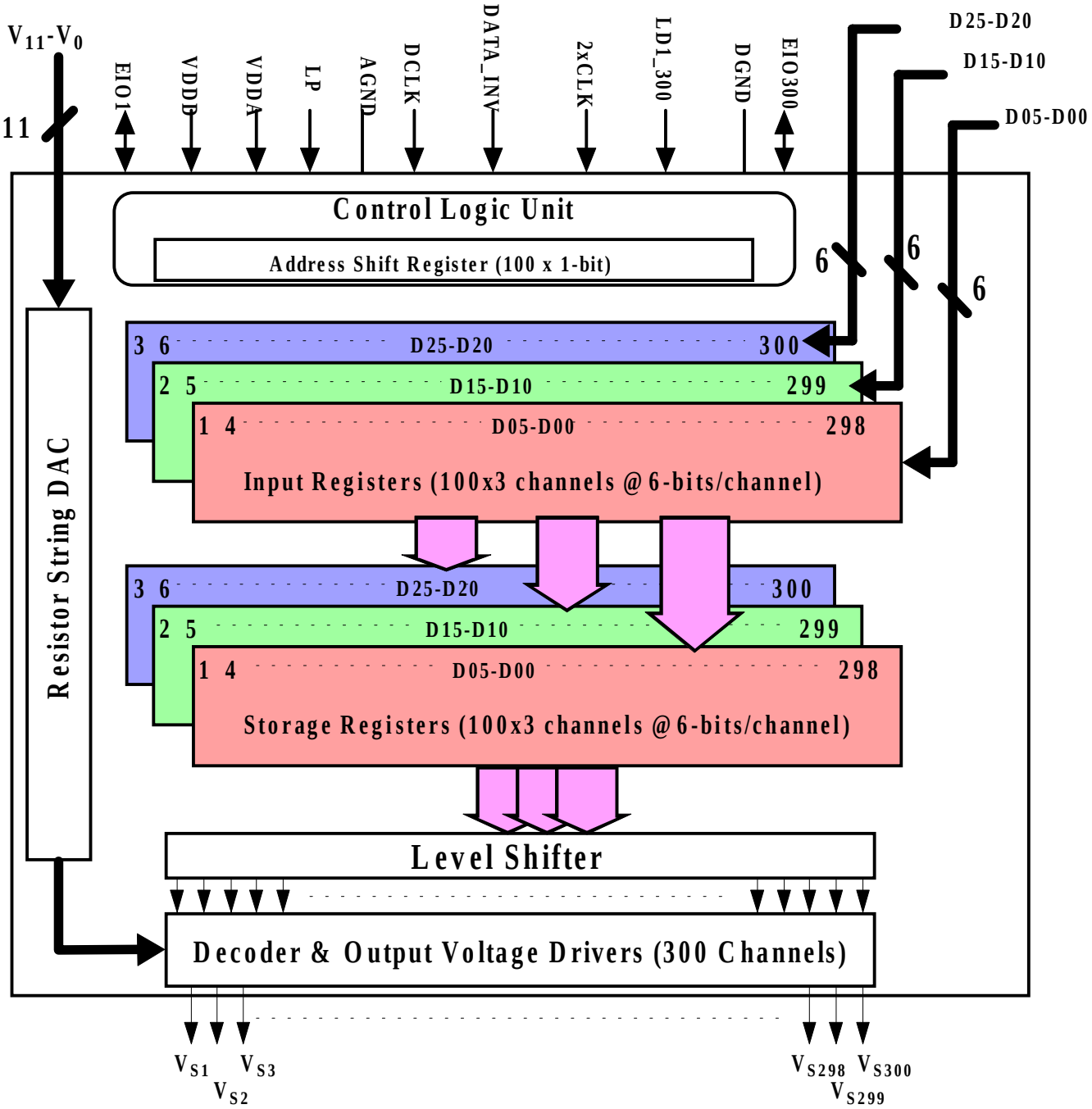


2. FEATURES & BENEFITS

Features	Benefits
• Weighted R-String: See Figure 4-1 & Table 4-1	• Reduces Power Dissipation 20-60% or more. Reduces dc current drive requirements of external reference amplifiers
• Low-power operation • Logic Supply: 2.5V, 3.3 V • Analog Supply: 3.3 V ± 0.3 to 5.0 V ± 0.5	• Extends battery-based operation • Low power and EMI from 2.5 V operation • Minimum dynamic-power dissipation
• Minimum Form Factor • 11.74 mm x 1.05 mm	• Minimum Bezel Size
• High Speed Operation • 65 MHz with 3.3V logic supply • 40 MHz with 2.5V logic supply	• Reduce EMI & power dissipation
• 9 or 11 Voltage References	• Allows user to optimize contrast ratio
• Data Inversion Feature	• Data inversion capability enables a complete internal solution for Vcom modulation. • Can be used in a data transition reduction scheme to reduce EMI & power dissipation
• Double Edge Clocking Feature (2xCLK pin)	• Lowers EMI & power dissipation
• High Integration • 300 output channels • Bi-directional shift register	• Minimizes external components and circuitry • 8 drivers for 800x600 color LCDs • Easy re-configuration from backlit operation to over head projector (OHP) operation
• Full Color Display	• 64 gray scales per primary color • 262,144 (256K) color palette
• Excellent Output Uniformity	• Output Error = 0.15 LSB (8 mV @ VDDA = 3.3V)

3. WFP6852A Block Diagram

The below block diagram shows the WFP6852A's architecture. The circuit contains 300 output channels, so that only 8 drivers are required for 800x600 LCD.



4. Internal Weighted R-String.

Table 4-1: Weighted R_{SEG} Values for WFP6852A (ignoring bus resistance)

R-Segment	Resistance (Ω)
V9 ~ V10	open (see Figure 4-1 below)
V8 ~ V9	25.6,25.6,25.6,25.6,25.6,25.6,51.2,102.4
V7 ~V8	19.2 Ω X 8
V6 ~V7	16 Ω X 8
V5 ~V6	16 Ω X 8
V4 ~V5	16 Ω X 8
V3 ~V4	16Ω X 8
V2 ~V3	19.2 Ω X 8
V1 ~V2	102.4, 51.2, 25.6,25.6, 25.6, 25.6,25.6
V0 ~V1	open (see Figure 4-1 below)

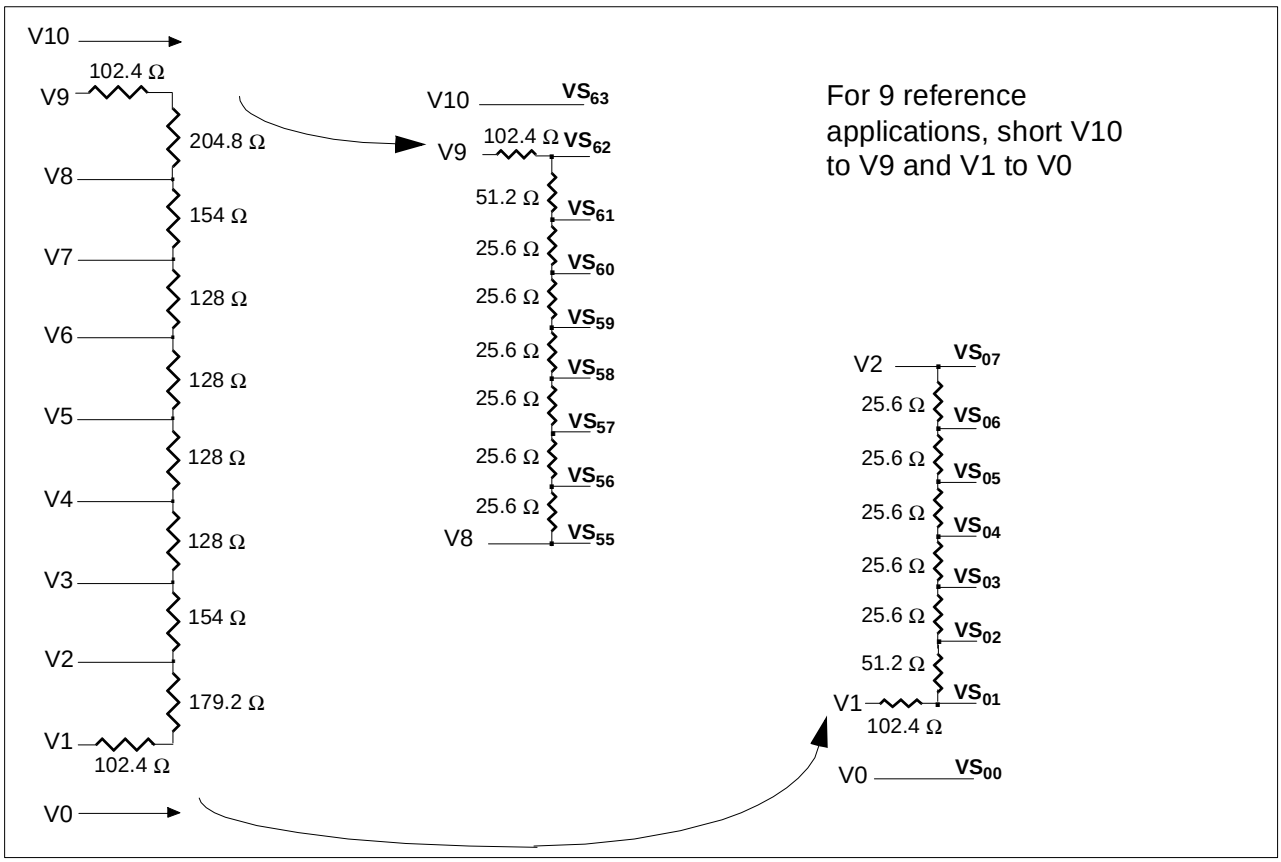


Figure 4-1

5. DIE DIMENSIONS

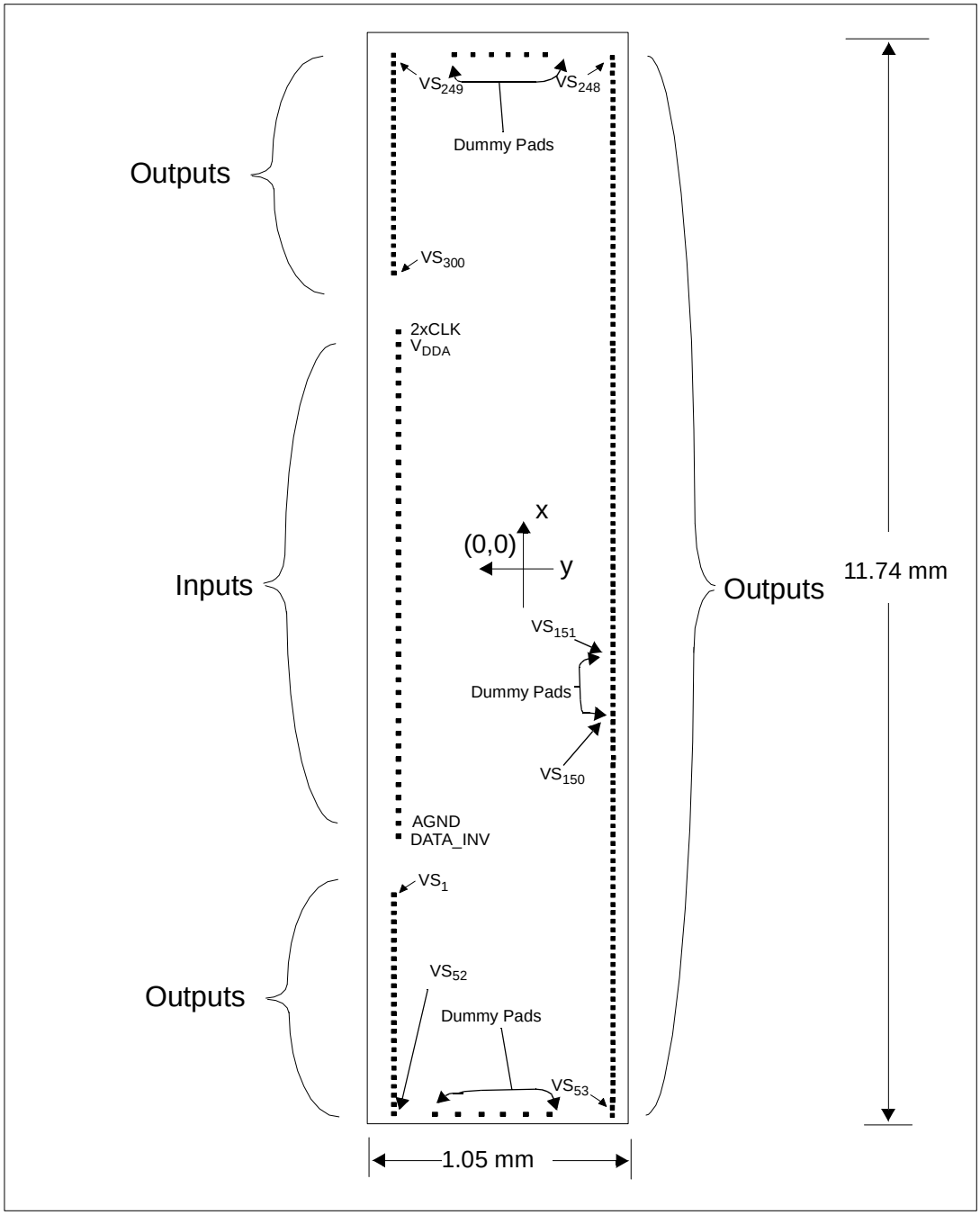


Figure 5-1: Die Dimensions

6. Input Signal Order

#	Signal
1	2xCLK
2	V_{DDA}
3	V_{10}
4	V_8
5	V_6
6	V_4
7	V_2
8	V_0
9	LD1_300
10	D_{20}
11	D_{21}
12	D_{22}
13	D_{23}
14	D_{24}
15	D_{25}
16	LP
17	EIO300
18	V_{DDD}
19	DCLK
20	DGND
21	EIO1
22	D_{10}
23	D_{11}
24	D_{12}
25	D_{13}
26	D_{14}
27	D_{15}
28	D_{00}
29	D_{01}
30	D_{02}
31	D_{03}
32	D_{04}
33	D_{05}
34	V_1
35	V_3
36	V_5
37	V_7
38	V_9
39	AGND
40	DATA_INV

7. DETAILED PAD DESCRIPTIONS & OUTPUT VOLTAGE RELATIONSHIP

The following abbreviations are used for pad types in the following sections: (I) input; (O) output; (I/O) Input/Output, (#) active 'low' signal.

Name	Pad #	Type	Description
LD1_300	9	I	**LOAD DIRECTION:** Controls the direction in which the data is loaded into the Input Register: When LD1_300 = '1', data is loaded from Channel V_{S1} to V_{S300}. When LD1_300 = '0', data is loaded from Channel V_{S300} to V_{S1}.
EIO1, EIO300	21,17	I/O	**ENABLE IN/OUT**: The EIO1 and EIO300 are active high signals that initiate the loading of data into the Input Register of the WFP6852A. When one of the EIOx 's is configured as an input, the other is configured as an output, with the direction determined by the LD1_300 input (see Table 7-1). The EIOx outputs are designed to be connected to the EIOx inputs of adjacent devices to allow a series of drivers to operate sequentially. When a high is applied to the EIOx pin configured as an input on the first device in the series, data is loaded from the three sets of 6-bit Data Inputs into the first three 6-bit Input-Register locations. On subsequent transitions of the DCLK, data continues to be loaded into the remaining 6-bit Input-Register locations. When the register is full (100 DCLK's if 2xCLK = low), the EIOx pin configured as an output goes high, enabling the next driver. The data load sequence is summarized in Table 7-1 and Figure 7-1.

Table 7-1: Input/Output Selection for EIO1 and EIO300

LD1_300 Input	EIO1, EIO300 Functionality		Data Loading Sequence
	EIO1	EIO300	
'1'	Input	Output	Channel 1 to 300
'0'	Output	Input	Channel 300 to 1

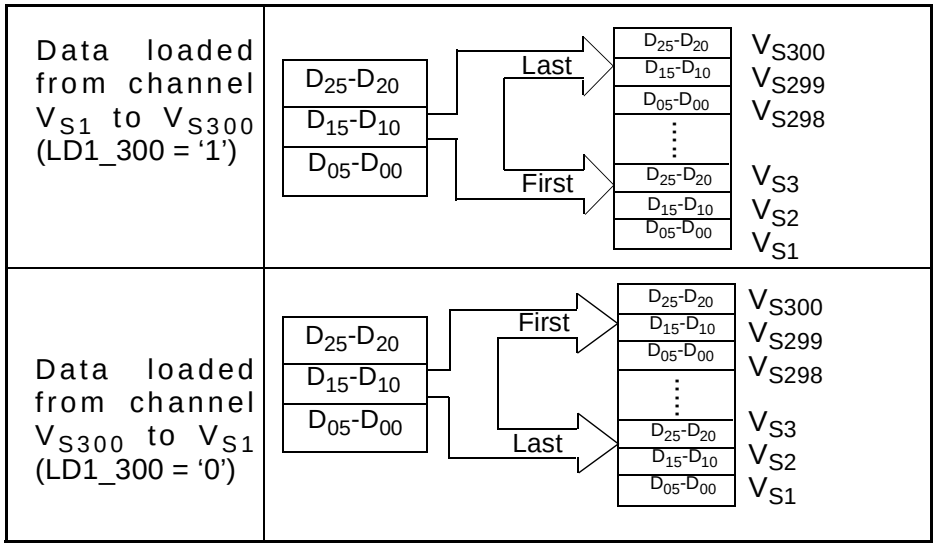


Figure 7–1. Display Data Sampling and Output Direction

Name	Number	Type	Description (*Cont.*)
V_{S1}-V_{S300}		O	**VOLTAGE OUTPUTS**: These outputs drive all 300 pixel inputs of the LCD simultaneously after the high-to-low transition of LP.
D_{00}-D_{05} D_{10}-D_{15} D_{20}-D_{25}	28-33 22-27 10-15	I	**DATA**: The Data inputs consist of 6-bit words for each of three channels. D_{i5} indicates the MSB and D_{i0} the LSB. All 3 data words are loaded in parallel.
LP	16	I	**Latch Pulse**: When LP is driven high, the display data is transferred from the Input Register into the Storage Register for all 300 channels. If DCLK is stopped, when LP goes low, all 300 outputs drive to the selected analog voltages. If DCLK is free running, the outputs begin to drive on the first rising edge of DCLK which samples LP high.
DCLK	19	I	**DATA CLOCK**: Data is loaded into the input registers on the ''low-to-'high' transition of DCLK when 2xCLK = logic low. Data is loaded into the input registers on both edges of DCLK when 2xCLK = logic high.
V_{DDD}	18	I	**DIGITAL SUPPLY VOLTAGE**: 2.5 V or 3.3 V should be provided on this pin to supply digital power to the device.

Name	Number	Type	Description (*Cont.*)
V_{DDA}	2	I	**ANALOG SUPPLY VOLTAGE**: Up to 5.0 V should be provided on this pin to supply analog power to the device. **Also, must have V_{DDA} >= V_{DDD}.**
V_{10} V_9 V_8 V_7 V_6 V_5 V_4 V_3 V_2 V_1 V_0	3 38 4 37 5 36 6 35 7 34 8	I	**REFERENCE ANALOG VOLTAGE INPUTS:** These 11 inputs are used to supply the adjustable-reference voltage inputs to the resistor-string DAC to provide the desired transmissivity-voltage response. .
AGND	39	I	**ANALOG GROUND**
DGND	20	I	**DIGITAL GROUND**
DATA_INV	40	I	**DATA INVERSION**: When logic high, enables inversion of the input display data (D_{ij}). This pad should be tied “low” or allowed to float if data inversion is not used. This signal may also be used in coordination with the control ASIC to reduce data transitions. **This pad has an internal pull-down and is disabled if no-connect**.
2xCLK	1	I	**2xCLK**: When logic high, the 2xCLK input enables sampling of input display data (D_{ij}) on **both** rising and falling edges of the DCLK input (see Fig. 9-2). When logic low, input data is sampled on the falling edge of DCLK only (Fig. 9-1).**This pad has an internal pull-down and is disabled if no-connect**.

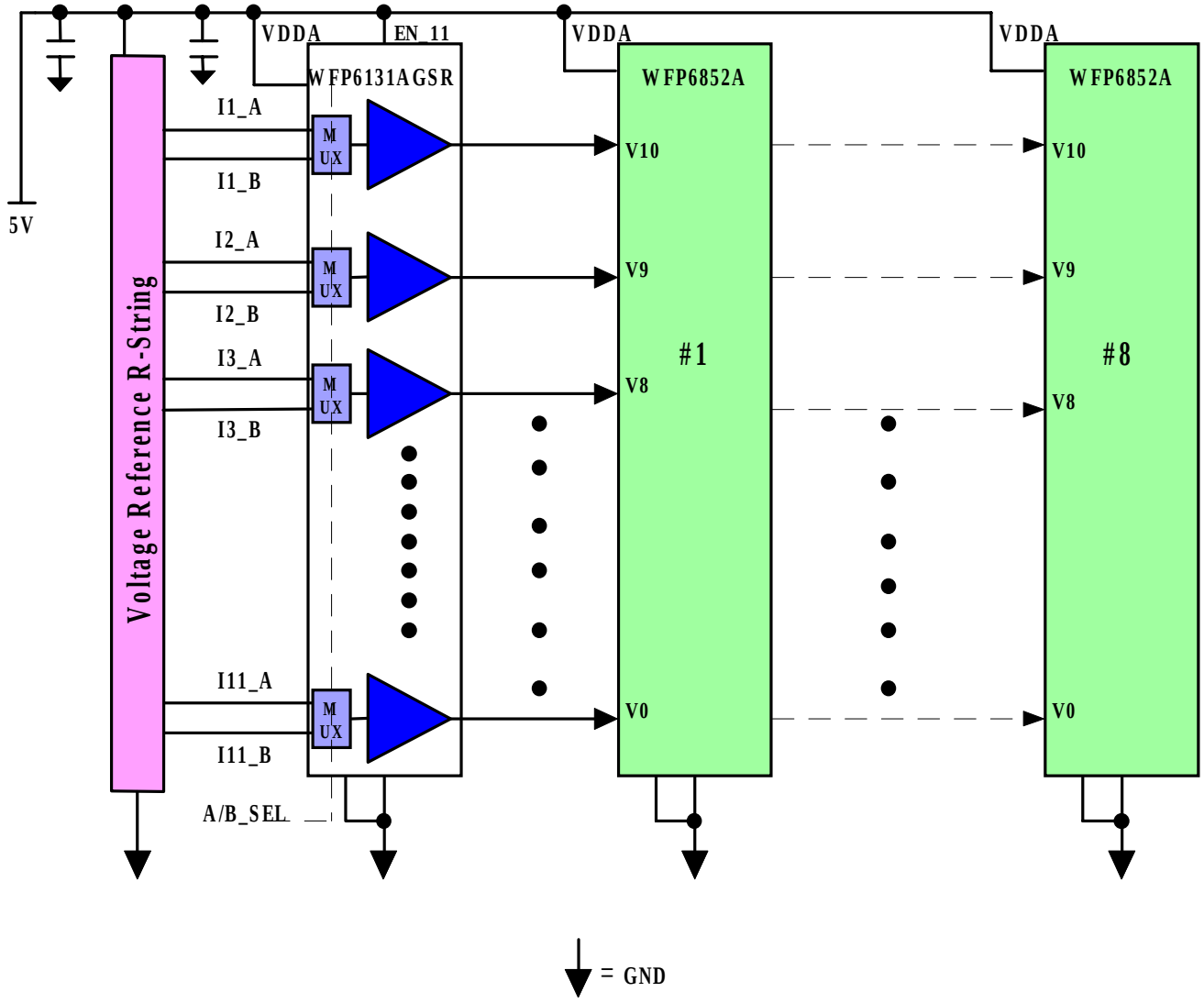
Table 7-2: Input Data vs. Output Voltage--All 11 References Used

MSB	Display Data				LSB	Output Voltage
D_5	D_4	D_3	D_2	D_1	D_0	
0	0	0	0	0	0	V_0
0	0	0	0	0	1	$V_1 + 128/352 \times (V_2 - V_1)$
0	0	0	0	1	0	$V_1 + 192/352 \times (V_2 - V_1)$
0	0	0	0	1	1	$V_1 + 224/352 \times (V_2 - V_1)$
0	0	0	1	0	0	$V_1 + 256/352 \times (V_2 - V_1)$
0	0	0	1	0	1	$V_1 + 288/352 \times (V_2 - V_1)$
0	0	0	1	1	0	$V_1 + 320/352 \times (V_2 - V_1)$
0	0	0	1	1	1	V_2
0	0	1	0	0	0	$V_2 + 1/8 \times (V_3 - V_2)$
0	0	1	0	0	1	$V_2 + 2/8 \times (V_3 - V_2)$
0	0	1	0	1	0	$V_2 + 3/8 \times (V_3 - V_2)$
0	0	1	0	1	1	$V_2 + 4/8 \times (V_3 - V_2)$
0	0	1	1	0	0	$V_2 + 5/8 \times (V_3 - V_2)$
0	0	1	1	0	1	$V_2 + 6/8 \times (V_3 - V_2)$
0	0	1	1	1	0	$V_2 + 7/8 \times (V_3 - V_2)$
0	0	1	1	1	1	V_3
0	1	0	0	0	0	$V_3 + 1/8 \times (V_4 - V_3)$
0	1	0	0	0	1	$V_3 + 2/8 \times (V_4 - V_3)$
0	1	0	0	1	0	$V_3 + 3/8 \times (V_4 - V_3)$
0	1	0	0	1	1	$V_3 + 4/8 \times (V_4 - V_3)$
0	1	0	1	0	0	$V_3 + 5/8 \times (V_4 - V_3)$
0	1	0	1	0	1	$V_3 + 6/8 \times (V_4 - V_3)$
0	1	0	1	1	0	$V_3 + 7/8 \times (V_4 - V_3)$
0	1	0	1	1	1	V_4
0	1	1	0	0	0	$V_4 + 1/8 \times (V_5 - V_4)$
0	1	1	0	0	1	$V_4 + 2/8 \times (V_5 - V_4)$
0	1	1	0	1	0	$V_4 + 3/8 \times (V_5 - V_4)$
0	1	1	0	1	1	$V_4 + 4/8 \times (V_5 - V_4)$
0	1	1	1	0	0	$V_4 + 5/8 \times (V_5 - V_4)$
0	1	1	1	0	1	$V_4 + 6/8 \times (V_5 - V_4)$
0	1	1	1	1	0	$V_4 + 7/8 \times (V_5 - V_4)$
0	1	1	1	1	1	V_5
1	0	0	0	0	0	$V_5 + 1/8 \times (V_6 - V_5)$
1	0	0	0	0	1	$V_5 + 2/8 \times (V_6 - V_5)$
1	0	0	0	1	0	$V_5 + 3/8 \times (V_6 - V_5)$
1	0	0	0	1	1	$V_5 + 4/8 \times (V_6 - V_5)$
1	0	0	1	0	0	$V_5 + 5/8 \times (V_6 - V_5)$
1	0	0	1	0	1	$V_5 + 6/8 \times (V_6 - V_5)$
1	0	0	1	1	0	$V_5 + 7/8 \times (V_6 - V_5)$
1	0	0	1	1	1	V_6
1	0	1	0	0	0	$V_6 + 1/8 \times (V_7 - V_6)$
1	0	1	0	0	1	$V_6 \times 2/8 \times (V_7 - V_6)$
1	0	1	0	1	0	$V_6 + 3/8 \times (V_7 - V_6)$
1	0	1	0	1	1	$V_6 + 4/8 \times (V_7 - V_6)$
1	0	1	1	0	0	$V_6 + 5/8 \times (V_7 - V_6)$
1	0	1	1	0	1	$V_6 + 6/8 \times (V_7 - V_6)$
1	0	1	1	1	0	$V_6 + 7/8 \times (V_7 - V_6)$
1	0	1	1	1	1	V_7
1	1	0	0	0	0	$V_7 + 1/8 \times (V_8 - V_7)$
1	1	0	0	0	1	$V_7 \times 2/8 \times (V_8 - V_7)$
1	1	0	0	1	0	$V_7 + 3/8 \times (V_8 - V_7)$
1	1	0	0	1	1	$V_7 + 4/8 \times (V_8 - V_7)$
1	1	0	1	0	0	$V_7 + 5/8 \times (V_8 - V_7)$
1	1	0	1	0	1	$V_7 + 6/8 \times (V_8 - V_7)$
1	1	0	1	1	0	$V_7 + 7/8 \times (V_8 - V_7)$
1	1	0	1	1	1	V_8
1	1	1	0	0	0	$V_8 + 32/384 \times (V_9 - V_8)$
1	1	1	0	0	1	$V_8 + 64/384 \times (V_9 - V_8)$
1	1	1	0	1	0	$V_8 + 96/384 \times (V_9 - V_8)$
1	1	1	0	1	1	$V_8 + 128/384 \times (V_9 - V_8)$
1	1	1	1	0	0	$V_8 + 160/384 \times (V_9 - V_8)$
1	1	1	1	0	1	$V_8 + 192/384 \times (V_9 - V_8)$
1	1	1	1	1	0	$V_8 + 256/384 \times (V_9 - V_8)$
1	1	1	1	1	1	V_{10}

Table 7-3: Input Data vs. Output Voltage--9 References Used (V_9-V_{10} & V_0-V_1 Shorted)

MSB	Display Data					LSB	Output Voltage
D_5	D_4	D_3	D_2	D_1	D_0		
0	0	0	0	0	0	$V_1=V_0$
0	0	0	0	0	1	$V_1 + 128/352 \times (V_2 - V_1)$
0	0	0	0	1	0	$V_1 + 192/352 \times (V_2 - V_1)$
0	0	0	0	1	1	$V_1 + 224/352 \times (V_2 - V_1)$
0	0	0	1	0	0	$V_1 + 256/352 \times (V_2 - V_1)$
0	0	0	1	0	1	$V_1 + 288/352 \times (V_2 - V_1)$
0	0	0	1	1	0	$V_1 + 320/352 \times (V_2 - V_1)$
0	0	0	1	1	1	V_2
0	0	1	0	0	0	$V_2 + 1/8 \times (V_3 - V_2)$
0	0	1	0	0	1	$V_2 + 2/8 \times (V_3 - V_2)$
0	0	1	0	1	0	$V_2 + 3/8 \times (V_3 - V_2)$
0	0	1	0	1	1	$V_2 + 4/8 \times (V_3 - V_2)$
0	0	1	1	0	0	$V_2 + 5/8 \times (V_3 - V_2)$
0	0	1	1	0	1	$V_2 + 6/8 \times (V_3 - V_2)$
0	0	1	1	1	0	$V_2 + 7/8 \times (V_3 - V_2)$
0	0	1	1	1	1	V_3
0	1	0	0	0	0	$V_3 + 1/8 \times (V_4 - V_3)$
0	1	0	0	0	1	$V_3 + 2/8 \times (V_4 - V_3)$
0	1	0	0	1	0	$V_3 + 3/8 \times (V_4 - V_3)$
0	1	0	0	1	1	$V_3 + 4/8 \times (V_4 - V_3)$
0	1	0	1	0	0	$V_3 + 5/8 \times (V_4 - V_3)$
0	1	0	1	0	1	$V_3 + 6/8 \times (V_4 - V_3)$
0	1	0	1	1	0	$V_3 + 7/8 \times (V_4 - V_3)$
0	1	0	1	1	1	V_4
0	1	1	0	0	0	$V_4 + 1/8 \times (V_5 - V_4)$
0	1	1	0	0	1	$V_4 + 2/8 \times (V_5 - V_4)$
0	1	1	0	1	0	$V_4 + 3/8 \times (V_5 - V_4)$
0	1	1	0	1	1	$V_4 + 4/8 \times (V_5 - V_4)$
0	1	1	1	0	0	$V_4 + 5/8 \times (V_5 - V_4)$
0	1	1	1	0	1	$V_4 + 6/8 \times (V_5 - V_4)$
0	1	1	1	1	0	$V_4 + 7/8 \times (V_5 - V_4)$
0	1	1	1	1	1	V_5
1	0	0	0	0	0	$V_5 + 1/8 \times (V_6 - V_5)$
1	0	0	0	0	1	$V_5 + 2/8 \times (V_6 - V_5)$
1	0	0	0	1	0	$V_5 + 3/8 \times (V_6 - V_5)$
1	0	0	0	1	1	$V_5 + 4/8 \times (V_6 - V_5)$
1	0	0	1	0	0	$V_5 + 5/8 \times (V_6 - V_5)$
1	0	0	1	0	1	$V_5 + 6/8 \times (V_6 - V_5)$
1	0	0	1	1	0	$V_5 + 7/8 \times (V_6 - V_5)$
1	0	0	1	1	1	V_6
1	0	1	0	0	0	$V_6 + 1/8 \times (V_7 - V_6)$
1	0	1	0	0	1	$V_6 \times 2/8 \times (V_7 - V_6)$
1	0	1	0	1	0	$V_6 + 3/8 \times (V_7 - V_6)$
1	0	1	0	1	1	$V_6 + 4/8 X (V_7 - V_6)$
1	0	1	1	0	0	$V_6 + 5/8 \times (V_7 - V_6)$
1	0	1	1	0	1	$V_6 + 6/8 \times (V_7 - V_6)$
1	0	1	1	1	0	$V_6 + 7/8 \times (V_7 - V_6)$
1	0	1	1	1	1	V_7
1	1	0	0	0	0	$V_7 + 1/8 \times (V_8 - V_7)$
1	1	0	0	0	1	$V_7 \times 2/8 \times (V_8 - V_7)$
1	1	0	0	1	0	$V_7 + 3/8 \times (V_8 - V_7)$
1	1	0	0	1	1	$V_7 + 4/8 X (V_8 - V_7)$
1	1	0	1	0	0	$V_7 + 5/8 \times (V_8 - V_7)$
1	1	0	1	0	1	$V_7 + 6/8 \times (V_8 - V_7)$
1	1	0	1	1	0	$V_7 + 7/8 \times (V_8 - V_7)$
1	1	0	1	1	1	V_8
1	1	1	0	0	0	$V_8 + 32/384 \times (V_9 - V_8)$
1	1	1	0	0	1	$V_8 + 64/384 \times (V_9 - V_8)$
1	1	1	0	1	0	$V_8 + 96/384 \times (V_9 - V_8)$
1	1	1	0	1	1	$V_8 + 128/384 \times (V_9 - V_8)$
1	1	1	1	0	0	$V_8 + 160/384 \times (V_9 - V_8)$
1	1	1	1	0	1	$V_8 + 192/384 \times (V_9 - V_8)$
1	1	1	1	1	0	$V_8 + 256/384 \times (V_9 - V_8)$
1	1	1	1	1	1	$V_9=V_{10}$

8. WFP6852A Hook-up to WFP6131AR (Buffer AMP)



9. ELECTRICAL SPECIFICATIONS

9.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Notes
V_{DDD}	Digital Power Supply Voltage	-0.3	smaller of 6.0 or V_{DDA}	Volts	1,2,4
V_{DDA}	Analog Power Supply Voltage	-0.3	6.0	Volts	1,2,4
V_{10} - V_0	Analog Reference Voltage Inputs	-0.3	V_{DDA} + 0.3	Volts	1,2
V_{S300}-V_{S1}	Output Voltage	-0.3	V_{DDA} + 0.3	Volts	1,2
V_{IN}	Voltage on any Digital Input	-0.3	V_{DDD} + 0.3	Volts	1,2,3
P_D	Operating Power Dissipation		300	mW	
T_A	Operating Temperature (Ambient Temperature under bias)	-10	85	°C	1
T_{STR}	Storage Temperature	-20	85	°C	1

NOTES: 1) Stresses above those listed may cause permanent damage to system components. These are stress ratings only. Functional operation at these or any conditions above those indicated in the operational ratings of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

2) All voltages are with respect to ground (DGND) unless otherwise noted.

3) For D_{25}-D_{20}, D_{15}-D_{10}, D_{05}-D_{00}, DCLK,DATA_INV, 2xCLK, LP, EIO1, EIO300 & LD1_300 inputs.

4) **V_{DDA} must be greater than or equal to V_{DDD} for proper circuit operation**. V_{DDA} should be powered on first, or the same time as V_{DDD}. V_{DDD} should be powered off first, or the same time as V_{DDA}.

9.2 Recommended Operating Conditions

Symbol	Parameter	Min	Typical	Max	Units	Notes
V_{DDD}	Digital Supply Voltage	2.3 3.0	2.5 3.3	2.7 3.6	Volts Volts	1 1
V_{DDA}	Analog Supply Voltage	3.0		5.5	Volts	1
T_A	Ambient Temperature	0	25	70	°C	
V_{10} - V_0	Analog Reference Voltage	0		V_{DDA}	Volts	1, 2
I_{REF}	Analog Reference Current			20	mA	

NOTES: 1) All voltages are with respect to ground (DGND) unless otherwise noted.

2) Case I: $V_{DA} \geq V_{10} \geq V_9 \geq V_8 \geq V_7 \geq V_6 \geq V_5 \geq V_4 \geq V_3 \geq V_2 \geq V_1 \geq V_0$

Case II: $V_{DA} \geq V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5 \geq V_6 \geq V_7 \geq V_8 \geq V_9 \geq V_{10}$

9.3 DC Characteristics (Preliminary data – subject to change)

V_{DDA} = 5 V ± 0.5 V, T_A = 25° C, unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Units	Test Conditions	Note
V_S	Analog Output Voltage				VDDA-0.03	Volts		1
V_{ST}	Analog Output Transition Band				$\|V_{10}-V_0\|$	Volts		
V_{ERR}	Analog Output Error Voltage		-0.15		+0.15	LSB		2
V_{IH}	Logic Input high Voltage		$0.7V_{DDD}$			Volts		3
V_{IL}	Logic Input low Voltage				$0.3V_{DDD}$	Volts		3
V_{OH}	Logic Output high Voltage		V_{DDD} - 0.4			Volts	I_{OH} = - 0.4 mA	4
V_{OL}	Logic Output low Voltage				0.4	Volts	I_{OL} = 0.4 mA	4
I_{DDA}	Analog Supply Current				400	µA	V_{DDA} = 5.0 V	5
I_{DDD}	Digital-Supply Current (active)			4.0	8	mA	V_{DDD} = 2.5 V	5
				5.0	10	mA	V_{DDD} = 3.3 V	5
I_{DDD}	Digital-Supply Current (Stand-by)			80	400	µA	V_{DDD} = 2.5 V	6
				80	400	µA	V_{DDD} = 3.3 V	6
I_{IN}	Input Leakage Current (no pull-down)		-5		+5	µA	$0 < V_{IN} < V_{DDD}$	
	Input Leakage Current (w/ pull-down)		-5		+150	µA	$0 < V_{IN} < V_{DDD}$	7
C_{IN}	Input Capacitance				5	pF		3
R_{String}	String Resistance	V1-V9	1126	1408	1690	Ω		
		V1-V2	236	295	354			
		V2-V3	134	168	202			
		V3-V4	115	144	173			
		V4-V5	115	144	173			
		V5-V6	115	144	173			
		V6-V7	115	144	173			
		V7-V8	134	168	202			
		V8-V9	253	316	379			
R_{OUT}	Output Resistance							
	V0 (code 0) or V10 (code 63)				13.8	kΩ		8
	V1-V2 (at code 2)				29.4			
	V2-V3 (at code 11)				18.5			
	V3-V4 (at code 19)				16.3			
	V4-V5 (at code 27)				16.3			
	V5-V6 (at code 35)				16.3			
	V6-V7 (at code 43)				16.3			
	V7-V8 (at code 51)				18.5			
	V8-V9 (at code 61)				31.9			

NOTES:

1) See Tables 7-2 & 7-3 for digital code-Voltage relationship.
2) For all codes
3) 2xCLK, DCLK, LP, D_{25}-D_{20}, D_{15}-D_{10}, D_{05}-D_{00}, EIO1, EIO300, and LD1_300 inputs
4) EIO1 and EIO300 outputs
5) f_{DCLK}=12.5 MHz, f_{LP} = 30 kHz, device is loading,100% of data lines toggle each DCLK cycle
6) f_{DCLK}=12.5 MHz, f_{LP} = 30 kHz, device is not loading,100% of data lines toggle each DCLK cycle
7) The 2xCLK and DATA_INV input pins have internal pull-downs. Maximum input current occurs when these pins are driven to V_{DDD}.
8) Effective output resistance at output with highest resistance when all outputs drive the same code.

9.4 AC Characteristics (V_{DDD} = 2.5 V ± 0.2 V) – (Preliminary data – subject to change)

See Figures 9-1 to 9-6 for waveforms.
Conditions: V_{DDA} = 5.0 V ± 0.5 V, T_A = 25° C

Symbol	Parameter	Min 2xCLK/2xCLK	Max 2xCLK/2xCLK	Units	Note
f_{CLK}	Guaranteed Max DCLK frequency	40/20		MHz	
t_{CLK}	DCLK period	25/50		ns	
t_1	DCLK high pulse width	8/16		ns	
t_2	DCLK low pulse width	8/16		ns	
t_3	DCLK rise time		6/6	ns	
t_4	DCLK fall time		6/6	ns	
t_5	Data, DATA_INV setup time	2/2		ns	
t_6	Data, DATA_INV hold time	14/18		ns	
t_7	Enable-In setup time	5/5		ns	
t_8	Enable-In hold time	10/ 1/2 DCLK			
t_9	DCLK to Enable-Out		17/17	ns	1
t_{10}	LP high pulse width	100/100		ns	
t_{11}	LP low pulse width	100/100		ns	2
t_{12}	Last Pixel DCLK to LP	10/10		ns	
t_{13}	Blanking Time	2/1		DCLK's	

NOTES: 1) C_{LOAD} = 15 pF (See Figure 9-7)

2) Free running DCLK operation: LP must be sampled low by at least 1 rising edge of DCLK before the DCLK edge which samples LP high. Stopped DCLK operation: LP must be sampled low by one rising edge of DCLK before DCLK is stopped.

9.5 AC Characteristics (V_{DDD} = 3.3 V ± 0.3 V) – (Preliminary data – subject to change)

See Figures 9-1 to 9-6 for waveforms.
Conditions: V_{DDA} = 5.0 V ± 0.5 V, T_A = 25° C

Symbol	Parameter	Min 2xCLK/2xCLK	Max 2xCLK/2xCLK	Units	Note
f_{CLK}	Guaranteed Max DCLK frequency	55/27.5		MHz	
t_{CLK}	DCLK period	18.2/36.4		ns	
t_1	DCLK high pulse width	6/12		ns	
t_2	DCLK low pulse width	6/12		ns	
t_3	DCLK rise time		6/6	ns	
t_4	DCLK fall time		6/6	ns	
t_5	Data, DATA_INV setup time	2/1		ns	
t_6	Data, DATA_INV hold time	10/11		ns	
t_7	Enable-In setup time	3/3		ns	
t_8	Enable-In hold time	10/ 1/2 DCLK			
t_9	DCLK to Enable-Out		12/12	ns	1
t_{10}	LP high pulse width	50/50		ns	
t_{11}	LP low pulse width	100/100		ns	2
t_{12}	Last Pixel DCLK to LP	10/10		ns	
t_{13}	Blanking Time	2/1		DCLK's	

NOTES: 1) C_{LOAD} = 15 pF (See Figure 9-7)

2) Free running DCLK operation: LP must be sampled low by at least 1 rising edge of DCLK before the DCLK edge which samples LP high. Stopped DCLK operation: LP must be sampled low by one rising edge of DCLK before DCLK is stopped.

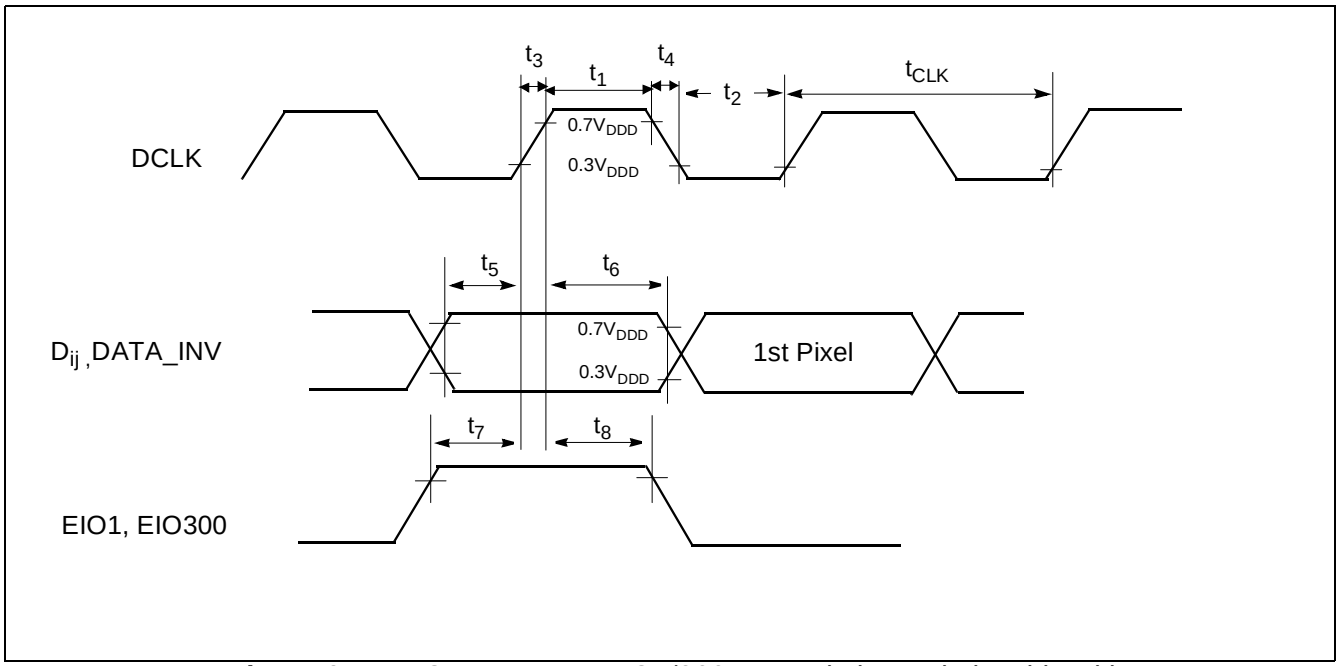


Figure 9-1: DCLK, Data, & EIO1/300 Input Timing Relationship with 2xCLK = low

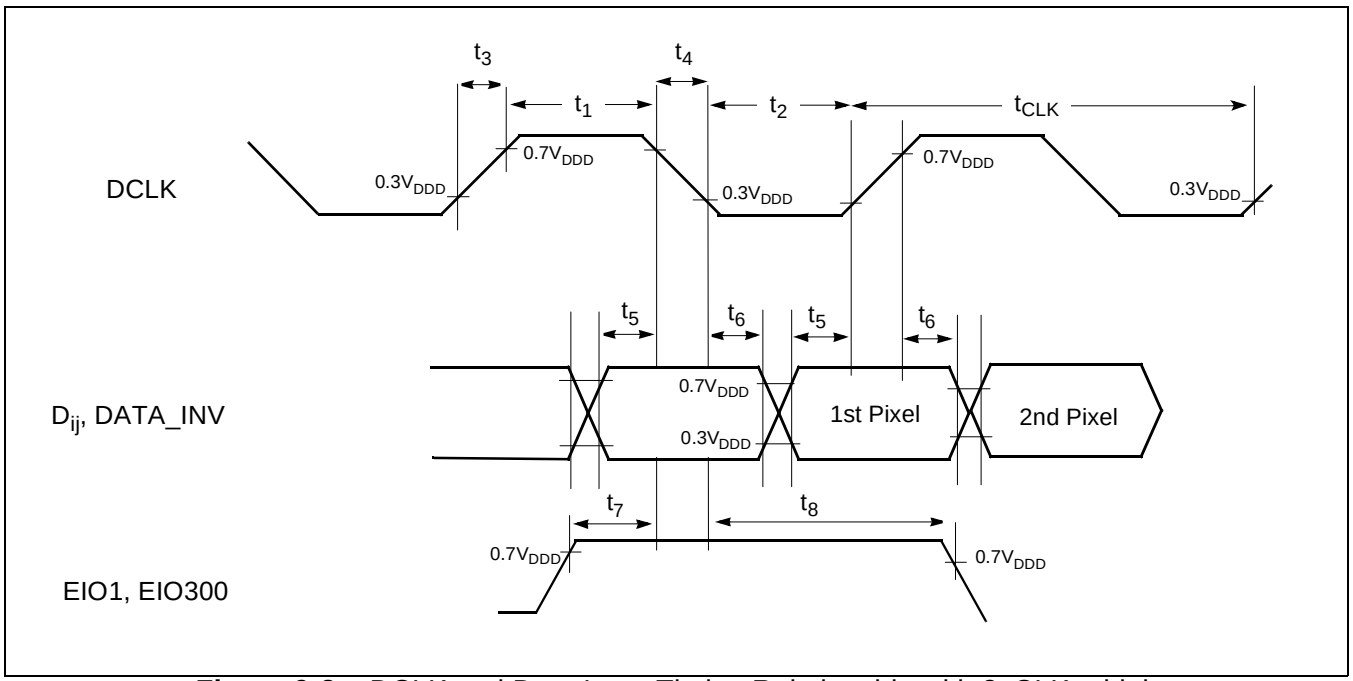


Figure 9-2: DCLK and Data Input Timing Relationship with 2xCLK = high

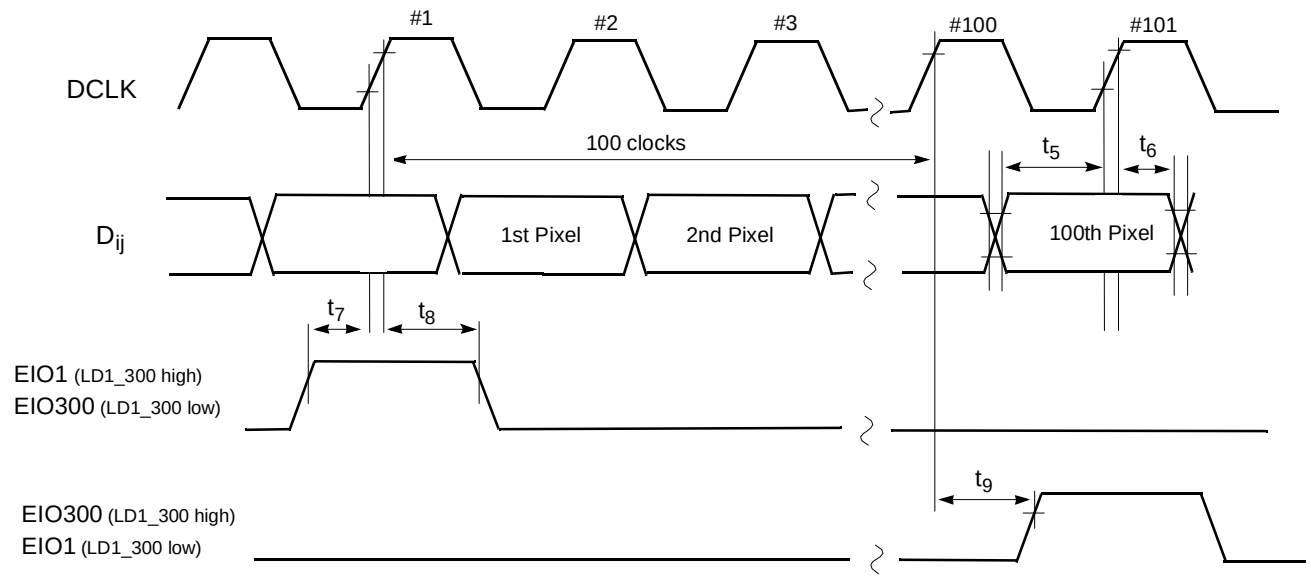


Figure 9-3: EIO1/300 Timing (2xCLK = low)

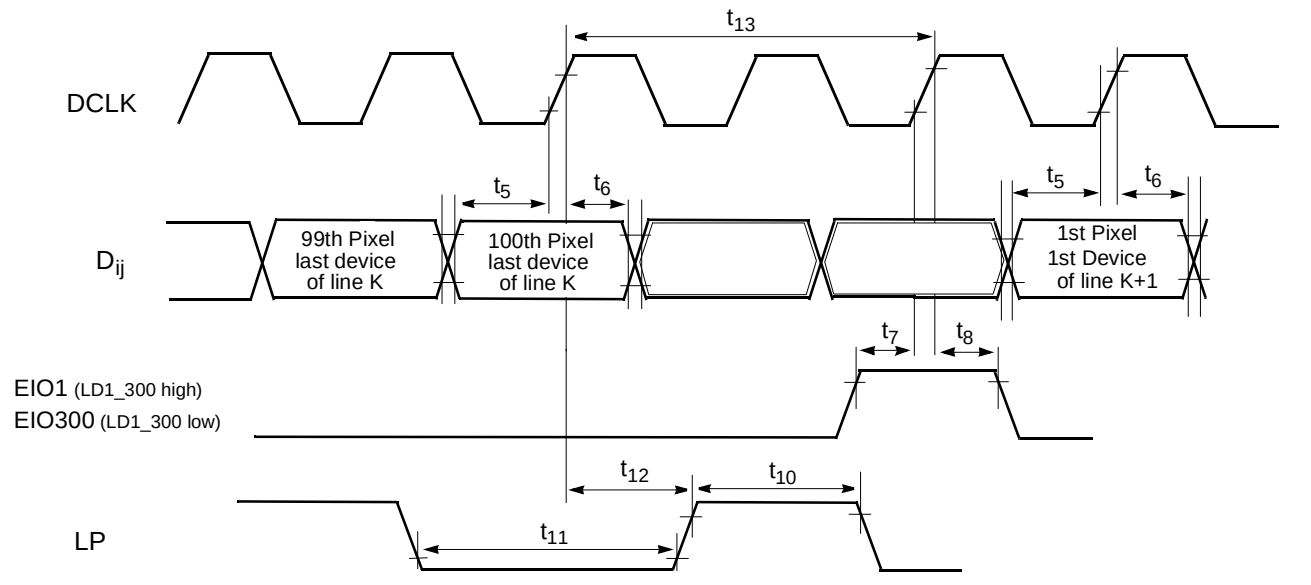


Figure 9-4: End of Line Timing (2xCLK = low)

notes: 1) Figure 9-4 shows minimum blanking time (t_{13} = 2 clocks)

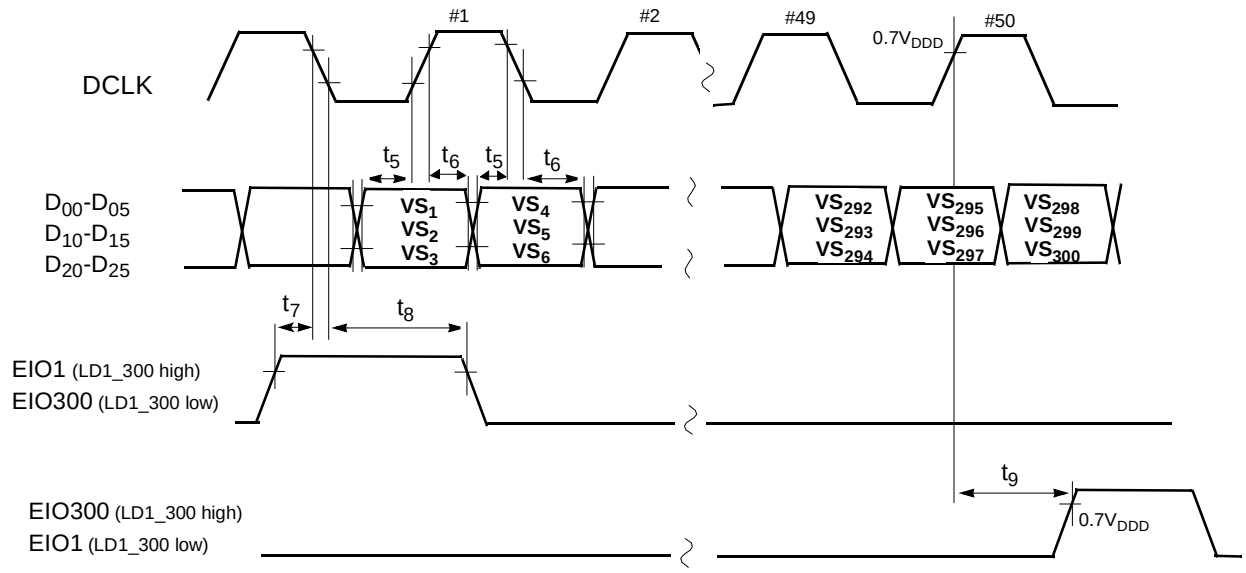


Figure 9-5: EIO1/300 Timing (2xCLK = high)

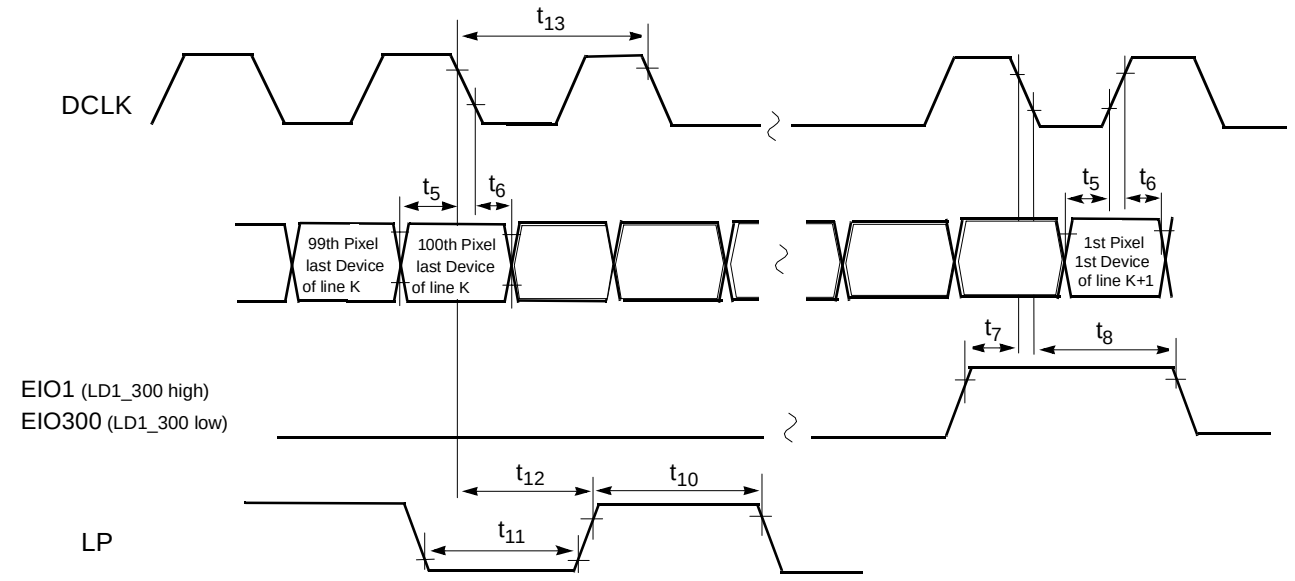


Figure 9-6: End of Line Timing (2xCLK = high)

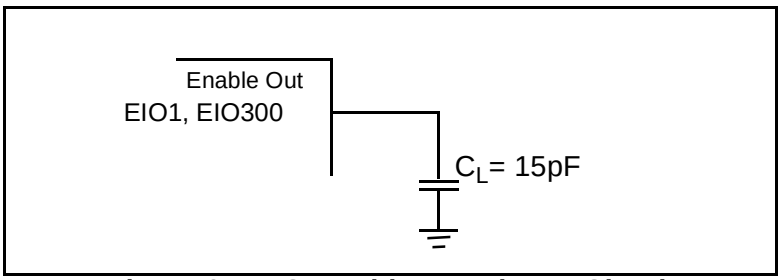


Figure 9-7: Capacitive Load Test Circuit