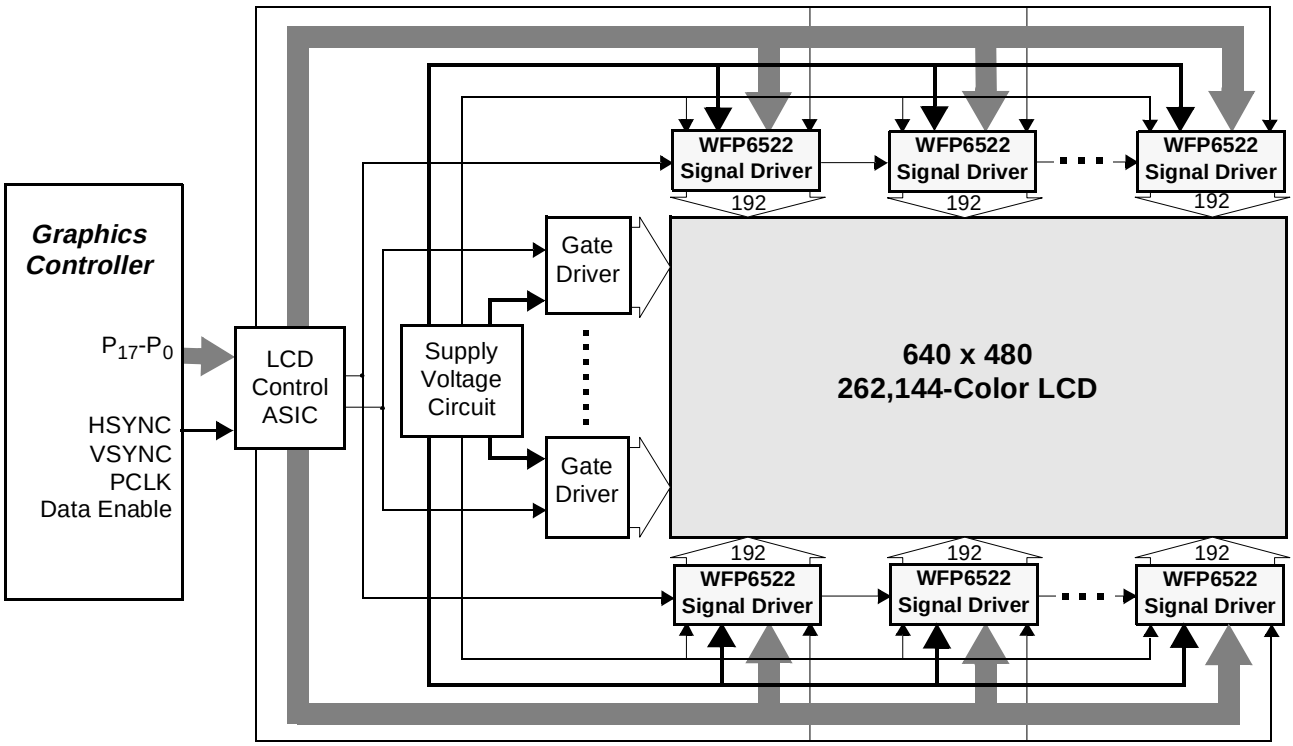
6-Bit 6.5 Volt Source Driver
(For LCD Column Driving Applications)

1. Product Description

- Full Color Display
  - 64 distinct gray levels per each sub-pixel
  - 262,144 simultaneous colors
- High Speed Operation
  - 55 MHz operation (5.0 V logic supply)
  - 40 MHz operation (3.3 V logic supply)
- High Integration
  - 192 output voltage channels
  - Bi-directional shift register
  - Row buffer updates all output channels simultaneously
  - Internal chip enable signal generator
- Low Power Operation
  - Logic supply: 3.3 V ± 0.3 V (or 5.0 V ± 0.5 V)
  - Analog supply voltage: Up to 6.5 V
  - Automatic standby-by function
- Highly Accurate Voltage Generation
  - Output voltage transition band: Up to 5.0 V
  - Output error (max): ±12 mV
  - LCD operation with wide transition band (up to 5.0 V) with low-power 3.3 V digital interface

APPLICATIONS

- Color and monochrome TFT-LCDs with resolutions:
  - 640x480 pixels
  - 800 x 600pixels
- Color and monochrome STN-LCDs with resolutions:
  - 640x480 pixels
  - 800 x 600pixels



2. Features & Benefits

Features	Benefits
■ 64 output voltage levels per channel	■ 64 gray scales per primary color ■ 262,144 (256K) color palette
■ 9 input voltage references	■ Supports User Defined T-V curve
■ High speed operation • 40 MHz (3.3 V logic supply) • 55 MHz (5 V logic supply)	■ Support for wide range of LCD resolutions • Single driver bank supports up to 800 x 600-color LCDs • Dual driver banks support up to 1280 x 1024-color LCDs
■ High integration • 192 output voltage channels • Bi-directional shift register	■ Minimizes external components and circuitry • Only 12 drivers to support 800 x 600-color LCD • Easy re-configuration from backlit operation to overhead projector (OHP) operation
■ Low-power operation • 3.3 V digital interface option • Automatic standby function	■ Extends battery-based operation • Low power from 3.3 V operation ■ Minimum dynamic-power dissipation
■ Separate digital and analog power inputs ■ Internal voltage level shifting	■ Wide transition band with 3.3 V digital inputs
■ Key specifications: • ±12 mV Output Error • 6.5 Volt output transition band • Drives up to 120 pF column capacitance	■ Superior display quality • Excellent channel-to-channel uniformity • High contrast ratio • Drives highly capacitive LCDs • Fast charging of liquid crystal material
■ 35 pins on input side	■ Minimizes LCD interconnects ■ Enables 0.5 to 0.6 mm pitch on TCP's input OLB

3. Die Pad Coordinates

Table 3–1: Input Signal Bonding Pad Coordinates

Pad #	Signal Name	x Coordinate (in μm)	y Coordinate (in μm)
1	EIO2#	7653.6	689.8
2	D_{25}	7228.4	689.8
3	D_{24}	6803.2	689.8
4	D_{23}	6378.0	689.8
5	D_{22}	5952.8	689.8
6	D_{21}	5527.6	689.8
7	D_{20}	5102.4	689.8
8	D_{15}	4677.2	689.8
9	D_{14}	4252.0	689.8
10	D_{13}	3826.8	689.8
11	D_{12}	3401.6	689.8
12	D_{11}	2976.4	689.8
13	D_{10}	2551.2	689.8
14	DCLK	2126.0	689.8
15	VDDD	1700.8	689.8
16	VDDA	1275.6	689.8
17	V_4	850.4	689.8
18	V_3	425.2	689.8
19	V_6	0.0	689.8
20	V_1	-425.2	689.8
21	V_8	-850.4	689.8
22	V_0	-1275.6	689.8
23	V_7	-1700.8	689.8
24	V_2	-2126.0	689.8
25	V_5	-2551.2	689.8
26	GNDA	-2976.4	689.8
27	GNDD	-3401.6	689.8
28	Reserved	-3826.8	689.8
29	D_{05}	-4252.0	689.8
30	D_{04}	-4677.2	689.8
31	D_{03}	-5102.4	689.8
32	D_{02}	-5527.6	689.8
33	D_{01}	-5952.8	689.8
34	D_{00}	-6378.0	689.8
35	LP	-6803.2	689.8
36	DIR	-7228.4	689.8
37	EIO1#	-7653.6	689.8

Pin #	Signal	x Coordinate (in μm)	y Coordinate (in μm)
38	Dummy	-8078.8	689.8
39	Dummy	-8080	-689.8
40	V_{S1}	-8000	-689.8
41	V_{S2}	-7920	-689.8
42	V_{S3}	-7840	-689.8
43	V_{S4}	-7760	-689.8
44	V_{S5}	-7680	-689.8
45	V_{S6}	-7600	-689.8
46	V_{S7}	-7520	-689.8
47	V_{S8}	-7440	-689.8
48	V_{S9}	-7360	-689.8
49	V_{S10}	-7280	-689.8
50	V_{S11}	-7200	-689.8
51	V_{S12}	-7120	-689.8
52	V_{S13}	-7040	-689.8
53	V_{S14}	-6960	-689.8
54	V_{S15}	-6880	-689.8
55	V_{S16}	-6800	-689.8
56	V_{S17}	-6720	-689.8
57	V_{S18}	-6640	-689.8
58	V_{S19}	-6560	-689.8
59	V_{S20}	-6480	-689.8
60	V_{S21}	-6400	-689.8
61	V_{S22}	-6320	-689.8
62	V_{S23}	-6240	-689.8
63	V_{S24}	-6160	-689.8
64	V_{S25}	-6080	-689.8
65	V_{S26}	-6000	-689.8
66	V_{S27}	-5920	-689.8
67	V_{S28}	-5840	-689.8
68	V_{S29}	-5760	-689.8
69	V_{S31}	-5680	-689.8
70	V_{S31}	-5600	-689.8
71	V_{S32}	-5520	-689.8
72	V_{S33}	-5440	-689.8
73	V_{S34}	-5360	-689.8
74	V_{S35}	-5280	-689.8
75	V_{S36}	-5200	-689.8
76	V_{S37}	-5120	-689.8
77	V_{S38}	-5040	-689.8
78	V_{S39}	-4960	-689.8
79	V_{S40}	-4880	-689.8
80	V_{S41}	-4800	-689.8
81	V_{S42}	-4720	-689.8
82	V_{S43}	-4640	-689.8
83	V_{S44}	-4560	-689.8
84	V_{S45}	-4480	-689.8
85	V_{S46}	-4400	-689.8
86	V_{S47}	-4320	-689.8
87	V_{S48}	-4240	-689.8
88	V_{S49}	-4160	-689.8
89	V_{S50}	-4080	-689.8
90	V_{S51}	-4000	-689.8
91	V_{S52}	-3920	-689.8
92	V_{S53}	-3840	-689.8
93	V_{S54}	-3760	-689.8
94	V_{S55}	-3680	-689.8
95	V_{S56}	-3600	-689.8
96	V_{S57}	-3520	-689.8
97	V_{S58}	-3440	-689.8
98	V_{S59}	-3360	-689.8
99	V_{S60}	-3280	-689.8
100	V_{S61}	-3200	-689.8
101	V_{S62}	-3120	-689.8
102	V_{S63}	-3040	-689.8
103	V_{S64}	-2960	-689.8
104	V_{S65}	-2880	-689.8
105	V_{S66}	-2800	-689.8
106	V_{S67}	-2720	-689.8
107	V_{S68}	-2640	-689.8
108	V_{S69}	-2560	-689.8
109	V_{S70}	-2480	-689.8
110	V_{S71}	-2400	-689.8
111	V_{S72}	-2320	-689.8
112	V_{S73}	-2240	-689.8
113	V_{S74}	-2160	-689.8
114	V_{S75}	-2080	-689.8
115	V_{S76}	-2000	-689.8
116	V_{S77}	-1920	-689.8
117	V_{S78}	-1840	-689.8
118	V_{S79}	-1760	-689.8
119	V_{S80}	-1680	-689.8
120	V_{S81}	-1600	-689.8
121	V_{S82}	-1520	-689.8
122	V_{S83}	-1440	-689.8
123	V_{S84}	-1360	-689.8
124	V_{S85}	-1280	-689.8
125	V_{S86}	-1200	-689.8
126	V_{S87}	-1120	-689.8
127	V_{S88}	-1040	-689.8
128	V_{S89}	-960	-689.8
129	V_{S90}	-880	-689.8
130	V_{S91}	-800	-689.8
131	V_{S92}	-720	-689.8
132	V_{S93}	-640	-689.8
133	V_{S94}	-560	-689.8
134	V_{S95}	-480	-689.8
135	V_{S96}	-400	-689.8
136	V_{S97}	-320	-689.8
137	V_{S98}	-240	-689.8
138	V_{S99}	-160	-689.8

Pin #	Signal	x Coordinate (in μm)	y Coordinate (in μm)
139	V_{S100}	-80	-689.8
140	V_{S101}	0	-689.8
141	V_{S102}	80	-689.8
142	V_{S103}	160	-689.8
143	V_{S104}	240	-689.8
144	V_{S105}	320	-689.8
145	V_{S106}	400	-689.8
146	V_{S107}	480	-689.8
147	V_{S108}	560	-689.8
148	V_{S109}	640	-689.8
149	V_{S110}	720	-689.8
150	V_{S111}	800	-689.8
151	V_{S112}	880	-689.8
152	V_{S113}	960	-689.8
153	V_{S114}	1040	-689.8
154	V_{S115}	1120	-689.8
155	V_{S116}	1200	-689.8
156	V_{S117}	1280	-689.8
157	V_{S118}	1360	-689.8
158	V_{S119}	1440	-689.8
159	V_{S120}	1520	-689.8
160	V_{S121}	1600	-689.8
161	V_{S122}	1680	-689.8
162	V_{S123}	1760	-689.8
163	V_{S124}	1840	-689.8
164	V_{S125}	1920	-689.8
165	V_{S126}	2000	-689.8
166	V_{S127}	2080	-689.8
167	V_{S128}	2160	-689.8
168	V_{S129}	2240	-689.8
169	V_{S130}	2320	-689.8
170	V_{S131}	2400	-689.8
171	V_{S132}	2480	-689.8
172	V_{S133}	2560	-689.8
173	V_{S134}	2640	-689.8
174	V_{S135}	2720	-689.8
175	V_{S136}	2800	-689.8
176	V_{S137}	2880	-689.8
177	V_{S138}	2960	-689.8
178	V_{S139}	3040	-689.8
179	V_{S140}	3120	-689.8
180	V_{S141}	3200	-689.8
181	V_{S142}	3280	-689.8
182	V_{S143}	3360	-689.8
183	V_{S144}	3440	-689.8
184	V_{S145}	3520	-689.8
185	V_{S146}	3600	-689.8
186	V_{S147}	3680	-689.8
187	V_{S148}	3760	-689.8
188	V_{S149}	3840	-689.8
189	V_{S150}	3920	-689.8
190	V_{S151}	4000	-689.8

Pin #	Signal	x Coordinate (in μm)	y Coordinate (in μm)
191	V_{S152}	4080	-689.8
192	V_{S153}	4160	-689.8
193	V_{S154}	4240	-689.8
194	V_{S155}	4320	-689.8
195	V_{S156}	4400	-689.8
196	V_{S157}	4480	-689.8
197	V_{S158}	4560	-689.8
198	V_{S159}	4640	-689.8
199	V_{S160}	4720	-689.8
200	V_{S161}	4800	-689.8
201	V_{S162}	4880	-689.8
202	V_{S163}	4960	-689.8
203	V_{S164}	5040	-689.8
204	V_{S165}	5120	-689.8
205	V_{S166}	5200	-689.8
206	V_{S167}	5280	-689.8
207	V_{S168}	5360	-689.8
208	V_{S169}	5440	-689.8
209	V_{S170}	5520	-689.8
210	V_{S171}	5600	-689.8
211	V_{S172}	5680	-689.8
212	V_{S173}	5760	-689.8
213	V_{S174}	5840	-689.8
214	V_{S175}	5920	-689.8
215	V_{S176}	6000	-689.8
216	V_{S177}	6080	-689.8
217	V_{S178}	6160	-689.8
218	V_{S179}	6240	-689.8
219	V_{S180}	6320	-689.8
220	V_{S181}	6400	-689.8
221	V_{S182}	6480	-689.8
222	V_{S183}	6560	-689.8
223	V_{S184}	6640	-689.8
224	V_{S185}	6720	-689.8
225	V_{S186}	6800	-689.8
226	V_{S187}	6880	-689.8
227	V_{S188}	6960	-689.8
228	V_{S189}	7040	-689.8
229	V_{S190}	7120	-689.8
230	V_{S191}	7200	-689.8
231	V_{S192}	7280	-689.8
232	Dummy	7360	-689.8
233	Dummy	7440	-689.8
234	Dummy	7520	-689.8
235	Dummy	7600	-689.8
236	Dummy	7680	-689.8
237	Dummy	7760	-689.8
238	Dummy	7840	-689.8
239	Dummy	7920	-689.8
240	Dummy	8000	-689.8
241	Dummy	8080	-689.8
242	Dummy	8078.8	-689.8

4. DETAILED PIN DESCRIPTIONS

The following abbreviations are used for pin types in the following sections: (I) indicates input; (O) indicates output; (I/O) indicates Input/Output, (#) indicates active 'low' signal.

Name	Number	Type	Description
DIR	34	I	**DIRECTION:** Controls the direction in which the data is loaded into the Input Register: When DIR = '0', Channel V_{S1} to V_{S192}. When DIR = '1', Channel V_{S192} to V_{S1}.
EIO1#, EIO2#	35,1	I/O	**ENABLE IN/OUT**: The EIO1# and EIO2# active 'low' signals initiate the loading of data into the Input Register of the device. One of these pins is configured as an input, while the other is configured as an output, with the direction determined by the DIR input (see Table 4-1). These pins are designed to be connected to adjacent devices to enable a series of drivers in sequence. When a 'low' is applied to the pin configured as an input on the first device in the series, data is loaded from the three sets of 6-bit Data Inputs into the first three 6-bit Input-Register locations. On subsequent transitions of the DCLK, data is loaded into the next three 6-bit Input-Register locations. When the register is full (192 words), the EIO1/2# pin, configured as an output, goes 'low', enabling the next device in the sequence. **Note**: When DIR is tied high, the EIO2# input of the first device should be connected to the LP input signal rather than ground. When DIR is tied low, the EIO1# input of the first device should be tied to the LP input. The data load sequence is defined in Table 4–1 and Figure 4–1.

Table 4–1. Input/Output Selection for EIO1# and EIO2#

DIR Input	EIO1#,EIO2# Functionality		Data Loading Sequence
	EIO1#	EIO2#	
'0'	Input	Output	Channel 1 to 192
'1'	Output	Input	Channel 192 to 1

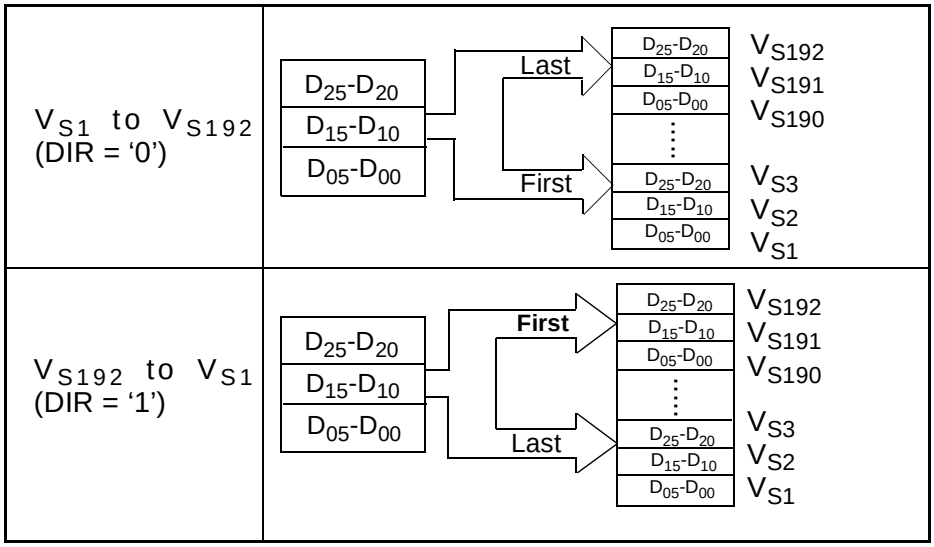


Figure 4–1. Display Data Sampling and Output Direction

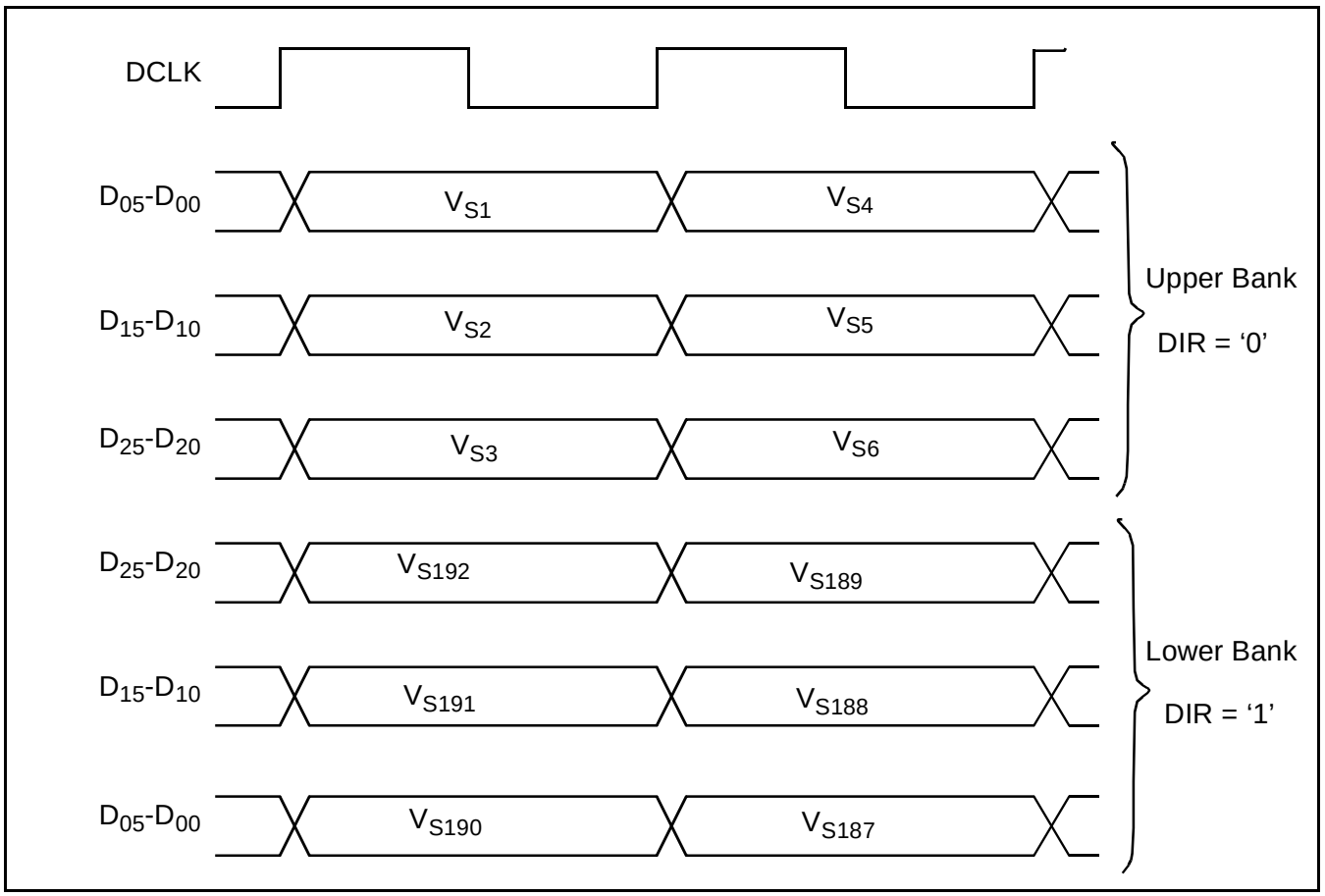


Figure 4–2. Display Data Channel Assignment and Output Sequence

V_{S1}-V_{S192}	36-227	O	**VOLTAGE OUTPUTS:** D/A outputs. Output voltage per Table 4-2.
D_{05}-D_{00} D_{15}-D_{10} D_{25}-D_{20}	27-32 8-13 2-7	I	**DATA**: The Data inputs consist of 6-bit words for each of three channels. At the falling edge of DCLK, three 6-bit words for three adjacent channels are loaded in parallel, which may be represented as Dij where: i = 2-0 indicates the channel j = 5-0 indicates the significance of the bit in each word D_{i5} indicates the MSB, and D_{i0} indicates the LSB of the input word.
LP	33	I	**LATCH PULSE**: On the 'low'-to-'high' transition on the LP input, the data is loaded from the Input Register into the Storage Register, all 192 D/A outputs are updated simultaneously, and EIO1(2)# outputs are reset to the 'high' level.
DCLK	14	I	**DATA CLOCK**: The DCLK synchronizes the 18-bit (three 6-bit channels) data word sampling, and synchronizes the internal control logic of the WFP6522. All data is sampled on the 'high'-to-'low' transition of DCLK. Please refer to **Section 5.0 Electrical-Specification** for the DCLK, LP and Data setup and hold-time relationships.
V_{DDD}	15	I	**DIGITAL SUPPLY VOLTAGE**: 3.3 +/- 0.3 or or 5.0 +/- 0.5 Volt operation is specified.
V_{DDA}	16	I	**ANALOG SUPPLY VOLTAGE**: Up to 6.5 Volts may be applied to this pin to supply the voltage for the resistive-string DAC and the output drivers.
V_8 V_7 V_6 V_5 V_4 V_3 V_2 V_1 V_0	21 23 19 25 17 18 24 20 22	I	**REFERENCE ANALOG VOLTAGE INPUTS:** These nine inputs are used to supply the adjustable-reference voltage inputs to the resistive-string DAC to provide the transmissivity-voltage response required for each type of LCD panel.
GND	26	I	**GROUND**

Table 4-2: Input Display Data vs. Output Voltage

MSB	Display Data				LSB	Refer. Voltage	Output Voltage
D_5	D_4	D_3	D_2	D_1	D_0		
0	0	0	0	0	0	V_0, V_0	$V_0 + 1/8 \times (V_1 - V_0)$
0	0	0	0	0	1	V_0, V_1	$V_0 + 2/8 \times (V_1 - V_0)$
0	0	0	0	1	0	V_0, V_1	$V_0 + 3/8 \times (V_1 - V_0)$
0	0	0	0	1	1	V_0, V_1	$V_0 + 4/8 \times (V_1 - V_0)$
0	0	0	1	0	0	V_0, V_1	$V_0 + 5/8 \times (V_1 - V_0)$
0	0	0	1	0	1	V_0, V_1	$V_0 + 6/8 \times (V_1 - V_0)$
0	0	0	1	1	0	V_0, V_1	$V_0 + 7/8 \times (V_1 - V_0)$
0	0	0	1	1	1	V_0, V_1	V_1
0	0	1	0	0	0	V_1, V_2	$V_1 + 1/8 \times (V_2 - V_1)$
0	0	1	0	0	1	V_1, V_2	$V_1 + 2/8 \times (V_2 - V_1)$
0	0	1	0	1	0	V_1, V_2	$V_1 + 3/8 \times (V_2 - V_1)$
0	0	1	0	1	1	V_1, V_2	$V_1 + 4/8 \times (V_2 - V_1)$
0	0	1	1	0	0	V_1, V_2	$V_1 + 5/8 \times (V_2 - V_1)$
0	0	1	1	0	1	V_1, V_2	$V_1 + 6/8 \times (V_2 - V_1)$
0	0	1	1	1	0	V_1, V_2	$V_1 + 7/8 \times (V_2 - V_1)$
0	0	1	1	1	1	V_1, V_2	V_2
0	1	0	0	0	0	V_2, V_3	$V_2 + 1/8 \times (V_3 - V_2)$
0	1	0	0	0	1	V_2, V_3	$V_2 + 2/8 \times (V_3 - V_2)$
0	1	0	0	1	0	V_2, V_3	$V_2 + 3/8 \times (V_3 - V_2)$
0	1	0	0	1	1	V_2, V_3	$V_2 + 4/8 \times (V_3 - V_2)$
0	1	0	1	0	0	V_2, V_3	$V_2 + 5/8 \times (V_3 - V_2)$
0	1	0	1	0	1	V_2, V_3	$V_2 + 6/8 \times (V_3 - V_2)$
0	1	0	1	1	0	V_2, V_3	$V_2 + 7/8 \times (V_3 - V_2)$
0	1	0	1	1	1	V_2, V_3	V_3
0	1	1	0	0	0	V_3, V_4	$V_3 + 1/8 \times (V_4 - V_3)$
0	1	1	0	0	1	V_3, V_4	$V_3 + 2/8 \times (V_4 - V_3)$
0	1	1	0	1	0	V_3, V_4	$V_3 + 3/8 \times (V_4 - V_3)$
0	1	1	0	1	1	V_3, V_4	$V_3 + 4/8 \times (V_4 - V_3)$
0	1	1	1	0	0	V_3, V_4	$V_3 + 5/8 \times (V_4 - V_3)$
0	1	1	1	0	1	V_3, V_4	$V_3 + 6/8 \times (V_4 - V_3)$
0	1	1	1	1	0	V_3, V_4	$V_3 + 7/8 \times (V_4 - V_3)$
0	1	1	1	1	1	V_3, V_4	V_4
1	0	0	0	0	0	V_4, V_5	$V_4 + 1/8 \times (V_5 - V_4)$
1	0	0	0	0	1	V_4, V_5	$V_4 + 2/8 \times (V_5 - V_4)$
1	0	0	0	1	0	V_4, V_5	$V_4 + 3/8 \times (V_5 - V_4)$
1	0	0	0	1	1	V_4, V_5	$V_4 + 4/8 \times (V_5 - V_4)$
1	0	0	1	0	0	V_4, V_5	$V_4 + 5/8 \times (V_5 - V_4)$
1	0	0	1	0	1	V_4, V_5	$V_4 + 6/8 \times (V_5 - V_4)$
1	0	0	1	1	0	V_4, V_5	$V_4 + 7/8 \times (V_5 - V_4)$
1	0	0	1	1	1	V_4, V_5	V_5
1	0	1	0	0	0	V_5, V_6	$V_5 + 1/8 \times (V_6 - V_5)$
1	0	1	0	0	1	V_5, V_6	$V_5 + 2/8 \times (V_6 - V_5)$
1	0	1	0	1	0	V_5, V_6	$V_5 + 3/8 \times (V_6 - V_5)$
1	0	1	0	1	1	V_5, V_6	$V_5 + 4/8 \times (V_6 - V_5)$
1	0	1	1	0	0	V_5, V_6	$V_5 + 5/8 \times (V_6 - V_5)$
1	0	1	1	0	1	V_5, V_6	$V_5 + 6/8 \times (V_6 - V_5)$
1	0	1	1	1	0	V_5, V_6	$V_5 + 7/8 \times (V_6 - V_5)$
1	0	1	1	1	1	V_5, V_6	V_6
1	1	0	0	0	0	V_6, V_7	$V_6 + 1/8 \times (V_7 - V_6)$
1	1	0	0	0	1	V_6, V_7	$V_6 \times 2/8 \times (V_7 - V_6)$
1	1	0	0	1	0	V_6, V_7	$V_6 + 3/8 \times (V_7 - V_6)$
1	1	0	0	1	1	V_6, V_7	$V_6 + 4/8 \times (V_7 - V_6)$
1	1	0	1	0	0	V_6, V_7	$V_6 + 5/8 \times (V_7 - V_6)$
1	1	0	1	0	1	V_6, V_7	$V_6 + 6/8 \times (V_7 - V_6)$
1	1	0	1	1	0	V_6, V_7	$V_6 + 7/8 \times (V_7 - V_6)$
1	1	0	1	1	1	V_6, V_7	V_7
1	1	1	0	0	0	V_7, V_8	$V_7 + 1/8 \times (V_8 - V_7)$
1	1	1	0	0	1	V_7, V_8	$V_7 + 2/8 \times (V_8 - V_7)$
1	1	1	0	1	0	V_7, V_8	$V_7 + 3/8 \times (V_8 - V_7)$
1	1	1	0	1	1	V_7, V_8	$V_7 + 4/8 \times (V_8 - V_7)$
1	1	1	1	0	0	V_7, V_8	$V_7 + 5/8 \times (V_8 - V_7)$
1	1	1	1	0	1	V_7, V_8	$V_7 + 6/8 \times (V_8 - V_7)$
1	1	1	1	1	0	V_7, V_8	$V_7 + 7/8 \times (V_8 - V_7)$
1	1	1	1	1	1	V_7, V_8	V_8

5. ELECTRICAL SPECIFICATIONS

5.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Notes
V_{DDD}	Digital Power Supply Voltage	-0.3	7.0	Volts	1,2
V_{DDA}	Analog Power Supply Voltage	-0.3	7.0	Volts	1,2
V_8 - V_0	Analog Reference-Voltage Inputs		V_{DDA} + 0.3	Volts	1,2
V_{S192}-V_{S1}	Output Voltage	-0.3	V_{DDA} + 0.3	Volts	1,2
V_{IN}	Voltage on any Digital Input	-0.3	V_{DDD} + 0.3	Volts	1,2,3
P_D	Operating Power Dissipation		300	mW	
T_A	Operating Temperature (Ambient Temperature under bias)	-10	85	°C	1
T_{STR}	Storage Temperature	-20	85	°C	1

NOTES: 1) Stresses above those listed may cause permanent damage to system components. These are stress ratings only. Functional operation at these or any conditions above those indicated in the operational ratings of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

2) All voltages are with respect to ground (GND) unless otherwise noted.

3) For D_{25}-D_{20}, D_{15}-D_{10}, D_{05}-D_{00}, DCLK, LP, EIO1# and EIO2# input pins

5.2 Recommended Operating Conditions

Symbol	Parameter	Min	Typical	Max	Units	Notes
V_{DDD}	Digital Supply Voltage	3.0 4.5	3.3 5.0	3.6 5.5	Volts Volts	1 1
V_{DDA}	Analog Supply Voltage	4.5	5.0	6.5	Volts	1
T_A	Ambient Temperature	-20	25	75	°C	

NOTES: 1) All voltages are with respect to ground unless otherwise noted.

5.3 DC Characteristics (Preliminary data – subject to change)

V_{DDA} = 6.5 ± 0.5 Volts, T_A = 25° C, unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions	Note
V_S	Analog Output Voltage	0.03		VDDA - 0.03	Volts		1
V_{ERR}	Analog Output Voltage Output Error	-12		+12	mV		2
V_{IH}	Logic Input 'high' Voltage	$0.8V_{DDD}$			Volts		3
V_{IL}	Logic Input 'low' Voltage			$0.2V_{DDD}$	Volts		3
V_{OH}	Logic Output 'high' Voltage	V_{DDD} - 0.4			Volts	I_{OH} = - 0.4 mA	4
V_{OL}	Logic Output 'low' Voltage			0.4	Volts	I_{OL} = 0.4 mA	4
I_{QR}	Reference Quiescent Current	1.75	2.3	3.3	mA		5
I_{DDA}	Analog Supply Current			500	µA	V_{DDA} = 6.5 V	8
I_{DDD}	Digital Supply Current (active)		4.5 7	7 10	mA mA	V_{DDD} = 3.3 V V_{DDD} = 5.0 V	6
I_{DDD}	Digital Supply Current (standby)		0.2 0.3	0.4 0.6	mA mA	V_{DDD} = 3.3 V V_{DDD} = 5.0 V	7
I_{IN}	Input Leakage Current	-5		+5	µA	$0V < V_{IN} < V_{DDD}$	
C_{IN}	Input Capacitance			5	pF	Digital I/O	
R_{String}	R between adjacent V_{REF} Pins	190	270	350	Ω		9
R_{OUT}	Driver Output Resistance	0.9		21	kΩ		6

NOTES:
1) See Table 4-2 for code-voltage relationship
2) At the center of the Transition Band
3) DCLK, LP, D_{25}-D_{20}, D_{15}-D_{10}, D_{05}-D_{00}, EIO1# and EIO2# inputs
4) EIO1#, EIO2#
5) Quiescent current between V_0 and V_8 with linearly spaced V_0..V_8 and $|V_8-V_0|$= 5.0 V
6) f_{clk} = 12.5 MHz, f_{LP} = 30 kHz, and device is enabled (100% of data lines toggle each clock cycle).
7) f_{clk} = 12.5 MHz, f_{LP} = 30 kHz, and device is disabled (100% of data lines toggle each clock cycle).
8) f_{LP} = 30 KHz, 100% of driver outputs changing each line
9) The resistance is measured between adjacent Reference Voltage (V_8 - V_7, etc.) pins.

5.4 AC Characteristics (V_{DDD} = 3.3 ± 0.3 Volts)

V_{DDA} = 6.5 ± 0.5 Volts, T_A = 25° C, unless otherwise specified

Symbol	Parameter	Min	Typical	Max	Units	Note
f_{CLK}	Guaranteed DCLK frequency	40			MHz	
t_{CLK}	DCLK period	25			ns	
t_1	DCLK 'high' pulse width	10			ns	
t_2	DCLK 'low' pulse width	10			ns	
t_3	DCLK, LP rise time			10	ns	
t_4	DCLK, LP fall time			10	ns	
t_5	Data setup time to DCLK	7			ns	
t_6	Data hold time to DCLK	8.5			ns	
t_7	LP 'high' pulse width	50			ns	
t_8	Enable-In setup time to DCLK	11.5			ns	
t_9	Enable-Out 'low' delay from DCLK			10	ns	1
t_{10}	DCLK low to LP high	50			ns	
t_{11}	LP low to DCLK high	56			ns	

NOTES: 1 The output load for this test is 15 pF.

5.5 AC Characteristics (V_{DDD} = 5.0 ± 0.5 Volts)

V_{DDA} = 6.5 ± 0.5 Volts, T_A = 25° C, unless otherwise specified

Symbol	Parameter	Min	Typical	Max	Units	Note
f_{CLK}	Guaranteed DCLK frequency	55			MHz	
t_{CLK}	DCLK period	18			ns	
t_1	DCLK 'high' pulse width	6			ns	
t_2	DCLK 'low' pulse width	6			ns	
t_3	DCLK, LP rise time			10	ns	
t_4	DCLK, LP fall time			10	ns	
t_5	Data setup time to DCLK	6			ns	
t_6	Data hold time to DCLK	7.5			ns	
t_7	LP 'high' pulse width	40			ns	
t_8	Enable-In setup time to DCLK	8			ns	
t_9	Enable-Out 'low' delay from DCLK			7.5	ns	1
t_{10}	DCLK low to LP high	40			ns	
t_{11}	LP low to DCLK high	40			ns	

NOTES: 1) The output load for this test is 15 pF.

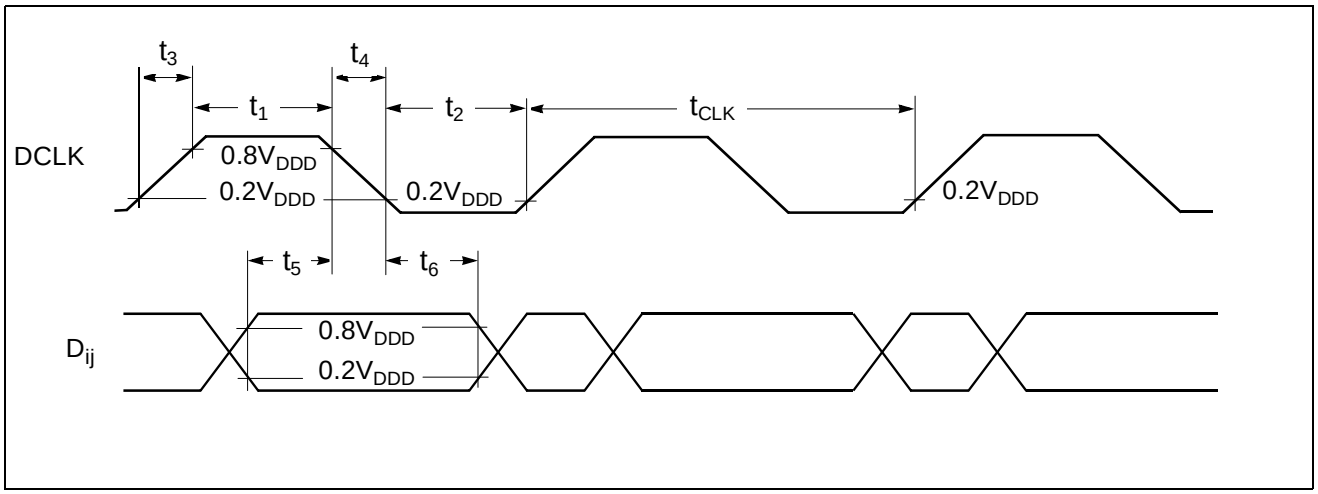


Figure 5–1: DCLK and Data Input Timing Relationship

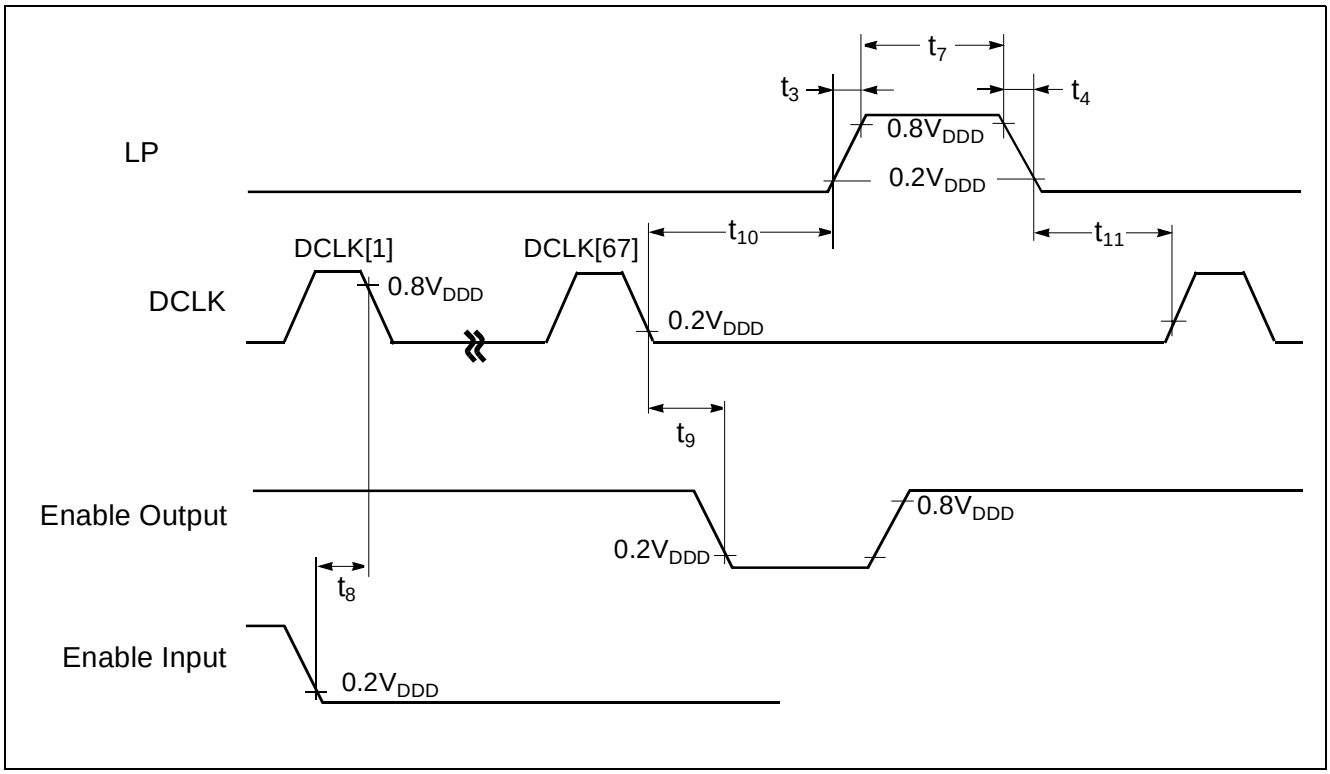


Figure 5–2: LP, DCLK, EIO1#/EIO2# and LCD Output timing relationship

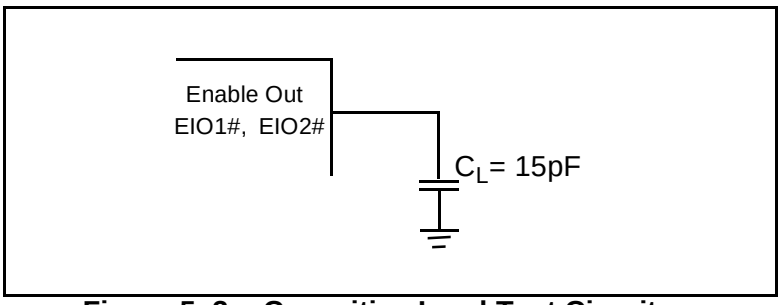


Figure 5–3: Capacitive Load Test Circuit