24-Channel Buffer Amplifier

Features

- High Integration--24 High Drive Amplifiers and 4 Multiplexers on a Chip
- High Output Current: 150mA (min)
- Low Supply Current: 8mA (typical)
- Fast Settling Time: 6usec with 150nF load
- Rail-to-Rail outputs
- Built-In Thermal Shutdown Protection
- Available in 56-pin TSSOP Package

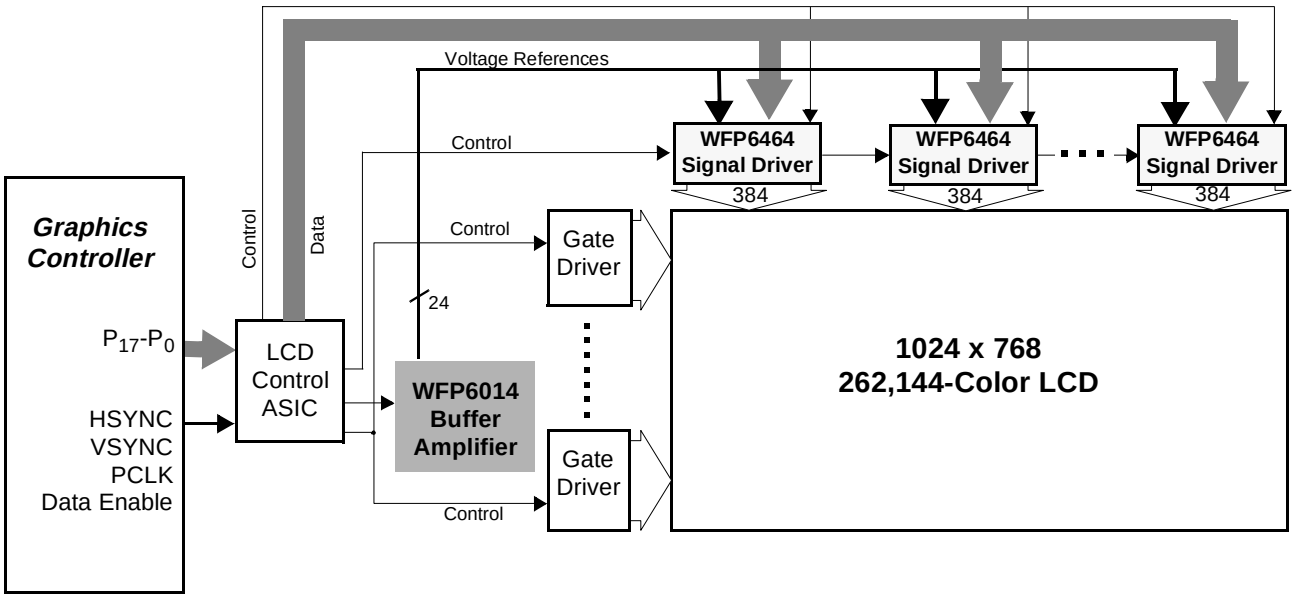
Applications

- Reference Buffer for SVGA/XGA TFT-LCD Drive Circuit
- Electronic Notebooks
- Electronic Games
- Personal Communication Devices
- Personal Digital Assistants
- Active Filters
- Multi-Voltage Buffering

Product Description

The WFP6014 is a 24-channel buffer amplifier that provides a **single-chip solution** to the reference voltage requirements of TFT-LCD column drivers. It can also be used in any **cost sensitive** application that requires a large number (24 maximum) of high drive and high performance buffers in a space saving 56-pin TSSOP package.

The amplifiers are designed for high current drive, low power, and rail-to-rail output voltage range. The device provides for automatic shutdown on thermal overload.



1. Features & Benefits

Features	Benefits
• **High Integration**	• 22 high drive amplifiers designed for fast settling. • 2 ultra high drive amplifiers (VCOM1 & VCOM2) designed for fast recovery. • 4 Internal multiplexors allow polarity-dependent reference values to be selected via a SEL input.
• **Low Power Operation**	• Analog supply voltage: 4.5 to 5.5 Volts. • Low supply headroom allows wide output dynamic range and minimizes power dissipation. • Low quiescent current of less than 0.5 mA per amplifier (typical).
• **High Performance Amplifiers**	• High drive amplifiers settle to within 50mV of final value in 6 µS with 0.15 µF load. • VCOM1 & VCOM2 amplifiers recover to with 50mV of final value in 1µS with 0.3 µF load.
• **Drives Large Load Capacitance**	• Maintains stable operation with load capacitance of 100 pF to 0.15 µF (with only 2 Ohms series resistance).
• **High current outputs**	• 400 ma short circuit current per buffer.
• **Thermal protection**	• Protects against device failure.
• **56-pin TSSOP Package**	• TSSOP package reduces cost and board space.

2. 56 Pin TSSOP Package Dimensions (millimeters)

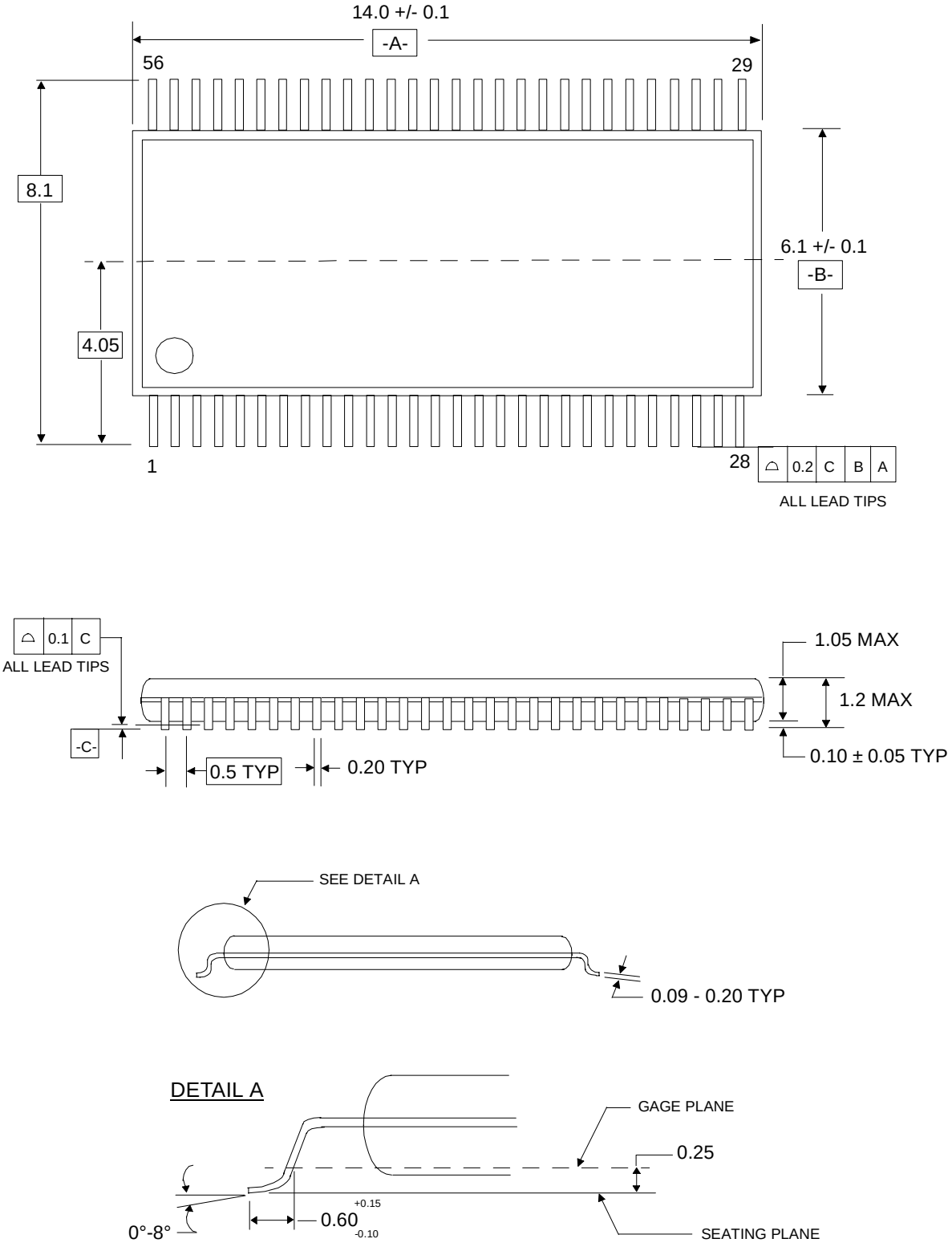
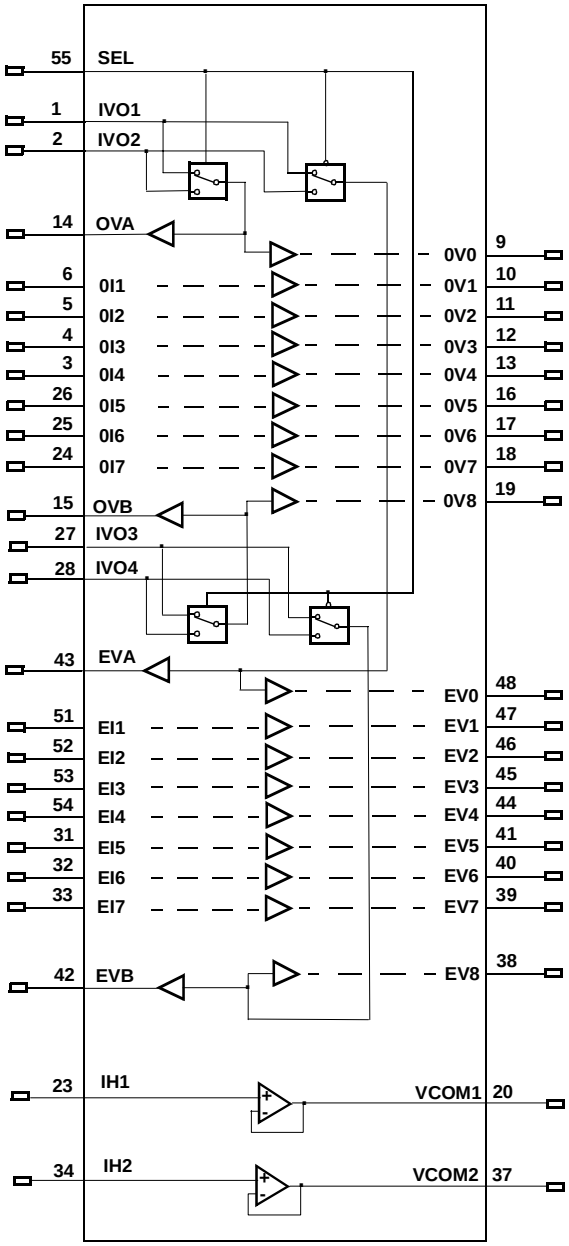


FIGURE 2-1

3. Pin Definition & Functionality



5 pins VDDA (7,22,30,35,50)
5 pins GND (8,21,29,36,49)
1 pin spare (56)

FIGURE 3-1: Pin Diagram

Switch Function

Output	Sel=0	Sel=1
OVA	IVO2	IVO1
OV0	IVO2	IVO1
OVB	IVO4	IVO3
OV8	IVO4	IVO3
EVA	IVO1	IVO2
EV0	IVO1	IVO2
EVB	IVO3	IVO4
EV8	IVO3	IVO4

4. Specifications

4.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Notes
VIN	Input Voltage	-0.3	V_{DDA} + 0.3	Volts	1
V_{DDA}	Supply Voltage	-0.3	6.0	Volts	1
I_L	Injection Current	-100	100	mA	
T_J	Junction Temperature		150	°C	
T_A	Operating temperature	-20	85	°C	2
T_{pd}	Thermal Limit Temperature	120	140	°C	
T_{STG}	Storage temperature	-55	150	°C	

Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

NOTES: 1) Voltages are with respect to ground (GND).
2) Ambient temperature under bias.

4.2 Recommended Operating Conditions (Preliminary data – subject to change)

Symbol	Parameter	Min	Typical	Max	Units	Notes
V_{DDA}	Analog supply voltage	4.5		5.5	Volts	1
T_A	Ambient air temperature	0	25	70	°C	
C_L	Output load capacitance	100pF		0.15µF		2
C_L	Output load capacitance	100pF		0.3µF		3

NOTES: 1) Voltages are with respect to GND.
2) OV0..OV8, EV0..EV8, OVA, OVB, EVA, EVB.
3) VCOM1, VCOM2

4.3. DC Characteristics (Preliminary data – subject to change)

V_{DDA} = 5.5 V, T_A = 25° C.
All voltages are with respect to GND.

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions	Note
A_V	Large Signal Gain	0.985	1.0	1.015	V/V	Fig. 4-1	1
V_{IO}	Input Offset Voltage			20	mV	Fig. 4-1	7
V_{01}	Output Voltage Range	0.2		5.3	V	Fig. 4-1	2
V_{02}	Output Voltage Range	0.2		5.3	V	Fig. 4-5	3
I_{SC}	Output Short Circuit Current	0.4			A	Fig. 4-3	4
I_{VDDA}	Analog Power Supply Current		11	15	mA		7
V_{IH}	Input Logic High	2.3			V		5
V_{IL}	Input logic low			0.8	V		5
I_{IN}	Input Leakage Current	-5.0		5.0	µA	$0 < V_{IN} < V_{DDA}$	6

NOTES: 1) R_L = 1k and V_X = 0.0 V; VOUT = 2.5V. Applies to all amplifiers.
2) -30 mA < I_{OUTDC} < 30mA. Applies to EV0..EV8, OV0..OV8, EVA, EVB, OVA, OVB.
3) Applies to VCOM1, VCOM2. For conditions see Fig 4-5
4) Applies to all amplifiers
5) Applies to SEL input pin
6) Applies to all input pins
7) Outputs are not loaded

4.4. AC Characteristics (Preliminary data – subject to change)

V_{DDA} = 5.5 V +/- 0.1V, T_A = 25° C.
All voltages are with respect to GND.

OV0..8,EV0..8,OVA,OVB,EVA,EVB

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions	Note
T_{SET}	Settling Time			6.0	µsec	Fig. 4-2	1
SR+,SR-	Pos. & Neg. Slew Rate	1.2			V/µsec	Fig. 4-2	1,2
VCOM1,2							
$T_{SETvcom}$	Settling Time		6.0		µsec	Fig. 4-5	3
T_{REC}	Recovery Time			1.0	µsec	Fig. 4-4	4

NOTES: 1) -30 mA < I_{OUTDC} < 30mA. R_S=2 Ω, C_L = 0.15 µF.
Measured for a 5V step settling to within 50 mV of final value.

2) Slew rate measured between 20% and 80% points of step.

3) Measured for a 5.1V step settling to within 50 mV of final value.

4) R_S=2 Ω, C_L= 0.3 uF. Time to recover to within 50 mV of final voltage after switch (see Figure 4-4) closes at T = 0, applying Vs to amplifier per table below:

Case	VCOM1,2	V_S
A	2.75	0.2
B	2.75	5.3

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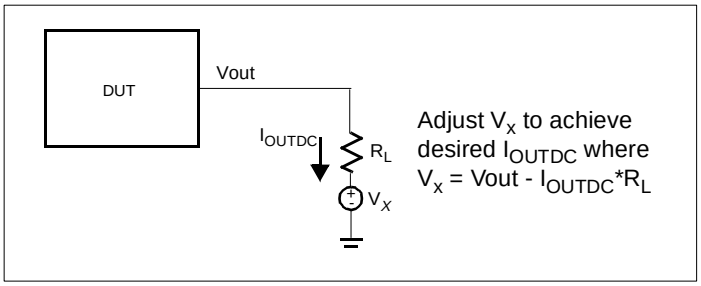


Figure 4-1

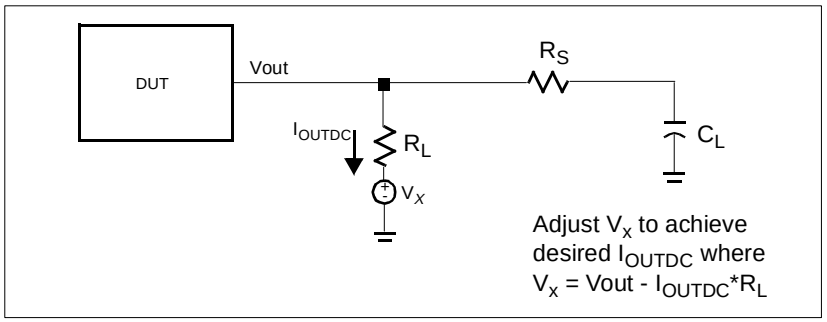


Figure 4-2

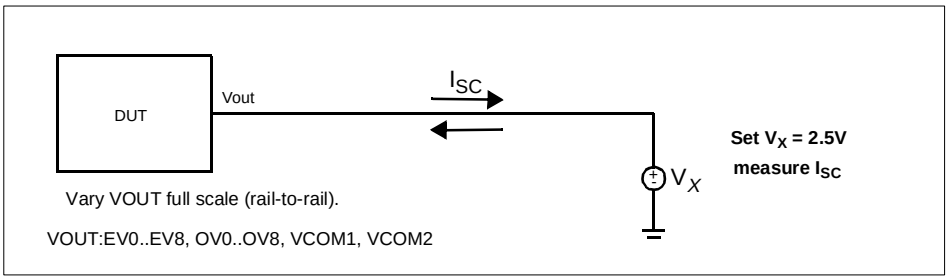
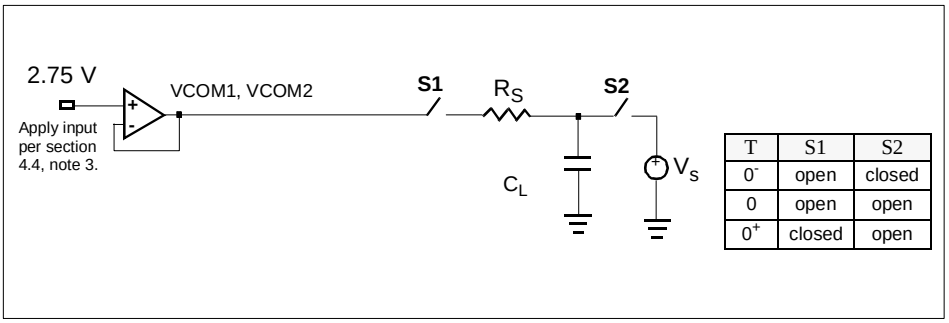


Figure 4-3



T	S1	S2
0^-	open	closed
0	open	open
0^+	closed	open

Figure 4-4

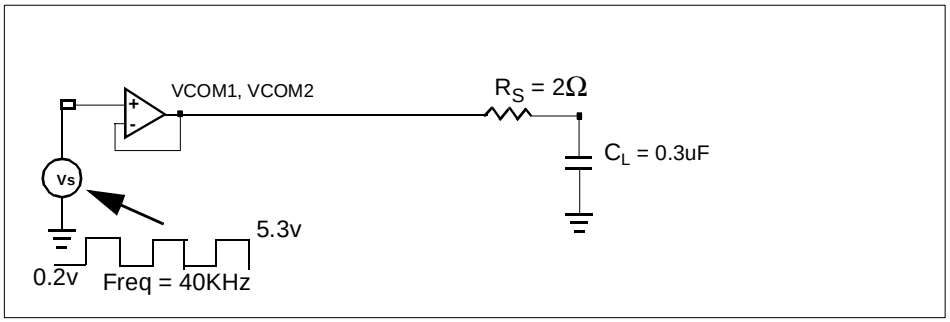
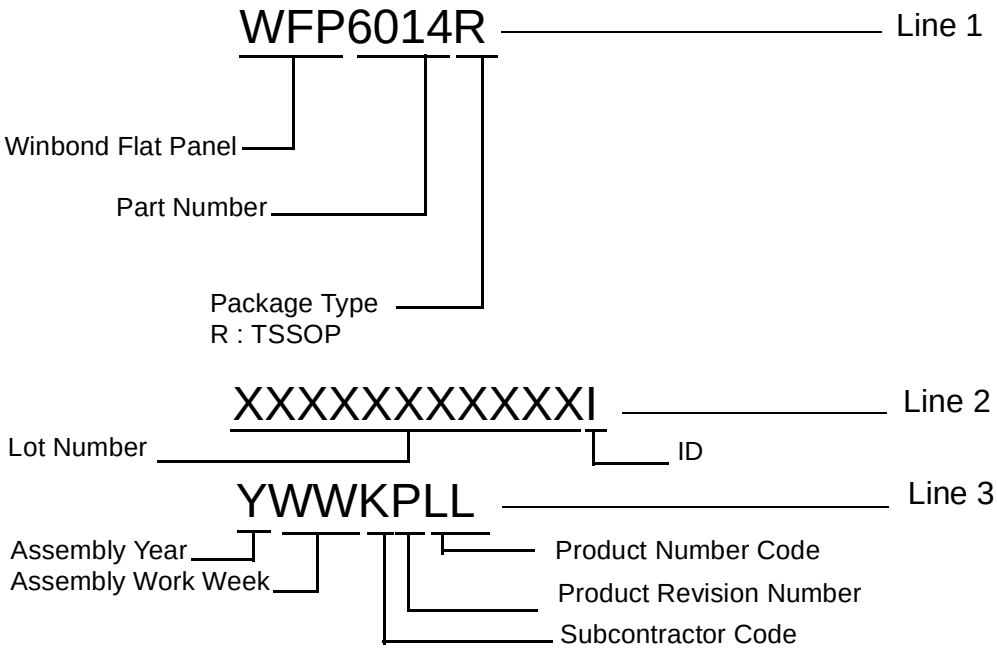


Figure 4-5

5. Package Marking Guide



Date of Issue	Description of Changes in Rev. 0.02
April 20, 2000	• Changed overall package thickness from 1.1 mm to 1.2 mm MAX. • Changed package body thickness from 0.8~1.05 mm to 1.05 mm MAX • Changed package lead width from 0.17~0.27 mm TYP to 0.2 mm TYP.