POCSAG MICROCONTROLLER

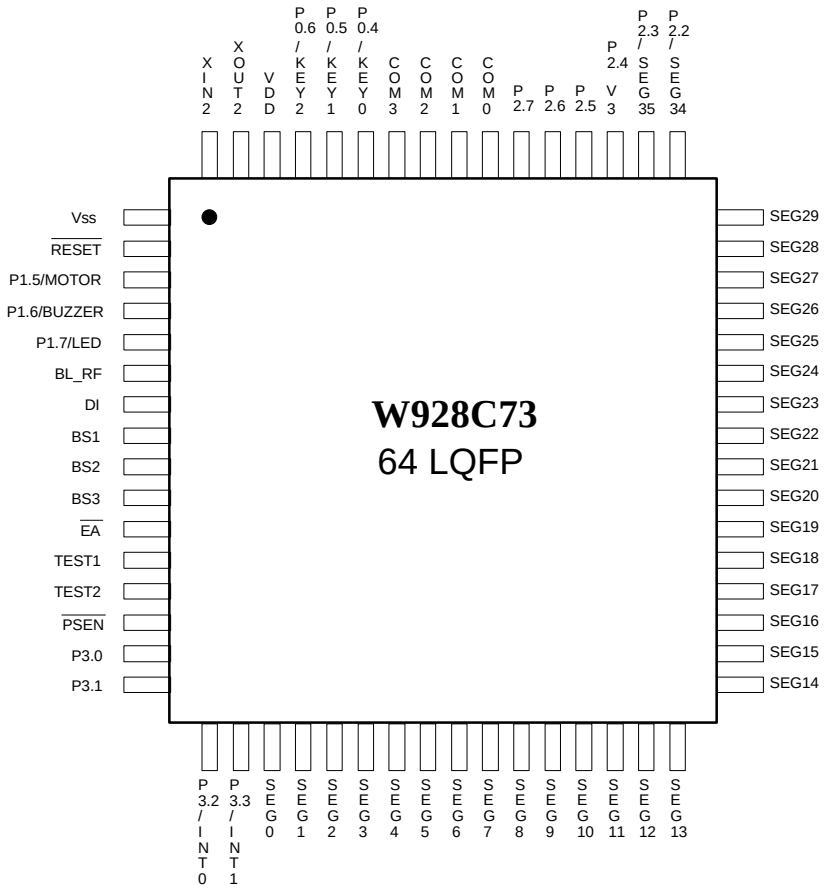
GENERAL DESCRIPTION

The W928C73 is a high performance 8 bits microcontroller with build-in POCSAG decoder and LCD driver. It is possible to switch the normal mode, idle mode and power down mode for power saving purpose. The W928C73 is an extended μC from standard 8031 (excluding UART) that it can be easily applied to pager system or other telecommunication system.

FEATURES

- 512, 1200 and 2400 bps POCSAG decoder
- 6 independent user addresses
- Instruction set compatible with MCS51
- System clock
  - OSC2: 76.8 KHz
- 128 bytes on-chip fast RAM
- 384 bytes on-chip MOVX RAM
- 16K bytes on-chip program ROM
- 32 × 32 bits on-chip flash RAM
- Timer
  - Two 16-bit timer/counters
  - One RTC timer
  - One Watch-dog timer
  - One Buzzer timer
- Four 8-bit bit-addressable I/O ports
- Three external interrupt source, INT0, INT1 (BAT_DET_INT), INT3 (KEY_INT)
- Battery low detector
- Battery detector
- Power fail detector
- Power down wake-up via external interrupts
- Two 16-bit Data Pointers (Selected by DPS.0)
- 10 source, 10 vector interrupts structure with two priority-level interrupts
- Built-in programmable power-saving modes - Idle mode & Power-down mode
- Operating voltage range: 2.4V to 3.3V
- 32 segment × 4 common, 1/3 bias, 1/4 duty LCD driver output
- Packaged in 64-pin LQFP

PIN CONFIGURATION



PIN DESCRIPTIONS

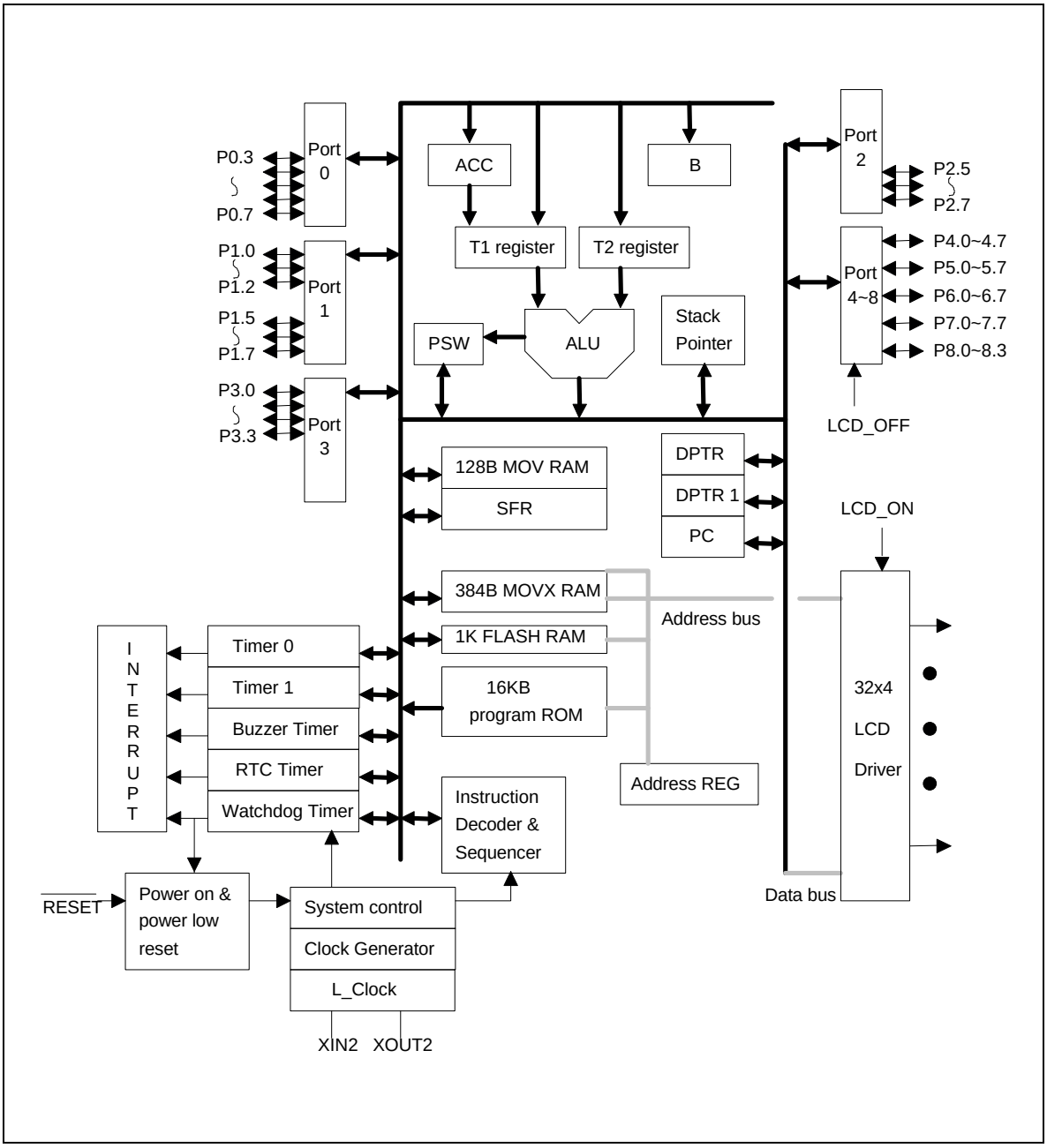
SYMBOL	TYPE	DESCRIPTIONS
VSS	I	GROUND: ground potential
$\overline{RST}$	I H	RESET: A low on this pin for two machine cycles while the oscillator is running resets the device.
P1.5	O	Motor output, hi-drive
P1.6	O	Buzzer clock output, hi-drive
P1.7	O	LED output, hi-drive
BL_RF	I	Connect to LVS of IF chip
DI	I	POCSAG signal input
BS1	O	RF control 1
BS2	O	RF control 2
BS3	O	RF control 3
$\overline{EA}$	I	External access enable pin. Should connect to VDD.
TEST1	I	No connection. Test pin. Internal pull low
TEST2	I	No connection. Test pin. Internal pull low
$\overline{PSEN}$	O	No connection. Test pin.
P3.0	I/O	Bit addressable general I/O port 3.0
P3.1	I/O	Bit addressable general I/O port 3.1
P3.2/INT0	I/O	Bit addressable general I/O port 3.2 or INT0 defined by SFR
P3.3/INT1	I	Battery fail interrupt input. Connect to V1.5. If voltage potential of battery is less than the 0.8V, the INT1 interrupt flag will be set.
SEG0	O	LCD segment signal out
SEG1	O	LCD segment signal out
SEG2	O	LCD segment signal out
SEG3	O	LCD segment signal out
SEG4	O	LCD segment signal out
SEG5	O	LCD segment signal out
SEG6	O	LCD segment signal out
SEG7	O	LCD segment signal out
SEG8	O	LCD segment signal out
SEG9	O	LCD segment signal out
SEG10	O	LCD segment signal out
SEG11	O	LCD segment signal out
SEG12	O	LCD segment signal out
SEG13	O	LCD segment signal out

Pin Descriptions, continued

SYMBOL	TYPE	DESCRIPTIONS
SEG14	O	LCD segment signal out
SEG15	O	LCD segment signal out
SEG16	O	LCD segment signal out
SEG17	O	LCD segment signal out
SEG18	O	LCD segment signal out
SEG19	O	LCD segment signal out
SEG20	O	LCD segment signal out
SEG21	O	LCD segment signal out
SEG22	O	LCD segment signal out
SEG23	O	LCD segment signal out
SEG24	O	LCD segment signal out
SEG25	O	LCD segment signal out
SEG26	O	LCD segment signal out
SEG27	O	LCD segment signal out
SEG28	O	LCD segment signal out
SEG29	O	LCD segment signal out
P2.2/SEG34	O	LCD segment signal out
P2.3/SEG35	O	LCD segment signal out
P2.4/V_{DD}3	I	LCD voltage input (V_{DD})
P2.5	I/O	I/O pin
P2.6	I/O	I/O pin
P2.7	I/O	I/O pin
COM0	O	LCD common signal output pins.
COM1	O	LCD common signal output pins.
COM2	O	LCD common signal output pins.
COM3	O	LCD common signal output pins.
P0.4	I	Bit addressable general I/O port 0.4 and Key_0 interrupt
P0.5	I	Bit addressable general I/O port 0.5 and Key_1 interrupt
P0.6	I	Bit addressable general I/O port 0.6 and Key_2 interrupt
V_{DD}	I	POWER SUPPLY: Supply voltage for operation.
XOUT2	O	Output pin for clock_2. It is the inversion of XIN2.
XIN2	I	Input pin for clock_2

Note 1: I/O TYPE I: input, O: output, I/O: bi-directional, H: pull-high, L: pull-low, D: open drain

BLOCK DIAGRAM



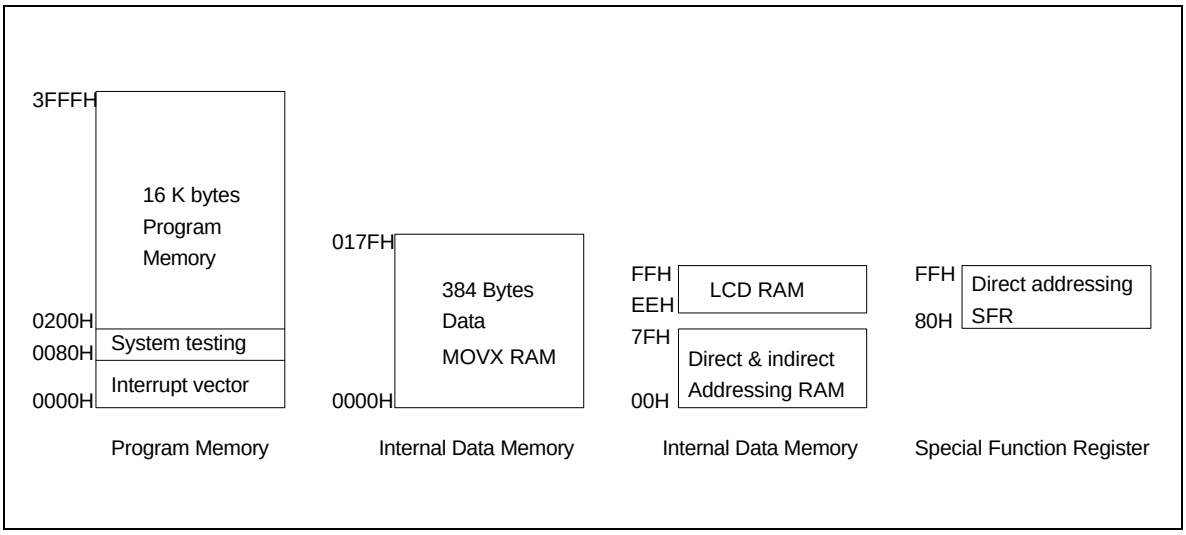
FUNCTIONAL DESCRIPTION

The W928C73 is a high performance 8 bits POCSAG microcontroller with build-in LCD driver and POCSAG decoder. The uC is 8031 instruction set compatible with one addition: DEC DPTR (op-code A5H, the DPTR is decreased by 1). The W928C73 has all the standard features of the 8031 except the UART, and has a few extra peripherals and features like watchdog, RTC, buzzer timers, LCD driver, and build-in POCSAG decoder.

The W928C73 features a faster running and better performance 8-bit CPU by reducing the machine cycle duration from the standard 8031 period of twelve clocks to four clock cycles for the majority of instructions. The W928C73 also provides dual Data Pointers (DPTRs) to speed up block data memory transfers. In addition, the W928C73 contains on-chip 384B MOVX SRAM. It only can be accessed by MOVX instruction; this on-chip data memory can be enabled by software commend.

Memory Organization

The W928C73 separates the memory into two sections, the Program Memory and Data Memory. The Program Memory is used to store the instruction op-codes, while the Data Memory is used for storing data or memory mapped devices. The $\overline{EA}$ pin must connect to high to access on-chip program ROM.



On-chip memory space of W928C73

Stack

The scratch-pad RAM can be used for the stack. This area is selected by the Stack Pointer (SP), which stores the address of the top of the stack. Whenever a jump, call or interrupt is invoked the return address is placed on the stack. There is no restriction as to where the stack can begin in the RAM. By default however, the Stack Pointer contains 07H at reset. The user can then change this to any value desired. The SP will point to the last used value. Therefore, the SP will be incremented and then address saved onto the stack. Conversely, while popping from the stack the contents will be read first, then the SP is decreased.

LCD Data Area

When LCD ON, the indirect RAM area EEH–FFH work as the LCD data RAM (LCD00–LCD35). Instruction such as "MOV @R0, #I" (Where R0 = EEH–FFH) are used to control the LCD data RAM. The data in the LCD data RAM (bit7–bit0) are transferred to the segment output pins automatically without program control. When the bit value of the LCD data RAM is "1", the LCD is turned on. When the bit value of the LCD data RAM is "0", LCD is turned off. The relation between the LCD data RAM and segment/common pins is shows below.

LCD	COM3	COM2	COM1	COM0	COM3	COM2	COM1	COM0
Data RAM	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
EEH	SEG1				SEG0			
EFH	SEG3				SEG2			
F0H	SEG5				SEG4			
F1H	SEG7				SEG6			
F2H	SEG9				SEG8			
F3H	SEG11				SEG10			
F4H	SEG13				SEG12			
F5H	SEG15				SEG14			
F6H	SEG17				SEG16			
F7H	SEG19				SEG18			
F8H	SEG21				SEG20			
F9H	SEG23				SEG22			
FAH	SEG25				SEG24			
FBH	SEG27				SEG26			
FCH	SEG29				SEG28			
FFH	SEG35				SEG34			

Descriptions Of Special Function Registers(SFRS)

ADDRESS /NAME	BIT	BIT NAME	R/W	1	0	INITIAL	FUNCTION
80H/P0	B7		R			1	No use
	B6	Key_2	R			1	Key_2 input. A corresponding key_INT(INT3_3) can be enabled.
	B5	Key_1	R			1	Key_1 input. A corresponding key_INT(INT3_3) can be enabled.
	B4	Key_0	R			1	Key_0 input. A corresponding key_INT(INT3_3) can be enabled.
	B3	DEC_ADDT	R	Matched	Unmatched	1	POCSAG address matched flag. A corresponding INT(INT2) could be setup.
	B2	F_ADR	W			1	Flash ROM serial address output
	B1	DEC_ SYNVAL	R	SYNC	Lost SYNC	1	Decoder synchronization condition
	B0	F_data	R/W			1	Flash ROM data I/O
81H/SP	B7~0	SP	R/W			00000111	Stack pointer address. Always points to top of the stack.
82H/DPL	B7~0	DPL	R/W			00000000	Low byte of 16 bit data pointer
83H/DPH	B7~0	DPH	R/W			00000000	High byte of 16 bit data pointer
84H/DPL1	B7~0	DPL1	R/W			00000000	Low byte of 16 bit data pointer 1
85H/DPH1	B7~0	DPH1	R/W			00000000	High byte of 16 bit data pointer 1
86H/DPS	B0	DPS.0	R/W	Pointer 1	Pointer 0	0	Selection of data pointer, B7~1 are not used
87H/PCON	B7	SMOD				0	No use. Clear to “o” after power_on reset
	B6	SMOD0				0	No use. Clear to “o” after power_on reset
	B5	-				0	No use. Clear to “o” after power_on reset
	B4	-				0	No use. Clear to “o” after power_on reset
	B3	GF1				0	General purpose user defined flag
	B2	GF0				0	General purpose user defined flag
	B1	PD	W	Enable	Disable	0	Power down mode enable bit. Set this bit to “1” will stop the CPU and oscillation.
	B0	IDL	W	Enable	Disable	0	Idle mode enable bit. Set this bit to “1” will stop the CPU clock, but the oscillator keep running.
88H/TCON	B7	TF1	R/W	Overflow		0	Timer 1 overflow flag,. TF1 will automatically clear after INT service routine.
	B6	TR1	W	Enable	Disable	0	Timer 1 enable
	B5	TF0	R/W	Overflow		0	Timer 0 overflow flag, TF0 will automatically clear after INT service routine
	B4	TR0	R/W	Enable	Disable	0	Timer 0 enable
	B3	IE1 (Bat_fail)	R/W	INT	No INT	0	Interrupt 1(battery fail INT) flag. Set by hardware when a pre-selected INT level (high or low) is detected on INT1. The INT flag will keep only if the level is held.

Descriptions Of Special Function Registers (SFRS), continued

ADDRESS /NAME	BIT	BIT NAME	R/W	1	0	INITIAL	FUNCTION
	B2	IT1	R/W	High level	Low level	0	Interrupt 1 level selection. Set by software to specify high (>0.8V) / low (<0.8V) level external INT 1 triggered.
	B1	IE0	R/W	INT	No INT	0	Interrupt 0 edge detect: Set by hardware when an edge/level is detected on INT0. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the pin.
	B0	IT0	R/W	Falling edge	Low level	0	Interrupt 0 type selection. Set/cleared by software to specify falling edge/ low level triggered external inputs
89H/TMOD	B7	T1_GATE	R/W			0	Timer 1 & timer 0 control: Tx_GATE (gating control): When this bit is set, Timer/counter x will be enabled if both INTx pin is high and TRx control bit is set. When this bit is cleared, Timerx is enabled whenever TRx control bit is set. Tx_C/T (timer or counter select): When cleared, the timer is incremented by internal clocks. When set, the timer counts high-to-low edges of the Tx pin. M1 M0 Mode 0 0 8-bits with 5-bit pre-scalar. 0 1 16-bits, no pre-scalar. 1 0 8-bits with auto-reload from THx 1 1 (Timer 0) TL0 is an 8-bit timer/counter controlled by the standard Timer 0 control bits. TH0 is an 8-bit timer only controlled by Timer 1 control bits. (Timer 1) Timer/counter is stopped.
	B6	T1_T	R/W		Timer	0	
	B5	T1_M1	R/W			0	
	B4	T1_M0	R/W			0	
	B3	T0_GATE	R/W			0	
	B2	T0_T	R/W		Timer	0	
	B1	T0_M1	R/W			0	
	B0	T0_M0	R/W			0	
8AH/TL0	B7~0	TL0	R/W			00000000	Low byte of timer 0
8BH/TL1	B7~0	TL1	R/W			00000000	Low byte of timer 1
8CH/TH0	B7~0	TH0	R/W			00000000	High byte of timer 0
8DH/TH1	B7~0	TH1	R/W			00000000	High byte of timer 1
8EH/CKCON	B7	WD1	R/W			0	WD1 WD0 (watchdog timeout period) 0 0 $Fs/2^{14}$+512 clock 0 1 $Fs/2^{16}$+512 clock 1 0 $Fs/2^{18}$+512 clock 1 1 $Fs/2^{21}$+512 clock
	B6	WD0	R/W			0	
	B5	RTC1	R/W			0	RTC1 RTC0 (RTC timeout period) 0 0 32 Hz for RTLCD = 74 0 1 8 Hz 1 0 2 Hz 1 1 1 Hz
	B4	RTC0	R/W			0	

Descriptions Of Special Function Registers (SFRS), continued

ADDRESS /NAME	BIT	BIT NAME	R/W	1	0	INITIAL	FUNCTION
	B3	-	R/W			1	Set B3 and B2 to 1 after power on reset.
	B2	-	R/W			1	
	B1	ELC	R/W	Enable	Disable	1	ELC: enable L_clock. Keep this bit high for whole operation.
	B0	EHC	R/W			0	Clear to "0" after reset.
90H/P1	B7	LED	W	High	Low	1	LED output port P1.7 (HI-drive)
	B6	Buz_out	W	High	Low	1	Initial value of buzzer output pin
	B5	Motor	W	High	Low	1	Motor output pin(Hi-drive)
	B4		W			1	No use
	B3	DEC_RST	W	High	Low	1	Decoder reset control bit
	B2	DEC_ON	W	High	Low	1	Decoder enable control bit
	B1	DEC_ DATA	W	High	Low	1	Decoder option setup data output control bit
	B0	DEC_CLK	W	High	Low	1	Decoder option setup clock output control bit
91H/PBCON	B7	-	W			0	Clear B7~B2 to 0 after power on reset.
	B6	-	W			0	
	B5	-	W			0	
	B4	-	W			0	
	B3	-	W			0	
	B2	-	W			0	
	B1	ENBT	W	Enable	Disable	0	Buzzer timer enable (used as a general timer)
	B0	ENBUZ	W	Enable	Disable	0	Buzzer output enable
92H/TONE0	B7~0	TONE0	W			00000000	Auto reload value of buzzer timer
96H/PLC	B7~0	PLC	R			00000000	Low byte of program counter
97H/PLH	B7~0	PLH	R			00000000	High byte of program counter
A0H/P2	B7	P2.7	W/R	High	Low	1	I/O P2.7
	B6	P2.6	W/R			1	B6~B4 no use when LCD is on.
	B5	P2.5	W/R			1	
	B4	P2.4	W/R			1	
	B3	P2.3	W/R	High	Low	1	No use if SEG35~32 work as LCD segment. I/O P2.3 value if SEG35~32 work as P2.3~P2.0 function (P2M (A1.1H) = 0)
	B2	P2.2	W/R	High	Low	1	I/O P2.2 value if SEG35~32 work as P2.3~P2.0 function (P2M (A1.1H) = 0)
	B1	P2.1	W/R	High	Low	1	No use if SEG35~32 work as LCD segment. I/O P2.1 value if SEG35~32 work as P2.3~P2.0 function (P2M (A1.1H) = 0)

Descriptions Of Special Function Registers (SFRS), continued

ADDRESS /NAME	BIT	BIT NAME	R/W	1	0	INITIAL	FUNCTION
	B0	P2.0	W/R	High	Low	1	No use if SEG35~32 work as LCD segment. I/O P2.0 value if SEG35~32 work as P2.3~P2.0 function (P2M (A1.1H) = 0)
A1H/LCDR	B7	LCDWAVE	W	A Type	B Type	0	Clear B7~B4 to "0" after reset. Default LCDWAVE =0 (B type)
	B6	-	W			0	
	B5	-	W			0	
	B4	-	W			0	
	B3	FLCD1	W			0	FLCD1 FLCD0 LCD frequency 0 0 512 Hz, set RTLCD = 74 0 1 256 Hz 1 0 128 Hz 1 1 64 Hz LCD scan rate = LCD frequency/ 4
	B2	FLCD0	W			0	
	B1	P2M	W	SEG out	P2	0	P2.0~2.3/SEG32~35 pin function selection. This bit can only be set while LCD is on. While set to 1, these 4 pins work as SEG32~35 output. If clear to 0, these 4 pins will work as P2.0~2.3.
	B0	LCDON	W	LCD ON	LCD OFF	0	LCD driver enable control
A2H/RTLCD	B7~0	RTLCD	W			11111111	RTC timer value. Set RTLCD = 74 for 76.8 KHz crystal
A8H/IE	B7	EA	W	Enable	Disable	0	Global interrupt enable control
	B6	ES1	W	Enable	Disable	0	POCSAG receiving buffer interrupt enable control
	B5	-	W			0	Clear this bit to 0 after power on reset
	B4	-	W			0	Clear this bit to 0 after power on reset
	B3	ET1	W	Enable	Disable	0	Timer 1 interrupt enable control
	B2	EX1	W	Enable	Disable	0	External interrupt 1 (battery fail INT) enable control
	B1	ET0	W	Enable	Disable	0	Timer 0 interrupt enable control
	B0	EX0	W	Enable	Disable	0	External interrupt 0 enable control
AAH/SDTMF	B7	INT33	W	Enable	Disable	0	Clear this bit to 0 after reset
	B6	INT32	W	Enable	Disable	0	Enable INT32 (key2)
	B5	INT31	W	Enable	Disable	0	Enable INT31 (key1)
	B4	INT30	W	Enable	Disable	0	Enable INT30 (key0)
	B3	-	W			0	Clear B3~B0 after reset
	B2	-	W			0	
	B1	-	W			0	
	B0	-	W			0	

Descriptions Of Special Function Registers (SFRS), continued

ADDRESS /NAME	BIT	BIT NAME	R/W	1	0	INITIAL	FUNCTION
B0H/P3	B7	DEC_BL	R	Battery low	Battery OK	1	Battery condition. If battery voltage is lower than 1 volt, this bit will change to 1, otherwise this bit will be 0. This bit works only if BL_RF pin is connect to IF IC LVS output.
	B6	F_Mode	W	High	Low	1	Flash ROM mode control bit
	B5	F_CLK	W	High	Low	1	Flash ROM clock output bit
	B4	F_ctrl	W	High	Low	1	Flash ROM control bit
	B3	Bat_fail/ INT1	R	Battery OK	Battery fail or no battery	1	Battery fail condition. If battery voltage is lower than 0.8 volt, this bit will change to 0, otherwise this bit will be 1. An additional level interrupt(INT1) can be enabled to monitor this bit.
	B2	P3.2/INT0	R/W			1	I/O P3.2 & external interrupt 0 input
	B1	P3.1	R/W			1	I/O P3.1
	B0	P3.0	R/W			1	I/O P3.0
B2/HB	B7~0	HB	R/W			00000000	High byte address of "MOVX @Ri"
B8H/IP	B7	BTF	W	High	Low	0	Buzzer timer interrupt priority level
	B6	PS1	W	High	Low	0	POCSAG receiving buffer interrupt priority level
	B5	-	W			0	Clear this bit to 0 after reset
	B4	-	W			0	Clear this bit to 0 after reset
	B3	PT1	W	High	Low	0	Timer 1 interrupt priority level
	B2	PX1	W	High	Low	0	Interrupt 1 (INT1) interrupt priority level
	B1	PT0	W	High	Low	0	Timer 0 interrupt priority level
	B0	PX0	W	High	Low	0	Interrupt 0 (INT0) interrupt priority level
C0H/CSCON	B7	-	W			0	Clear B7~B4 to 0 after reset
	B6	-	W			0	
	B5	-	W			0	
	B4	-	W			0	
	B3	OVFH	R			0	No use
	B2	OVFL	R			0	OSC2 clock stable flag
	B1	SIF	R			0	POCSAG receiving buffer interrupt request flag
	B0	REN1	W	Enable	Disable	0	POCSAG receiving buffer enable control
C1H/SMODE	B7~0	SMODE	W			00000000	POCSAG mode control, Set SMODE = 11101101 after reset
C2H/SB1	B7~0	SB1	R			00000000	POCSAG receiving buffer 1
C3H/SB2	B7~0	SB2	R			00000000	POCSAG receiving buffer 2

Descriptions Of Special Function Registers (SFRS), continued

ADDRESS /NAME	BIT	BIT NAME	R/W	1	0	INITIAL	FUNCTION
C4H/SB3	B7~0	SB3	R			00000000	POCSAG receiving buffer 3
C9H/T2MOD	B7	DME0	W	On-chip	External	1	MOVX RAM selection (384 bytes), set to 1 after reset
	B6	-	W			0	Clear this bit to "0" after reset
	B5	-	W			0	Clear this bit to "0" after reset
	B4	-	W			0	Clear this bit to "0" after reset
	B3	-	W			0	Clear this bit to "0" after reset
	B2	TONESEL	W	PWM	50-50duty	0	Buzzer tone duty control
	B1	-	W			0	Clear this bit to "0" after reset
	B0	-	W			0	Clear this bit to "0" after reset
D0H/PSW	B7	CY	R			0	Carry flag: Set for an arithmetic operation which results in a carry being generated from the ALU. It is also used as the accumulator for the bit operations.
	B6	AC	R			0	Auxiliary carry: Set when the previous operation resulted in a carry (during addition) or a borrowing (during subtraction) from the high order nibble.
	B5	F0	R/W			0	User define flag
	B4	RS1	R/W			0	RS1 RS0 Register bank selection 0 0 Bank 0 00-07(B0-B7) 0 1 Bank 1 08-0F(B0-B7) 1 0 Bank 2 10-17(B0-B7) 1 1 Bank 3 18-1F(B0-B7)
	B3	RS0	R/W			0	
	B2	OV	R			0	Overflow flag: Set when a carry was generated from the seventh bit but not from the 8th bit as a result of the previous operation or vice-versa.
	B1	F1	R/W			0	User defined flag
	B0	P	R			0	Parity flag: Set/cleared by hardware to indicate odd/even number of 1's in the accumulator.
D8H/WDCON	B7	RTIF	R			0	RTC interrupt request flag
	B6	POR	R/W			X	Power-on reset flag: Hardware will set this flag on a power up condition. This flag can be read or written by software. A write by software is the only way to clear this bit once it is set.
	B5	-	R/W			0	Clear this be after reset
	B4	-	R/W			0	Clear this be after reset

Descriptions Of Special Function Registers (SFRS), continued

ADDRESS /NAME	BIT	BIT NAME	R/W	1	0	INITIAL	FUNCTION
D8H/WDCON	B3	WDIF	R			0	Watchdog Timer Interrupt Flag: If the watchdog interrupt is enabled, hardware will set this bit to indicate that the watchdog interrupt has occurred. If the interrupt is not enabled, then this bit indicates that the time-out period has elapsed.
	B2	WTRF				X	Watchdog Timer Reset Flag: Hardware will set this bit when the watchdog timer causes a reset. Software can read it but must clear it manually. A power-fail reset will also clear the bit. This bit helps software in determining the cause of a reset. If EWT = 0, the watchdog timer will have no affect on this bit.
	B1	EWT				X	Enable Watchdog timer Reset: Setting this bit will enable the Watchdog timer Reset function.
	B0	RWT				0	Reset Watchdog Timer: This bit helps in putting the watchdog timer into a know state. It also helps in resetting the watchdog timer before a time-out occurs. Failing to set the EWT before time-out will cause an interrupt, if EWDI (EIE.4) is set, and 512 clocks after that a watchdog timer reset will be generated if EWT is set. This bit is self-clearing.
D9H/P0IO	B7	P0IO.7	W			0	R/W control for P0.7 (key3): No use, clear this bit to 0 after.
	B6	P0IO.6	W			0	R/W control for P0.6 (key2): 1: input mode without pull high R 0: output mode or input with pull high R Clear this bit after reset for key2 input with pull high R function.
	B5	P0IO.5	W			0	R/W control for P0.5 (key1): 1: input mode without pull high R 0: output mode or input with pull high R Clear this bit after reset for key1 input with pull high R function.
	B4	P0IO.4	W			0	R/W control for P0.4 (key0): 1: input mode without pull high R 0: output mode or input with pull high R Clear this bit after reset for key0 input with pull high R function.
	B3	P0IO.3	W			0	R/W control for P0.3: Set this bit to “1” after reset for DEC_ADDT input
	B2	P0IO.2	W			0	R/W control for P0.2: Clear this bit to “0” after reset for F_ADR output function
	B1	P0IO.1	W			0	R/W control for P0.1: Set this bit to “1” after reset for DEC_SYNVAL input
	B0	P0IO.0	W			0	R/W control for P0.0: Set this bit to “1” after reset. For read-in F_data, set this bit to ”1”. For write-out F_data, clear this bit to “0”.

Descriptions Of Special Function Registers (SFRS), continued

ADDRESS /NAME	BIT	BIT NAME	R/W	1	0	INITIAL	FUNCTION
DAH/P1IO	B7~0	P1IO	W			00000000	Bit addressable R/W control for P1: 1: input mode without pull high R 0: output mode or input with pull high R Set DA to "00000000 " after reset, since P1 are all output mode.
DBH/P2IO	B7~0	P2IO	W			00000000	Bit addressable R/W control for P2 1: input mode without pull high R 0: output mode or input with pull high R Set DB to "X0000000 " after reset. The value of P2IO.7 depends on the function of P2.7 (input of output)
DCH/P3IO	B7~0	P3IO	W			00000000	Bit addressable R/W control for P3 1: input mode without pull high R 0: output mode or input with pull high R Set DC to "10001XXX " after reset. The values of P3IO.2~P3IO.0 depend on the functions of P3.2~P3.0 (input of output)
DDH/P48IO	B4	P8IO	W			0	Clear DDH to "00" after reset.
	B3	P7IO	W			0	
	B2	P6IO	W			0	
	B1	P5IO	W			0	
	B0	P4IO	W			0	
E0H/ACC	B7~0	ACC	R/W			00000000	Accumulator
E8H/EIE	B7	ERTLC	W	Enable	Disable	0	RTC timer and LCD clock enable
	B6	EBTI	W	Enable	Disable	0	Buzzer timer interrupt enable
	B5	ERTI	W	Enable	Disable	0	RTC timer interrupt enable
	B4	EWDI	W	Enable	Disable	0	Watchdog timer interrupt enable
	B3	IE3	R			0	External interrupt 3 request flag
	B2	EX3	W	Enable	Disable	0	External interrupt 3 enable
	B1	IE2	R			0	External interrupt 2 request flag
	B0	EX2	W	Enable	Disable	0	External interrupt 2 enable
F0/B	B7~0	B	R/W			00000000	B register
F8H/EIP	B7	SMSC	W	H_clock	L_clock	0	System clock selection
	B6	PBTI	W	High	Low	0	Buzzer timer interrupt priority
	B5	PRTI	W	High	Low	0	RTC timer interrupt priority
	B4	PWDI	W	High	Low	0	Watchdog timer interrupt priority
	B3	IT3	W	Falling	Rising	0	INT3 (key_INT) trigger edge selection
	B2	PX3	W	High	Low	0	External interrupt 3 priority
	B1	IT2	W	Falling	Rising	0	INT2 (ADDT) trigger edge selection
	B0	PX2	W	High	Low	0	External interrupt 2 priority

Notes:
1. The SFRs in bold are bit addressable, others are byte addressable.
2. The SFRs can only be accessed by direct addressing.
3. P2.4 is pulled high internal, when external use V_{DD} to connect p2.4 for LCD. The S/W must do the following instruction mov P2IO,#10H and clr P2.4
4. P0IO~P8IO default are output mode(0), when need input mode then set P0IO~P8IO are 1.

Data Pointers

The original 8031 had only one 16-bit Data Pointer (DPL, DPH). In the W928C73, there is an additional 16-bit Data Pointer (DPL1, DPH1). This new Data Pointer uses two SFR locations which were unused in the original 8031. In addition there is an additional instruction, DEC DPTR (op-code A5H), which helps in improving programming flexibility for the user.

MOVX Instruction

The W928C73, like the standard 8031, uses the MOVX instruction to access the external Data Memory. The external data memory includes 384 bytes on-chip data RAM.

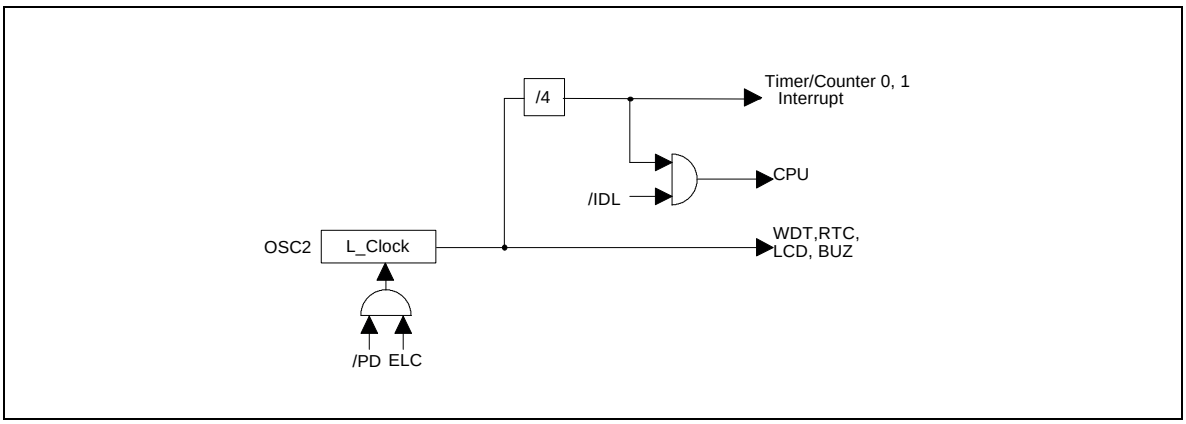
The MOVX instruction is of two types, the MOVX @Ri and MOVX @DPTR. In the MOVX @Ri, the address of the external data comes from two sources. The lower 8-bits of the address are stored in the Ri register of the selected working register bank. The upper 8-bits of the address are store in the HB register (B2h of SFR). In the MOVX @DPTR type, the full 16-bit address is supplied by the Data Pointer.

Since the W928C73 has two Data Pointers, DPTR and DPTR1, the user has to select between the two by setting or clearing the DPS bit. The Data Pointer Select bit (DPS) is the LSB of the DPS SFR, which exists at location 86h. Rest bits in this SFR have no effect, and are set to 0. When DPS is 0, then DPTR is selected, and when set to 1, DPTR1 is selected. The user can switch between DPTR and DPTR1 by toggling the DPS bit. The quickest way to do this is by the INC instruction. The HB register and dual Data Pointers will provide enough flexibility for performing block move operations.

SYSTEM CLOCK

The W928C73 provides one oscillation circuit, OSC2 - L_clock (76.8 KHz), for the whole system. During the power on reset, the L_clock is activated. The RTC Timer, WDT timer, buzzer output and LCD frequency clock sources directly come from L_clock. The CPU, timer0, timer1 and interrupt operation are based on the machine cycle. The machine cycle consists of four oscillator clock sequence (4 states).

ELC is the control bit to activate the L_clock. The OVFL is the clock stable flag for the L_clock. The power on state of system is ELC = 1. For proper operation, the L_clock is suggested to turn on all the time. The clock architecture of the system is shown below.



Power Management

Operation Mode (Normal Mode)

After the power on reset, the W928C73 will enter the normal operation mode. In this mode, all the system is operable with the main clock.

Idle Mode

While setting the PCON.0 to 1, the system will go to idle mode. In idle mode, the CPU is stopped but rest of the system and the oscillator is still running as previous state The idle mode can be waked up by all the interrupt sources.

Power Down Mode

The instruction setting PCON.1 is the last executed prior to going into the Power-down mode. In Power-down mode the oscillator is stopped. The contents of the on-chip RAM and SFRS are preserved. The port pins output the values held by their respective SFRs. PSEN are held LOW.

In Power-down mode V_{DD} may be reduced to minimize power consumption. However, the supply voltage must not be reduce until Power-down mode is active, and must be restored before the hardware reset is applied and frees the oscillator. Reset must be held active until the oscillator has restarted and stabilized.

The wake-up operation of W928C73 after power-down mode has two approaches, wake-up using external interrupt INT0, INT1or wake-up using RESET. For INT0 or INT1 wake-up, the controller will enter the interrupt service routine and is in the slow operation mode and the contents of the on-chip RAM and SFRS are preserved. For RESET wake-up, the RESET pin has to be kept HIGH for a minimum of 24 oscillator periods, the uC will enter the power on reset state after wake up.

OPERATION MODE	NORMAL MODE	IDLE	POWER DOWN
Setting Command	Power on reset Idle mode wake up 3. Power down mode wake up	Set PCON.0 to 1	Set PCON.1 to1
Oscillator	L_clock on	Clock keeps oscillation	Clock stops
CPU	Operable	Stopped	Stopped
Interrupt	All interrupt operable		INT0, INT1
Watchdog Timer	Operable		Stopped
Timer0, Timer1	L_clock/4 operable		Stopped
RTC	L_clock operable		Stopped
Buzzer Timer	L_clock operable		Stopped
Release Condition		All enabled interrupts	1. RESET 2. External interrupt INT0, INT1
Release Time			2^{14} main clock

Timer 0 & 1

The W928C73 has two 16-bit Timer. Each of these Timer has two 8 bit registers which form the 16 bit counting register. For Timer 0 they are TH0, the upper 8 bits register, and TL0, the lower 8 bit register. Similarly Timer 1 has two 8 bit registers, TH1 and TL1. The two can be configured to operate as timers, counting machine cycles.

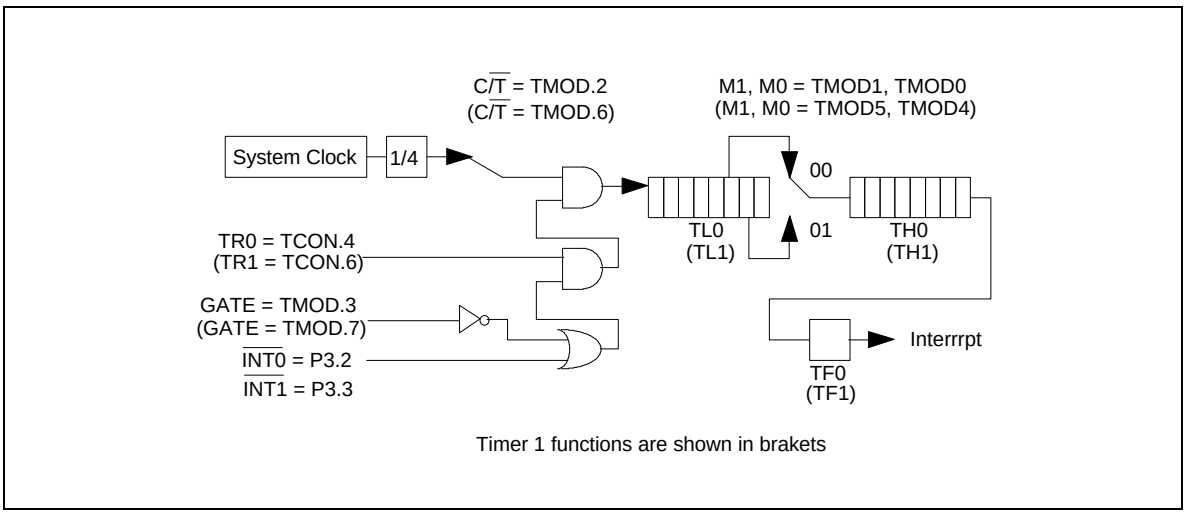
The timer clock is 1/4 of the system clock. The T0 and T1 inputs are sampled in every machine cycle at C4. If the sampled value is high in one machine cycle and low in the next, then a valid high to low transition on the pin is recognized and the count register is incremented. Since it takes two machine cycles to recognize a negative transition on the pin, the maximum rate at which counting will take place is 1/24 of the master clock frequency. In the "Timer" mode, the recognized negative transition on pin T0 and T1 can cause the count register value to be updated only in the machine cycle following the one in which the negative edge was detected.

The "Timer" function is selected by the "C/T" bit in the TMOD Special Function Register. Each Timer has one selection bit for its own; bit 2 of TMOD selects the function for Timer 0 and bit 6 of TMOD selects the function for Timer 1. In addition each Timer can be set to operate in any one of four possible modes. The mode selection is done by bits M0 and M1 in the TMOD SFR.

Mode 0

In Mode 0, the timer act as a 8 bit counter with a 5 bit, divide by 32 pre-scale. In this mode we have a 13 bit timer. The 13 bit counter consists of 8 bits of THx and 5 lower bits of TLx. The upper 3 bits of TLx are ignored.

The negative edge of the clock increments the count in the TLx register. When the fifth bit in TLx moves from 1 to 0, then the count in the THx register is incremented. When the count in THx moves from FFh to 00h, then the overflow flag TFx in TCON SFR is set. The counted input is enabled only if TRx is set and either GATE = 0 or $\overline{INT}$x = 1. When C/$\overline{T}$ is set to 0, then it will count clock cycles, and if C/$\overline{T}$ is set to 1, then it will count 1 to 0 transitions on T0 (P3.4) for timer 0 and T1 (P3.5) for timer 1. When the 13 bit count reaches 1FFFh the next count will cause it to roll-over to 0000h. The timer overflow flag TFx of the relevant timer is set and if enabled an interrupts will occur. Note that when used as a timer, the time-base is clock cycles/4.



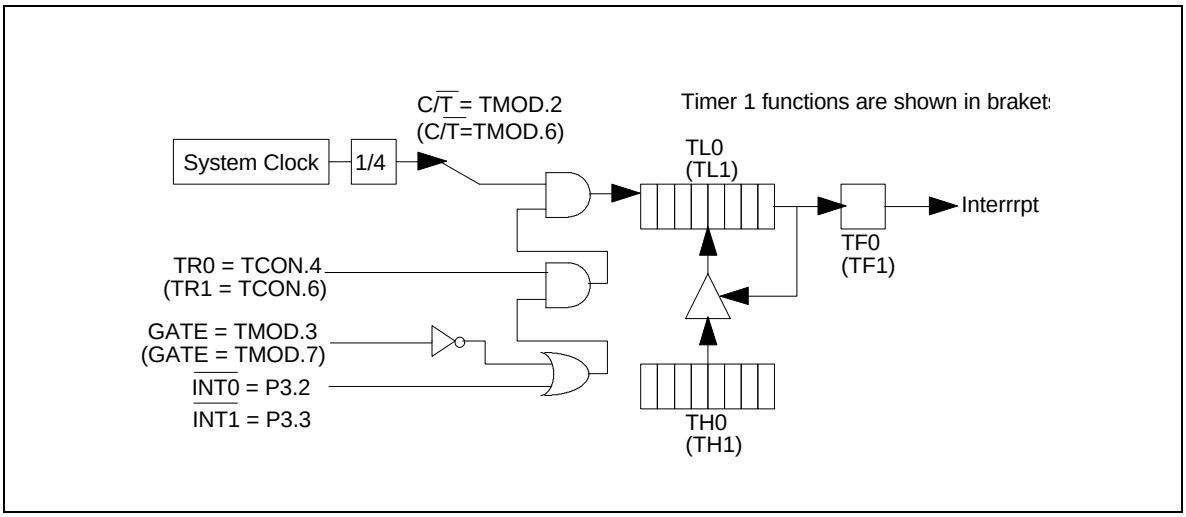
Mode 0 and 1 of Timer 0 & 1

Mode 1

Mode 1 is similar to Mode 0 except that the counting register forms a 16 bit counter, rather than a 13 bit counter. This means that all the bits of THx and TLx are used. Roll-over occurs when the timer moves from a count of FFFFh to 0000h. The timer overflow flag TFx of the relevant timer is set and if enabled an interrupt will occur. The selection of the time-base in the timer mode is similar to that in Mode 0. The gate function operates similarly to that in Mode 0.

Mode 2

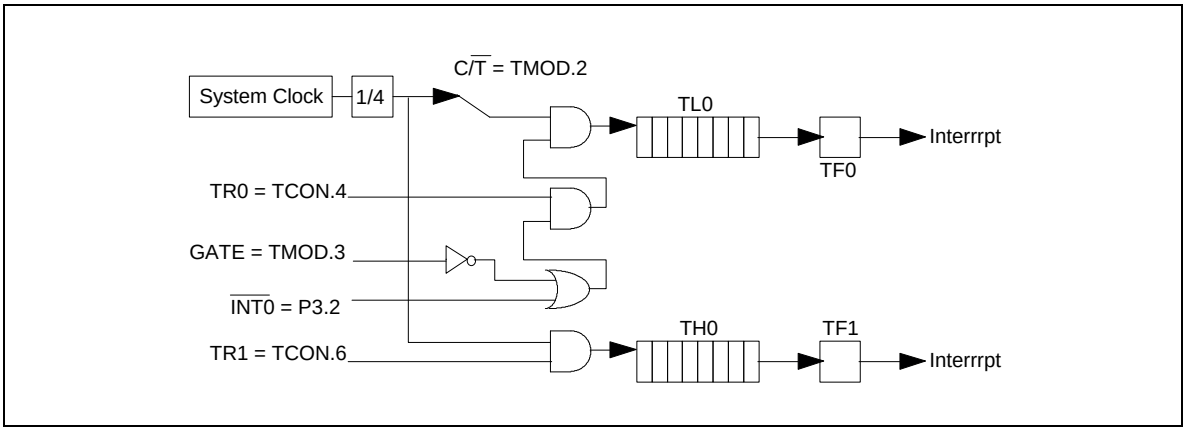
In Mode 2, the timer is in the Auto Reload Mode. In this mode, TLx acts as a 8 bit count register, while THx holds the reload value. When the TLx register overflows from FFh to 00h, the TFx bit in TCON is set and TLx is reloaded with the contents of THx, and the counting process continues from here. The reload operation leaves the contents of the THx register unchanged. Counting is enabled by the TRx bit and proper setting of GATE and INTx pins. As in the other two modes 0 and 1, mode 2 allows counting of either clock cycles (clock/4) or pulses on pin Tn.



Mode 2 of Timer 0 & 1

Mode 3

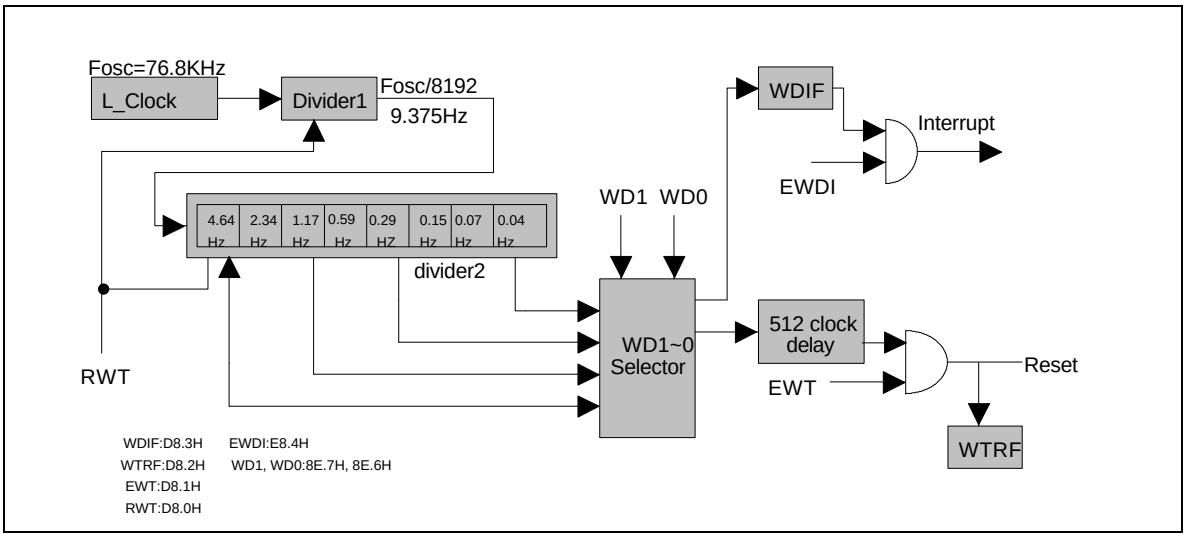
Mode 3 has different operating methods for the two timer. For timer 1, mode 3 simply freezes the counter. Timer 0, however, configures TL0 and TH0 as two separate 8 bit count registers in this mode. The logic for this mode is shown in the figure. TL0 uses the Timer 0 control bits C/T, GATE, TR0, INT0 and TF0. The TL0 can be used to count clock cycles (clock/12 or clock/4) or 1-to-0 transitions on pin T0 as determined by C/T (TMOD.2). TH0 is forced as a clock cycle counter (clock/12 or clock/4) and takes over the use of TR1 and TF1 from Timer 1. Mode 3 is used in cases where an extra 8 bit timer is needed. With Timer 0 in Mode 3, Timer 1 can still be used in Modes 0, 1 and 2., but its flexibility is somewhat limited. While its basic functionality is maintained, it no longer has control over its overflow flag TF1 and the enable bit TR1. Timer 1 can still be used as a timer and retains the use of GATE and INT1 pin. In this condition it can be turned on and off by switching it out of and into its own Mode 3.



Mode 3 of Timer 0 & 1

Watchdog Timer

The watchdog timer is a free-running timer which can be programmed by the user to serve as a system monitor, a time-base generator or an event timer. When the time out occurs a request flag is set, which can cause an interrupt or a system reset depend on the EWDI or EWT enable SFR. The interrupt and reset functions are independent of each other and may be used separately or together depending on the users software. The watchdog timer should first be restarted by using RWT. This ensures that the timer starts from a known state.



Buzzer Timer

The W928C73 provides a buzzer timer. The buzzer timer can output a single tone signal to the BUZ pin that frequency range from 150Hz to 38400 Hz.

The operation of buzzer timer is as following. First set the proper value of tone0 then set the ENBUZ to 1, the uC will output the corresponding frequency (50% duty cycle) to P1.6/BUZ output pin. The timer can also generate different duty cycle to control the buzzer volume.

The auto-reload condition:

1. When 8 bits down counter overflow (From "01H" change to "FFH")
2. ENBUZ or ENBT signal rising edge (From "L" change to "H")

The divider reset condition:

1. RESET
2. MOV TONE,#I instruction
3. ENBUZ rising edge

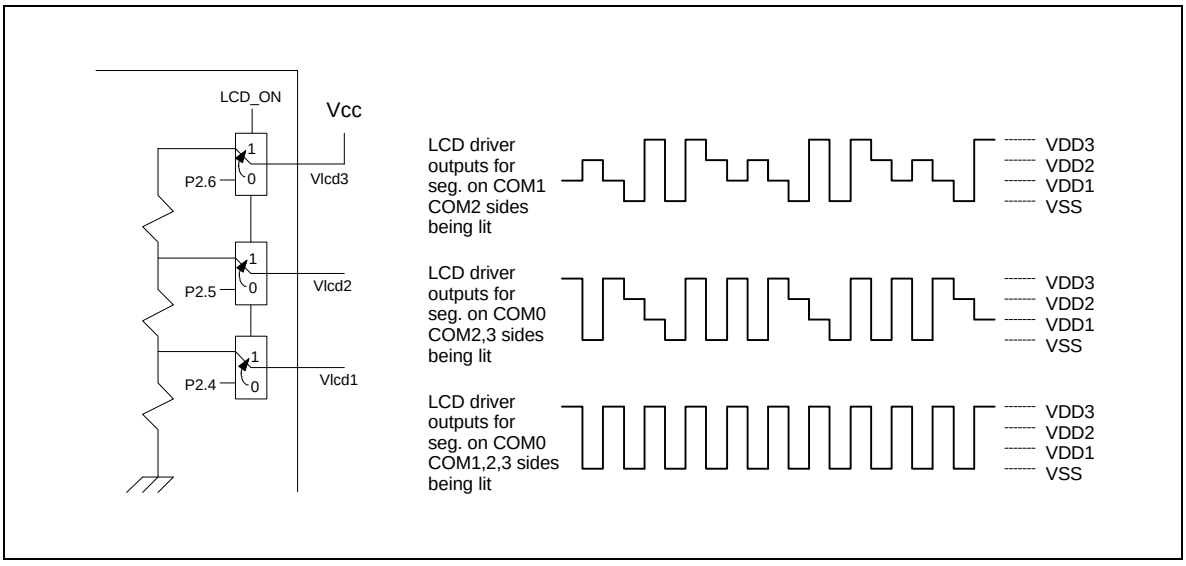
RTC Timer and LCD Frequency

The W928C73 provides flexible RTC timer for real time clock calculation. The 8 bit auto-reload down-counter, RTLCD, can download a suitable value for different main clock frequency to generate the clock interrupt. For 76800Hz crystal, the RTLCD value should be 74. This RTC timer is also used to provide the LCD frequency source.

LCD Controller/Driver

The W928C73 can directly drive a LCD with 32 segment output pins and 4 common output pins for a total of 36 × 4 dots. LCDR is used for the LCD driver control. The alternating frequency of the LCD can be set as 64 Hz, 128 Hz, 256 Hz, or 512 Hz. In addition, LCDON (LCDR.0) bit can also be used to set up four of the LCD driver output pins (segment 0 to segment 31/35) as a I/O port. (For 76.8 KHz and RTLCD = 74).

The LCD driving potentials are connected to external through port 2.4~2.6 while LCDON is set to 1. The pin connections and output waveforms for the 1/3 bias, 1/4 duty LCD driving modes are shown below.



LCD Voltage Pin Connection and Output Waveform (1/3 Bias 1/4 Duty)

I/O Ports

The W928C73 has four 8-bit bit addressable I/O ports, port 0 – port 3. The segment and common signal out of LCD driver can change to I/O port if LCD driver is disabled. The additional I/O port 4 – port 8 are byte addressable. Port 4, 5 can be used as an address bus and port 6 can be used as data bus when external program is running or external memory/device is accessed by MOVC or MOVX instruction. The I/O ports of W928C73 are same as 8031 but with extra pull high resister control. While read out the SFR value of port, the port will function as input mode. While write the data to port SFR, the I/O port will work as output port. SFR P0IO–P3IO define the pull high condition of port 0 – port 3. When setting the SFR bit to 1 will set the I/O port as input mode without pull high resister or open-drain output mode. When clear to 0 will set the I/O port as input mode with pull high resister or output mode. Port 0 – port 3 are bit addressable. The initial state of W928C73 is input mode with pull high resister. If LCD is off, P48IO is used to control the pull high resister of port 4 – port 8, and is byte controllable.

Interrupt

The W928C73 provides 10 interrupt sources with two priority levels. The External interrupt 0 has the highest natural priority. Software can assign high or low priority to each interrupt source. All interrupt source priorities are reset to low.

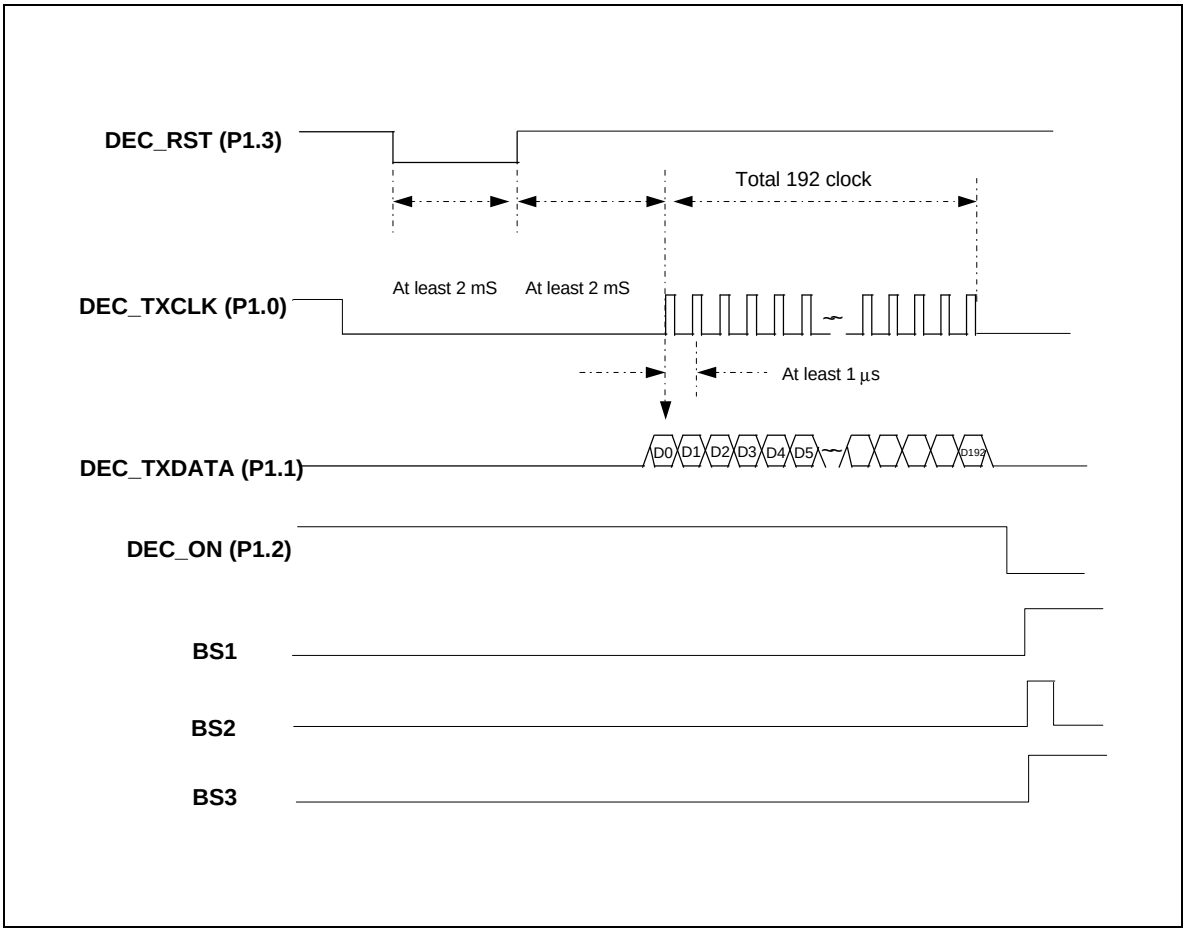
Name	DESCRIPTION	VECTOR	NATURAL PRIORITY
INT0	External interrupt 0	03H	1
TF0	Timer 0 overflow interrupt	0BH	2
INT1	External interrupt 1 (BAT_DET_INT)	13H	3
TF1	Timer 1 overflow interrupt	1BH	4
SCON1	POCSAG data buffer interrupt	3BH	5
INT2	External interrupt 2	43H	6
INT3	External interrupt 3 (Key_interrupt)	4BH	7
WDTI	Watchdog interrupt	53H	8
RTCI	Real-time timer interrupt	5BH	9
BTI	Buzzer timer interrupt	63H	10

POCSAG Decoder

The build-in decoder is fully compatible with CCIR Radio Paging Code Number 1 (POCSAG code) operating at 512, 1200, or 2400 bps. The build-in POCSAG decoder supports 6 user addresses in 6 independent frames.

Initial Option Bit Setup

The decoder should be initialized through SFR DEC_TXCLK (P1.0), DEC_TXDATA (P1.1), and DEC_RST (P1.3) as Fig 12. Clearing the SFR DEC_ON (P1.2) from high to low after the 192 option bits setting will enable the decoder. The BS1, BS2 and BS3 pins will then control the RF to receive POCSAG signal. The functions of the option bits are described below.



POCDSG Decoder Setup Option

CLOCK	DATA	CLOCK	DATA	CLOCK	DATA	CLOCK	DATA	CLOCK	DATA	CLOCK	DATA
D0	0	D32	0	D64	0	D96	0	D128	0	D160	0
D1	TEST0	D33	0	D65	0	D97	0	D129	0	D161	0
D2	TEST1	D34	0	D66	0	D98	0	D130	0	D162	0
D3	ADA17	D35	ADB17	D67	ADC17	D99	ADD17	D131	ADE17	D163	ADF17
D4	ADA16	D36	ADB16	D68	ADC16	D100	ADD16	D132	ADE16	D164	ADF16
D5	ADA15	D37	ADB15	D69	ADC15	D101	ADD15	D133	ADE15	D165	ADF15
D6	ADA14	D38	ADB14	D70	ADC14	D102	ADD14	D134	ADE14	D166	ADF14
D7	ADA13	D39	ADB13	D71	ADC13	D103	ADD13	D135	ADE13	D167	ADF13
D8	ADA12	D40	ADB12	D72	ADC12	D104	ADD12	D136	ADE12	D168	ADF12
D9	ADA11	D41	ADB11	D73	ADC11	D105	ADD11	D137	ADE11	D169	ADF11
D10	ADA10	D42	ADB10	D74	ADC10	D106	ADD10	D138	ADE10	D170	ADF10
D11	ADA9	D43	ADB9	D75	ADC9	D107	ADD9	D139	ADE9	D171	ADF9
D12	ADA8	D44	ADB8	D76	ADC8	D108	ADD8	D140	ADE8	D172	ADF8
D13	ADA7	D45	ADB7	D77	ADC7	D109	ADD7	D141	ADE7	D173	ADF7
D14	ADA6	D46	ADB6	D78	ADC6	D110	ADD6	D142	ADE6	D174	ADF6
D15	ADA5	D47	ADB5	D79	ADC5	D111	ADD5	D143	ADE5	D175	ADF5
D16	ADA4	D48	ADB4	D80	ADC4	D112	ADD4	D144	ADE4	D176	ADF4
D17	ADA3	D49	ADB3	D81	ADC3	D113	ADD3	D145	ADE3	D177	ADF3
D18	ADA2	D50	ADB2	D82	ADC2	D114	ADD2	D146	ADE2	D178	ADF2
D19	ADA1	D51	ADB1	D83	ADC1	D115	ADD1	D147	ADE1	D179	ADF1
D20	ADA0	D52	ADB0	D84	ADC0	D116	ADD0	D148	ADE0	D180	ADF0
D21	FA3	D53	FB3	D85	FC3	D117	FD3	D149	FE3	D181	FF3
D22	FA2	D54	FB2	D86	FC2	D118	FD2	D150	FE2	D182	FF2
D23	FA1	D55	FB1	D87	FC1	D119	FD1	D151	FE1	D183	FF1
D24	Baud1	D56	EnA	D88	PL1	D120	Outr1	D152	0	D184	0
D25	Baud0	D57	EnB	D89	PL2	D121	Outr2	D153	0	D185	0
D26	Inv	D58	EnC	D90	PL3	D122	PREL1	D154	0	D186	0
D27	Over1	D59	EnD	D91	PL4	D123	PREL0	D155	0	D187	0
D28	Over0	D60	EnE	D92	FIL	D124	0	D156	0	D188	0
D29	Smith	D61	EnF	D93	0	D125	0	D157	0	D189	0
D30	0	D62	0	D94	0	D126	0	D158	0	D190	0
D31	0	D63	0	D95	0	D127	0	D159	0	D191	0

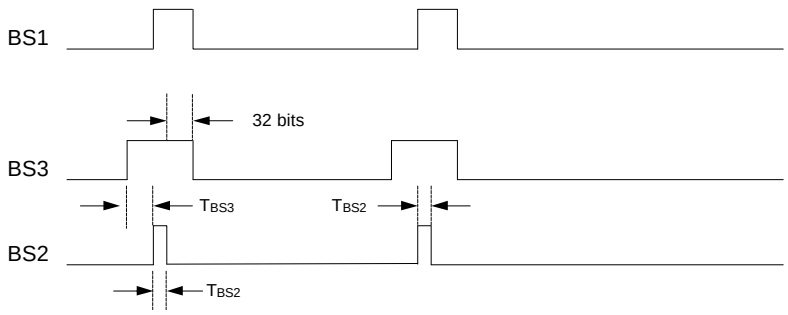
FUNCTION	OPTION
Address A, B, C, D, E, F	EnA, EnB, EnC, EnD, EnE, EnF
Disable	0
Enable	1

FUNCTION	OPTION	
Message reception error termination condition	Over1	Over0
Reception termination on first uncorrectable codeword	0	0
Reception termination on two consecutive uncorrectable codeword	0	1
Reserved	1	0
Reserved	1	1

FUNCTION	OPTION
NRZ Signal Input	Shmt
Without Schmitt Trigger	0
With Schmitt Trigger	1

FUNCTION		OPTION	
Out of range hold time when synchronization lost		OUTR1	OUTR2
512 bps	1200/2400 bps		
36 sec	31 sec	0	0
72 sec	61 sec	0	1
144 sec	123 sec	1	0
288 sec	246 sec	1	1

FUNCTION	OPTION	
Baud rate	Baud0	Baud1
512 bps	0	1
1200 bps	1	1
2400 bps	1	0



FUNCTION		OPTION	
TBS2		PL2	PL1
512 bps	1200/2400 bps		
3.90 mS	1.67 mS	0	0
11.71 mS	5.00 mS	0	1
19.53 mS	8.33 mS	1	0
27.34 mS	11.67 mS	1	1

FUNCTION		OPTION	
TBS3		PL4	PL3
512 bps	1200/2400 bps		
0.00 mS	0.00 mS	0	0
31.25 mS	13.33 mS	0	1
62.50 mS	26.67 mS	1	0
93.75 mS	40.00 mS	1	1

FUNCTION	OPTION	
Preamble length	PREL1	PREL0
512 bit	0	0
896 bit	0	1
1024 bit	1	0
1792 bit	1	1

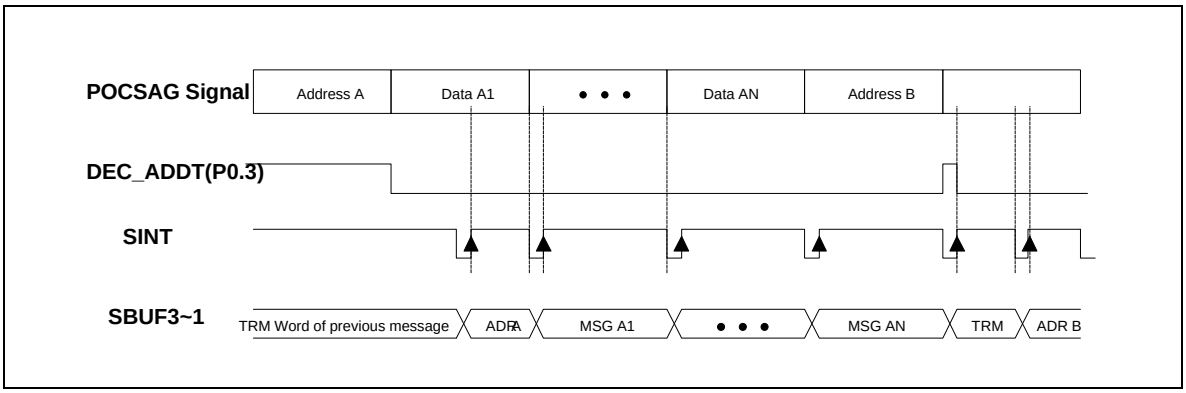
FUNCTION	OPTION
NRZ signal	Inv
Non-inversion	0
Inversion	1

The option bit TEST0, TEST1 and FIL are only used for IC testing. For normal operation, insert “0” for all those three option bits.

POCSAG data output format

While receiving an address matched message the SCON1 will generate interrupt and the data will present in SBUF1–3. The value of SBUF for the first interrupt is address word, followed by message words, and ended with the termination word. If another addressed matched message is received right after the first message, the second address word will come out followed by the previous termination word as shown below.

The detail formats of address word, message word and termination word are as following:



Address Word Format

SB3

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FUN21	FUN20	A19	A18	A17	A16	A15	A14

SB2

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
A13	A12	A11	A10	A9	A8	A7	A6

SB1

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
A5	A4	A3	A2	ADR2	ADR1	ADR0	CM (0)

Note: CM = 0: Address word, CM = 1: Message word, Termination word
Func21, 20: function bit of POCSAG
ADR2~0: define the received address number

ADR2- 0	000	001	010	011	100	101
Address	A	B	C	D	E	F

Message Word Format

SB3

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
M21	M20	M19	M18	M17	M16	M15	M14

SB2

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
M13	M12	M11	M10	M9	M8	M7	M6

SB1

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
M5	M4	M3	M2	SYNC	ER0	TM (0)	CM (1)

Note: SYNC: sync detection / 1: syncloss 0: catch sync
ER0: error condition after correction / 1:error 0:No error

Termination Word Format

SB3

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	0	0	0	0	0

SB2

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	0	0	0	0	0

SB1

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	0	0	TMC	TM (1)	CM (1)

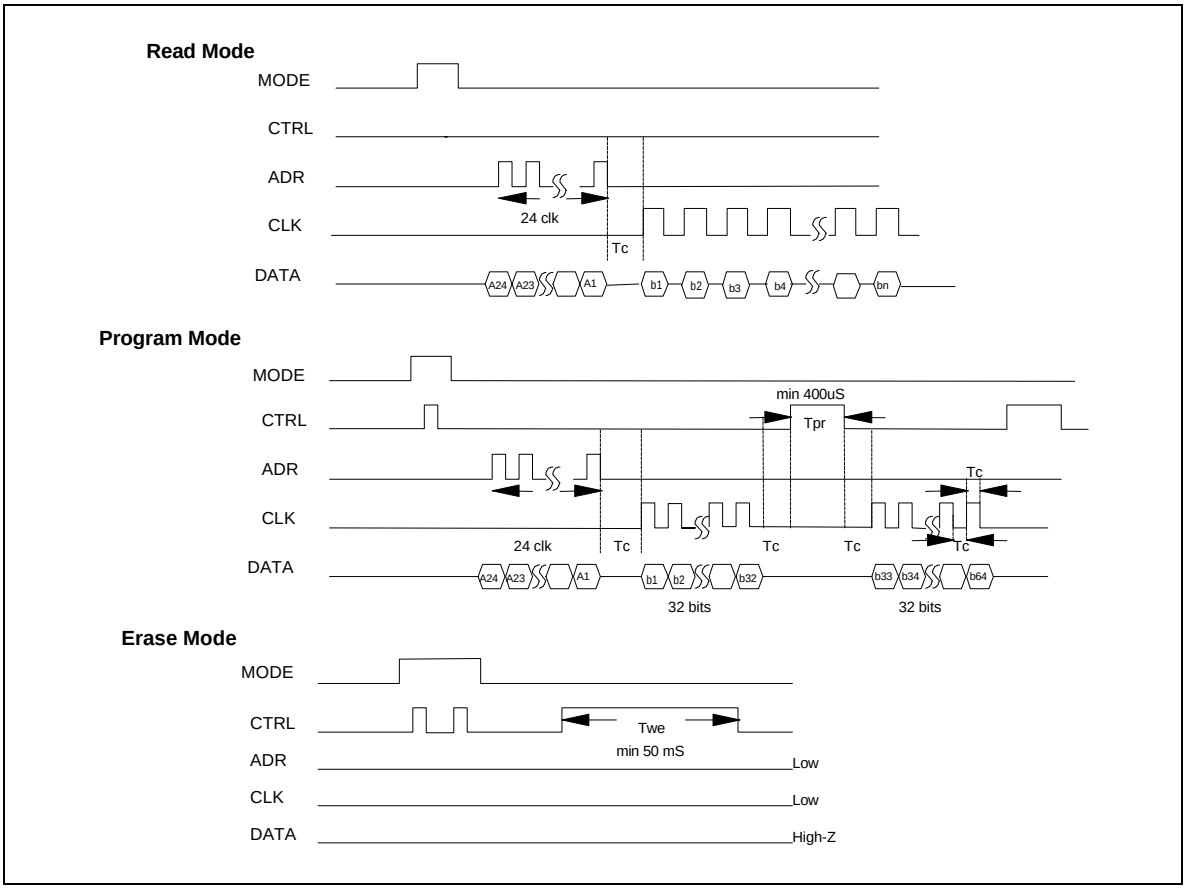
Note: TMC (termination condition): 0: proper termination, 1:Termination due to error condition

Decoder related SFR

SFR NAME	NAME	I/O	DESCRIPTION
P0.1	DEC_SYNVAL	I	Decoder synchronization
P0.3	DEC_ADDT	I/INT	Decoder
P1.0	DEC_TXCLK	O	Decoder option bit setup clock
P1.1	DEC_TXDATA	O	Decoder option bit setup data
P1.2	DEC_ON	O	Decoder on/off control
P1.3	DEC_RST	O	Decoder reset control
P3.7	DEC_BLDET	I	Battery low detector (1V)

32 x 32 bits Flash ROM Operation

The W928C73 provides 32 frame × 32 bit flash ROM cell typically used to store the POCSAG addresses and parameters. The single voltage supply eliminates the need for an extra pump circuit during programming and erasing. There are 3 different operation mode, read, program and erase. The different mode is determined by the number of the clocks of the CTRL bit while the SFR MODE is set to high. The programming timing is shown below.



Read mode

This mode will read out the data from the flash ROM. The first 24 bits of DATA are the starting frame address of reading-out. If DATA is low for these 24 bits, then the output data will start from address "0". The stored data will shift out bit by bit with each clock in. The LSB of data is shifted out first.

Program mode

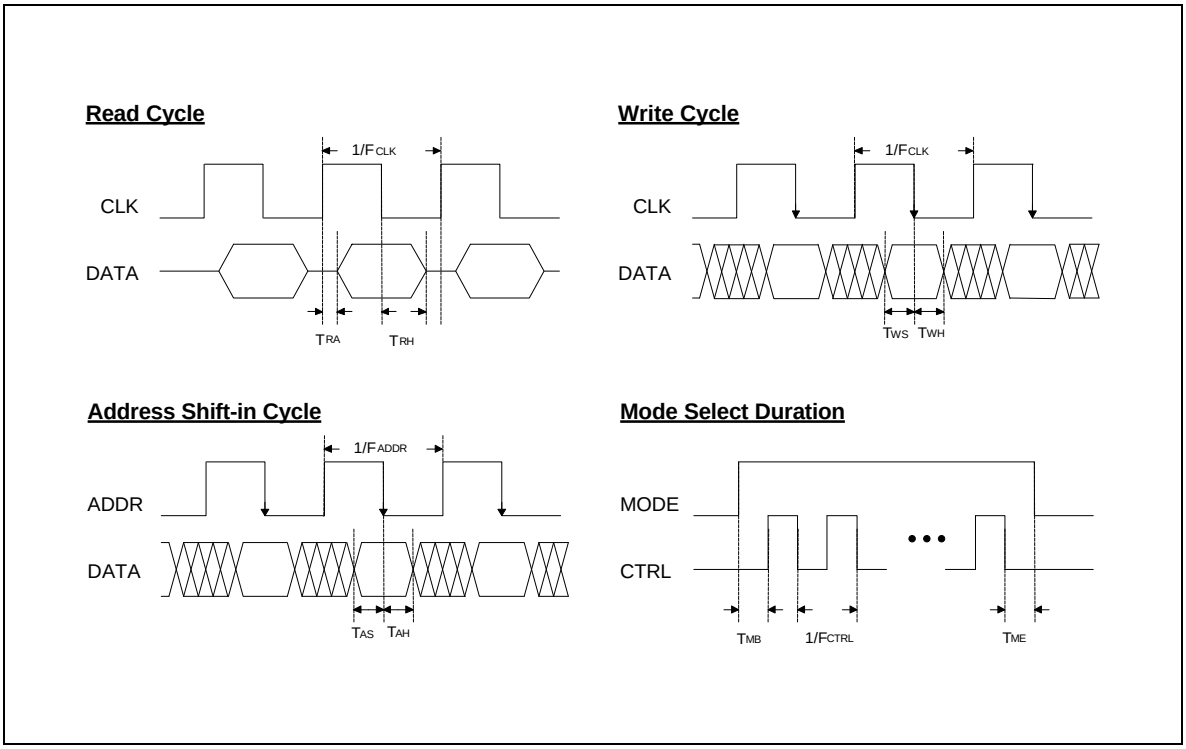
This mode will write data into the flash ROM. This flash ROM is programmed on a frame basis. Each frame contains 32 bits of data. The LSB of data is shift in first. The programming time (Tpr) must be more than 400 μS. Each programming pulse will increase the frame address by 1.

Erase Mode

This mode will erase all the data in the flash ROM. The typical whole-chip-erase time should be larger than 50 mS (Twe).

TIMING WAVEFORMS

Flash ROM Programming



Flash Programming SFR Configuration

SFR NAME	NAME	I/O	DESCRIPTION
P0.0	DATA	I/O	Bi-direction data line
P0.2	ADDR	O	Output clock for start address shift-out
P3.4	CTRL	O	Enable signal for program and erase operations when MODE = 0 (P3.6) Input clock for mode counter when MODE = 1 (P3.6)
P3.5	CLK	O	Output clock for data write-out and read-in
P3.6	MODE	O	Mode select control pin

- Fast frame-write operation: Frame (32 bits) program cycle time: 400 μS (typical)
- Fast whole-chip-erase duration: 50 mS (max.)
- Read data access time: 500 nS (max.)
- Program/erase cycles: 3000 (typical)
- Data retention: 10 years (typical)

Notes:

1. program mode, the DATA should be latched in the CLK falling edge.
2. read mode, the DATA should be latched in before CLK low.
3. when in the read mode, must let P0IO.0 and P0.0 (DATA) set 1 (input mode).
4. set GF1(general flag) to "1" will enable 1K flash.

DC CHARACTERISTICS

(V_{DD} = 3V, V_{SS} = 0V, T_A = 25° C)

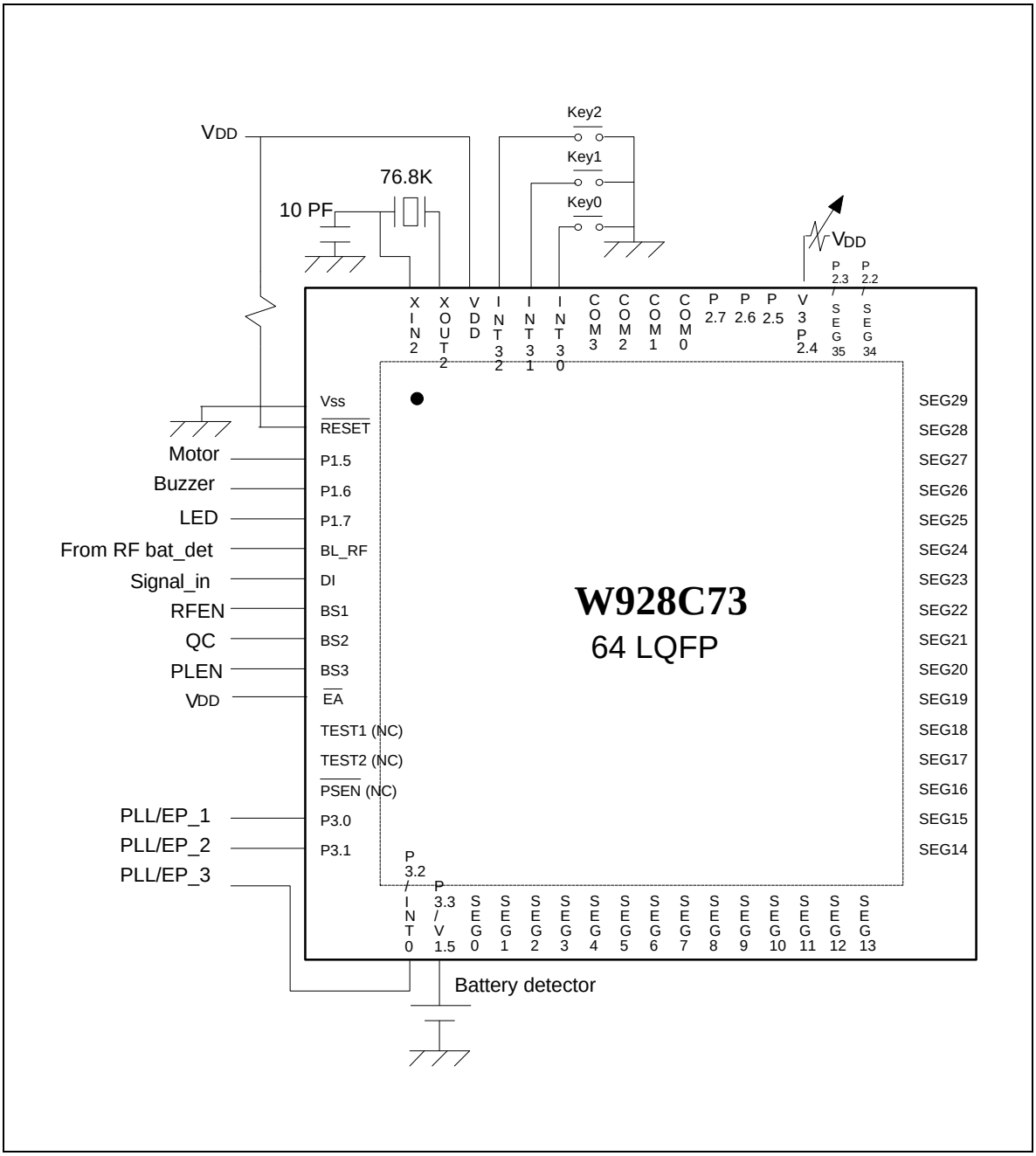
PARAMETER		SYM.	CONDITIONS	LIMITS			UNIT
				MIN.	TYP.	MAX.	
Operating Voltage		V_{DD}	-	2.4		3.6	V
Flash ROM Operating Voltage		V_{FLASH}	-	2.5		3.6	V
Normal Mode Current		I_{NORMAL}	No load, decoder and CPU operating at 76.8K Hz		100		μA
Idle Mode Current		I_{IDLE}	No load, main clock, decoder on, CPU off	-	25	60	μA
Stop Mode Current		I_{STOP}	No load, OSC stop			1	μA
Flash ROM Operating Current		I_{OP}	In read mode DATA open	-	5		mA
Input Voltage	High	V_{IH}	All input pins	2.0		V_{DD}	V
	Low	V_{IL}		-0.3	-	0.8	V
Output Current	Sink	I_{OL}	V_{OL} = 0.3V		0.6/0.1		mA
	Drive	I_{OH}	V_{OH} = 2.7V		-1		mA
High-drive Port Output Current P1.5 ~ P1.7	Sink	I_{OL}	V_{OL} = 0.3V		4	-	mA
	Drive	I_{OH}	V_{OH} = 2.7V		-4	-	mA

FLASH ROM AC CHARACTERISTICS

(V_{DD} = 3V, V_{SS} = 0V, T_A = 25° C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
MODE Pulse Width	TMP	-	1	-	-	µS
CTRL Pulse Width	TWP	Page coding mode	400	-	700	µS
Clock Frequency of ADDR	FADDR	-	-	-	1	MHz
Clock Frequency of CLK	FCLK	-	-	-	1	MHz
Clock Ffrequency of CTRL	FCTRL	-	-	-	1	MHz
Interval Between ADDR End & CLK Begin	TI	Read/Write mode	1	-	-	µS
Interval Between CLK & CTRL	TGCC	Write mode	1	-	-	µS
Interval Between ADDR & CTRL	TGCA	Page coding mode	1	-	-	µS
Interval Between Addressing End & Block-erase Begin	TAE	Block erase mode	1	-	-	µS
Interval Between MODE Rising Edge & CTRL Clock Begin	TMB	Mode selection	500	-	-	nS
Interval Between CTRL Clock End & MODE Falling Edge	TME	Mode selection	500	-	-	nS
Interval Between MODE Falling Edge & Another Pin Active	TGM	-	1	-	-	µS
Data Access Time	TRA	Read mode	-	-	500	nS
Data Set-up Time	TWS	Write mode	250	-	-	nS
	TAS	-	250	-	-	nS
Data Hold Time	TRH	Read mode	0	-	-	nS
	TWH	Write mode	10	-	-	nS
	TAH	-	10	-	-	nS
Programming Duration	TPR	Write mode	400	-	-	µS
Whole-chip-erase Time	TWE	Whole-chip-erase mode	45	-	50	mS
Block-erase Time	TBE	Block-erase mode	40	-	45	mS

APPLICATION CIRCUIT



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