



W24512A

64K × 8 HIGH SPEED CMOS STATIC RAM

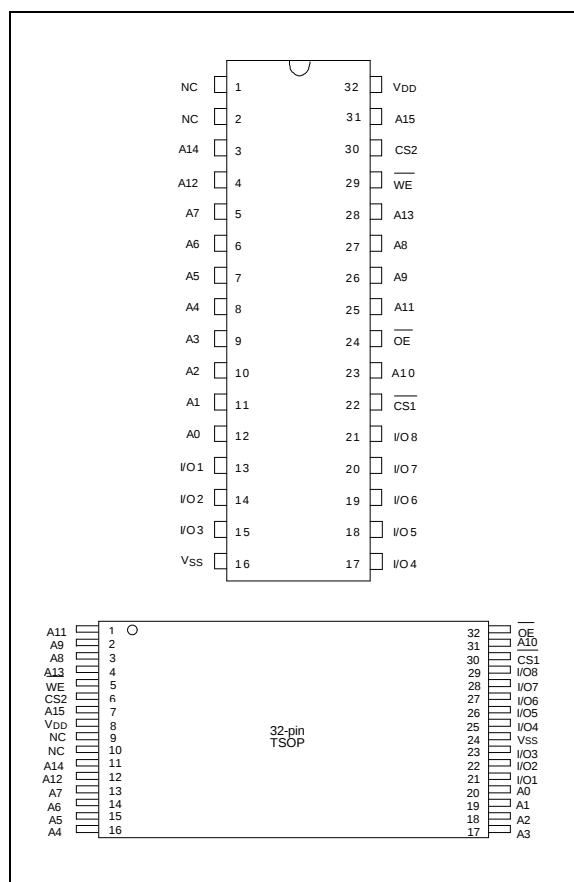
GENERAL DESCRIPTION

The W24512A is a high speed, low power CMOS static RAM organized as 65536 × 8 bits that operates on a single 5-volt power supply. This device is manufactured using Winbond's high performance CMOS technology.

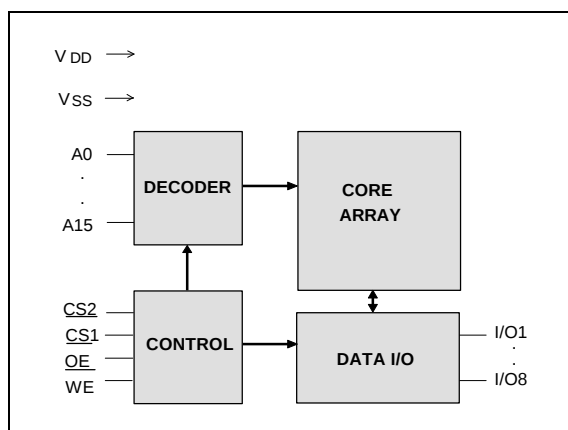
FEATURES

- High speed access time: 35 nS (max.)
- Low power consumption:
 - Active: 500 mW (typ.)
- Single +5V power supply
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three-state outputs
- Available packages: 32-pin 600 mil DIP, 450 mil SOP, and TSOP

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0–A15	Address Inputs
I/O1–I/O8	Data Inputs/Outputs
CS1, CS2	Chip Select Inputs
WE	Write Enable Input
OE	Output Enable Input
VDD	Power Supply
VSS	Ground
NC	No Connection



DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Supply Voltage to VSS Potential	-0.5 to +7.0	V
Input/Output to VSS Potential	-0.5 to VDD +0.5	V
Allowable Power Dissipation	1.0	W
Storage Temperature	-65 to +150	°C
Operating Temperature	0 to +70	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

TRUTH TABLE

CS1	CS2	OE	WE	MODE	I/O1- I/O8	VDD CURRENT
H	X	X	X	Not Selected	High Z	ISB, ISB1
X	L	X	X	Not Selected	High Z	ISB, ISB1
L	H	H	H	Output Disable	High Z	IDD
L	H	L	H	Read	Data Out	IDD
L	H	X	L	Write	Data In	IDD

OPERATING CHARACTERISTICS

(VDD = 5V ± 10%, VSS = 0V, Ta = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Input Low Voltage	VIL	-		-0.5	-	+0.8	V
Input High Voltage	VIH	-		+2.2	-	VDD +0.5	V
Input Leakage Current	ILI	VIN = VSS to VDD		-10	-	+10	μA
Output Leakage Current	ILO	VI/O = VSS to VDD CS1 = VIH or CS2 = VIL or OE = VIH or WE = VIL		-10	-	+10	μA
Output Low Voltage	VOL	IOL = +8.0 mA		-	-	0.4	V
Output High Voltage	VOH	IOH = -4.0 mA		2.4	-	-	V
Operating Power Supply Current	IDD	CS1 = VIL, CS2 = VIH I/O = 0mA, Cycle = MIN Duty = 100%	35	-	-	140	mA
Standby Power Supply Current	ISB	CS1 = VIH or CS2 = VIL Cycle = MIN, Duty = 100%		-	-	30	mA
	ISB1	CS1 ≥ VDD - 0.2V or CS2 ≤ 0.2V		-	-	10	mA

Note: Typical characteristics are at VDD = 5V, TA = 25° C.



CAPACITANCE

(VDD = 5V, TA = 25° C, f = 1 MHz)

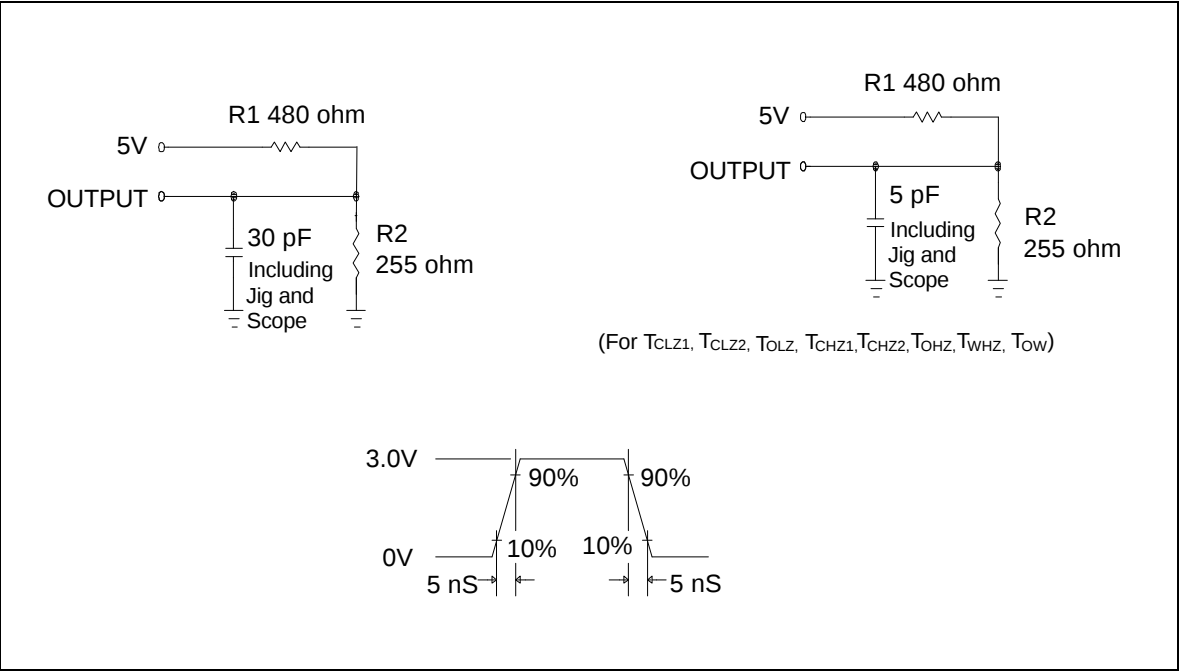
PARAMETER	SYM.	CONDITIONS	MAX.	UNIT
Input Capacitance	CIN	VIN = 0V	8	pF
Input/Output Capacitance	C/I/O	VOU = 0V	10	pF

Note: These parameters are sampled but not 100% tested.

AC TEST CONDITIONS

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	5 nS
Input and Output Timing Reference Level	1.5V
Output Load	CL = 30 pF, IOH/IOL = -4 mA/8 mA

AC TEST LOADS AND WAVEFORM



AC CHARACTERISTICS

(V_{DD} = 5V ±10%, V_{SS} = 0V, T_A = 0 to 70° C)

Read Cycle

PARAMETER		SYM.	W24512A-35		UNIT
			MIN.	MAX.	
Read Cycle Time		TRC	35	-	nS
Address Access Time		TAA	-	35	nS
Chip Select Access Time	$\overline{\text{CS1}}$	TACS1	-	35	nS
	$\overline{\text{CS2}}$	TACS2	-	35	nS
Output Enable to Output Valid		TAOE	-	17	nS
Chip Selection to Output in Low Z	$\overline{\text{CS1}}$	TCLZ1*	3	-	nS
	$\overline{\text{CS2}}$	TCLZ2*	3	-	nS
Output Enable to Output in Low Z		TOLZ*	0	-	nS
Chip Deselection to Output in High Z	$\overline{\text{CS1}}$	TCHZ1*	-	17	nS
	$\overline{\text{CS2}}$	TCHZ2*	-	17	nS
Output Disable to Output in High Z		TOHZ*	-	17	nS
Output Hold from Address Change		TOH	3	-	nS

* These parameters are sampled but not 100% tested.

Write Cycle

PARAMETER		SYM.	W24512A-35		UNIT
			MIN.	MAX.	
Write Cycle Time		TWC	35	-	nS
Chip Selection to End of Write	$\overline{\text{CS1}}$	TCW1	20	-	nS
	$\overline{\text{CS2}}$	TCW2	20	-	nS
Address Valid to End of Write		TAW	20	-	nS
Address Setup Time		TAS	0	-	nS
Write Pulse Width		TWP	18	-	nS
Write Recovery Time	$\overline{\text{CS1}}, \overline{\text{WE}}$	TWR1	0	-	nS
	$\overline{\text{CS2}}$	TWR2	0	-	nS
Data Valid to End of Write		TDW	15	-	nS
Data Hold from End of Write		TDH	0	-	nS
Write to Output in High Z		TWHZ*	-	15	nS
Output Disable to Output in High Z		TOHZ*	-	15	nS
Output Active from End of Write		TOW	0	-	nS

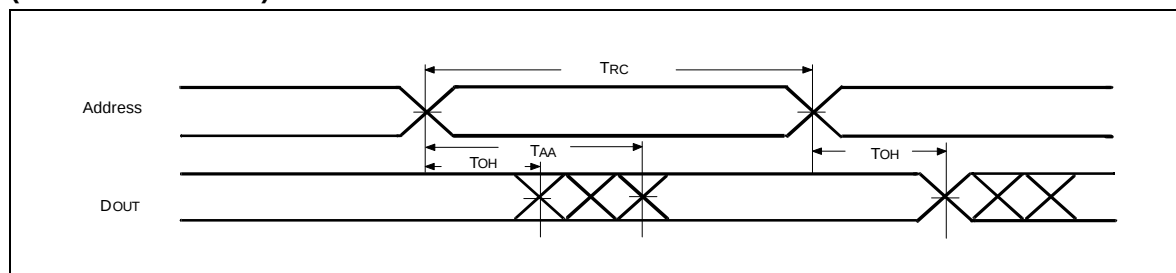
* These parameters are sampled but not 100% tested.



TIMING WAVEFORMS

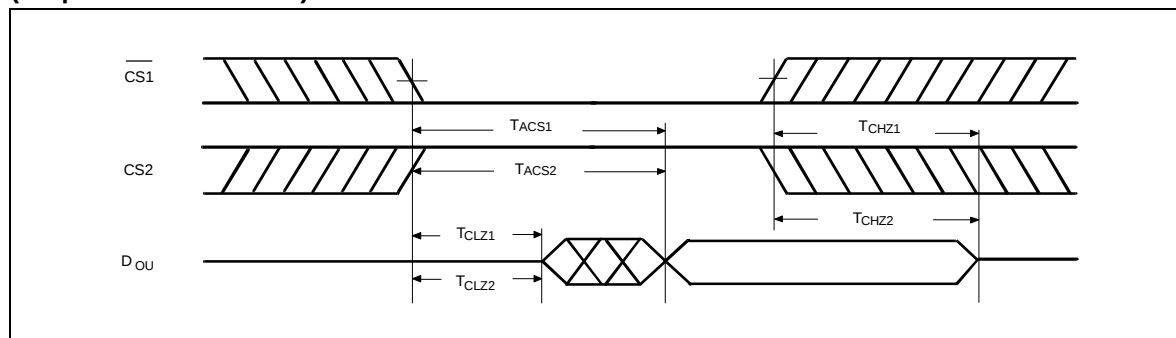
Read Cycle 1

(Address Controlled)



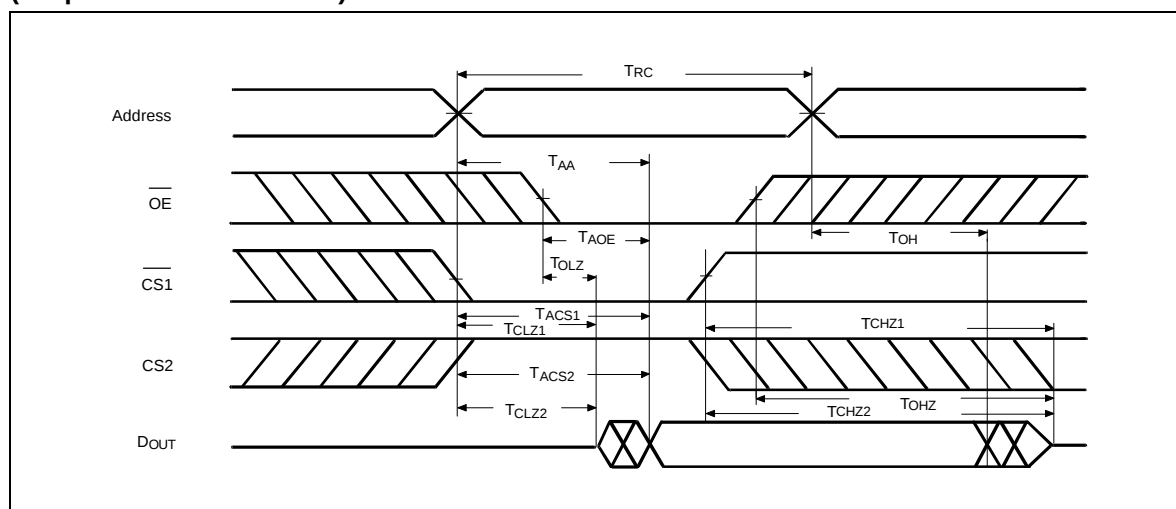
Read Cycle 2

(Chip Select Controlled)



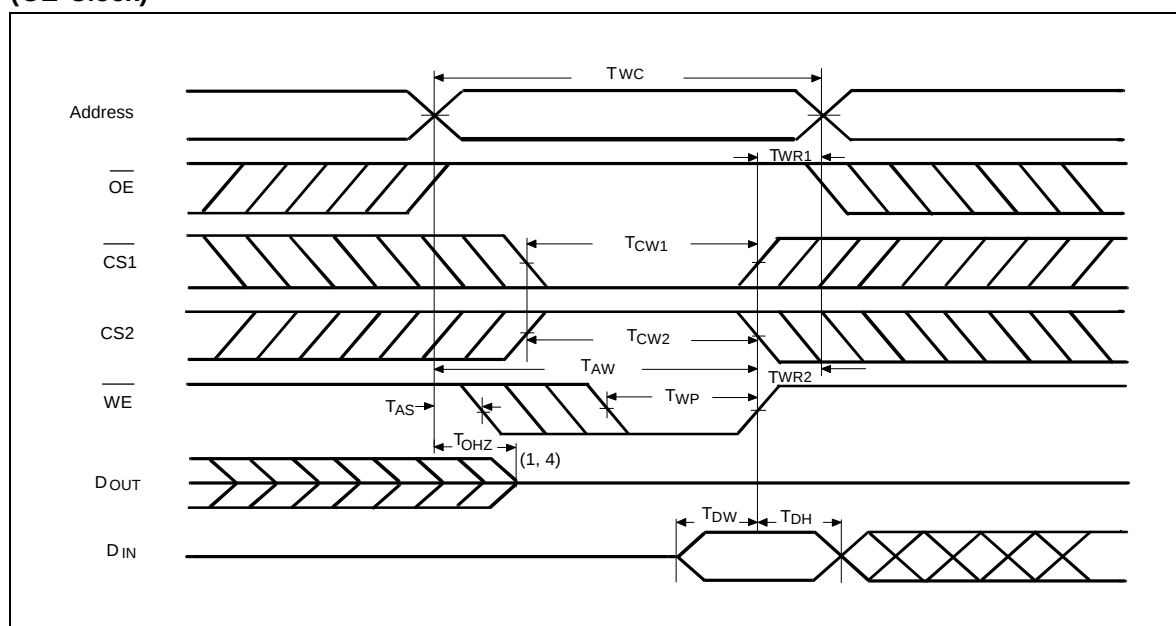
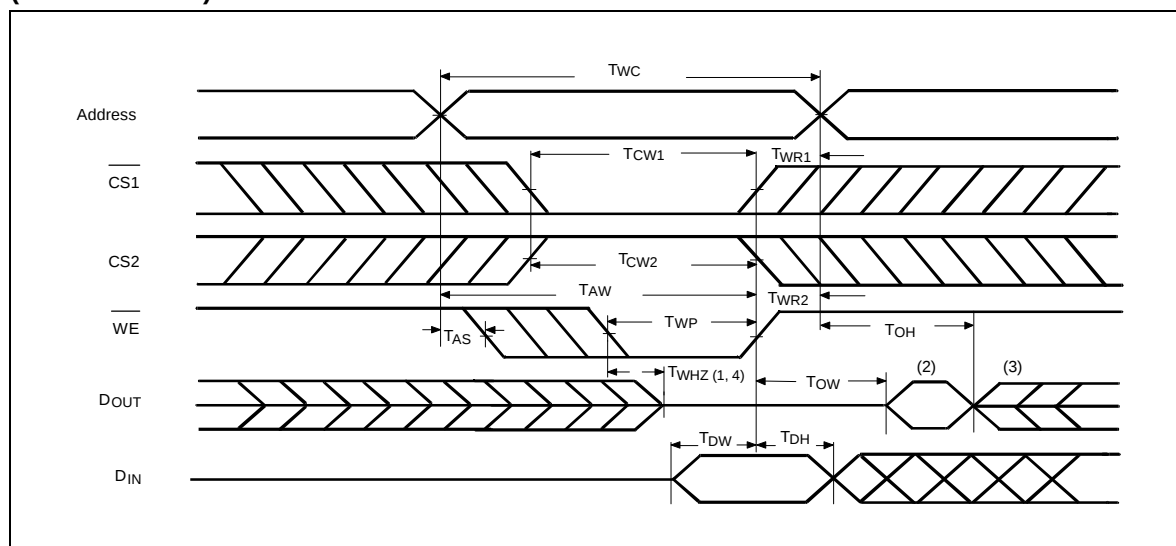
Read Cycle 3

(Output Enable Controlled)





Timing Waveforms, continued

Write Cycle 1**(OE Clock)****Write Cycle 2****(OE = VIL Fixed)**

Notes:

1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from DOUT are the same as the data written to DIN during the write cycle.
3. DOUT provides the read data for the next address.
4. Transition is measured ± 500 mV from steady state with $C_L = 5$ pF. This parameter is guaranteed but not 100% tested.

W24512A



ORDERING INFORMATION

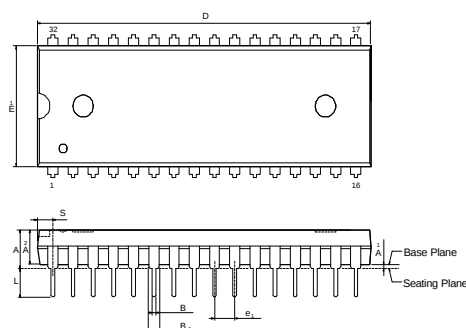
PART NO.	ACCESS TIME (nS)	OPERATING CURRENT MAX. (mA)	STANDBY CURRENT MAX. (mA)	PACKAGE
W24512A-35	35	140	10	600 mil DIP
W24512AS-35	35	140	10	450 mil SOP
W24512AT-35	35	140	10	Type one TSOP

Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

PACKAGE DIMENSIONS

32-pin P-DIP

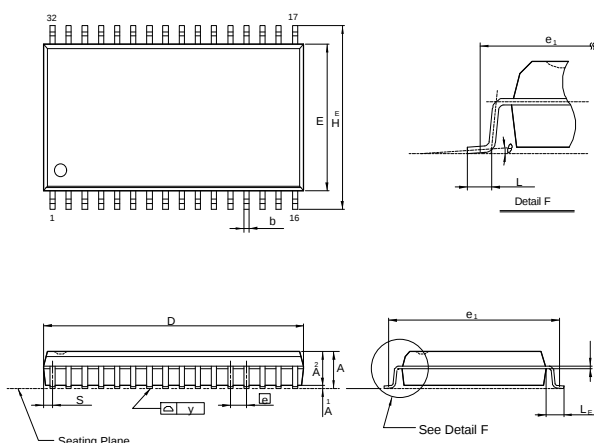


Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.210	—	—	5.33
A ₁	0.010	—	—	0.25	—	—
A ₂	0.150	0.155	0.160	3.81	3.94	4.06
B	0.016	0.018	0.022	0.41	0.46	0.56
B ₁	0.048	0.050	0.054	1.22	1.27	1.37
C	0.008	0.010	0.014	0.20	0.25	0.36
D	—	1.650	1.660	—	41.91	42.16
E	0.590	0.600	0.610	14.99	15.24	15.49
E ₁	0.540	0.550	0.555	13.84	13.97	14.10
e ₁	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
a	0	—	15	0	—	15
e _A	0.630	0.650	0.670	16.00	16.51	17.02
S	—	—	0.085	—	—	2.16

Notes:

1. Dimension D Max. & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead fillet.
3. Dimension D & E1 include mold mismatch ϵ are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/intrusion.
5. Controlling dimension: Inches.
6. General appearance spec. should be based on final visual inspection spec.

32-pin SO Wide Body



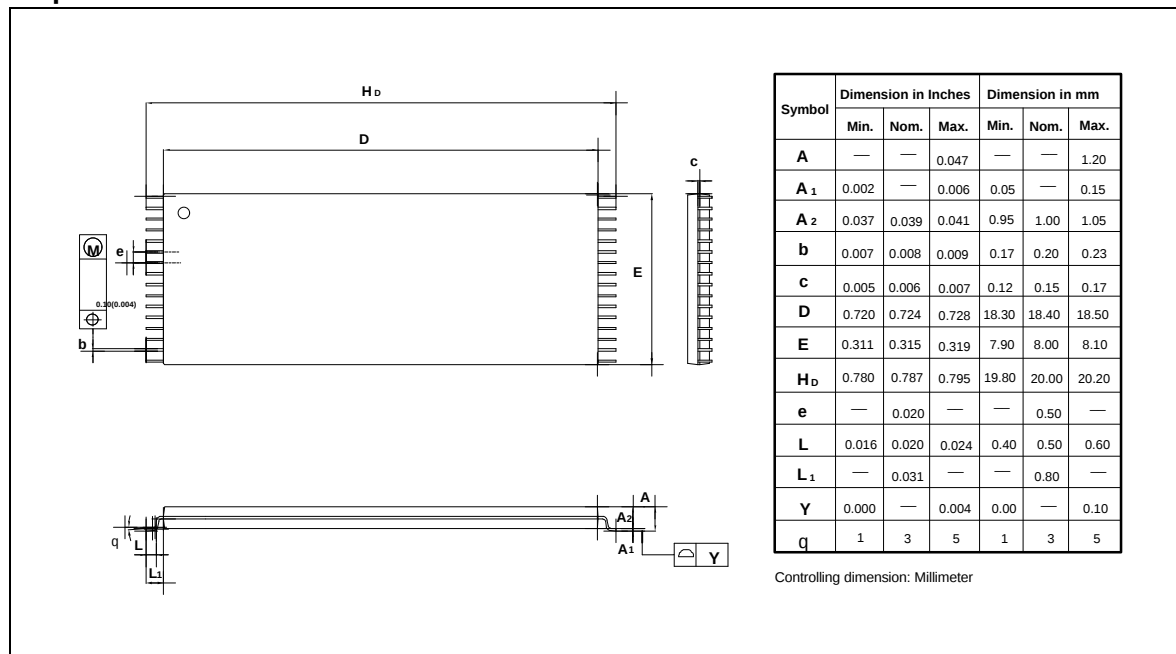
Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.118	—	—	3.00
A ₁	0.004	—	—	0.10	—	—
A ₂	0.101	0.106	0.111	2.57	2.69	2.82
b	0.014	0.016	0.020	0.36	0.41	0.51
c	0.006	0.008	0.012	0.15	0.20	0.31
D	—	0.805	0.817	—	20.45	20.75
E	0.440	0.445	0.450	11.18	11.30	11.43
E ₁	0.044	0.050	0.056	1.12	1.27	1.42
L	0.548	0.556	0.556	13.87	14.12	14.38
L ₁	0.023	0.031	0.039	0.58	0.79	0.99
L _E	0.047	0.055	0.063	1.19	1.40	1.60
S	—	—	0.036	—	—	0.91
Y	—	—	0.004	—	—	0.10
a	0*	—	10*	0*	—	10*

Notes:

1. Dimension D Max. & S include mold flash or tie bar burrs.
2. Dimension b does not include dambar protrusion/intrusion.
3. Dimension D & E include mold mismatch and are determined at the mold parting line.
4. Controlling dimension: Inches.
5. General appearance spec should be based on final visual inspection spec.

Package Dimensions, continued

32-pin TSOP





VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A2	Apr. 2000	7	Typo Correction in Standby Current Max.: mA -> μ A



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Note: All data and specifications are subject to change without notice.