WM8200-10/12

40MSPS ADC with PGA

DESCRIPTION

The WM8200 is a CMOS high speed, low power, pipeline analogue-to-digital converter (ADC) with 10 or 12-bit output options. It also has an on-chip programmable gain amplifier (PGA), dc clamp circuit and internal voltage references. Conversion is controlled by a single clock input.

The device has a high bandwidth differential sample and hold input, which gives excellent common-mode noise immunity and low distortion. Alternatively, it can be driven in single ended fashion with an optional voltage clamp for dc restoration that can take its reference from an on-chip 10-bit DAC.

The WM8200 provides internal reference voltages for setting the ADC full-scale range without the requirement for external circuitry. However, it can also accept external references for applications where shared or high-precision references are required.

A 3-wire serial interface is used to control the device and a 10 or 12-bit parallel interface is to read ADC conversion data. ADC data can be output in unsigned binary or two's complement format.

The WM8200 operates with a single 3V supply and is supplied in a 28-lead QFN package.

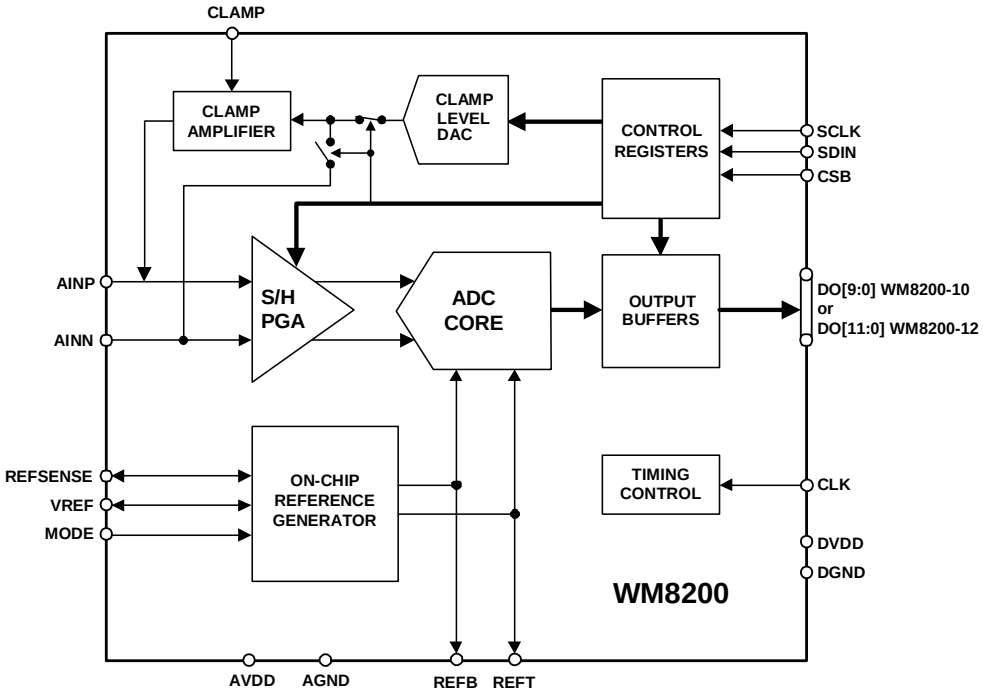
FEATURES

- 10 or 12-bit resolution ADC
- 40MSPS conversion rate
- Programmable Gain Amplifier (PGA)
- Adjustable internal voltage references
- Built in clamp function (dc restore) with 10-bit DAC
- Wide Input Bandwidth - 900MHz
- Unsigned Binary or Two's complement output format
- Programmable via 3-wire serial MPU interface
- Single 3V supply operation
- Low power - 100mW typical at 3.0V supplies
- Powerdown mode to <0.1mW typical
- 28 lead QFN package

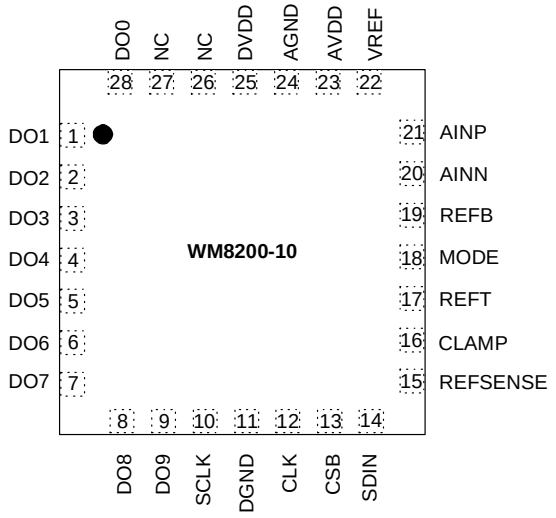
APPLICATIONS

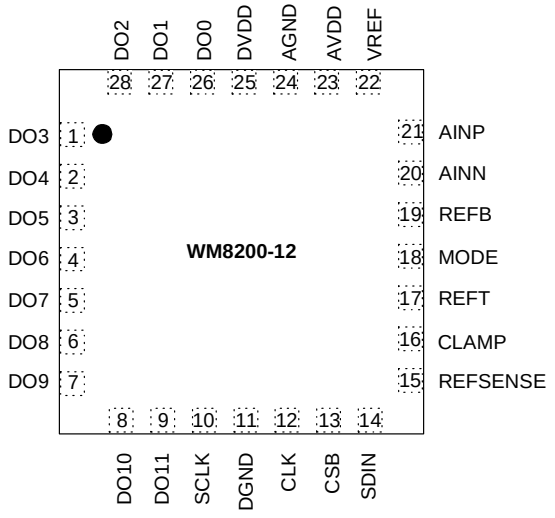
- Digital Still Cameras
- Composite Video Digitisation
- Digital Copiers
- Digital Video Cameras

BLOCK DIAGRAM



PIN CONFIGURATION





ORDERING INFORMATION

DEVICE	TEMP. RANGE	PACKAGE
WM8200-10IFL	-40 to +85°C	28-lead QFN
WM8200-12IFL	-40 to +85°C	28-lead QFN

PIN DESCRIPTION

PIN	NAME		TYPE	DESCRIPTION
1	DO1	DO3	Digital Output	Digital output bit
2	DO2	DO4	Digital Output	Digital output bit
3	DO3	DO5	Digital Output	Digital output bit
4	DO4	DO6	Digital Output	Digital output bit
5	DO5	DO7	Digital Output	Digital output bit
6	DO6	DO8	Digital Output	Digital output bit
7	DO7	DO9	Digital Output	Digital output bit
8	DO8	DO10	Digital Output	Digital output bit
9	DO9	DO11	Digital Output	Digital output bit (MSB)
10	SCLK		Digital Input	3-Wire Control Interface Clock Input
11	DGND		Ground	Negative Digital Supply
12	CLK		Analogue Input	Clock input
13	CSB		Digital Input	3-Wire Control Interface Chip Select
14	SDIN		Digital Input	3-Wire Control Interface Data Input
15	REFSENSE		Analogue Input	VREF feedback/configuration control
16	CLAMP		Digital Input	High to enable clamp mode, low to disable clamp mode
17	REFT		Analogue Input/Output	Top ADC reference voltage
18	MODE		Analogue Input	High (MODE=AVDD) to enable internal ADC references. Low (MODE=AVSS) to enable use of external ADC references applied to REFT and REFB.
19	REFB		Analogue Input/Output	Bottom ADC reference voltage
20	AINN		Analogue Input	Positive analogue input
21	AINP		Analogue Input	Negative analogue Input
22	VREF		Analogue Input/Output	Internal/external reference voltage
23	AVDD		Supply	Positive Analogue Supply
24	AGND		Ground	Negative Analogue Supply
25	DVDD		Supply	Positive Digital Supply
26	NC	DO0	Digital Output	Not internally connected (10-bit option)/ Digital output bit (LSB for 12-bit option only)
27	NC	DO1	Digital Output	Not internally connected (10-bit option) / Digital output bit (for 12-bit Option Only)
28	DO0	DO2	Digital Output	Digital output bit (LSB for 10-bit Option)

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

CONDITION	MIN	MAX
Digital supply voltage, DVDD to DGND	-0.3V	+3.63V
Analog supply voltage, AVDD to AGND	-0.3V	+3.63V
Maximum voltage difference between AGND and DGND	-0.3V	+0.3V
Voltage range digital input (SCLK, SDIN, CSB, CLAMP)	DGND - 0.3V	DVDD + 0.3V
Voltage range analog inputs	AGND - 0.3V	AVDD + 0.3V
Voltage range CLK, MODE inputs	AGND - 0.3V	AVDD + 0.3V
Operating junction temperature range, T_J	-40°C	+150°C
Storage temperature	-65°C	+150°C
Package Body Temperature (soldering 10 seconds)		+240°C
Package Body Temperature (soldering 2 minutes)		+183°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Digital supply range	DVDD		3.0	3.3	3.6	V
Analog supply range	AVDD		3.0	3.3	3.6	V
Ground	DGND, AGND			0		V
Clock frequency	f_{CLK}		5		40	MHz
Clock duty cycle			45	50	55	%
Operating Free Air Temperature	T_A		-40		85	°C

ELECTRICAL CHARACTERISTICS

Test Conditions:
AVDD = DVDD = 3.0V, f_{CLK} = 40MHz, 50% duty cycle, MODE = AVDD, VREF=1.0V (REFT = 2.0V, REFB = 1.0V),
PGA gain = 1.0, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Accuracy						
Integral nonlinearity	INL			±1.0		LSB
Differential nonlinearity	DNL			±0.3		LSB
Offset error				0.7		% of FSR
Full scale error				2.2		% of FSR
Missing codes			No missing codes guaranteed			
Analogue Input Signal to AIN pins						
Differential analogue input voltage (AINP-AINN)		PGA=1x gain	-1		1	V
Switched input capacitance				1.2		pF
Conversion Characteristics						
Conversion frequency	f_{CLK}		5		40	MHz
Pipeline delay				4		cycles of CLK
Dynamic Performance (differential input mode)						
Effective number of bits	ENOB	f_{IN} = 4.8MHz		9.6		bits
		f_{IN} = 20MHz		9.5		
Spurious free dynamic range	SFDR	f_{IN} = 4.8MHz		72		dB
		f_{IN} = 20MHz		70		
Total harmonic distortion	THD	f_{IN} = 4.8MHz		-72.5		dB
		f_{IN} = 20MHz		-71.6		
Signal to noise ratio	SNR	f_{IN} = 4.8MHz		60		dB
		f_{IN} = 20MHz		57		
Signal to noise and distortion ratio	SINAD	f_{IN} = 4.8MHz		59.7		dB
		f_{IN} = 20MHz		59.6		
PGA						
Gain range (linear scale)			0.5		4	V/V
Gain step size (linear scale)				0.5		V/V
Clamp						
Clamp DAC resolution				10		bits
Clamp DAC output voltage			REFB		REFT	V
Clamp DAC DNL				±1		LSB
Clamp output voltage error			-40		40	mV
REFB, REFT internal ADC reference voltage outputs (MODE= AVDD)						
Reference voltage top, REFT (AVDD=3V)		VREF = 0.5V		1.75		
		VREF= 1.0V		2		
Reference voltage bottom, REFB (AVDD=3V)		VREF = 0.5V		1.25		
		VREF= 1.0V		1		
VREF Input / Output specifications (ADC Input Range = VREFx2)						
Internal 0.5V reference to VREF		REFSENSE = VREF		0.5		V
Internal 1V reference to VREF		REFSENSE = AGND		1		V
External reference applied to VREF pin		REFSENSE = AVDD	0.5		1	V
Input impedance in internal ADC reference mode		REFSENSE = AVDD, MODE = AVDD		14		kΩ

Test Conditions:
AVDD = DVDD = 3.0V, f_{CLK} = 40MHz, 50% duty cycle, MODE = AVDD, VREF=1.0V (REFT = 2.0V, REFB = 1.0V), PGA gain = 1.0, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supplies						
Analogue supply current	I_{AVDD}	MODE = AGND		28.5		mA
		MODE = AVDD		31		mA
Digital supply current	I_{DVDD}	C_L = 10pF		5		mA
Standby power consumption (digital and analogue combined)	I_{VDD}(STBY)			75		uW
Digital Logic Levels (CMOS Levels)						
Input LOW level	V_{IL}	(Note 1)			0.2 x VDD	V
Input HIGH level	V_{IH}	(Note 1)	0.8 x VDD			V
Output LOW	V_{OL}	I_{OL} = -50µA			0.4	V
Output HIGH	V_{OH}	I_{OH} = 50µA	VDD – 0.4			V

Notes

1. Digital input and output levels refer to the supply used for the input/output buffer on the relevant pin. CLK and MODE refer to the AVDD supply, all other digital input/output refers to the DVDD supply.

CONTROL INTERFACE TIMING

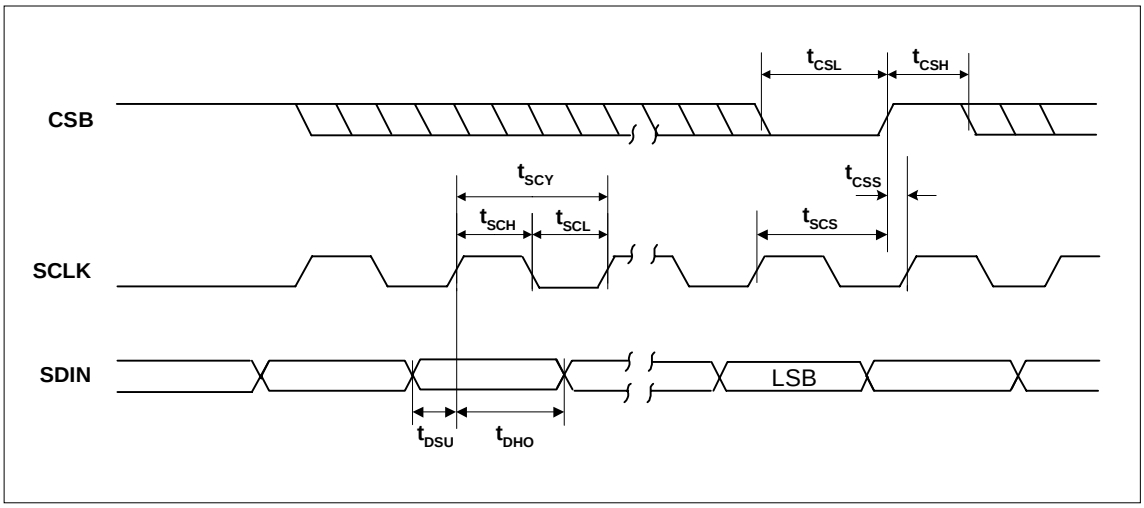


Figure 1: Control Interface Timing

Test Conditions

AVDD = DVDD = 3.0V, AGND = DGND = 0V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise stated

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Program Register Input Information						
SCLK rising edge to CSB rising edge	t_{SCS}		60			ns
SCLK pulse cycle time	t_{SCY}		80			ns
SCLK pulse width low	t_{SCL}		30			ns
SCLK pulse width high	t_{SCH}		30			ns
SDIN to SCLK set-up time	t_{DSU}		20			ns
SCLK to SDIN hold time	t_{DHO}		20			ns
CSB pulse width low	t_{CSL}		20			ns
CSB pulse width high	t_{CSH}		20			ns
CSB rising to SCLK rising	t_{CSS}		20			ns

Table 1 Control Interface Timing Information

CONTROL INTERFACE

The internal control registers are programmable via the 3-wire serial interface. SDIN is used for the program data, SCLK is used to clock in the data and CSB is used to latch in the program data. The 3-wire interface protocol is shown in Figure 2.

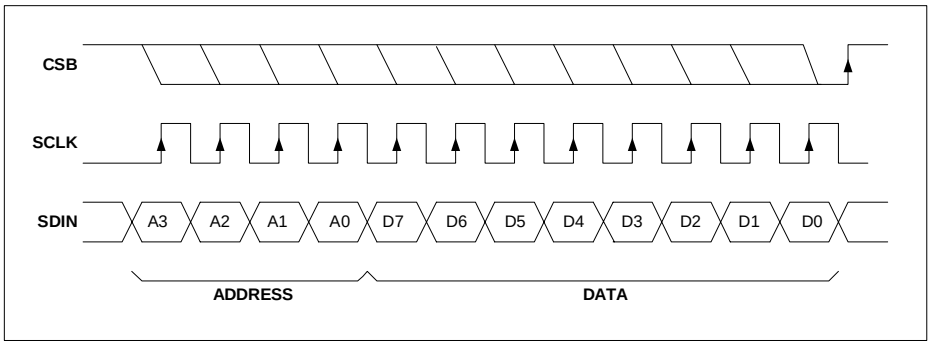


Figure 2: 3-Wire Serial Interface

1. A[3:0] are Control Address Bits
2. D[7:0] are Control Data Bits
3. CSB is edge sensitive – the data is latched on the rising edge of CSB.

REGISTER MAP

Table 2 shows the location of each control bit used to determine the operation of the WM8200. The procedure for programming the register map is described in the CONTROL INTERFACE section.

ADDR	NAME	DEFAULT (HEX)	BIT							
			B7	B6	B5	B4	B3	B2	B1	B0
0000	Clamp Reg 1	00	DAC[7]	DAC[6]	DAC[5]	DAC[4]	DAC[3]	DAC[2]	DAC[1]	DAC[0]
0001	Clamp Reg 2	00	0	0	0	0	0	0	DAC[9]	DAC[8]
0010	PGA Control	01	0	0	PGASENSE	PGAOFF	0	PGA[2]	PGA[1]	PGA[0]
0011	Control	00	0	0	0	CLPSEL	OEB	TWOSC	CLDIS	PD
0100 - 1111	Reserved	00	Reserved, do not write to these register locations							

Table 2: Register Map

REGISTER MAP DESCRIPTION

REGISTER	BIT	BIT NAMES	DEFAULT	DESCRIPTION
Clamp Register 1	7:0	DAC[7:0]	00000000	Clamp DAC value bits 7 to 0 (Unsigned binary format)
Clamp Register 2	1:0	DAC[9:8]	00	Clamp DAC value bits 9 to 8 (Unsigned binary format)
PGA Control Register	2:0	PGA[2:0]	001	PGA Gain control 000: PGA Gain = 0.5x / 100: PGA Gain = 2.5x 001: PGA Gain = 1.0x / 101: PGA Gain = 3.0x 010: PGA Gain = 1.5x / 110: PGA Gain = 3.5x 011: PGA Gain = 2.0x / 111: PGA Gain = 4.0x
	4	PGAOFF	0	Enables a coarse offset to be added to the output of the PGA. Allows the use of single ended input signals with no loss of ADC dynamic range.
	5	PGASENSE	0	Determines the sense of the coarse offset added to the output of the PGA. This bit only has an effect when PGAOFF=1. 0: PGA output is offset to full-scale positive for zero differential input (suitable for negative going video). 1: PGA output is offset to full-scale negative for zero differential input (suitable for positive going video).
ontrol Register	0	PD	0	Device power-down 0: Device is powered up 1: Device is powered down.
	1	CLDIS	0	CLAMP amplifier enable (for power saving) 0: Enable 1: Disable
	2	TWOSC	0	Output data format 0: Unsigned binary 1: Twos complement
	3	OEB	0	Output data pin enable 0: DO[9:0]/DO[11:0] enabled 1: DO[9:0]/DO[11:0] disabled (outputs are high impedance).
	4	CLPSEL	0	Clamp source select 0: Clamp to output of Clamp DAC 1: Clamp to voltage on AINN input pin

REFERENCE VOLTAGE GENERATION

The WM8200 incorporates an on-chip 0.5V bandgap voltage reference that can be used to derive a temperature and supply independent voltage on pin VREF. The VREF output can be used for driving external loads or setting the ADC input range. The voltage is programmed via connections made to the REFSENSE pin as shown in Table 3.

REFSENSE	VREF output	Refer to
AGND	1.0V	Figure 3
AVDD	Hi impedance – A1 amplifier disabled If using the ADC reference generator then an external VREF source must be applied to the VREF pin.	Figure 4
Connect to VREF	0.5V	Figure 5
R network to VREF / AGND	Between 0.5 V and 1 V VREF=0.5x(1+Ra/Rb)	Figure 6

Table 3: – VREF output control by REFSENSE connection

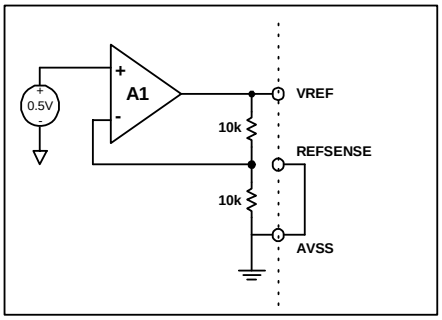


Figure 3: VREF=1V

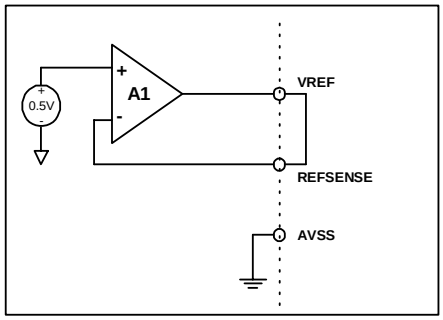


Figure 5: VREF=0.5V

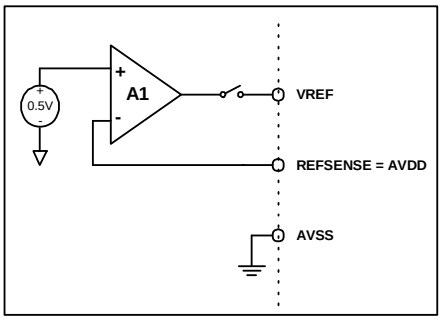


Figure 4: VREF=Hi Impedance

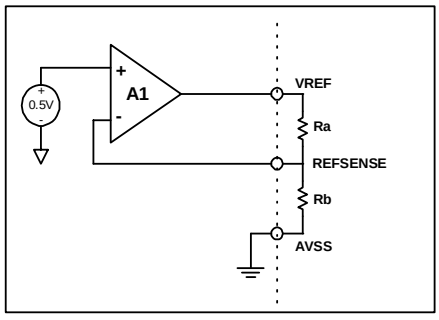


Figure 6: VREF between 0.5 and 1V

When enabled, the on-chip voltage reference should be externally decoupled (see Reference Decoupling Section for details).

In internal ADC references mode (MODE=AVDD), the voltages at REFT and REFB are:

REFT = (AVDD + VREF) / 2

REFB = (AVDD – VREF) / 2

If external ADC references mode (MODE=AVSS), the average value of the external voltages applied to REFT and REFB should be AVDD/2 for correct device operation.

REFERENCE DECOUPLING

VREF, REFT and REFB must be decoupled as shown in Figure 7.

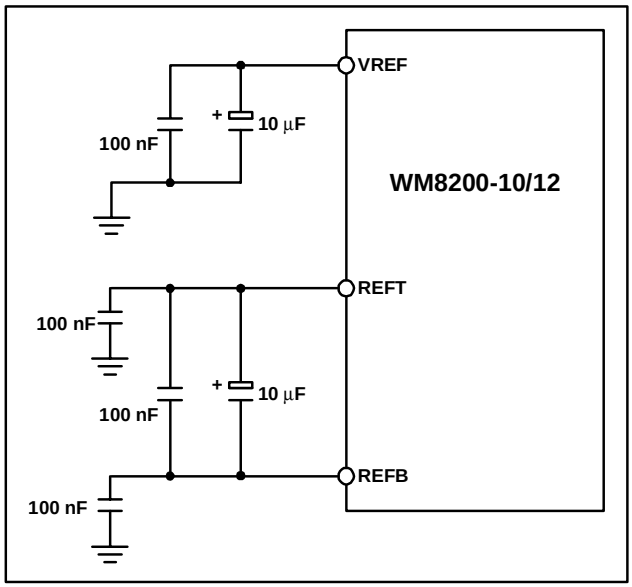
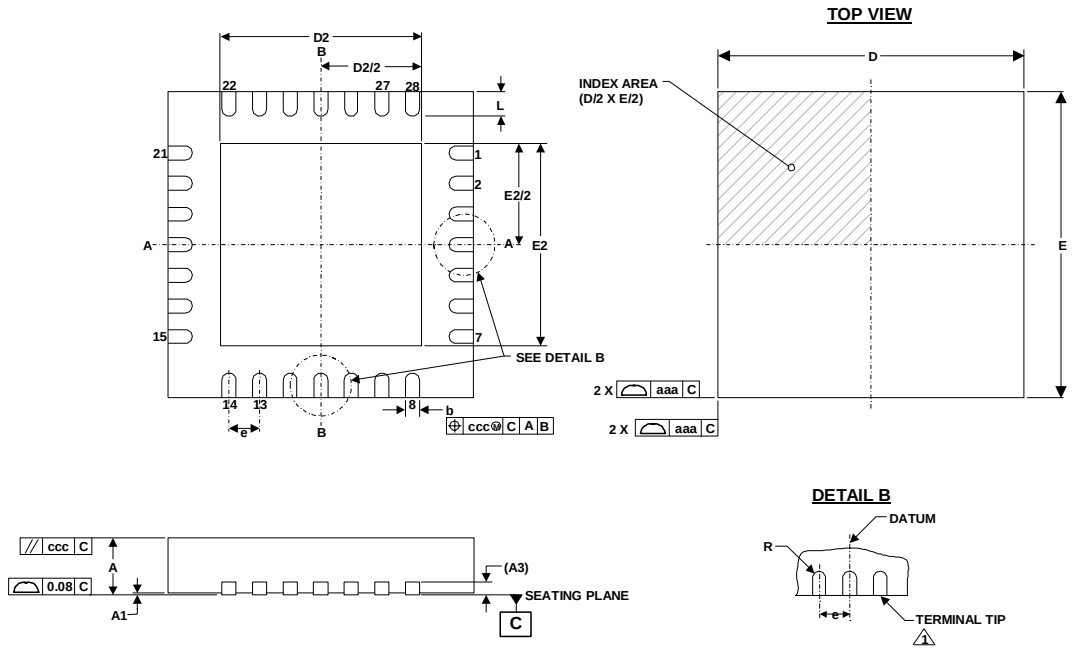


Figure 7: VREF, REFT and REFB decoupling

PACKAGE DIMENSIONS

FL: 28 PIN QFN PLASTIC PACKAGE 5 X 5 X 0.9 mm BODY, 0.50 mm LEAD PITCH **DM023.C**



Symbols	Dimensions (mm)			
	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	0	0.02	0.05	
A3		0.2 REF		2
b	0.18	0.23	0.30	1
D		5.00 BSC		
D2	3.2	3.3	3.4	2
E		5.00 BSC		
E2	3.2	3.3	3.4	2
e		0.5 BSC		
L	0.35	0.4	0.45	
R	b(min)/2			
Tolerances of Form and Position				
aaa		0.15		
ccc		0.10		
REF:	JEDEC.95, MO-220, VARIATION VHHD-1			

NOTES:
1. DIMENSION b APPLIED TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
2. FALLS WITHIN JEDEC.95, MO-220 WITH THE EXCEPTION OF D2, E2, A3:
   D2,E2: LARGER PAD SIZE CHOSEN WHICH IS JUST OUTSIDE JEDEC SPECIFICATION
   A3: NOMINAL VALUE LESS THAN JEDEC
3. ALL DIMENSIONS ARE IN MILLIMETRES
4. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.

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