# WM8763/4/5

## 24-bit, 192kHz 6-Channel DAC

### DESCRIPTION

The WM8763/4/5 are multi-channel audio DACs ideal for DVD and surround sound processing applications for home hi-fi, automotive and other audio visual equipment.

Three stereo 24-bit multi-bit sigma delta DACs are used with oversampling digital interpolation filters. Digital audio input word lengths from 16-32 bits and sampling rates from 8kHz to 192kHz are supported.

The audio data interface supports either 16-24-bit $I^2S$, 16-24-bit left justified, or 24-bit right justified digital audio formats.

The devices are controlled directly using the hardware interface. All members of the family are available in a 20-pin SSOP.

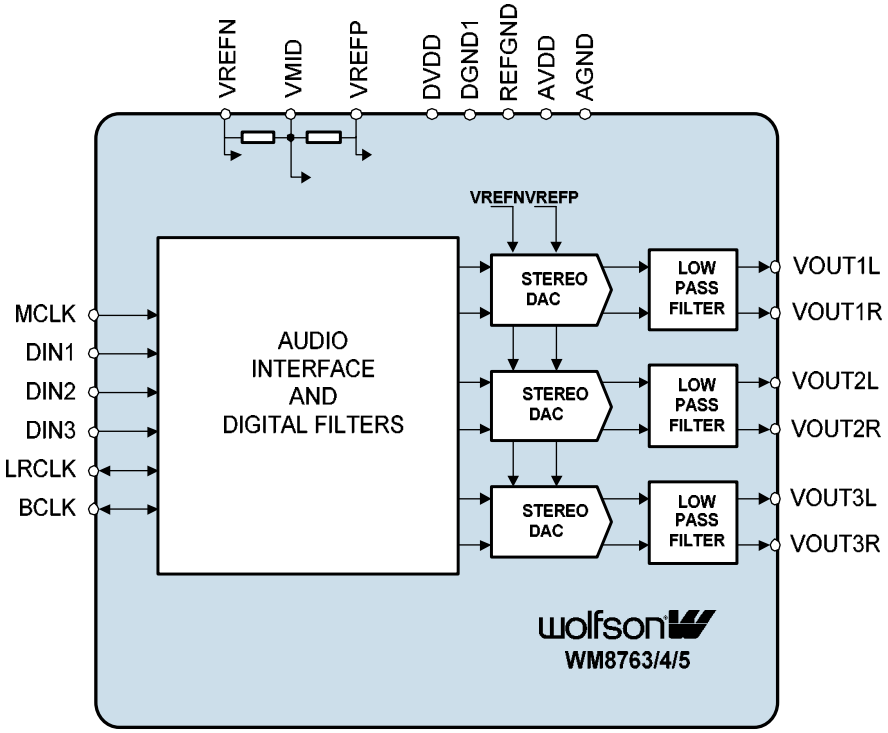
### FEATURES

- 6-Channel DAC with PCM.
- Audio Performance
  - 103dB SNR ('A' weighted @ 48kHz) DAC
- DAC Sampling Frequency: 8kHz – 192kHz
- Hardware Control Interface
- Choice of Audio Data Interface Modes
  - WM8763: 16-24-bit $I^2S$
  - WM8764: 16-24-bit Left Justified
  - WM8765: 16-24-Bit Right Justified
- Slave Audio Data Interface
- 2.7V to 5.5V Analogue, 2.7V to 3.6V Digital supply Operation
- 20 pin SSOP Package

### APPLICATIONS

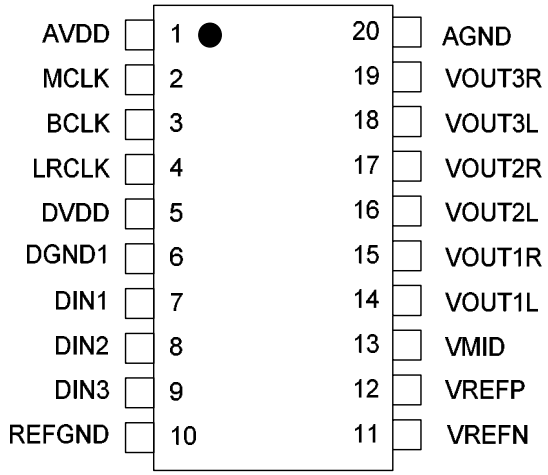
- DVD Players
- Surround Sound AV Processors and Hi-Fi systems
- Automotive Audio

### BLOCK DIAGRAM



# TABLE OF CONTENTS

## PIN CONFIGURATION 20 LEAD SSOP




## ORDERING INFORMATION

| DEVICE | TEMP. RANGE | PACKAGE | MOISTURE SENSITIVITY LEVEL |
|---|---|---|---|
| WM8763EDS | -25 to +85°C | 20-pin SSOP | MSL1 |
| WM8763GEDS | -25 to +85°C | 20-pin SSOP (lead free) | MSL1 |
| WM8763EDS/R | -25 to +85°C | 20-pin SSOP (tape and reel) | MSL1 |
| WM8763GEDS/R | -25 to +85°C | 20-pin SSOP (lead free, tape and reel) | MSL1 |

| DEVICE | TEMP. RANGE | PACKAGE | MOISTURE SENSITIVITY LEVEL |
|---|---|---|---|
| WM8764EDS | -25 to +85°C | 20-pin SSOP | MSL1 |
| WM8764GEDS | -25 to +85°C | 20-pin SSOP (lead free) | MSL1 |
| WM8764EDS/R | -25 to +85°C | 20-pin SSOP (tape and reel) | MSL1 |
| WM8764GEDS/R | -25 to +85°C | 20-pin SSOP (lead free, tape and reel) | MSL1 |

| DEVICE | TEMP. RANGE | PACKAGE | MOISTURE SENSITIVITY LEVEL |
|---|---|---|---|
| WM8765EDS | -25 to +85°C | 20-pin SSOP | MSL1 |
| WM8765GEDS | -25 to +85°C | 20-pin SSOP (lead free) | MSL1 |
| WM8765EDS/R | -25 to +85°C | 20-pin SSOP (tape and reel) | MSL1 |
| WM8765GEDS/R | -25 to +85°C | 20-pin SSOP (lead free, tape and reel) | MSL1 |

**Note:**

Reel quantity = 2,000

## PIN DESCRIPTION – 20 PIN SSOP

| PIN | NAME | TYPE | DESCRIPTION |
|---|---|---|---|
| 1 | AVDD | Supply | Analogue positive supply |
| 2 | MCLK | Digital input | Master clock; 128, 192, 256, 384, 512 or 768fs (fs = word clock frequency) |
| 3 | BCLK | Digital input | Audio interface bit clock |
| 4 | LRCLK | Digital input | Audio left/right word clock |
| 5 | DVDD | Digital supply | Digital positive supply |
| 6 | DGND1 | Digital ground | Digital Negative supply 1 |
| 7 | DIN1 | Digital input | DAC channel 1 data input |
| 8 | DIN2 | Digital input | DAC channel 2 data input |
| 9 | DIN3 | Digital input | DAC channel 3 data input |
| 10 | REFGND | Digital input | Ground Reference |
| 11 | VREFN | Analogue Input | DAC negative reference supply |
| 12 | VREFP | Analogue Input | DAC positive reference supply |
| 13 | VMID | Analogue output | Midrail divider decoupling pin; 10uF external decoupling |
| 14 | VOUT1L | Analogue output | DAC channel 1 left output |
| 15 | VOUT1R | Analogue output | DAC channel 1 right output |
| 16 | VOUT2L | Analogue output | DAC channel 2 left output |
| 17 | VOUT2R | Analogue output | DAC channel 2 right output |
| 18 | VOUT3L | Analogue output | DAC channel 3 left output |
| 19 | VOUT3R | Analogue output | DAC channel 3 right output |
| 20 | AGND | Supply | Analogue negative and substrate connection |

**Note** : Digital input pins have Schmitt trigger input buffers.

## ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

| CONDITION | MIN | MAX |
|---|---|---|
| Digital supply voltage | -0.3V | +5V |
| Analogue supply voltage | -0.3V | +7V |
| Voltage range digital inputs | AGND -0.3V | DVDD +0.3V |
| Voltage range analogue inputs | AGND -0.3V | AVDD +0.3V |
| Master Clock Frequency | | 37MHz |
| Operating temperature range, $T_A$ | -25°C | +85°C |
| Storage temperature after soldering | -65°C | +150°C |
| Package body temperature (soldering 10 seconds) | | +240°C |
| Package body temperature (soldering 2 minutes) | | +183°C |

**Notes:**

1. Analogue and digital grounds must always be within 0.3V of each other for normal operation of the device.

## RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Digital supply range | DVDD | | 2.7 | | 3.6 | V |
| Analogue supply range | AVDD, VREFP | | 2.7 | | 5.5 | V |
| Ground | GND, VREFN | | | 0 | | V |

**Note:** Digital supply DVDD must never be more than 0.3V greater than AVDD for normal operation of the device.

## ELECTRICAL CHARACTERISTICS

**Test Conditions**

AVDD, VREFP = 5V, DVDD = 3.3V, GND, VREFN = 0V, $T_A$ = +25°C, fs = 48kHz, MCLK = 256fs, unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Digital Logic Levels (CMOS Levels)** | | | | | | |
| Input LOW level | $V_{IL}$ | | | | 0.3 x DVDD | V |
| Input HIGH level | $V_{IH}$ | | 0.7 x DVDD | | | V |
| Output LOW | $V_{OL}$ | $I_{OL}$=1mA | | | 0.1 x DVDD | V |
| Output HIGH | $V_{OH}$ | $I_{OH}$= -1mA | 0.9 x DVDD | | | V |
| **Analogue Reference Levels** | | | | | | |
| Reference voltage | $V_{VMID}$ | | | VREFP/2 | | V |
| Potential divider resistance | $R_{VMID}$ | | | 100k | | Ω |
| **DAC Performance (Load = 10kΩ, 50pF)** | | | | | | |
| 0dBFs Full scale output voltage | | | | 1.0 x VREFP/5 | | Vrms |
| SNR (Note 1,2,4) | | A-weighted, @ fs = 48kHz | 95 | 103 | | dB |
| SNR (Note 1,2,4) | | A-weighted @ fs = 96kHz | | 101 | | dB |
| SNR (Note 1,2,4) | | A-weighted @ fs = 192kHz | | 101 | | dB |
| SNR (Note 1,2,4) | | A-weighted @ fs = 48kHz, AVDD = 3.3V | | 101 | | dB |
| SNR (Note 1,2,4) | | A-weighted @ fs = 96kHz, AVDD = 3.3V | | 96 | | dB |
| Dynamic Range (Note 2,4) | DNR | A-weighted, -60dB full scale input | 95 | 103 | | dB |
| Total Harmonic Distortion (THD) (Note 4) | | 1kHz, 0dBFs | | -90 | -85 | dB |
| Mute Attenuation | | 1kHz Input, 0dB gain | | 100 | | dB |
| DAC channel separation | | | | 100 | | dB |
| Power Supply Rejection Ratio | PSRR | 1kHz 100mVpp | | 50 | | dB |
| | | 20Hz to 20kHz 100mVp-p | | 45 | | dB |
| **Supply Current** | | | | | | |
| Analogue supply current | | AVDD = 5V | | 13.8 | | mA |
| Digital Supply Current | | DVDD = 3.3V | | 11 | | mA |

**Notes:**

1. Ratio of output level with 1kHz full scale input, to the output level with all zeros into the digital input, measured 'A' weighted.
2. All performance measurements done with 20kHz low pass filter, and where noted an A-weight filter. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.
3. VMID decoupled with 10uF and 0.1uF capacitors (smaller values may result in reduced performance).
4. The performance of each DAC is measured separately

# TERMINOLOGY

1. Signal-to-noise ratio (dB) - SNR is a measure of the difference in level between the full scale output and the output with no signal applied. (No Auto-zero or Automute function is employed in achieving these results).
2. Dynamic range (dB) - DNR is a measure of the difference between the highest and lowest portions of a signal. Normally a THD+N measurement at 60dB below full scale. The measured signal is then corrected by adding the 60dB to it. (e.g. THD+N @ -60dB= -32dB, DR= 92dB).
3. THD+N (dB) - THD+N is a ratio, of the rms values, of (Noise + Distortion)/Signal.
4. Stop band attenuation (dB) - Is the degree to which the frequency spectrum is attenuated (outside audio band).
5. Channel Separation (dB) - Also known as Cross-Talk. This is a measure of the amount one channel is isolated from the other. Normally measured by sending a full scale signal down one channel and measuring the other.
6. Pass-Band Ripple - Any variation of the frequency response in the pass-band region.

## MASTER CLOCK TIMING

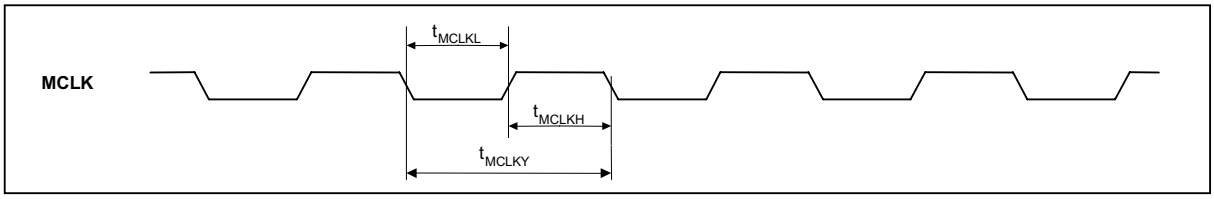



**Figure 1 DAC Master Clock Timing Requirements**

**Test Conditions**

AVDD, VREFP = 5V, DVDD = 3.3V, GND, VREFN = 0V, $T_A$ = +25°C, fs = 48kHz, DACMCLK and ADCMCLK = 256fs unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **System Clock Timing Information** | | | | | | |
| MCLK System clock pulse width high | $t_{MCLKH}$ | | 11 | | | ns |
| MCLK System clock pulse width low | $t_{MCLKL}$ | | 11 | | | ns |
| MCLK System clock cycle time | $t_{MCLKY}$ | | 28 | | | ns |
| MCLK Duty cycle | | | 40:60 | | 60:40 | |

**Table 1 Master Clock Timing Requirements**

## DIGITAL AUDIO INTERFACE

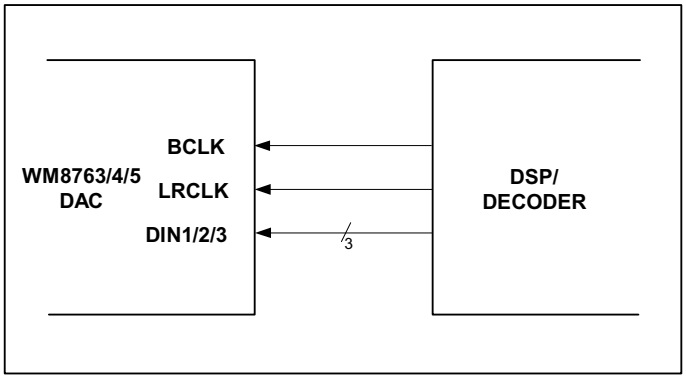



**Figure 2 Audio Interface**

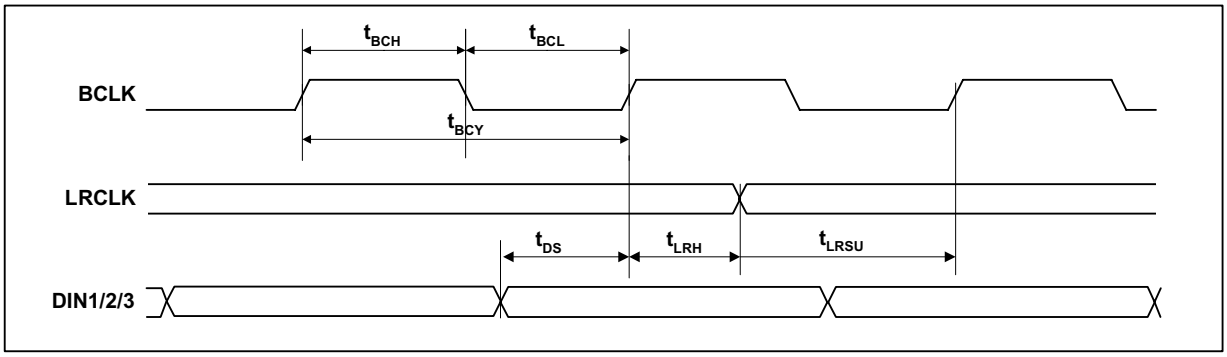



**Figure 3 Digital Audio Data Timing – Slave Mode**

**Test Conditions**

AVDD = 5V, DVDD = 3.3V, AGND = 0V, DGND = 0V, $T_A$ = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Audio Data Input Timing Information** | | | | | | |
| BCLK cycle time | $t_{BCY}$ | | 50 | | | ns |
| BCLK pulse width high | $t_{BCH}$ | | 20 | | | ns |
| BCLK pulse width low | $t_{BCL}$ | | 20 | | | ns |
| LRCLK set-up time to BCLK rising edge | $t_{LRSU}$ | | 10 | | | ns |
| LRCLK hold time from BCLK rising edge | $t_{LRH}$ | | 10 | | | ns |
| DIN1/2/3 set-up time to BCLK rising edge | $t_{DS}$ | | 10 | | | ns |
| DIN1/2/3 hold time from BCLK rising edge | $t_{DH}$ | | 10 | | | ns |

**Table 2 Digital Audio Data Timing – Slave Mode**

# DEVICE DESCRIPTION

## INTRODUCTION

WM8763/4/5 is a complete 6-channel DAC including digital interpolation and decimation filters and switched capacitor multi-bit sigma delta DACs with digital volume controls on each channel and output smoothing filters.

The device is implemented as 3 separate stereo DACs in a single package and controlled by a single interface.

Each stereo DAC has its own data input DIN1/2/3. DAC word clock LRCLK and DAC bit clock BCLK and DAC master clock MCLK are shared between them.

Operation using master clocks of 128fs, 192fs, 256fs, 384fs, 512fs or 768fs is provided for the DAC. The selection between clock rates is automatically controlled. Audio sample rates (fs) from less than 8ks/s up to 192ks/s are allowed for the DAC, provided the appropriate master clock is input.

The audio data interface supports right, left and $I^2S$ interface formats.

## AUDIO DATA SAMPLING RATES

In a typical digital audio system there is only one central clock source producing a reference clock to which all audio data processing is synchronised. This clock is often referred to as the audio system's Master Clock. The external master system clock can be applied directly through the MCLK input pin(s) with no software configuration necessary.

The DAC master clock for WM8763/4/5 supports audio sampling rates from 128fs to 768fs, where fs is the audio sampling frequency (LRCLK) typically 32kHz, 44.1kHz, 48kHz, 96kHz or 192kHz. The master clock is used to operate the digital filters and the noise shaping circuits.

In Slave mode the WM8763/4/5 has a master clock detection circuit that automatically determines the relationship between the system clock frequency and the sampling rate (to within +/- 32 master clocks). If there is a greater than 32 clocks error the interface defaults to 768fs mode. The WM8763/4/5 is tolerant of phase variations or jitter on the master clock. Table 3 shows the typical master clock frequency inputs for the WM8763/4/5.

The signal processing for the WM8763/4/5 typically operates at an oversampling rate of 128fs. The exception to this is for operation with a 128/192fs system clock, e.g. for 192kHz operation, when the oversampling rate is 64fs.

| SAMPLING RATE (LRCLK) | System Clock Frequency (MHz) | | | | | |
|---|---|---|---|---|---|---|
| | 128fs | 192fs | 256fs | 384fs | 512fs | 768fs |
| 32kHz | 4.096 | 6.144 | 8.192 | 12.288 | 16.384 | 24.576 |
| 44.1kHz | 5.6448 | 8.467 | 11.2896 | 16.9340 | 22.5792 | 33.8688 |
| 48kHz | 6.144 | 9.216 | 12.288 | 18.432 | 24.576 | 36.864 |
| 96kHz | 12.288 | 18.432 | 24.576 | 36.864 | Unavailable | Unavailable |
| 192kHz | 24.576 | 36.864 | Unavailable | Unavailable | Unavailable | Unavailable |

**Table 3 System Clock Frequencies Versus Sampling Rate**

## DIGITAL AUDIO INTERFACE

### SLAVE MODE

The audio interface operates in Slave mode. The default is Slave mode.

In Slave mode, LRCLK and BCLK are inputs to the WM8763/4/5 (Figure 4). DIN1/2/3 and LRCLK are sampled by the WM8763/4/5 on the rising edge of BCLK.

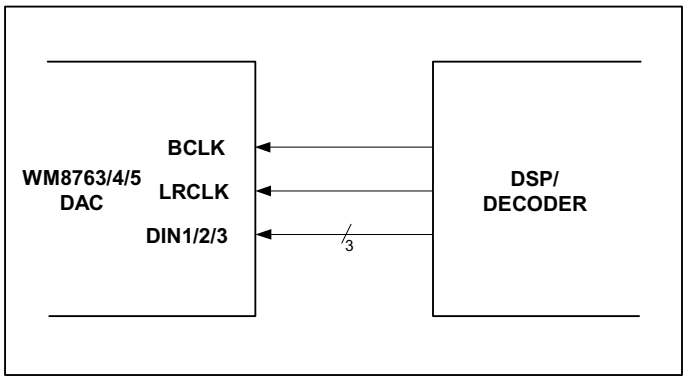



**Figure 4 Slave Mode**

### AUDIO INTERFACE FORMATS

Audio data is applied to the internal DAC filters via the Digital Audio Interface. Five popular interface formats are supported:

- Left Justified mode
- Right Justified mode
- $I^2S$ mode

All 3 formats send the MSB first and support word lengths of 16, 20, and 24.

In left justified, right justified and $I^2S$ modes, the digital audio interface receives DAC data on the DIN1/2/3 inputs. Audio Data for each stereo channel is time multiplexed with LRCLK indicating whether the left or right channel is present. LRCLK is also used as a timing reference to indicate the beginning or end of the data words.

In left justified, right justified and $I^2S$ modes, the minimum number of BCLKs per LRCLK period is 2 times the selected word length. LRCLK must be high for a minimum of word length BCLKs and low for a minimum of word length BCLKs. Any mark to space ratio on LRCLK is acceptable provided the above requirements are met. If exactly 32 bit clocks occur in one left/right clock (16 high, 16 low) the chip will auto detect and run at 16 bit data mode.

### LEFT JUSTIFIED MODE (WM8764 ONLY)

In left justified mode, the MSB of DIN1/2/3 is sampled by the WM8764 on the first rising edge of BCLK following a LRCLK transition. LRCLK is high during the left samples and low during the right samples (Figure 5).

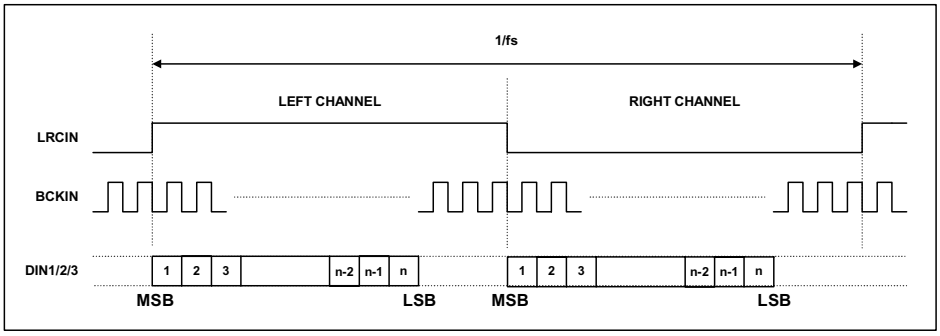



**Figure 5 Left Justified Mode Timing Diagram**

### RIGHT JUSTIFIED MODE (WM8765 ONLY)

In right justified mode, the LSB of DIN1/2/3 is sampled by the WM8765 on the rising edge of BCLK preceding a LRCLK transition. LRCLK are high during the left samples and low during the right samples (Figure 6).

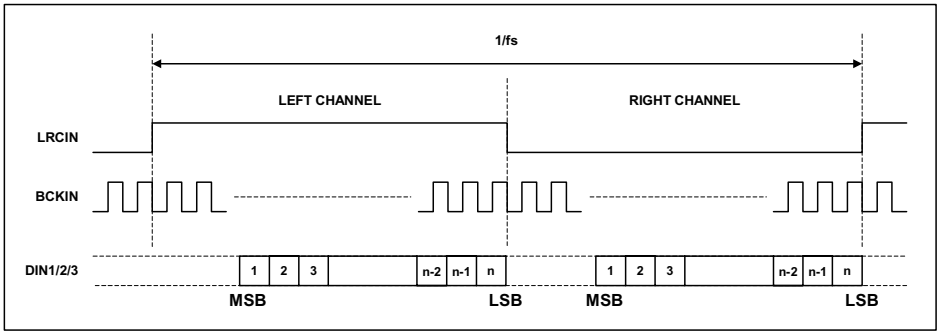



**Figure 6 Right Justified Mode Timing Diagram**

### I2S MODE (WM8763 ONLY)

In $I^2S$ mode, the MSB of DIN1/2/3 is sampled by the WM8763 on the second rising edge of BCLK following a LRCLK transition. LRCLK are low during the left samples and high during the right samples.

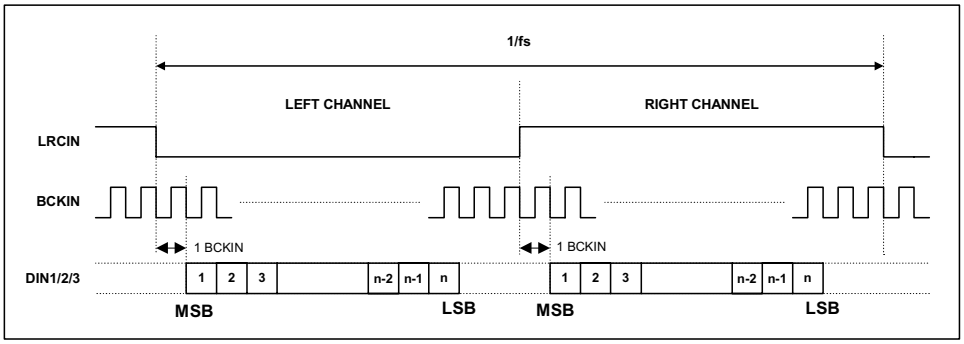



**Figure 7 $I^2S$ Mode Timing Diagram**

## DIGITAL FILTER CHARACTERISTICS

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Passband | ±0.05 dB | | | 0.444fs | |
| | -3dB | | 0.487fs | | |
| Passband ripple | | | | ±0.05 | dB |
| Stopband | | 0.555fs | | | |
| Stopband Attenuation | f > 0.555fs | -60 | | | dB |
| Group Delay | | | 21 | | fs |

**Table 11 Digital Filter Characteristics**

## DAC FILTER RESPONSES

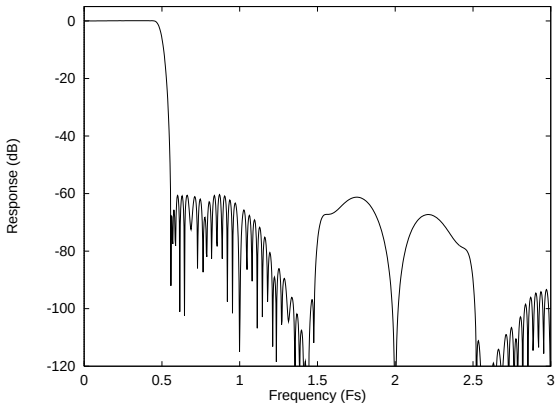



**Figure 8 DAC Digital Filter Frequency Response – 44.1, 48 and 96KHz**

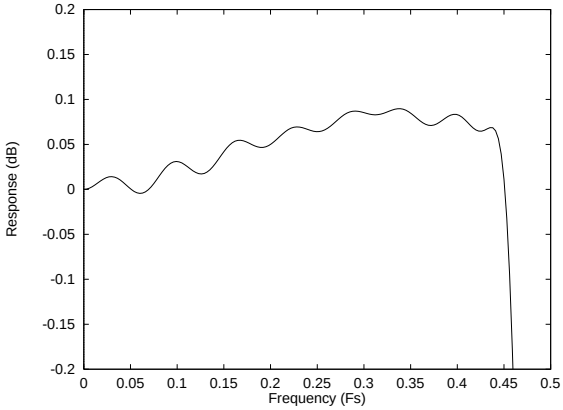



**Figure 9 DAC Digital Filter Ripple –44.1, 48 and 96kHz**

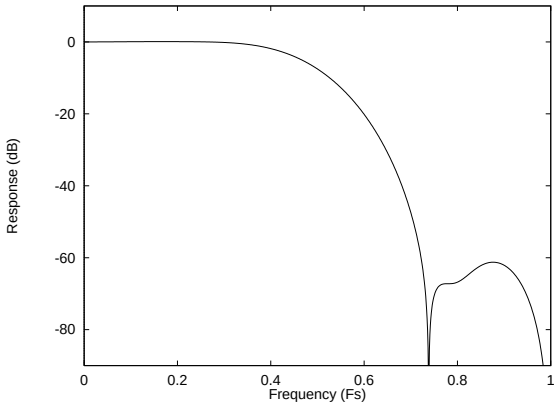



**Figure 10 DAC Digital Filter Frequency Response – 192kHz**

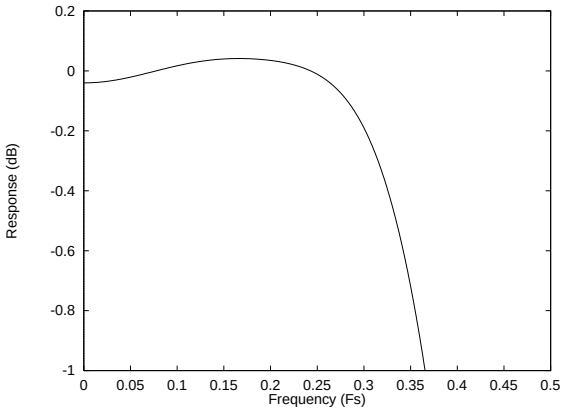



**Figure 11 DAC Digital filter Ripple – 192kHz**

## DIGITAL DE-EMPHASIS CHARACTERISTICS

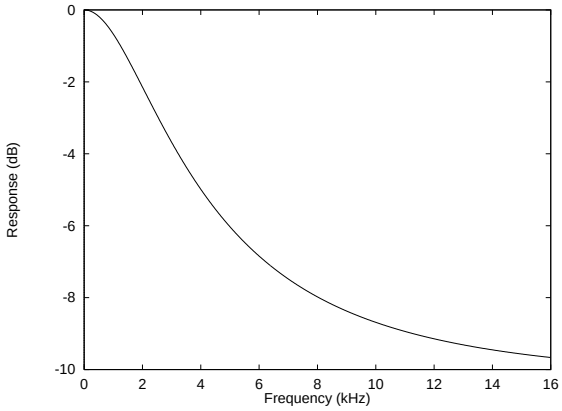



**Figure 12 De-Emphasis Frequency Response (32kHz)**

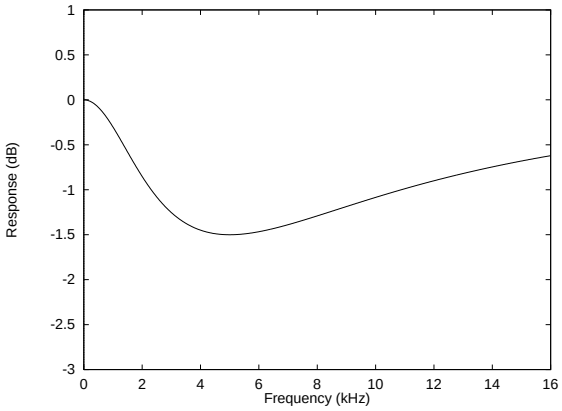



**Figure 13 De-Emphasis Error (32KHz)**

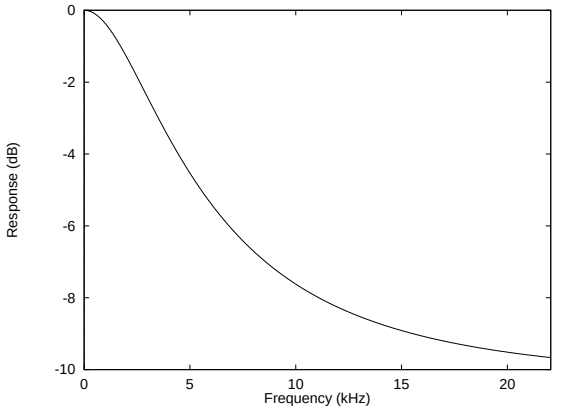



**Figure 14 De-Emphasis Frequency Response (44.1KHz)**

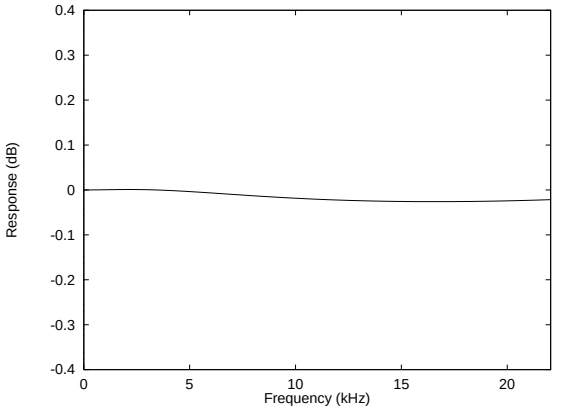



**Figure 15 De-Emphasis Error (44.1KHz)**

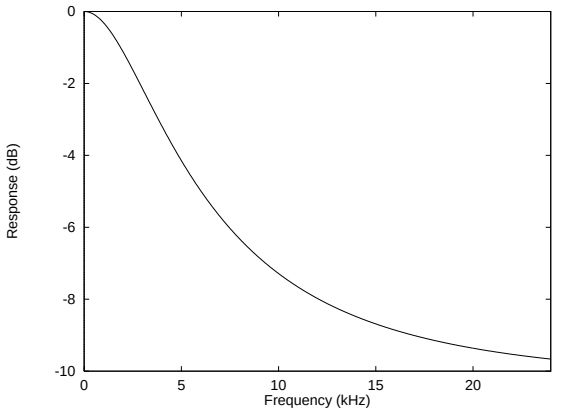



**Figure 16 De-Emphasis Frequency Response (48kHz)**

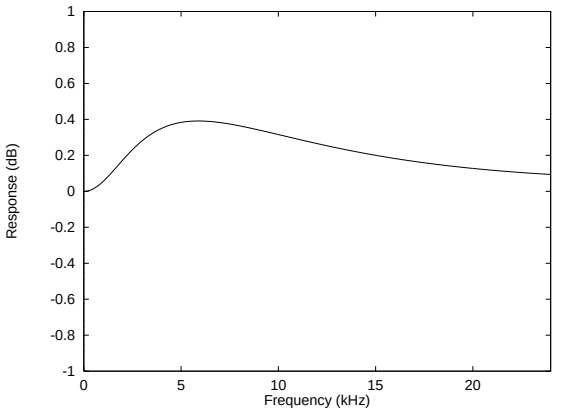
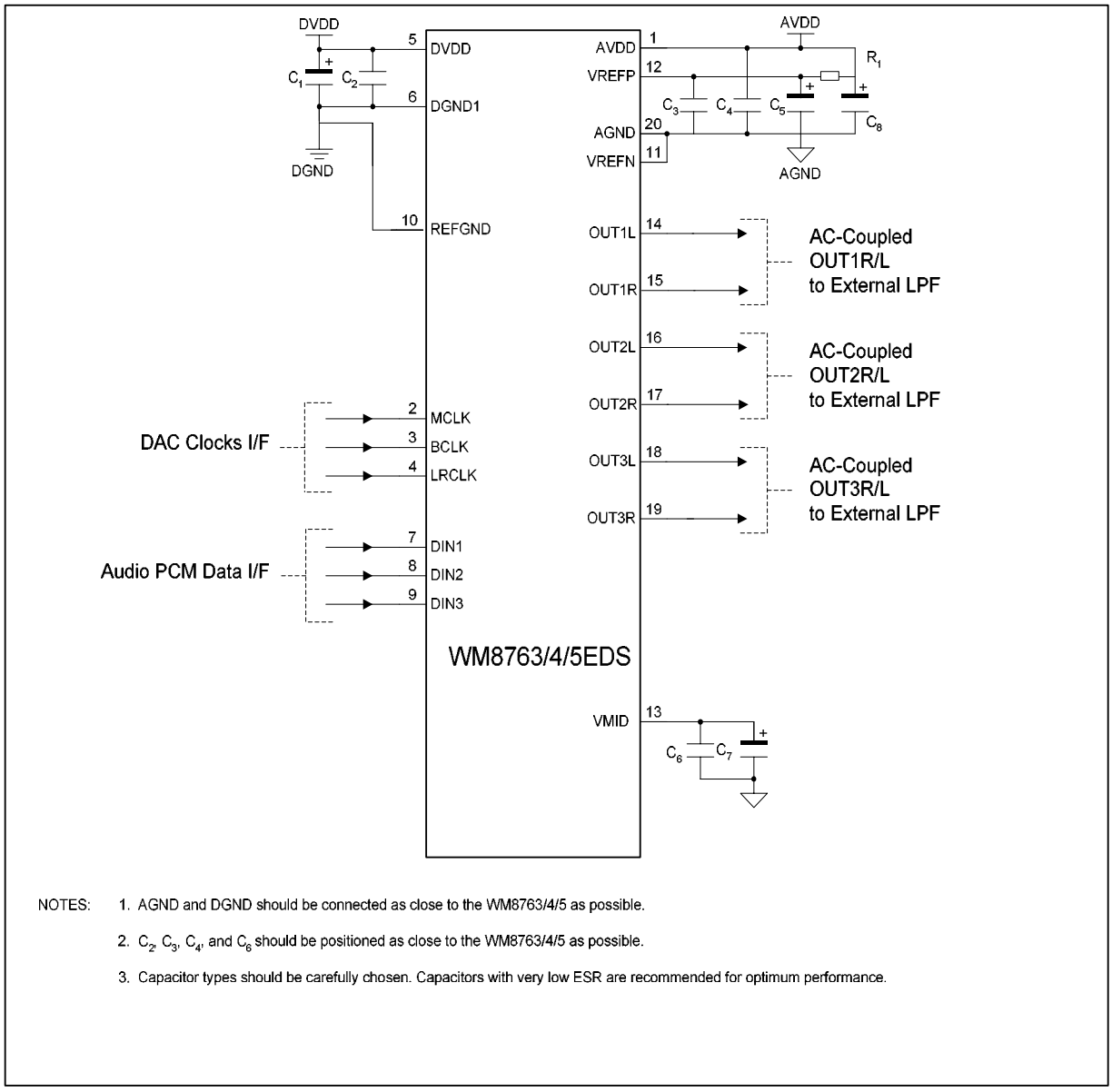



**Figure 17 De-Emphasis Error (48kHz)**

# APPLICATIONS INFORMATION

## RECOMMENDED EXTERNAL COMPONENTS




NOTES:
1. AGND and DGND should be connected as close to the WM8763/4/5 as possible.
2. $C_2$, $C_3$, $C_4$, and $C_6$ should be positioned as close to the WM8763/4/5 as possible.
3. Capacitor types should be carefully chosen. Capacitors with very low ESR are recommended for optimum performance.

**Figure 18 Recommended External Components Diagram**

## RECOMMENDED EXTERNAL COMPONENTS VALUES

| COMPONENT REFERENCE | SUGGESTED VALUE | DESCRIPTION |
|---|---|---|
| C1 and C5 | 10µF | De-coupling for DVDD and AVDD. |
| C2 to C4 | 0.1µF | De-coupling for DVDD and AVDD. |
| C6 | 0.1µF | Reference de-coupling capacitors for VMID. |
| C7 | 10µF | |
| C8 | 10µF | Filtering for VREFP. Omit if AVDD low noise. |
| R1 | 33VΩ | Filtering for VREP. Use 0Ω if AVDD low noise. |

**Table 4 External Components Description**

## SUGGESTED ANALOGUE LOW PASS POST DAC FILTERS

It is recommended that a lowpass filter be applied to the output from each DAC channel for Hi Fi applications. Typically a second order filter is suitable and provides sufficient attenuation of high frequency components (the unique low order, high bit count multi-bit sigma delta DAC structure used in WM8763/4/5 produces much less high frequency output noise than normal sigma delta DACs. This filter is typically also used to provide the 2x gain needed to provide the standard 2Vrms output level from most consumer equipment. Figure 19 shows a suitable post DAC filter circuit, with 2x gain. Alternative inverting filter architectures might also be used with as good results.

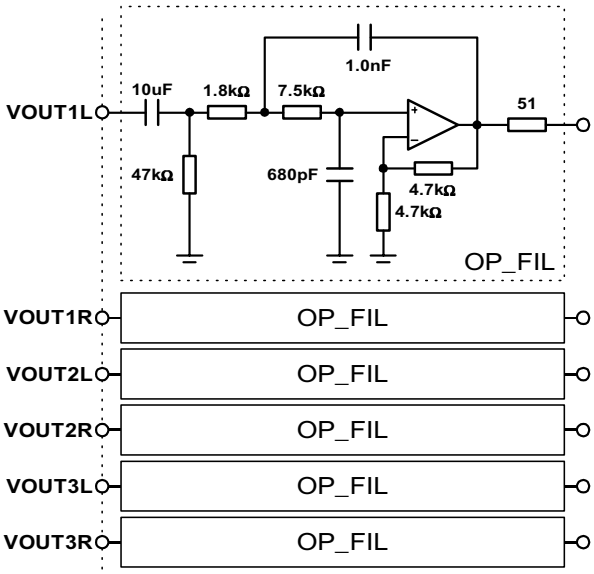
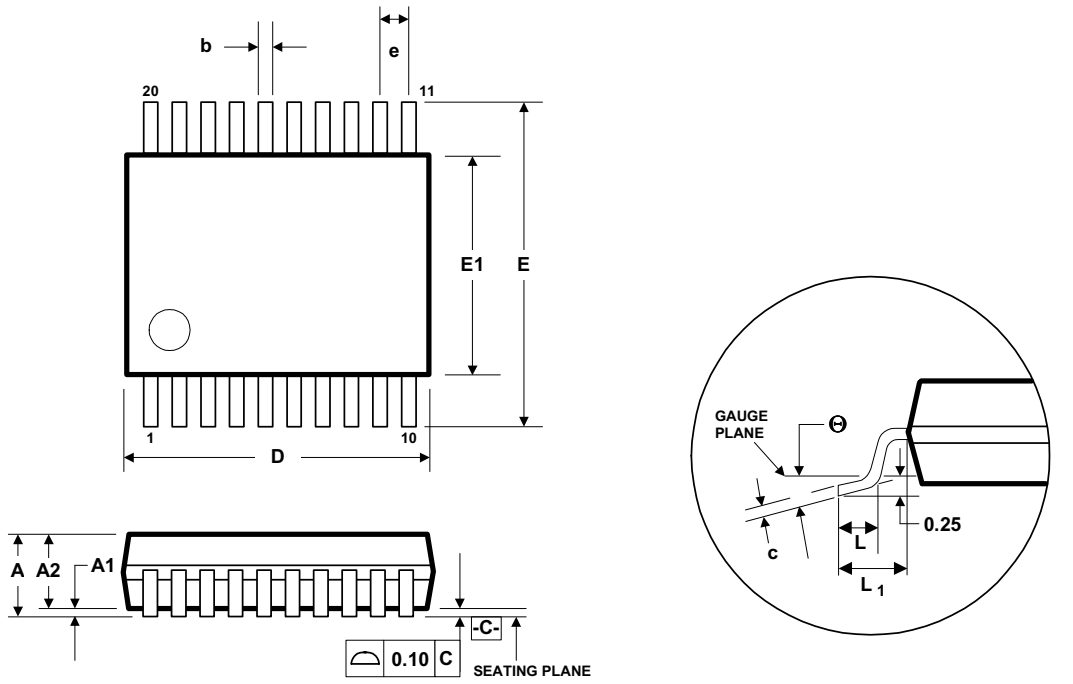



**Figure 19 Recommended Post DAC Filter Circuit**

## PACKAGE DRAWING

**DS: 20 PIN SSOP (7.2 x 5.3 x 1.75 mm)** **DM0015.B**




| Symbols | Dimensions (mm) | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | ----- | ----- | 2.0 |
| $A_1$ | 0.05 | ----- | ----- |
| $A_2$ | 1.65 | 1.75 | 1.85 |
| b | 0.22 | 0.30 | 0.38 |
| c | 0.09 | ----- | 0.25 |
| D | 6.90 | 7.20 | 7.50 |
| e | | 0.65 BSC | |
| E | 7.40 | 7.80 | 8.20 |
| $E_1$ | 5.00 | 5.30 | 5.60 |
| L | 0.55 | 0.75 | 0.95 |
| $L_1$ | | 0.125 REF | |
| θ | $0^o$ | $4^o$ | $8^o$ |
| | | | |
| REF: | JEDEC.95, MO-150 | | |

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.20MM.
D. MEETS JEDEC.95 MO-150, VARIATION = AE. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.

## IMPORTANT NOTICE

Wolfson Microelectronics plc (WM) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current. All products are sold subject to the WM terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

WM warrants performance of its products to the specifications applicable at the time of sale in accordance with WM's standard warranty. Testing and other quality control techniques are utilised to the extent WM deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

In order to minimise risks associated with customer applications, adequate design and operating safeguards must be used by the customer to minimise inherent or procedural hazards. Wolfson products are not authorised for use as critical components in life support devices or systems without the express written approval of an officer of the company. Life support devices or systems are devices or systems that are intended for surgical implant into the body, or support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided, can be reasonably expected to result in a significant injury to the user. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

WM assumes no liability for applications assistance or customer product design. WM does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of WM covering or relating to any combination, machine, or process in which such products or services might be or are used. WM's publication of information regarding any third party's products or services does not constitute WM's approval, license, warranty or endorsement thereof.

Reproduction of information from the WM web site or datasheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations and notices. Representation or reproduction of this information with alteration voids all warranties provided for an associated WM product or service, is an unfair and deceptive business practice, and WM is not responsible nor liable for any such use.

Resale of WM's products or services with statements different from or beyond the parameters stated by WM for that product or service voids all express and any implied warranties for the associated WM product or service, is an unfair and deceptive business practice, and WM is not responsible nor liable for any such use.

## ADDRESS:

Wolfson Microelectronics plc

20 Bernard Terrace

Edinburgh

EH8 9NX

United Kingdom

Tel :: +44 (0)131 272 7000

Fax :: +44 (0)131 272 7001

Email :: sales@wolfsonmicro.com