Preliminary Data Sheet

WA02

A high-density HDLC communications processor

Highlights

* **Supports up to 1024-channel HDLC processing for four channelized, unchannelized or transparent DS3/E3s**
* **Unique complete-frame-store-then-forward architecture eliminates frame storage and buffering needs elsewhere in the system**
* **Delivers direct connection to the Nortel Networks WA01 and WA03 Framer/MUX devices through the pin-efficient OSIF bus**
* **Provides POS-PHY Level 2 system side interface, and PCI bus interface for status and configuration**

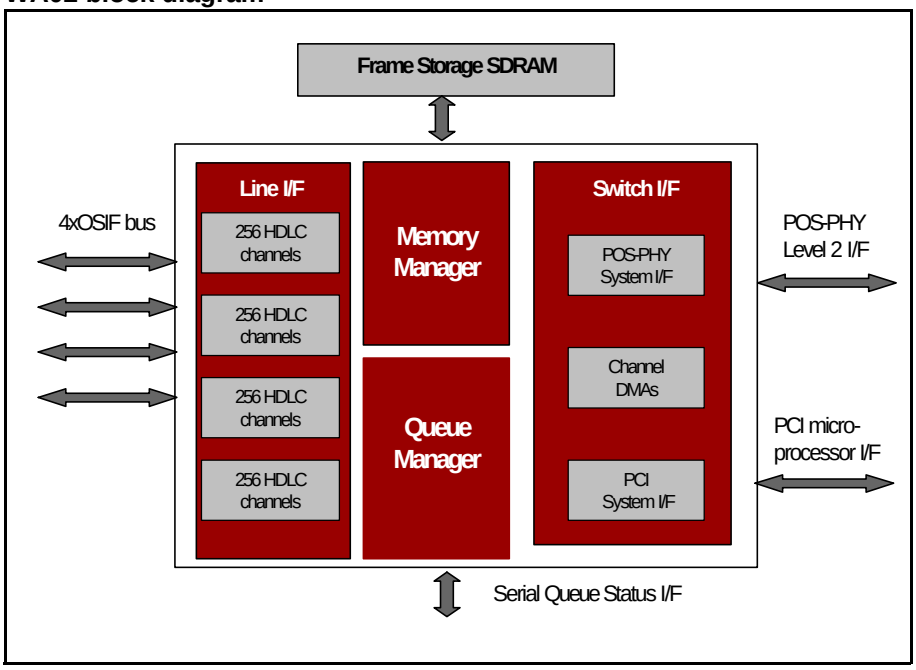
Introduction

The Nortel Networks WA02 is a high-density, multi-channel HDLC (High-level Data Link Control) communications processor. Available from the Nortel Networks WAN Access portfolio, WA02 supports up to 1024 bi-directional HDLC channels and connects directly to the Nortel Networks family of high-density Framers/MUXes through the pin-efficient Octet Stream Interface (OSIF) bus, creating a highly integrated WAN Access and HDLC termination solution for networking applications.

Seamless connection

The WA02 is a high-density bit synchronous HDLC communications processor for all data protocols that use HDLC framing, such as IP, frame relay, and PPP. Designed as a 2-chip solution with the Nortel Networks WA01 or WA03 Framer/MUX devices, there is no other offering on the market today

WA02 block diagram



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that accomplishes as much, in as little space. The WA02 connects seamlessly to single or multiple WA01 155 Mb/s framer with integrated T3, T1 framers and VT1.5 mappers, as well as to single or multiple WA03 155 Mb/s framer with integrated T3, T1/E1 framers and VT1.5/TU12 mappers.

High functional density

Using a single WA02 in tandem with the WA03, systems designers can terminate an entire channelized STS-3/STM-1 data stream. This Nortel Networks solution also allows you to terminate an OC-12/STM-4 down to the DSO level with fewer devices than any competing solution on the market, requiring only three WA02s and four WA03s. Alternatively, by pairing a single WA02 with a single WA03 users can expect to handle three DS3 payloads of full duplex aggregate bandwidth at 135 megabits per second. For higher aggregation still, this chipset is well suited to STS-48 termination, allowing users to handle an entire STS-48 with 16 WA01 devices paired with 12 WA02 devices. This represents the highest density solution, with channelization down to DS0, available on the market today.

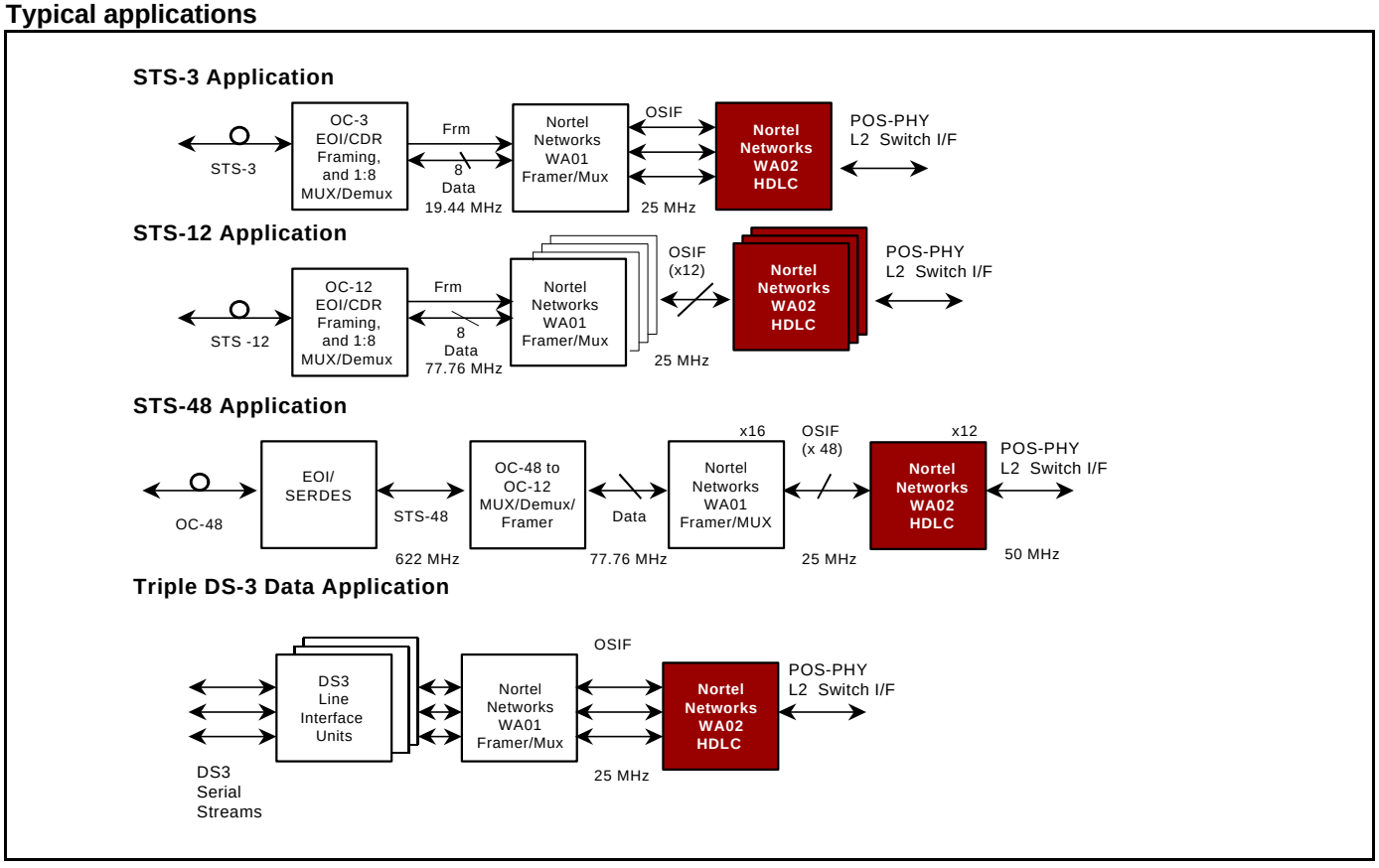
Superior frame and performance management

The unique complete-frame-store-then-forward architecture of WA02 eliminates the need for segmentation, re-assembly and frame buffering elsewhere in the system. This complete-frame-store-then-forward architecture simplifies board design by reducing the number of devices needed to design into a product, delivers significantly more buffering, eliminates the danger of in-transit loss common to cut-through devices and eases the per channel FIFO servicing requirements which are also increasingly difficult in cut-through devices. Additionally, the WA02's unique frame storage capabilities allow for the delivery of enhanced performance monitoring statistics, featuring maximum length and/or non-octet aligned frame counts per channel in the ingress path and good byte counts per channel in both the ingress and egress directions.

Typical applications

The WA02 device is typically suited for use in Frame Relay switches and multiplexers, routers, along with possible uses in Frame Relay/ATM interworking equipment, and packet-based DSLAMS.

Typical applications



Features

Line interface

- supports four separate Nortel Networks standard OSIF (Octet Stream Interface) buses
- each OSIF transports a single DS3/E3 in channelized, unchannelized, or transparent mode down to the DS0s
- supports any mixture of channelized, unchannelized, or transparent DS1s in channelized DS3 mode

Switch interface

- provides 16 bit, 25-50 MHz, Packet-Over-SONET (POS-PHY) Level 2 streaming packet interface as defined by the SATURN(R) working group
- provides prepended routing tags including two bytes for channel ID (user selectable mask) and two bytes for frame length. The order of channel ID and length is programmable
- provides configuration option for byte-level transfer mode or packet-level transfer mode operation

HDLC processors

General

- provides four high-density HDLC controllers each supporting from 1 to 256 channels per OSIF and rates from 56Kb/s to 44.736 Mb/s
- allows non-contiguous time slot assignment

HDLC features (per channel)

- flag delineation/insertion with programmable interframe fill on TX
- bit stuffing/de-stuffing
- optional checksum calculation/verification per CRC-16 or CRC-32
- octet alignment, abort sequence, and length checks on received packets
- transparent mode
- optional data inversion
- programmable TxData value for disabled channels
- programmable idle bit value for 56Kbps TxData
- optional Tx CRC corruption mode
- optional Rx CRC pass through mode

Extensive HDLC performance monitoring and statistics

- **Ingress (receive)**
  - good frames count per channel
  - good bytes count per channel
  - aborted frames count per channel
  - maximum length frames count per channel
  - non-octet aligned frames count per channel
  - CRC errored frames count per channel
  - overrun events count
- **Egress (transmit)**
  - good frames count per channel
  - good bytes count per channel
  - abort/underrun events count

Interrupts

- maskable per channel interrupts for all error counts

PCI interface

- provides external processor access through 32 bit, 33MHz, v2.1 compliant PCI bus interface (target only)
- does all chip management, configuration, and statistics gathering through the PCI bus
- provides support for PCI frame injection and PCI frame retrieval (useful for diagnostics and in-band messaging)

External frame memory

- 64 bit 100 MHz single data rate SDRAM frame memory
- configurable number of frames (up to 16K supported) and frame buffer sizes using 16MB, 32MB, 64MB, 128MB, or 256MB of total memory
- optional error protection via vertical byte lane CRC-8

Queue management

- two ingress queues with per channel selection and programmable arbitration
- 1024 egress queues
- Serial Queue Status Bus Interface
  - simple 3-pin interface
  - gapped clock support 0-50MHz
  - master supplies clock and frame pulse, WA02 shifts out serial stream of threshold status (above or below indication) for 1024 egress queues
- programmable queue threshold registers (per queue, used for serial queue status bus)
- programmable high and low watermark registers (per queue, used to generate interrupts)
- optional discard frames on high watermark
- threshold/watermark checking against byte count
- optional per channel loopbacks
- full read/write access of frame and byte counts per queue
- optional per channel mode to pass errored ingress frames

General

- packaged in a 480 pin, 35 mm BGA with 1mm ball pitch spacing
- 3.3 volt I/O
- 1.8 volt core
- IEEE 1149.1 JTAG test port for boundary scan
- -40 to +85^{o}C Industrial temperature operation
- Operating Frequency: 100MHz

For additional information on Nortel Networks products and services please contact your local representative.

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