STEP-LESS 3-DIMM K7 CLOCK

W83194BR-KT

Data Sheet Revision History

	Pages	Dates	Version	Version On Web	Main Contents
1	n.a.			n.a.	All of the versions before 0.50 are for internal use.
2	n.a.	02/Apr	1.0	1.0	Change version and version on web site to 1.0
3					
4					
5					
6					
7					
8					
9					
10					

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.

1.0 GENERAL DESCRIPTION

The W83194BR-KT is a Clock Synthesizer, which provides all clocks required for AMD K7. W83194BR-KT provides 64 CPU/PCI frequencies, which are selectable with smooth transitions by hardware or software. W83194BR-KT also provides 13 SDRAM clocks controlled by the none-delay buffer_in pin.

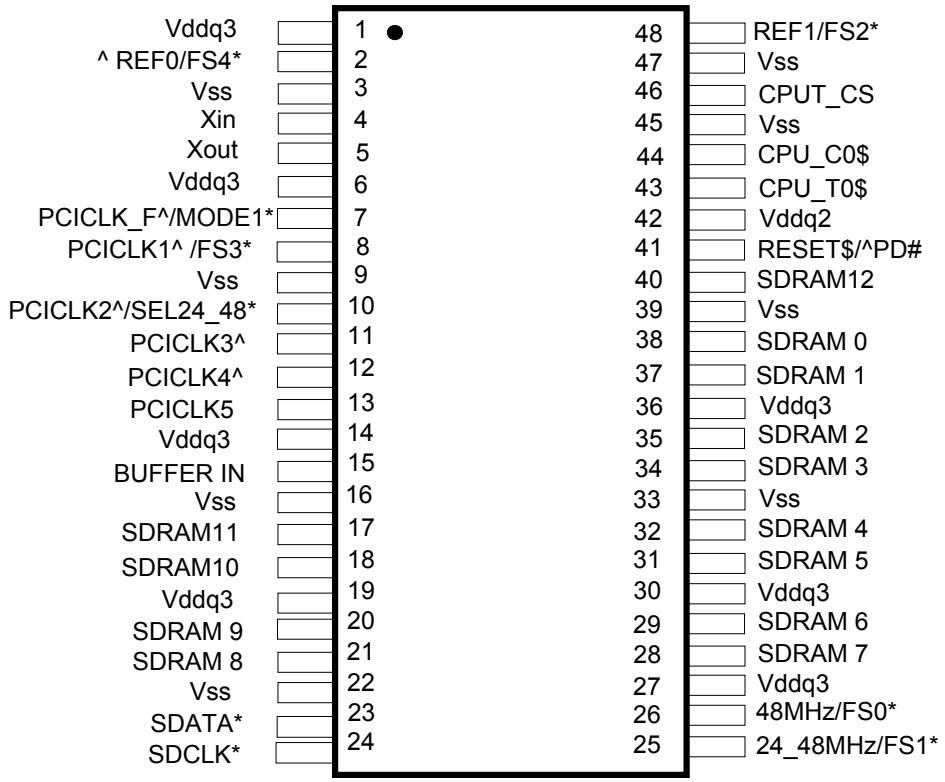
The W83194BR-KT provides step-less frequency programming by controlling the VCO freq. and the programmable PCI clock output divisor ratio. A watchdog timer is quipped and when time out, the RESET# pin will output 4ms pulse signal.

The W83194BR-KT accepts a 14.318 MHz reference crystal as its input. Spread spectrum built in at ±0.5% or ±0.25% to reduce EMI. Programmable stopping individual clock outputs and frequency selection through I^2C interface. The device meets the Pentium power-up stabilization, which requires CPU and PCI clocks be stable within 2 ms after power-up. Using dual function pin for the slots (ISA, PCI, CPU, DIMM) is not recommend.

2.0 PRODUCT FEATURES

- Supports AMD CPU with I^2C.
- 3 CPU clocks (one free-running chipset clock controlled by I2C)
- 13 SDRAM clocks for 3 DIMMs
- 6 PCI synchronous clocks
- Optional single or mixed supply:
  (Vddq2 =2.5V, Vddq3 =3.3V)
- < 250ps skew among CPU and SDRAM clocks
- < 250ps skew among PCI clocks
- < 5ns propagation delay SDRAM from buffer input
- Skew from CPU (earlier) to PCI clock 1 to 4ns, center 2.6ns.
- Smooth frequency switch with selections from 66 MHz to 200 MHz CPU
- Step-less frequency programming by controlling the VCO freq. and the clock output divisor ratio
- I^2C 2-Wire serial interface and I^2C read back
- ±0.25% or ±0.5% spread spectrum function to reduce EMI
- Programmable spread spectrum in the M/N step-less mode
- Programmable registers to enable/stop each output and select modes
- MODE pin for power Management and RESET# out when Watch Dog Timer time out
- One 48 MHz for USB & one 24 MHz for super I/O
- 48-pin SSOP package

3.0 PIN CONFIGURATION



*: Internal pull-up
^: 1.5X~2X driving strength
&: Internal pull-low
$: Open Drain
#: Active Low

4.0 PIN DESCRIPTION

IN - Input

OUT - Output

I/O - Bi-directional Pin

- Active Low

& - Internal 120kΩ pull-down

* - Internal 120kΩ pull-up

4.1 Crystal I/O

SYMBOL	PIN	I/O	FUNCTION
Xin	4	IN	Crystal input with internal loading capacitors and feedback resistors.
Xout	5	OUT	Crystal output at 14.318MHz nominally.

4.2 CPU, SDRAM, PCI, IOAPIC Clock Outputs

SYMBOL	PIN	I/O	FUNCTION
CPU_C0$ CPU_T0$	43 44	OD	CPU_C0 and CPU_T0 are the differential open drain CPU clocks for AMD Athlone™ CPU. CPUT_CS is the open drain pin for the chipset. It has the same phase relationship as CPU_T0.
CPUT_CS	46	OUT	CPUT_CS is the output pin for the chipset. It has the same phase relationship as CPU_T0.
SDRAM [0 :12]	17,18,20,21,28, 29,31,32,34, 35,37,38,40	OUT	SDRAM clock outputs. Fanout buffer outputs from BUFFER IN pin.(Controlled by chipset) They are disabled when PD# is set LOW.
PCICLK_F^/ *MODE1	7	I/O	Free running PCI clock during normal operation. Latched Input. Mode1=1(default), Pin 41 is RESET# open drain. (4ms low active pulse when Watch Dog time out), *Mode1=0, PD# input
PCICLK1^/*FS1	8	I/O	Low skew (< 250ps) PCI clock outputs. Latched input for FS1 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks.
PCICLK2^/SEL24_48*	10	I/O	Low skew (< 250ps) PCI clock outputs. Latched input for at initial power up for H/W selecting the output frequency of 24_48MHz. SEL24_48*=1(default), pin25 is 24MHz, SEL24_48=0, pin25 is 48MHz.
PCICLK ^[3: 4] PCICLK 5	11,12,13	OUT	Low skew (< 250ps) PCI clock outputs. PCICLK_F and PCICLK [1:4] are double strength pins PCICLK 5 is not.
BUFFER IN	15	IN	Inputs to fanout for SDRAM outputs.
RESET$/*PD#	41	I/O	The all clocks will be stopped when this pin set to LOW. Mode1=1(default), Pin41 is RESET$ open drain. (4ms low active pulse when Watch Dog time

			out); *Mode1=0, PD# input

4.3 I²C Control Interface

SYMBOL	PIN	I/O	FUNCTION
*SDATA	23	I/O	Serial data of I²C 2-wire control interface with internal pull-up resistor.
*SDCLK	24	IN	Serial clock of I²C 2-wire control interface with internal pull-up resistor.

4.4 Fixed Frequency Outputs

SYMBOL	PIN	I/O	FUNCTION
^REF0/ *FS4	2	I/O	14.318MHz reference clock. Latched input for FS4 at initial power up for H/W selecting the output frequency of CPU and PCI clocks
REF1/FS2*	48	I/O	14.318MHz reference clock. Latched input for FS2 at initial power up for H/W selecting the output frequency of CPU and PCI clocks.
24_48MHz / *FS1	25	I/O	24MHz output clock. Latched input for FS1 at initial power up for H/W selecting the output frequency of CPU and PCI clocks.
48MHz / *FS0	26	I/O	48MHz output for USB during normal operation. Latched input for FS0 at initial power up for H/W selecting the output frequency of CPU and PCI clocks.

4.5 Power Pins

SYMBOL	PIN	FUNCTION
Vddq2	42	Power supply for CPU clocks, 2.5V or 3.3V.
Vddq3	1,6,14,19,27,30,36	Power supply for PCI, 24_48MHz, SDRAM [0:12], and CPU PLL core, nominal 3.3V.

Vss	3,9,16,22,33,39,45, 47	Circuit Ground.

5.0 FREQUENCY SELECTION

5.1 H/W Setting Frequency Table

FS4	FS3	FS2	FS1	FS0	CPU (MHz)	PCI (MHz)
0	0	0	0	0	166.00	41.60
0	0	0	0	1	160.00	40.00
0	0	0	1	0	155.00	38.70
0	0	0	1	1	150.00	37.50
0	0	1	0	0	145.00	36.20
0	0	1	0	1	140.00	35.00
0	0	1	1	0	136.00	34.00
0	0	1	1	1	130.00	32.50
0	1	0	0	0	127.00	31.70
0	1	0	0	1	124.00	31.00
0	1	0	1	0	120.00	40.00
0	1	0	1	1	118.00	39.30
0	1	1	0	0	116.00	38.60
0	1	1	0	1	115.00	38.30
0	1	1	1	0	114.00	38.00
0	1	1	1	1	113.00	37.60
1	0	0	0	0	112.00	37.30
1	0	0	0	1	111.00	37.00
1	0	0	1	0	110.00	36.60
1	0	0	1	1	109.00	36.30
1	0	1	0	0	108.00	36.00
1	0	1	0	1	107.00	35.60
1	0	1	1	0	106.00	35.30
1	0	1	1	1	104.00	34.60
1	1	0	0	0	102.00	34.00
1	1	0	0	1	133.60	33.40
1	1	0	1	0	133.90	33.40
1	1	0	1	1	133.30	33.30
1	1	1	0	0	95.00	31.70
1	1	1	0	1	100.30	33.30
1	1	1	1	0	100.90	33.40
1	1	1	1	1	100.60	33.30

6.0 MODE PIN -POWER MANAGEMENT INPUT CONTROL

MODE1, Pin7 (Latched Input)	PIN 41
1	RESET# (Open Drain)
0	PD# (Input)

7.0 FUNTION DESCRIPTION

7.1 SERIAL CONTROL REGISTERS

The Pin column lists the affected pin number and the @PowerUp column gives the default state at true power up. "Command Code" byte and "Byte Count" byte must be sent following the acknowledge of the Address Byte. Although the data (bits) in these two bytes are considered "don't care", they must be sent and will be acknowledge. After that, the sequence described below (Register 0, Register 1, Register 2...) will be valid and acknowledged.

Frequency table by software via I2C

SSEL4	SSEL3	SSEL2	SSEL1	SSEL0	CPU (MHz)	PCI (MHz)
0	0	0	0	0	166.00	41.60
0	0	0	0	1	160.00	40.00
0	0	0	1	0	155.00	38.70
0	0	0	1	1	150.00	37.50
0	0	1	0	0	145.00	36.20
0	0	1	0	1	140.00	35.00
0	0	1	1	0	136.00	34.00
0	0	1	1	1	130.00	32.50
0	1	0	0	0	127.00	31.70
0	1	0	0	1	124.00	31.00
0	1	0	1	0	120.00	40.00
0	1	0	1	1	118.00	39.30
0	1	1	0	0	116.00	38.60
0	1	1	0	1	115.00	38.30
0	1	1	1	0	114.00	38.00
0	1	1	1	1	113.00	37.60

SSEL4	SSEL3	SSEL2	SSEL1	SSEL0	CPU (MHz)	PCI (MHz)
1	0	0	0	0	112.00	37.30
1	0	0	0	1	111.00	37.00
1	0	0	1	0	110.00	36.60
1	0	0	1	1	109.00	36.30
1	0	1	0	0	108.00	36.00
1	0	1	0	1	107.00	35.60
1	0	1	1	0	106.00	35.30
1	0	1	1	1	104.00	34.60
1	1	0	0	0	102.00	34.00
1	1	0	0	1	133.60	33.40
1	1	0	1	0	133.90	33.40
1	1	0	1	1	133.30	33.30
1	1	1	0	0	95.00	31.70
1	1	1	0	1	100.30	33.30
1	1	1	1	0	100.90	33.40
1	1	1	1	1	100.60	33.30

7.2.1 Register 0 : Frequency Select Register (default = 0)

Bit	@PowerUp	Pin	Description
7	0	-	Reserved
6	0	-	SSEL2 (for frequency table selection by software via I^2C)
5	0	-	SSEL1 (for frequency table selection by software via I^2C)
4	0	-	SSEL0 (for frequency table selection by software via I^2C)
3	0	-	0 = Selection by hardware 1 = Selection by software I^2C - Bit 6:4, Bit2
2	0	-	SSEL4 (for frequency table selection by software via I^2C)
1	0	-	SSEL3 (for frequency table selection by software via I^2C)
0	0	-	0 = Running 1 = Tristate all outputs

7.2.2 Register 1 : CPU Clock Register (1 = enable, 0 = Stopped)

Bit	@PowerUp	Pin	Description
7	1	-	Reserved
6	1	-	1=center type S.S.T. 0= 0-0.5% down type S.S.T.
5	0	-	0 = Normal 1 = Spread Spectrum enabled
4	0	-	0 = ±0.25% Spread Spectrum Modulation 1 = ±0.5% Spread Spectrum Modulation
3	1	-	Reserved
2	1	40	SDRAM12 (Active / Inactive)
1	1	43 44	CPUT0 CPUC0 (Active / Inactive)
0	1	46	CPUT_CS (Active / Inactive)

7.2.3 Register 2: PCI Clock Register (1 = enable, 0 = Stopped)

Bit	@PowerUp	Pin	Description
7	1	-	Reserved
6	1	7	PCICLK_F (Active / Inactive)
5	1	-	Reserved
4	1	13	PCICLK5 (Active / Inactive)
3	1	12	PCICLK4 (Active / Inactive)
2	1	11	PCICLK3 (Active / Inactive)
1	1	10	PCICLK2 (Active / Inactive)
0	1	8	PCICLK1 (Active / Inactive)

7.2.4 Register 3: SDRAM, 24MHz, 48MHz Clock Register (1 = enable, 0 = Stopped)

Bit	@PowerUp	Pin	Description
7	1	48	REF1 (Active / Inactive)
6	1	2	REF0 (Active / Inactive)
5	1	26	48MHz (Active / Inactive)
4	1	25	24_48MHz (Active / Inactive)
3	1	17	SDRAM11 (Active / Inactive)
2	1	18	SDRAM10 (Active / Inactive)
1	1	20	SDRAM 9 (Active / Inactive)
0	1	21	SDRAM 8 (Active / Inactive)

7.2.5 Register 4: Reserved Register (1 = enable, 0 = Stopped)

Bit	@PowerUp	Pin	Description
7	X	-	Latched FS4#
6	X	-	Latched FS3#
5	X	-	Latched FS2#
4	X	-	Latched FS1#
3	X	-	Latched FS0#
2	X	-	Latched SEL24_48#
1	1	-	Reserved
0	1	-	Reserved

7.2.6 Register 5: Peripheral Control (1 = enable, 0 = Stopped)

Bit	@PowerUp	Pin	Description
7	1	28	SDRAM 7 (Active / Inactive)
6	1	29	SDRAM 6 (Active / Inactive)
5	1	31	SDRAM 5 (Active / Inactive)
4	1	32	SDRAM 4 (Active / Inactive)
3	1	34	SDRAM 3 (Active / Inactive)
2	1	35	SDRAM 2 (Active / Inactive)
1	1	37	SDRAM 1 (Active / Inactive)
0	1	38	SDRAM 0 (Active / Inactive)

7.2.7 Register 6: Watchdog Timer Register

Bit	@PowerUp	Pin	Description
7	0	-	Enable Count 1 = start timer 0 = stop timer
6	X	-	Second timeout status (READ ONLY)
5	0	-	Second count 5
4	0	-	Second count 4
3	0	-	Second count 3
2	0	-	Second count 2
1	0	-	Second count 1
0	0	-	Second count 0

7.2.8 Register 7: M/N Program Register

Bit	@PowerUp	Pin	Description
7	0	-	N value bit 8
6	0	-	Test 1(Please do not modify)
5	1	-	Test 0 (Please do not modify)
4	0	-	M value bit 4
3	0	-	M value bit 3
2	0	-	M value bit 2
1	0	-	M value bit 1
0	0	-	M value bit 0

7.2.9 Register 8: M/N Program Register

Bit	@PowerUp	Pin	Description
7	0	-	N value bit 7
6	0	-	N value bit 6
5	0	-	N value bit 5
4	0	-	N value bit 4
3	0	-	N value bit 3
2	0	-	N value bit 2
1	0	-	N value bit 1
0	0	-	N value bit 0

7.2.10 Register 9: Spread Spectrum Programming Register

Bit	@PowerUp	Pin	Description
7	0	-	Spread spectrum up count 3
6	0	-	Spread spectrum up count 2
5	0	-	Spread spectrum up count 1
4	0	-	Spread spectrum up count 0
3	0	-	Spread spectrum down count 3
2	0	-	Spread spectrum down count 2
1	0	-	Spread spectrum down count 1
0	0	-	Spread spectrum down count 0

7.2.11 Register 10: Divisor and Step-less Enable Register

Bit	@PowerUp	Pin	Description
7	0	-	0: use frequency table 1: use M/N register to program frequency The equation is VCO **freq. = 14.318MHz * (N+4)/ M**
6	0	-	Reserved
5	X	-	PCI Ratio SEL2 0,0,0 = 2 0,0,1 = 3
4	X	-	PCI Ratio SEL1 0,1,0 = 4 0,1,1 = 5
3	X	-	PCI Ratio SEL 0 1,0,0 = 6 1,0,1... = X
2	0	-	Reserved
1	0	-	Reserved
0	0	-	Reserved

7.2.12 Register 11: Winbond Chip ID Register (Read Only)

Bit	@PowerUp	Pin	Description
7	0	-	Winbond Chip ID
6	1	-	Winbond Chip ID
5	1	-	Winbond Chip ID
4	0	-	Winbond Chip ID
3	0	-	Winbond Chip ID
2	0	-	Winbond Chip ID
1	1	-	Winbond Chip ID
0	0	-	Winbond Chip ID

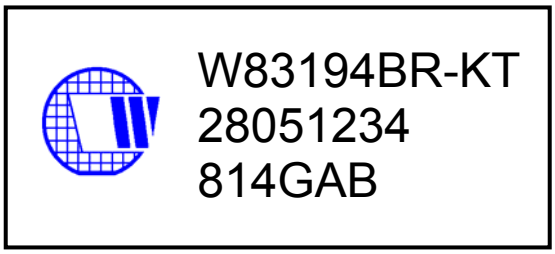
7.2.13 Register 12: Winbond Chip ID Register (Read Only)

Bit	@PowerUp	Pin	Description
7	**0**	**-**	**Winbond Chip ID**
6	**1**	**-**	**Winbond Chip ID**
5	**1**	**-**	**Winbond Chip ID**
4	**0**	**-**	**Winbond Chip ID**
3	**0**	**-**	**Winbond Version ID**
2	**0**	**-**	**Winbond Version ID**
1	**0**	**-**	**Winbond Version ID**
0	**1**	**-**	**Winbond Version ID**

8.0 ORDERING INFORMATION

Part Number	Package Type	Production Flow
W83194BR-KT	48 PIN SSOP	Commercial, 0°C to +70°C

9.0 HOW TO READ THE TOP MARKING



1st line: Winbond logo and the type number: W83194BR-KT

2nd line: Tracking code 2 8051234

2: wafers manufactured in Winbond FAB 2

8051234: wafer production series lot number

3rd line: Tracking code 814 G A B

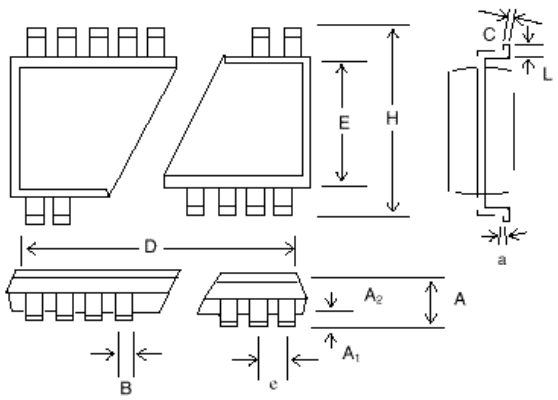
814: packages made in '98, week 14

G: assembly house ID; A means ASE, S means SPIL, G means GR

A: Internal use ID

B: IC revision

10.0 PACKAGE DRAWING AND DIMENSIONS



48 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.110	0	0	2.79
A_1	0.008	0.012	0.016	0.20	0.30	0.41
A2	0.085	0.090	0.095	2.16	2.29	2.41
b	0.008	0.010	0.013	0.20	0.25	0.33
C	0.006	0.008	0.010	0.15	0.20	0.25
D	-	0.625	0.637	-	15.88	16.18
E	0.291	0.295	0.299	7.39	7.49	7.59
e	0.025 BSC			0.64 BSC		
H	0.395	0.408	0.420	10.03	10.36	10.67
L	0.025	0.030	0.040	0.64	0.76	1.02
a	0°	5°	8°	0°	5°	8°

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