



# W83194R-630

166MHZ CLOCK FOR SIS CHIPSET

## W83194R-630 Data Sheet Revision History

	Pages	Dates	Version	Version On Web	Main Contents
1	n.a.			n.a.	All of the versions before 0.50 are for internal use.
2	n.a.	02/Apr	1.0	1.0	Change version and version on web site to 1.0
3					
4					
5					
6					
7					
8					
9					
10					

Please note that all data and specifications are subject to change without notice. All the trademarks of products and companies mentioned in this data sheet belong to their respective owners.

### LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.



## 1. GENERAL DESCRIPTION

The W83194R-630 is a Clock Synthesizer for SiS 540/630 chipset. W83194R-630 provides all clocks required for high-speed RISC or CISC microprocessor such as AMD, Cyrix, Intel Pentium and also provides 16 different frequencies of CPU clocks frequency setting. All clocks are externally selectable with smooth transitions. The W83194R-630 makes SDRAM in synchronous or asynchronous frequency with CPU clocks.

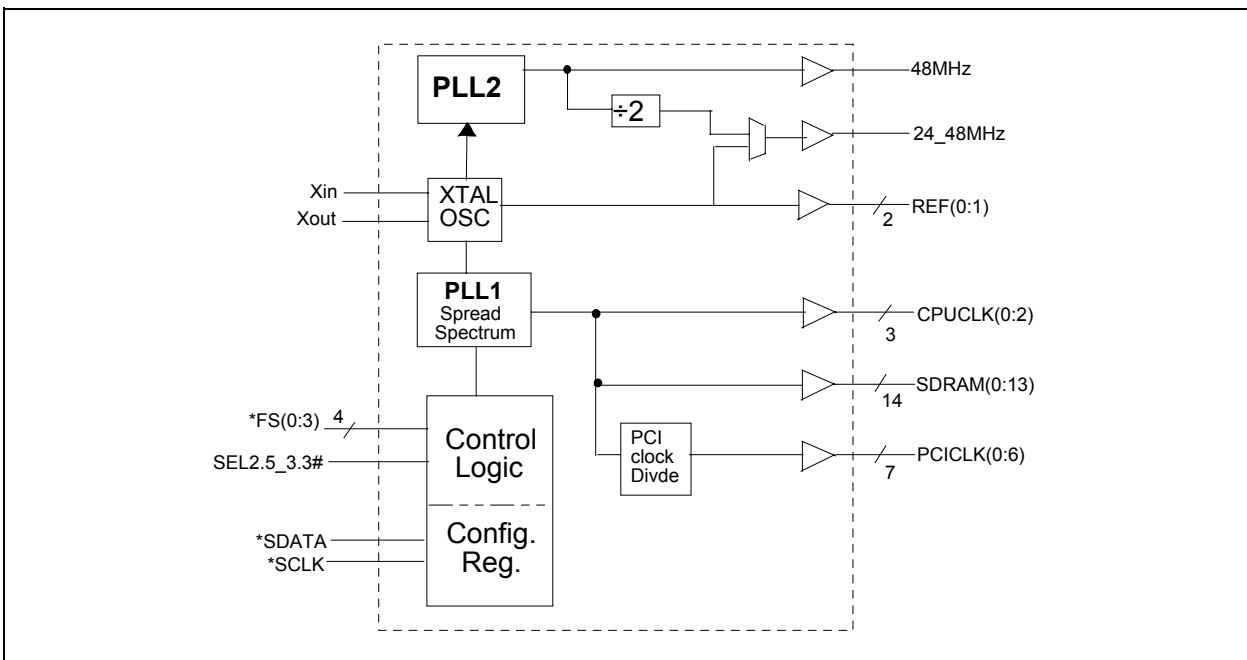
The W83194R-630 provides I<sup>2</sup>C serial bus interface to program the registers to enable or disable each clock outputs and W83194R-630 provides the 0.5%, 0.75% center type spread spectrum to reduce EMI.

The W83194R-630 accepts a 14.318 MHz reference crystal as its input and runs on a 3.3V supply. High drive PCI and SDRAM CLOCK outputs typically provide greater than 1 V/ns slew rate into 30 pF loads. CPU CLOCK outputs typically provide better than 1 V/ns slew rate into 20 pF loads as maintaining 50± 5% duty cycle. The fixed frequency outputs as REF, 24MHz, and 48 MHz provide better than 0.5V/ns slew rate.

## 2. PRODUCT FEATURES

- Supports Pentium™, Pentium™ Pro, AMD and Cyrix CPUs with I<sup>2</sup>C.
- 3 CPU clocks
- 14 SDRAM clocks for 3 DIMMs
- 7 PCI synchronous clocks.
- Optional single or mixed supply:  
(All Vdd = 3.3V) or (Other s Vdd = 3.3V, VddLCPU=2.5V)
- Skew form CPU to PCI clock -1 to 4 ns, center 2.6 ns
- SDRAM frequency synchronous or asynchronous to CPU clocks
- Smooth frequency switch with selections from 66 to 166mhz
- I<sup>2</sup>C 2-Wire serial interface and I<sup>2</sup>C read back
- 0.5%, 0.75% center type spread spectrum to reduce EMI
- Programmable registers to enable/stop each output and select modes  
(mode as Tri-state or Normal )
- 48 MHz for USB
- 24 MHz for super I/O
- Packaged in 48-pin SSOP

## 3. BLOCK DIAGRAM



## 4. PIN CONFIGURATION

Vdd	1	48	REF1
REF0X2/ *FS3	2	47	VddLCPU
Vss	3	46	CPUCLK0
Xin	4	45	CPUCLK1
Xout	5	44	Vss
VddP	6	43	CPUCLK2
PCICLK0/ *FS1	7	42	VddSD
PCICLK1/ *FS2	8	41	SDRAM13
PCICLK2	9	40	SDRAM12
Vss	10	39	Vss
PCICLK3	11	38	SDRAM11
PCICLK4	12	37	SDRAM 10
PCICLK5	13	36	VddSD
PCICLK6	14	35	SDRAM 9
VddP	15	34	SDRAM 8
Vss	16	33	Vss
SDRAM 0	17	32	SDRAM 7
SDRAM 1	18	31	SDRAM 6
VddSD	19	30	VddSD
SDRAM 2	20	29	SDRAM 5
SDRAM 3	21	28	SDRAM 4
Vss	22	27	VddSD
*SDATA	23	26	48MHz/*FS0
*SDCLK	24	25	24_48MHz/SEL2.5_3.3#