512K x 32/256K x 32 Dual Array Synchronous Pipeline Burst NBL SRAM

FEATURES

- Fast clock speed: 166, 150, 133, and 100MHz
- Fast access times: 3.5ns, 3.8ns, 4.2ns, and 5.0ns
- Fast $\overline{OE}$ access times: 3.5ns, 3.8ns, 4.2ns, and 5.0ns
- Single +2.5V ± 5% power supply (VDD)
- Snooze Mode for reduced-standby power
- Individual Byte Write control
- Clock-controlled and registered addresses, data I/Os and control signals
- Burst control (interleaved or linear burst)
- Packaging:
  - 209-bump BGA package
- Low capacitive bus loading

DESCRIPTION

The WED2ZLRSP01S, Dual Independent Array, NBL-SSRAM device employs high-speed, Low-Power CMOS silicon and is fabricated using an advanced CMOS process. WEDC's 24Mb, Sync Burst SRAM MCP integrates two totally independent arrays, the first organized as a 512K x 32, and the second a 256K x 32.

All Synchronous inputs pass through registers controlled by a positive edge triggered, single clock input per array. The NBL or No Bus Latency Memory provides 100% bus utilizaton, with no loss of cycles caused by change in modal operation (Write to Read/Read to Write). All inputs except for Asynchronous Output Enable and Burst Mode control are synchronized on the positive or rising edge of Clock. Burst order control must be tied either HIGH or LOW, Write cycles are internally self-timed, and writes are initiated on the rising edge of clock. This feature eliminates the need for complex off-chip write pulse generation and proved increased timing flexibility for incoming signals.

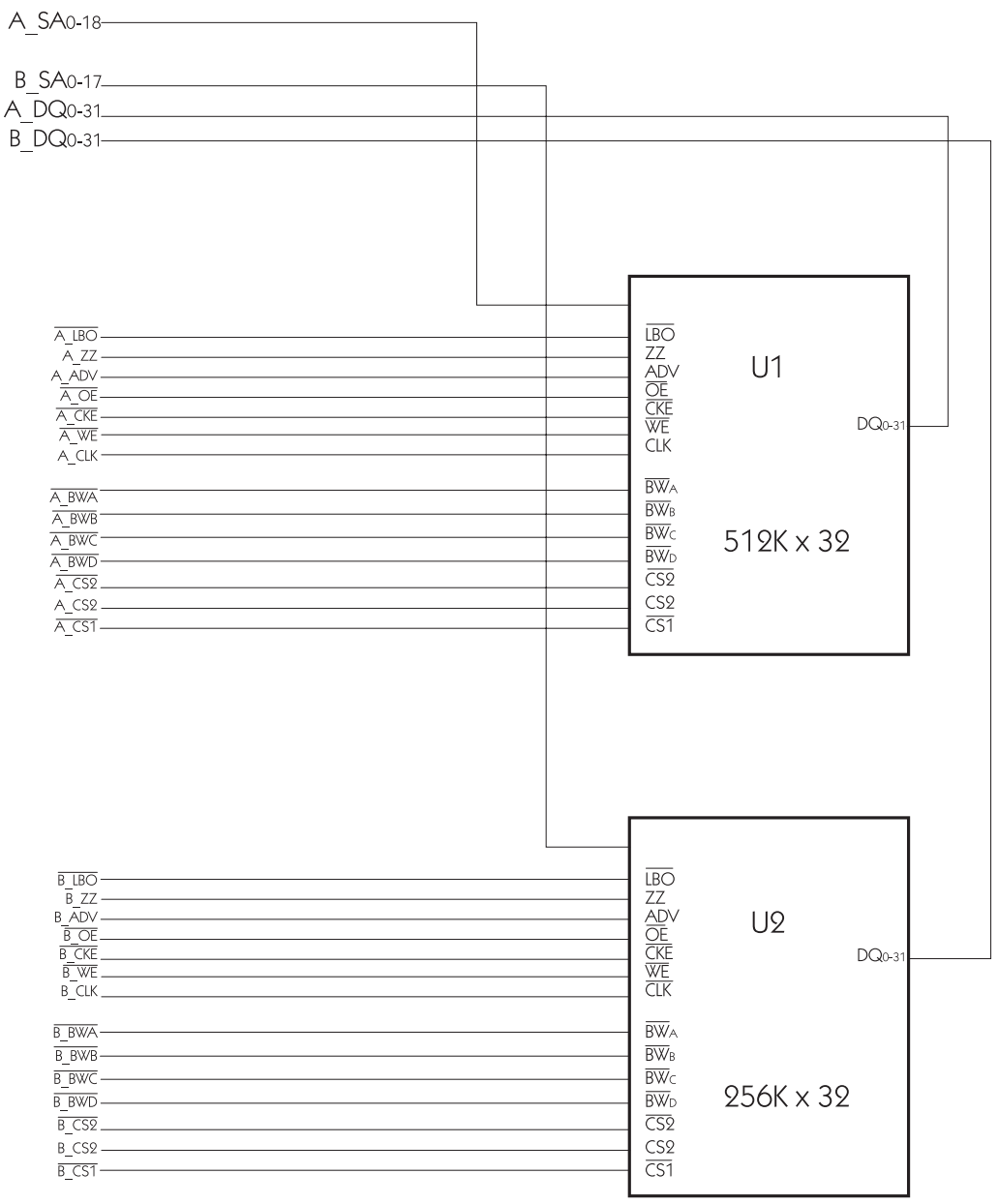
FIG. 1 PIN CONFIGURATION

(TOP VIEW)

	1	2	3	4	5	6	7	8	9	10	11
A	V_{SS}	A_DAT_{B0}	A_DAT_{B1}	A_DAT_{B2}	A_DAT_{B3}	V_{SS}	A_DAT_{A0}	A_DAT_{A1}	A_DAT_{A2}	A_DAT_{A3}	V_{SS}
B	NC	A_DAT_{B4}	A_DAT_{B5}	A_DAT_{B6}	A_DAT_{B7}	V_{SS}	A_DAT_{A4}	A_DAT_{A5}	A_DAT_{A6}	A_DAT_{A7}	NC
C	A_ADR	A_ADR	A_$\overline{OE}$	A_ADV	A_BWE_B	V_{SS}	A_BWE_A	A_ZZ	A_ADR	A_ADR	A_ADR
D	A_ADR	V_{SS}	A_$\overline{CKE}$	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	A_ADR	A_ADR
E	A_ADR	A_CLK	A_$\overline{GWE}$	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	A_ADR_1	A_ADR_0
F	A_ADR	V_{SS}	A_$\overline{CS_2}$	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	A_ADR	A_ADR
G	A_ADR	A_ADR	A_$\overline{CS_1}$	A_CS_2	A_BWE_C	V_{SS}	A_BWE_D	A_$\overline{LBO}$	A_ADR	A_ADR	A_ADR
H	NC	A_DAT_{C0}	A_DAT_{C1}	A_DAT_{C2}	A_DAT_{C3}	V_{SS}	A_DAT_{D0}	A_DAT_{D1}	A_DAT_{D2}	A_DAT_{D3}	NC
J	V_{SS}	A_DAT_{C4}	A_DAT_{C5}	A_DAT_{C6}	A_DAT_{C7}	V_{SS}	A_DAT_{D4}	A_DAT_{D5}	A_DAT_{D6}	A_DAT_{D7}	V_{SS}
K	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
L	V_{SS}	B_DAT_{B0}	B_DAT_{B1}	B_DAT_{B2}	B_DAT_3	V_{SS}	B_DAT_{A0}	B_DAT_{A1}	B_DAT_{A2}	B_DAT_{A3}	V_{SS}
M	NC	B_DAT_{B4}	B_DAT_{B5}	B_DAT_{B6}	B_DAT_7	V_{SS}	B_DAT_{A4}	B_DAT_{A5}	B_DAT_{A6}	B_DAT_{A7}	NC
N	B_ADR	B_ADR	B_$\overline{OE}$	B_ADV	B_BWE_B	V_{SS}	B_BWE_A	B_ZZ	B_ADR	B_ADR	B_ADR
P	B_ADR	V_{SS}	B_$\overline{CKE}$	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	B_ADR	B_ADR
R	B_ADR	B_CLK	B_$\overline{GWE}$	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	B_ADR_1	B_ADR_0
T	B_ADR	V_{SS}	B_$\overline{CS_2}$	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	B_ADR	B_ADR
U	B_ADR	NC	B_$\overline{CS_1}$	B_CS_2	B_BWE_C	V_{SS}	B_BWE_D	B_$\overline{LBO}$	B_ADR	B_ADR	B_ADR
V	NC	B_DAT_{C4}	B_DAT_{C5}	B_DAT_{C6}	B_DAT_{C7}	V_{SS}	B_DAT_{D4}	B_DAT_{D5}	B_DAT_{D6}	B_DAT_{D7}	NC
W	V_{SS}	B_DAT_{C0}	B_DAT_{C1}	B_DAT_{C2}	B_DAT_{C3}	V_{SS}	B_DAT_{D0}	B_DAT_{D1}	B_DAT_{D2}	B_DAT_{D3}	V_{SS}

FIG. 1 PIN CONFIGURATION, CONT.

BLOCK DIAGRAM



FUNCTION DESCRIPTION

The WWED2ZLRSP01S is an NBL Dual Array SSRAM designed to sustain 100% bus bandwidth by eliminating turnaround cycle when there is transition from Read to Write, or vice versa. All inputs (with the exception of $\overline{OE}$, $\overline{LBO}$ and ZZ) are synchronized to rising clock edges, and all features are available on each of the independent arrays.

All read, write and deselect cycles are initiated by the ADV input. Subsequent burst addresses can be internally generated by the burst advance pin (ADV). ADV should be driven to Low once the device has been deselected in order to load a new address for next operation.

Clock Enable ($\overline{CKE}$) pin allows the operation of the chip to be suspended as long as necessary. When $\overline{CKE}$ is high, all synchronous inputs are ignored and the internal device registers will hold their previous values. NBL SSRAM latches external address and initiates a cycle when $\overline{CKE}$ and ADV are driven low at the rising edge of the clock.

Output Enable ($\overline{OE}$) can be used to disable the output at any given time. Read operation is initiated when at the rising edge of the clock, the address presented to the address inputs are latched in the address register, $\overline{CKE}$ is driven low, the write enable input signals $\overline{WE}$ are driven high, and ADV driven low. The internal array is read between the first rising edge and the second rising edge of the clock and the data is latched in the output register. At the second clock edge the data is driven out of the SRAM. During read operation $\overline{OE}$ must be driven low for the device to drive out the requested data.

Write operation occurs when $\overline{WE}$ is driven low at the rising edge of the clock. $\overline{BW}$[d:a] can be used for byte write operation. The pipe-lined NBL SSRAM uses a late-late write cycle to utilize 100% of the bandwidth. At the first rising edge of the clock, $\overline{WE}$ and address are registered, and the data associated with that address is required two cycle later.

Subsequent addresses are generated by ADV High for the burst access as shown below. The starting point of the burst seguence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the $\overline{LBO}$ pin. When this pin is low, linear burst sequence is selected. And when this pin is high, Interleaved burst sequence is selected.

During normal operation, ZZ must be driven low. When ZZ is driven high, the SRAM will enter a Power Sleep Mode after 2 cycles. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM operates after 2 cycles of wake up time.

BURST SEQUENCE TABLE

(Interleaved Burst, $\overline{LBO}$ = High)

$\overline{LBO}$ Pin	High	Case 1		Case 2		Case 3		Case 4	
		A_1	A_0	A_1	A_0	A_1	A_0	A_1	A_0
First Address		0	0	0	1	1	0	1	1
		0	1	0	0	1	1	1	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	1	0	0	1	0	0

(Linear Burst, $\overline{LBO}$ = Low)

$\overline{LBO}$ Pin	High	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
		0	1	1	0	1	1	0	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	0	0	0	1	1	0

NOTE 1: LBO pin must be tied to High or Low, and Floating State must not be allowed.

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

$\overline{CEx}$	ADV	$\overline{WE}$	$\overline{BWx}$	$\overline{OE}$	$\overline{CKE}$	CLK	Address Accessed	Operation
H	L	X	X	X	L	↑	N/A	Deselect
X	H	X	X	X	L	↑	N/A	Continue Deselect
L	L	H	X	L	L	↑	External Address	Begin Burst Read Cycle
X	H	X	X	L	L	↑	Next Address	Continue Burst Read Cycle
L	L	H	X	H	L	↑	External Address	NOP/Dummy Read
X	H	X	X	H	L	↑	Next Address	Dummy Read
L	L	L	L	X	L	↑	External Address	Begin Burst Write Cycle
X	H	X	L	X	L	↑	Next Address	Continue Burst Write Cycle
L	L	L	H	X	L	↑	N/A	NOP/Write Abort
X	H	X	H	X	L	↑	Next Address	Write Abort
X	X	X	X	X	H	↑	Current Address	Ignore Clock

NOTES:
1. X means "Don't Care."
2. The rising edge of clock is symbolized by (↑)
3. A continue deselect cycle can only be entered if a deselect cycle is executed first.
4. $\overline{WRITE}$ = L means Write operation in WRITE TRUTH TABLE.
$\overline{WRITE}$ = H means Read operation in WRITE TRUTH TABLE.
5. Operation finally depends on status of asynchronous input pins (ZZ and $\overline{OE}$).
6. $\overline{CEx}$ refers to the combination of $\overline{CE_1}$, CE_2 and $\overline{CE_2}$.
7. Applies to each of the independent arrays.

WRITE TRUTH TABLE

$\overline{WE}$	$\overline{BWa}$	$\overline{BWb}$	$\overline{BWc}$	$\overline{BWd}$	Operation
H	X	X	X	X	Read
L	L	H	H	H	Write Byte a
L	H	L	H	H	Write Byte b
L	H	H	L	H	Write Byte c
L	H	H	H	L	Write Byte d
L	L	L	L	L	Write All Bytes
L	H	H	H	H	Write Abort/NOP

NOTES:
1. X means "Don't Care."
2. All inputs in this table must meet setup and hold time around the rising edge of CLK (↑).
3. Applies to each of the independent arrays.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{DD} Supply Relative to V_{SS}	-0.3V to +3.6V
V_{IN} (DQx)	-0.3V to +3.6V
V_{IN} (Inputs)	-0.3V to +3.6V
Storage Temperature (BGA)	-55°C to +125°C
Short Circuit Output Current	100mA

**Stress greater than those listed under "Absolute Maximum Ratings": may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.*

ELECTRICAL CHARACTERISTICS ($0°C \le T_A \le 70°C$)

Description	Symbol	Conditions	Min	Max	Units	Notes
Input High (Logic 1) Voltage	V_{IH}		1.7	V_{DD} +0.3	V	1
Input Low (Logic 0) Voltage	V_{IL}		-0.3	0.7	V	1
Input Leakage Current	I_{LI}	$0V \le V_{IN} \le V_{DD}$	-5	5	µA	2
Output Leakage Current	I_{LO}	Output(s) Disabled, $0V \le V_{IN} \le V_{DD}$	-5	5	µA	
Output High Voltage	V_{OH}	I_{OH} = -1.0mA	2.0	---	V	1
Output Low Voltage	V_{OL}	I_{OL} = 1.0mA	---	0.4	V	1
Supply Voltage	V_{DD}		2.375	2.625	V	1

NOTES:
1. All voltages referenced to V_{SS} (GND)
2. ZZ pin has an internal pull-up, and input leakage is higher.

DC CHARACTERISTICS

Description	Symbol	Conditions	Typ	166 MHz	150 MHz	133 MHz	100 MHz	Units	Notes
Power Supply Current: Operating	I_{DD}	Device Selected; All Inputs $\le V_{IL}$ or $\ge V_{IH}$; Cycle Time = t_{CYC} MIN; V_{DD} = MAX; Output Open		650	600	560	500	mA	1, 2
Power Supply Current: Standby	I_{SB2}	Device Deselected; V_{DD} = MAX; All Inputs $\le V_{SS}$ + 0.2 or V_{DD} - 0.2; All Inputs Static; CLK Frequency = 0; ZZ $\le V_{IL}$	30	60	60	60	60	mA	2
Power Supply Current: Current	I_{SB3}	Device Selected; All Inputs $\le V_{IL}$ or $\ge V_{IH}$; Cycle Time = t_{CYC} MIN; V_{DD} = MAX; Output Open; ZZ $\ge V_{DD}$ - 0.2V	20	40	40	40	40	mA	2
Clock Running Standby Current	I_{SB4}	Device Deselected; V_{DD} = MAX; All Inputs $\le V_{SS}$ + 0.2 or V_{DD} - 0.2; Cycle Time = t_{CYC} MIN; ZZ $\le V_{IL}$		140	120	100	80	mA	2

NOTES:
1. I_{DD} is specified with no output current and increases with faster cycle times. I_{DD} increases with faster cycle times and greater output loading.
2. Typical values are measured at 2.5V, 25°C, and 10ns cycle time.

BGA CAPACITANCE

Description	Symbol	Conditions	Typ	Max	Units	Notes
Control Input Capacitance	C_I	T_A = 25°C; f = 1MHz	5	7	pF	1
Input/Output Capacitance (DQ)	C_O	T_A= 25°C; f = 1MHz	6	8	pF	1
Address Capacitance	C_A	T_A = 25°C; f = 1MHz	5	7	pF	1
Clock Capacitance	C_{CK}	T_A = 25°C; f = 1MHz	3	5	pF	1

NOTES:
1. This parameter is sampled.

AC CHARACTERISTICS

	Symbol	166MHz		150MHz		133MHz		100MHz		
Parameter		Min	Max	Min	Max	Min	Max	Min	Max	Units
Clock Time	t_{CYC}	6.0		6.7		7.5		10.0		ns
Clock Access Time	t_{CD}	—	3.5	—	3.8	—	4.2	—	5.0	ns
Output enable to Data Valid	t_{OE}	—	3.5	—	3.8	—	4.2	—	5.0	ns
Clock High to Output Low-Z	t_{LZC}	1.5	—	1.5	—	1.5	—	1.5	—	ns
Output Hold from Clock High	t_{OH}	1.5	—	1.5	—	1.5	—	1.5	—	ns
Output Enable Low to output Low-Z	t_{LZOE}	0.0	—	0.0	—	0.0	—	0.0	—	ns
Output Enable High to Output High-Z	t_{HZOE}	—	3.0	—	3.0	—	3.5	—	3.5	ns
Clock High to Output High-Z	t_{HZC}	—	3.0	—	3.0	—	3.5	—	3.5	ns
Clock High Pulse Width	t_{CH}	2.2	—	2.5	—	3.0	—	3.0	—	ns
Clock Low Pulse Width	t_{CL}	2.2	—	2.5	—	3.0	—	3.0	—	ns
Address Setup to Clock High	t_{AS}	1.5	—	1.5	—	1.5	—	1.5	—	ns
CKE Setup to Clock High	t_{CES}	1.5	—	1.5	—	1.5	—	1.5	—	ns
Data Setup to Clock High	t_{DS}	1.5	—	1.5	—	1.5	—	1.5	—	ns
Write Setup to Clock High	t_{WS}	1.5	—	1.5	—	1.5	—	1.5	—	ns
Address Advance to Clock High	t_{ADVS}	1.5		1.5		1.5		1.5		ns
Chip Select Setup to Clock High	t_{CSS}	1.5		1.5		1.5		1.5		ns
Address Hold to Clock high	t_{AH}	0.5	—	0.5	—	0.5	—	0.5	—	ns
CKE Hold to Clock High	t_{CEH}	0.5	—	0.5	—	0.5	—	0.5	—	ns
Data Hold to Clock High	t_{DH}	0.5	—	0.5	—	0.5	—	0.5	—	ns
Write Hold to Clock High	t_{WH}	0.5	—	0.5	—	0.5	—	0.5	—	ns
Address Advance to Clock High	t_{ADVH}	0.5	—	0.5	—	0.5	—	0.5	—	ns
Chip Select Hold to Clock High	t_{CSH}	0.5	—	0.5	—	0.5	—	0.5	—	ns

NOTES:

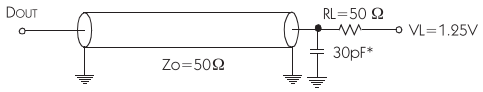
1. *All Address inputs must meet the specified setup and hold times for all rising clock (CLK) edges when ADV is sampled low and $\overline{CEx}$ is sampled valid. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.*
2. *Chip enable must be valid at each rising edge of CLK (when ADV is Low) to remain enabled.*
3. *A write cycle is defined by $\overline{WE}$ low having been registered into the device at ADV Low. A Read cycle is defined by $\overline{WE}$ High with ADV Low. Both cases must meet setup and hold times.*
4. *Applies to each of the independent arrays.*

AC TEST CONDITIONS

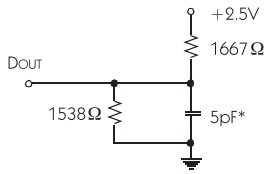
(T_A = 0 TO 70°C, V_{DD} = 2.5V ± 5%, UNLESS OTHERWISE SPECIFIED)

Parameter	Value
Input Pulse Level	0 to 2.5V
Input Rise and Fall Time (Measured at 20% to 80%)	1.0V/ns
Input and Output Timing Reference Levels	1.25V
Output Load	See Output Load (A)

OUTPUT LOAD (A)



OUTPUT LOAD (B)
(FOR t_{LZC}, t_{LZOE}, t_{HZOE}, AND t_{HZC})



**Including Scope and Jig Capacitance*

SNOOZE MODE

SNOOZE MODE is a low-current, "power-down" mode in which the device is deselected and current is reduced to I_{SB2Z}. The duration of SNOOZE MODE is dictated by the length of time Z is in a HIGH state. After the device enters SNOOZE MODE, all inputs except ZZ become gated inputs and are ignored. ZZ is an asynchronous, active HIGH input that causes the device to enter SNOOZE MODE.

When ZZ becomes a logic HIGH, I_{SB2Z} is guaranteed after the setup time t_{ZZ} is met. Any READ or WRITE operation pending when the device enters SNOOZE MODE is not guaranteed to complete successfully. Therefore, SNOOZE MODE must not be initiated until valid pending operations are completed.

SNOOZE MODE

Description	Conditions	Symbol	Min	Max	Units	Notes
Current during SNOOZE MODE	ZZ ≥ V_{IH}	I_{SB2Z}		10	mA	
ZZ active to input ignored		t_{ZZ}		2(t_{KC})	ns	1
ZZ inactive to input sampled		t_{RZZ}	2(t_{KC})		ns	1
ZZ active to snooze current		t_{ZZI}		2(t_{KC})	ns	1
ZZ inactive to exit snooze current		t_{RZZI}			ns	1

FIG. 2 SNOOZE MODE TIMING DIAGRAM

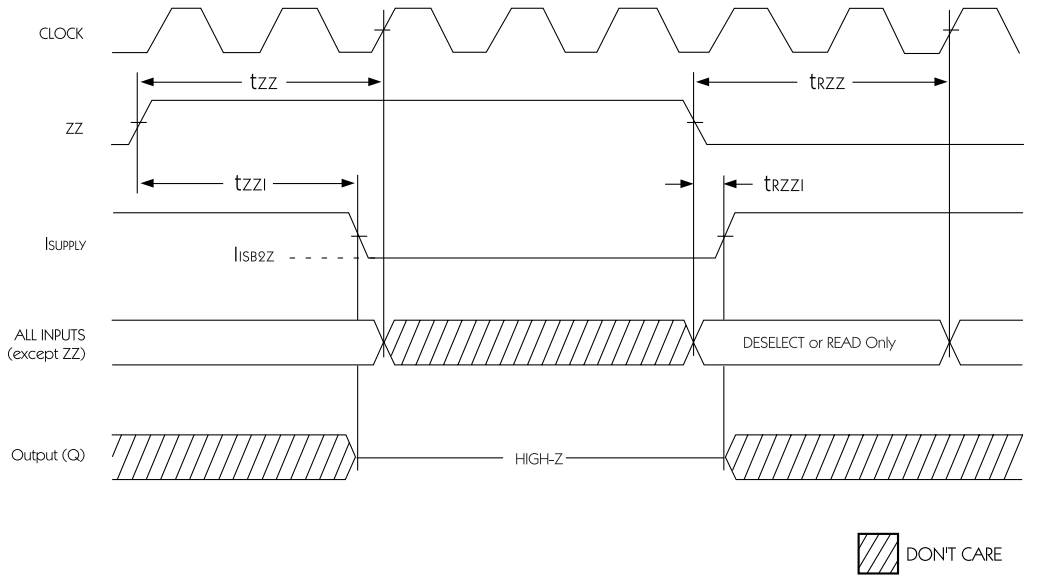
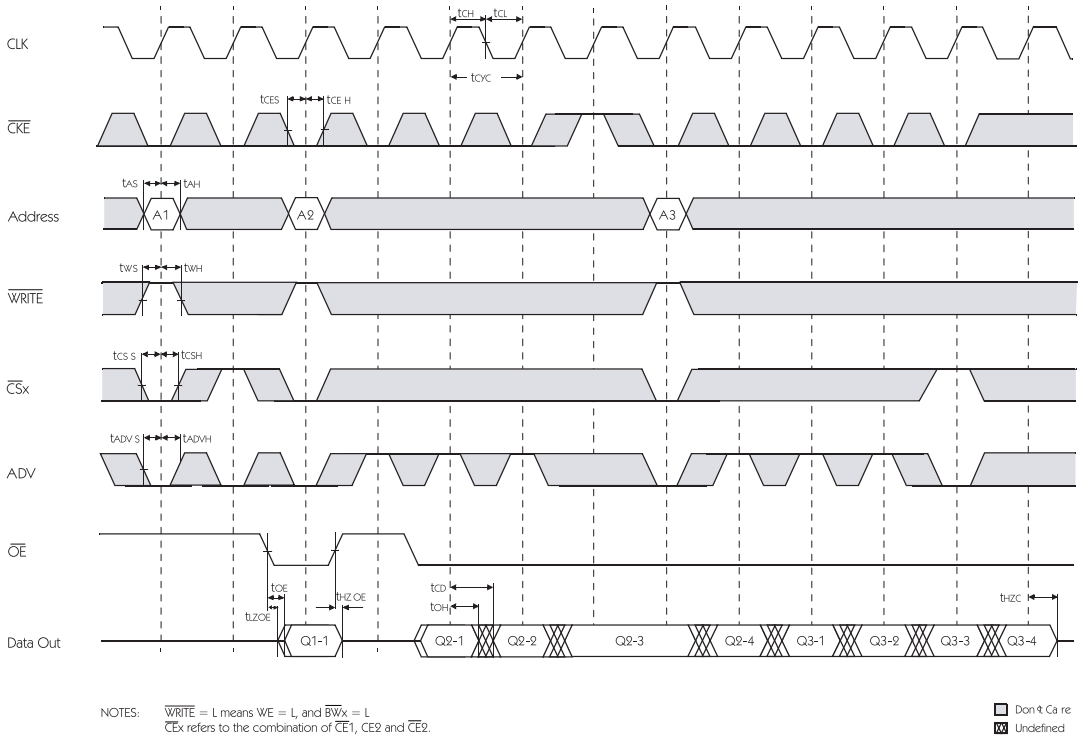
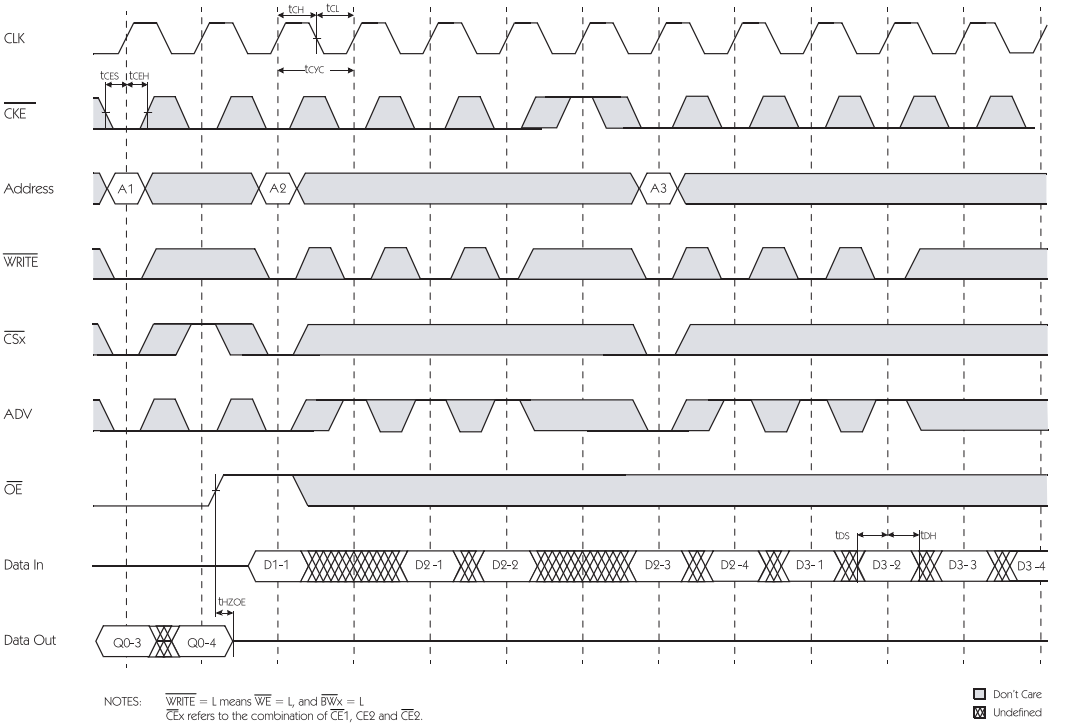


FIG. 3 TIMING WAVEFORM OF READ CYCLE



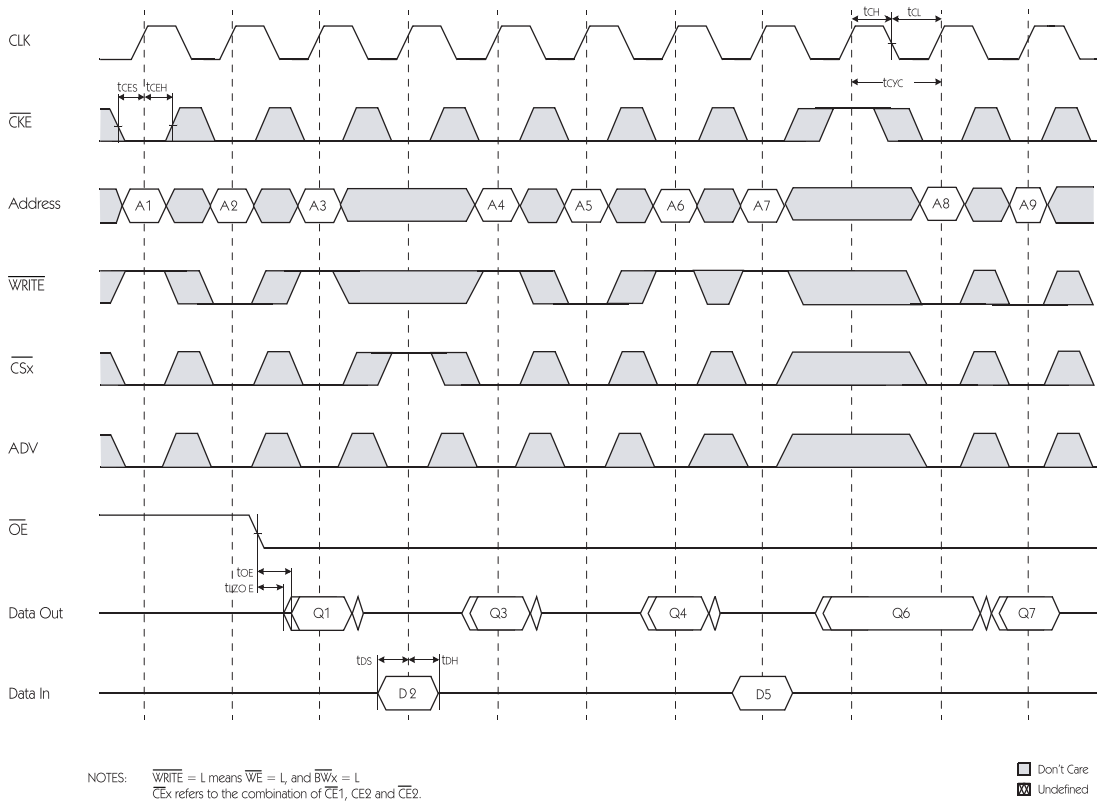
Note:
Applies to both independent arrays.

FIG. 4 TIMING WAVEFORM OF WRITE CYCLE



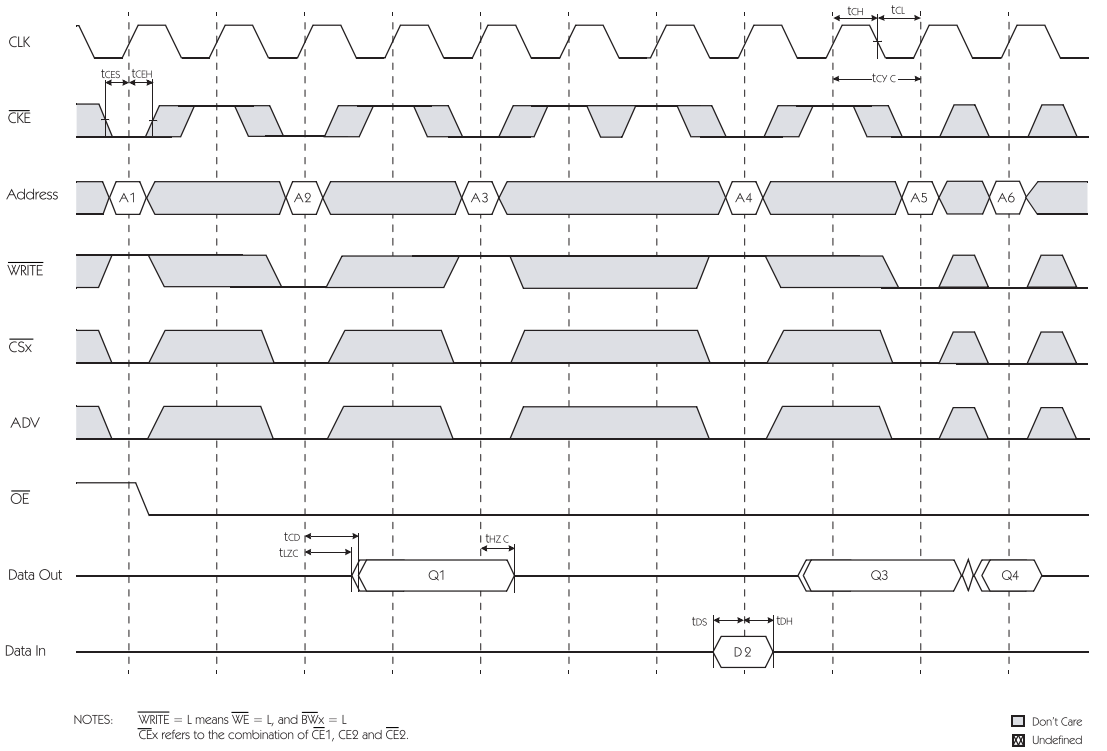
Note:
Applies to both independent arrays.

FIG. 5 TIMING WAVEFORM OF SINGLE READ/WRITE



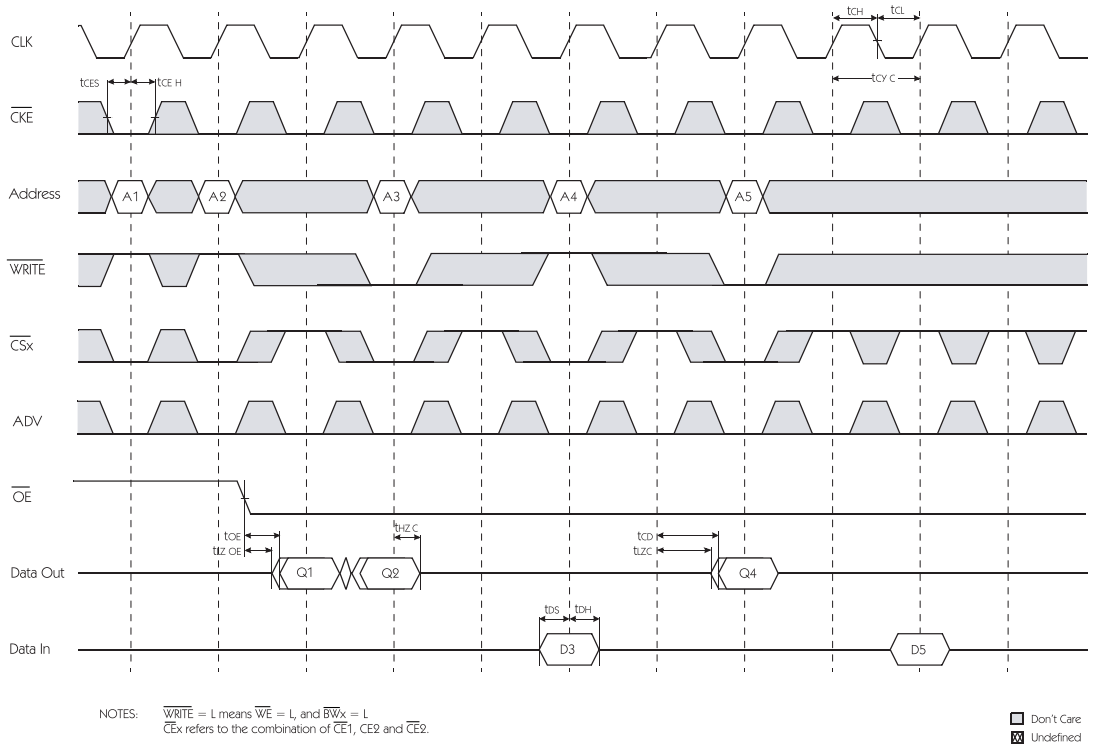
Note:
Applies to both independent arrays.

FIG. 6 TIMING WAVEFORM OF $\overline{CKE}$ OPERATION



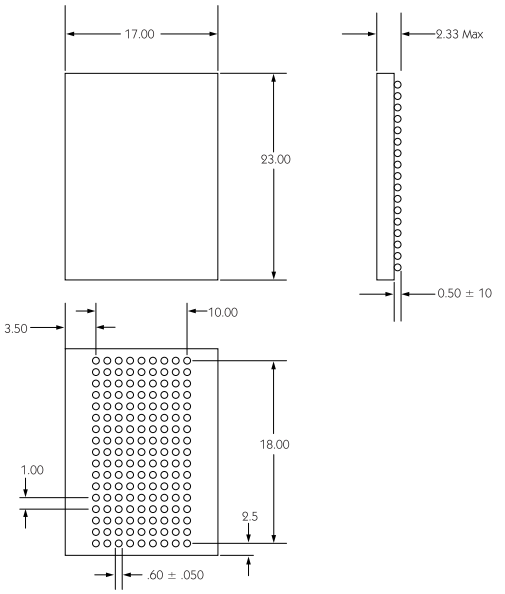
Note:
Applies to both independent arrays.

FIG. 7 TIMING WAVEFORM OF $\overline{CE}$ OPERATION



Note:
Applies to both independent arrays.

PACKAGE DIMENSION: 119 BUMP PBGA



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE: Ball attach pad for above BGA package is 620 microns in diameter. Pad is solder mask defined.

ORDERING INFORMATION

COMMERCIAL TEMP RANGE (0°C TO 70°C)

Part Number	Configuration	t_{CD} (ns)	Clock (MHz)	Operating Range	Temperature Range
WED2ZLRSP01S35BC	512K x 32/256K x 32	3.5	166	Commercial	0° - 70° C
WED2ZLRSP01S38BC	512K x 32/256K x 32	3.8	150	Commercial	0° - 70°C
WED2ZLRSP01S42BC	512K x 32/256K x 32	4.2	133	Commercial	0° - 70°C
WED2ZLRSP01S50BC	512K x 32/256K x 32	5.0	100	Commercial	0° - 70°C
WED2ZLRSP01S38BI	512K x 32/256K x 32	3.8	150	Industrial	-40° - 85°C
WED2ZLRSP01S42BI	512K x 32/256K x 32	4.2	133	Industrial	-40° - 85°C
WED2ZLRSP01S50BI	512K x 32/256K x 32	5.0	100	Industrial	-40° - 85°C