

# Preliminary W28J160B/T



## 16M (1M ´ 16/2M ´ 8) BOOT BLOCK FLASH MEMORY

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## 1. GENERAL DESCRIPTION

WINBOND's W28J160B/T Flash memory is a high-density, low-cost, nonvolatile, read/write storage solution for a wide range of applications. It can operate at  $V_{DD} = 2.7V - 3.6V$  and  $V_{PP} = 2.7V - 3.6V$  or  $11.7V - 12.3V$ . Its low voltage operation capability realize battery life and suits for cellular phone application. Its Boot, Parameter and Main-blocked architecture, low voltage and extended cycling provide for highly flexible component suitable for portable terminals and personal computers. Its enhanced suspend capabilities provide for an ideal solution for code + data storage applications. For secure code storage applications, such as networking, where code is either directly executed out of flash or downloaded to DRAM, the device offers four levels of protection: absolute protection with  $V_{PP} \leq V_{PPLK}$ , selective hardware block locking or flexible software block locking. These alternatives give designers ultimate control of their code security needs. The device is manufactured on 0.25  $\mu m$  process technology. It comes in industry-standard package: the 48-lead TSOP, ideal for board constrained applications.

## 2. FEATURES

- Low Voltage Operation
  - $V_{DD} = V_{PP} = 2.7V - 3.6V$  Single Voltage
- User-Configurable x 8 or x 16 Operation
- High-Performance Read Access Time
  - 90 nS ( $V_{DD} = 2.7V - 3.6V$ )
- Operating Temperature
  - $0^{\circ}C$  to  $+70^{\circ}C$  (W28J160BT/TT90C)
  - $-40^{\circ}C$  to  $+85^{\circ}C$  (W28J160BT/TT90L)
- Low Power Management
  - Typ. 2  $\mu A$  ( $V_{DD} = 3.0V$ ) Standby Current
  - Automatic Power Savings Mode Decreases ICCR in Static Mode
  - Typ. 120  $\mu A$  ( $V_{DD} = 3.0V$ ,  $T_A = +25^{\circ}C$ ,  $f = 32$  KHz) Read Current
- Optimized Array Blocking Architecture
  - Two 4K-word (8K-byte) Boot Blocks
  - Six 4K-word (8K-byte) Parameter Blocks
  - Thirty-one 32K-word (64K-byte) Main Blocks
  - Top or Bottom Boot Location
- Extended Cycling Capability
  - Minimum 100,000 Block Erase Cycles
- Enhanced Automated Suspend Options
  - Word/Byte Write Suspend to Read
  - Block Erase Suspend to Word/Byte Write
  - Block Erase Suspend to Read
- Enhanced Data Protection Features
  - Absolute Protection with  $V_{PP} \leq V_{PPLK}$
  - Block Erase, Full Chip Erase, Word/Byte Write and Lock-Bit Configuration Lockout during Power Transitions
  - Block Locking with Command and #WP
  - Permanent Locking
- Automated Block Erase, Full Chip Erase, Low Power Management Word/Byte Write and Lock-Bit Configuration
  - Command User Interface (CUI)
  - Status Register (SR)
- SRAM-Compatible Write Interface
- Industry-Standard Packaging
  - 48-Lead TSOP
- Nonvolatile Flash Technology
- CMOS Process (P-type silicon substrate)
- Not designed or rated as radiation hardened



## 3. PRODUCT OVERVIEW

The W28J160B/T is a high-performance 16M-bit Boot Block Flash memory organized as 1M-word of 16 bits or 2M-byte of 8 bits. The 1M-word/2M-byte of data is arranged in two 4K-word/8K-byte boot blocks, six 4Kword/ 8K-byte parameter blocks and thirty-one 32Kword/64K-byte main blocks which are individually erasable, lockable and unlockable in-system. The memory map is shown in Figure 3.

The dedicated VPP pin gives complete data protection when VPP = VPPLK.

A Command User Interface (CUI) serves as the interface between the system processor and internal operation of the device. A valid command sequence written to the CUI initiates device automation. An internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for block erase, full chip erase, word/byte write and lock-bit configuration operations.

A block erase operation erases one of the device's 32Kword/64K-byte blocks typically within 1.2s (3V VDD, 3V VPP), 4K-word/8K-byte blocks typically within 0.6s (3V VDD, 3V VPP) independent of other blocks. Each block can be independently erased minimum 100,000 times. Block erase suspend mode allows system software to suspend block erase to read or write data from any other block.

Writing memory data is performed in word/byte increments of the device's 32K-word blocks typically within 33  $\mu$ S (3V VDD, 3V VPP), 64K-byte blocks typically within 31  $\mu$ S (3V VDD, 3V VPP), 4K-word blocks typically within 36  $\mu$ S (3V VDD, 3V VPP), 8Kbyte blocks typically within 32  $\mu$ S (3V VDD, 3V VPP). Word/byte write suspend mode enables the system to read data or execute code from any other flash memory array location.

Individual block locking uses a combination of bits, thirty-nine block lock-bits, a permanent lock-bit and #WP pin, to lock and unlock blocks. Block lock-bits gate block erase, full chip erase and word/byte write operations, while the permanent lock-bit gates block lock-bit modification and locked block alternation. Lock-bit configuration operations (Set Block Lock-Bit, Set Permanent Lock-Bit and Clear Block Lock-Bits commands) set and cleared lock-bits.

The status register indicates when the WSM's block erase, full chip erase, word/byte write or lock-bit configuration operation is finished.

The RY/#BY output gives an additional indicator of WSM activity by providing both a hardware signal of status (versus software polling) and status masking (interrupt masking for background block erase, for example). Status polling using RY/#BY minimizes both CPU overhead and system power consumption. When low, RY/#BY indicates that the WSM is performing a block erase, full chip erase, word/byte write or lock-bit configuration. RY/#BY-high Z indicates that the WSM is ready for a new command, block erase is suspended (and word/byte write is inactive), word/byte write is suspended, or the device is in reset mode.

The access time is 90 nS (tAVQV) over the operating temperature range and VDD supply voltage range of 2.7V – 3.6V.

The Automatic Power Savings (APS) feature substantially reduces active current when the device is in static mode (addresses not switching). In APS mode, the typical ICCR current is 2  $\mu$ A (CMOS) at 3.0V VDD.

When #CE and #RESET pins are at VDD, the ICC CMOS standby mode is enabled. When the #RESET pin is at Vss, reset mode is enabled which minimizes power consumption and provides write protection. A reset time (tPHQV) is required from #RESET switching high until outputs are valid. Likewise, the device has a wake time (tPHEL) from #RESET-high until writes to the CUI are recognized. With #RESET at Vss, the WSM is reset and the status register is cleared.

Please do not execute reprogramming "0" for the bit which has already been programed "0". Overwrite operation may generate inerasable bit. In case of reprogramming "0" to the data which has been programmed "1".

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- Program "0" for the bit in which you want to change data from "1" to "0".
- Program "1" for the bit which has already been programmed "0".

For example, changing data from "10111101" to "10111100" requires "11111110" programming.

## 4. BLOCK DIAGRAM

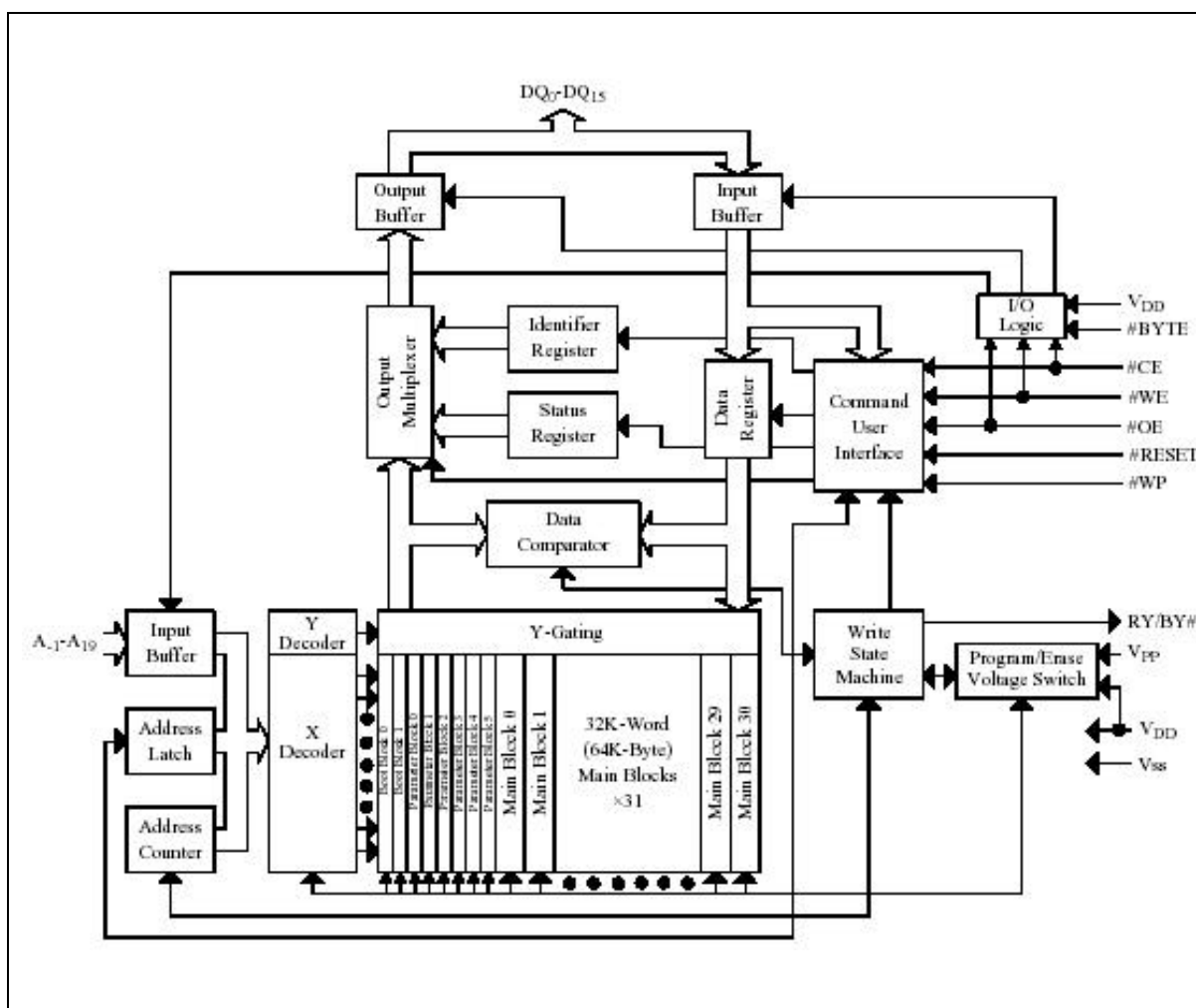


Figure 1. Block Diagram

## Block Organization

This product features an asymmetrically-blocked architecture providing system memory integration. Each erase block can be erased independently of the others up to 100,000 times. For the address locations of the blocks, see the memory map in Figure 3.

**Boot Blocks:** The boot block is intended to replace a dedicated boot PROM in a microprocessor or microcontroller-based system. This boot block 4K words (4,096 words) features hardware controllable write protection to protect the crucial microprocessor boot code from accidental modification. The

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protection of the boot block is controlled using a combination of the VPP, #RESET, #WP pins and block lock-bit.

**Parameter Blocks:** The boot block architecture includes parameter blocks to facilitate storage of frequently update small parameters that would normally require an EEPROM. By using software techniques, the word-rewrite functionality of EEPROMs can be emulated. Each boot block component contains six parameter blocks of 4K words (4,096 words) each. The protection of the parameter block is controlled using a combination of the VPP, #RESET and block lock-bit.

**Main Blocks:** The reminder is divided into main blocks for data or code storage. Each 16M-bit device contains thirty-one 32K words (32,768 words) blocks. The protection of the main block is controlled using a combination of the VPP, #RESET and block lock-bit.

## 5. PIN CONFIGURATION

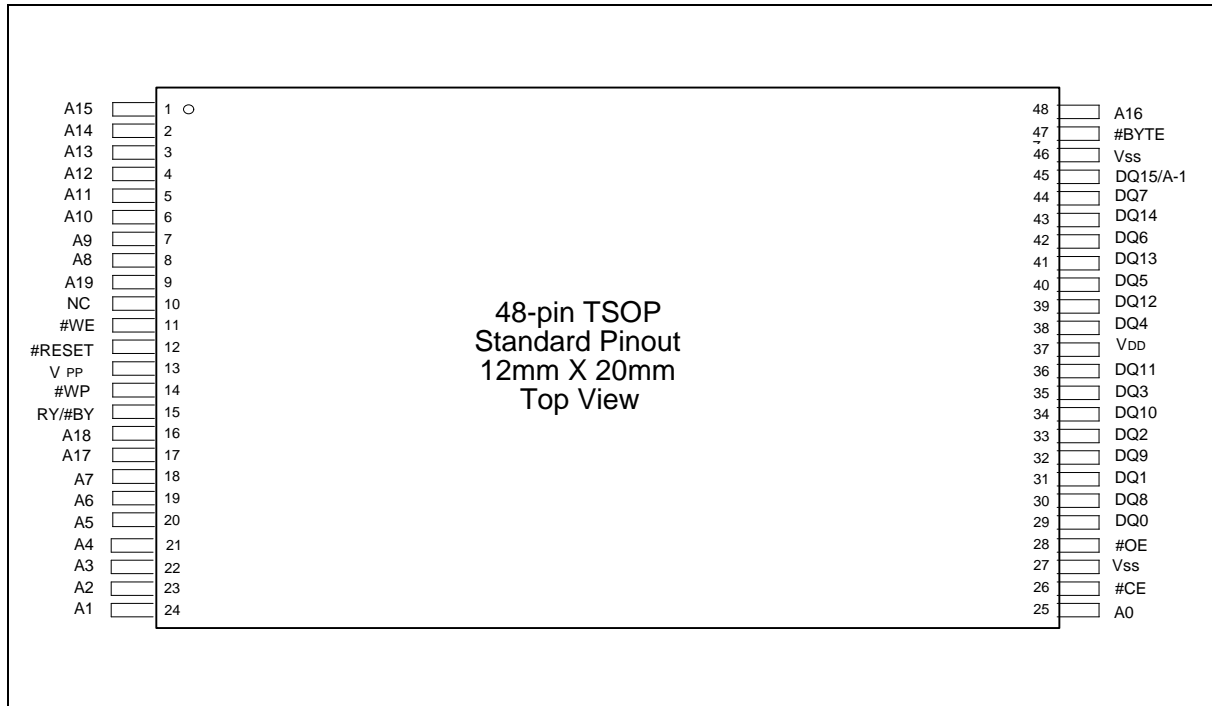


Figure 2. TSOP 48-Lead Pinout

## 6. PIN DESCRIPTION

SYM.	TYPE	NAME AND FUNCTION
A – 1 A0 – A19	INPUT	ADDRESS INPUTS: Inputs for addresses during read and write operations. Addresses are internally latched during a write cycle. A – 1: Lower address input while #BYTE is V <sub>IL</sub> . A – 1 pin changes DQ15 pin while #BYTE is V <sub>IH</sub> . A15 – A19: Main Block Address. A12 – A19: Boot and Parameter Block Address.
DQ0-DQ15	INPUT/ OUTPUT	DATA INPUT/OUTPUTS: Inputs data and commands during CUI write cycles; outputs data during memory array, status register and identifier code read cycles. Data pins float to high-impedance when the chip is deselected or outputs are disabled. Data is internally latched during a pin write cycle. DQ8 – DQ15 pins are not used while byte mode (#BYTE = V <sub>IL</sub> ). Then, DQ15 changes A-1 address input.
#CE	INPUT	CHIP ENABLE: Activates the device's control logic, input buffers, decoders and sense amplifiers. #CE-high deselects the device and reduces power consumption to standby levels.
#RESET	INPUT	RESET: Resets the device internal automation. #RESET-high enables normal operation. When driven low, #RESET inhibits write operations which provides data protection during power transitions. Exit from reset mode sets the device to read array mode. #RESET must be V <sub>IL</sub> during power-up.
#OE	INPUT	OUTPUT ENABLE: Gates the device's outputs during a read cycle.
#WE	INPUT	WRITE ENABLE: Controls writes to the CUI and array blocks. Addresses and data are latched on the rising edge of the #WE pulse.
#WP	INPUT	WRITE PROTECT: When #WP is V <sub>IL</sub> , boot blocks cannot be written or erased. When #WP is V <sub>IH</sub> , locked boot blocks can not be written or erased. #WP is not affected parameter and main places device in byte mode (× 8). All data is then input or output on blocks.
#BYTE	INPUT	BYTE ENABLE: #BYTE V <sub>IL</sub> places the device in byte mode (× 8), All data is then input or output on DQ0 – 7, and DQ8 – 15 float. #BYTE V <sub>IH</sub> places the device in word mode (× 16), and turns off the A-1 input buffer.
RY/#BY	OPEN DRAIN OUTPUT	READY/BUSY#: Indicates the status of the internal WSM. When low, the WSM is performing an internal operation (block erase, full chip erase, word/byte write or lock-bit configuration). RY/#BY-high Z indicates that the WSM is ready for new commands, block erase is suspended, and word/byte write is inactive, word/byte write is suspended, or the device is in reset mode.
V <sub>PP</sub>	SUPPLY	BLOCK ERASE, FULL CHIP ERASE, WORD/BYTE WRITE OR LOCK-BIT CONFIGURATION POWER SUPPLY: For erasing array blocks, writing words/bytes or configuring lock-bits. With V <sub>PP</sub> = V <sub>PP</sub> PLK, memory contents cannot be altered. Block erase, full chip erase, word/byte write and lock-bit configuration with an invalid V <sub>PP</sub> (see DC Characteristics) produce spurious results and should not be attempted. Applying 12V ±0.3V to V <sub>PP</sub> during erase/write can only be done for a maximum of 1000 cycles on each block. V <sub>PP</sub> may be connected to 12V±0.3V for a total of 80 hours maximum.
V <sub>DD</sub>	SUPPLY	DEVICE POWER SUPPLY: Do not float any power pins. With V <sub>DD</sub> = V <sub>LKO</sub> , all write attempts to the flash memory are inhibited. Device operations at invalid V <sub>DD</sub> voltage (see DC Characteristics) produce spurious results and should not be attempted.
V <sub>SS</sub>	SUPPLY	GROUND: Do not float any ground pins.
NC		NO CONNECT: Lead is not internal connected; it may be driven or floated.

Table 1



## 7. PRINCIPLES OF OPERATION

The W28J160B/T flash memory includes an on-chip WSM to manage block erase, full chip erase, word/byte write and lock-bit configuration functions. It allows for: 100% TTL-level control inputs, fixed power supplies during block erase, full chip erase, word/byte write and lock-bit configuration, and minimal processor overhead with RAM-like interface timings.

After initial device power-up or return from reset mode (see Bus Operations section) device defaults to read array mode. Manipulation of external memory control pins allow array read, standby and output disable operations.

Status register and identifier codes can be accessed through the CUI independent of the VPP voltage. High voltage on VPP enables successful block erase, full chip erase, word/byte write and lock-bit configurations. All functions associated with altering memory contents-block erase, full chip erase, word/byte write, lock-bit configuration, status and identifier codes-are accessed via the CUI and verified through the status register.

Commands are written using standard microprocessor write timings. The CUI contents serve as input to the WSM, which controls the block erase, full chip erase, word/byte write and lock-bit configuration. The internal algorithms are regulated by the WSM, including pulse repetition, internal verification and margining of data. Addresses and data are internally latched during write cycles. Writing the appropriate command outputs array data, accesses the identifier codes or outputs status register data.

Interface software that initiates and polls progress of block erase, full chip erase, word/byte write and lock-bit configuration can be stored in any block. This code is copied to and executed from system RAM during flash memory updates. After successful completion, reads are again possible via the Read Array command. Block erase suspend allows system software to suspend a block erase to read/write data from/to blocks other than that which is suspend. Word/byte write suspend allows system software to suspend a word/byte write to read data from any other flash memory array location.

### Data Protection

When VPP = VPPLK, memory contents cannot be altered. The CUI, with two-step block erase, full chip erase, word/byte write or lock-bit configuration command sequences, provides protection from unwanted operations even when high voltage is applied to VPP. All write functions are disabled when VDD is below the write lockout voltage VLKO or when #RESET is at VIL. The device's block locking capability provides additional protection from inadvertent code or data alteration by gating block erase, full chip erase and word/byte write operations.

Refer to Table 5 for write protection alternatives.



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[A <sub>19</sub> -A <sub>0</sub> ]	Top Boot	[A <sub>19</sub> -A <sub>1</sub> ]	[A <sub>19</sub> -A <sub>0</sub> ]	Bottom Boot	[A <sub>19</sub> -A <sub>1</sub> ]
FFFFF	4KW/8KB Boot Block 0	1FFFFF	FFFFF	32KW/64KB Main Block 30	1FFFFF
FF000	4KW/8KB Boot Block 1	1FE000	FF000	32KW/64KB Main Block 29	1FE000
FEFFF	4KW/8KB Boot Block 1	1FD0FF	FEFFF	32KW/64KB Main Block 28	1FEFFF
FE000	4KW/8KB Parameter Block 0	1FC000	FE000	32KW/64KB Main Block 27	1FE000
FDFFF	4KW/8KB Parameter Block 1	1FBFFF	FDFFF	32KW/64KB Main Block 26	1FDFFF
FD000	4KW/8KB Parameter Block 2	1FA000	FD000	32KW/64KB Main Block 25	1FD000
FCFFF	4KW/8KB Parameter Block 3	1F9FFF	FCFFF	32KW/64KB Main Block 24	1FCFFF
FC000	4KW/8KB Parameter Block 4	1F8000	FC000	32KW/64KB Main Block 23	1FC000
FBFFF	4KW/8KB Parameter Block 5	1F7FFF	FBFFF	32KW/64KB Main Block 22	1FBFFF
FB000	32KW/64KB Main Block 0	1F6000	FB000	32KW/64KB Main Block 21	1FB000
FAFFF	32KW/64KB Main Block 1	1F5FFF	FAFFF	32KW/64KB Main Block 20	1FAFFF
FA000	32KW/64KB Main Block 2	1F4000	FA000	32KW/64KB Main Block 19	1FA000
F9FFF	32KW/64KB Main Block 3	1F3FFF	F9FFF	32KW/64KB Main Block 18	1F9FFF
F9000	32KW/64KB Main Block 4	1F2000	F9000	32KW/64KB Main Block 17	1F9000
F8FFF	32KW/64KB Main Block 5	1F1FFF	F8FFF	32KW/64KB Main Block 16	1F8FFF
F8000	32KW/64KB Main Block 6	1F0000	F8000	32KW/64KB Main Block 15	1F8000
F7FFF	32KW/64KB Main Block 7	1EF000	F7FFF	32KW/64KB Main Block 14	1EF000
F7000	32KW/64KB Main Block 8	1EFFFF	F7000	32KW/64KB Main Block 13	1EFFFF
FEFFF	32KW/64KB Main Block 9	1E0000	FEFFF	32KW/64KB Main Block 12	1FEFFF
FE000	32KW/64KB Main Block 10	1DFFFF	FE000	32KW/64KB Main Block 11	1FE000
FDFFF	32KW/64KB Main Block 11	1D0000	FDFFF	32KW/64KB Main Block 10	1FDFFF
FD000	32KW/64KB Main Block 12	1CFFFF	FD000	32KW/64KB Main Block 9	1FD000
FCFFF	32KW/64KB Main Block 13	1C0000	FCFFF	32KW/64KB Main Block 8	1FCFFF
FC000	32KW/64KB Main Block 14	1BFFFF	FC000	32KW/64KB Main Block 7	1FC000
FBFFF	32KW/64KB Main Block 15	1B0000	FBFFF	32KW/64KB Main Block 6	1FBFFF
FB000	32KW/64KB Main Block 16	1AFFFF	FB000	32KW/64KB Main Block 5	1FB000
FAFFF	32KW/64KB Main Block 17	1A0000	FAFFF	32KW/64KB Main Block 4	1FAFFF
FA000	32KW/64KB Main Block 18	19FFFF	FA000	32KW/64KB Main Block 3	1FA000
F9FFF	32KW/64KB Main Block 19	190000	F9FFF	32KW/64KB Main Block 2	1F9FFF
F9000	32KW/64KB Main Block 20	18FFFF	F9000	32KW/64KB Main Block 1	1F9000
F8FFF	32KW/64KB Main Block 21	180000	F8FFF	32KW/64KB Main Block 0	1F8FFF
F8000	32KW/64KB Main Block 22	17FFFF	F8000	4KW/8KB Parameter Block 5	1F8000
F7FFF	32KW/64KB Main Block 23	170000	F7FFF	4KW/8KB Parameter Block 4	1F7FFF
F7000	32KW/64KB Main Block 24	16FFFF	F7000	4KW/8KB Parameter Block 3	1F7000
FEFFF	32KW/64KB Main Block 25	160000	FEFFF	4KW/8KB Parameter Block 2	1FEFFF
FE000	32KW/64KB Main Block 26	15FFFF	FE000	4KW/8KB Parameter Block 1	1FE000
FDFFF	32KW/64KB Main Block 27	150000	FDFFF	4KW/8KB Parameter Block 0	1FDFFF
FD000	32KW/64KB Main Block 28	14FFFF	FD000	4KW/8KB Boot Block 1	1FD000
FCFFF	32KW/64KB Main Block 29	140000	FCFFF	4KW/8KB Boot Block 0	1FCFFF
FC000	32KW/64KB Main Block 30	13FFFF	FC000		1FC000
FBFFF		130000	FBFFF		1FBFFF
FB000		12FFFF	FB000		1FB000
FAFFF		120000	FAFFF		1FAFFF
FA000		11FFFF	FA000		1FA000
F9FFF		110000	F9FFF		1F9FFF
F9000		10FFFF	F9000		1F9000
F8FFF		100000	F8FFF		1F8FFF
F8000		0FFFFF	F8000		1F8000
F7FFF		0F0000	F7FFF		1F7FFF
F7000		0EFFFF	F7000		1F7000
FEFFF		0E0000	FEFFF		1F6FFF
FE000		0DFFFF	FE000		1F6000
FDFFF		0D0000	FDFFF		1F5FFF
FD000		0CFFFF	FD000		1F5000
FCFFF		0C0000	FCFFF		1F4FFF
FC000		0BFFFF	FC000		1F4000
FBFFF		0B0000	FBFFF		1F3FFF
FB000		0AFFFF	FB000		1F3000
FAFFF		0A0000	FAFFF		1F2FFF
FA000		09FFFF	FA000		1F2000
F9FFF		090000	F9FFF		1F1FFF
F9000		08FFFF	F9000		1F1000
F8FFF		080000	F8FFF		1F0FFF
F8000		07FFFF	F8000		1F0000
F7FFF		070000	F7FFF		1EFFFF
F7000		06FFFF	F7000		1E0000
FEFFF		060000	FEFFF		1DFFFF
FE000		05FFFF	FE000		1D0000
FDFFF		050000	FDFFF		1CFFFF
FD000		04FFFF	FD000		1C0000
FCFFF		040000	FCFFF		1BFFFF
FC000		03FFFF	FC000		1B0000
FBFFF		030000	FBFFF		1AFFFF
FB000		02FFFF	FB000		1A0000
FAFFF		020000	FAFFF		19FFFF
FA000		01FFFF	FA000		190000
F9FFF		010000	F9FFF		18FFFF
F9000		00FFFF	F9000		180000
F8FFF		000000	F8FFF		17FFFF
F8000			F8000		170000

Figure 3. Memory Map



## 8. BUS OPERATION

The local CPU reads and writes flash memory in-system. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles.

### Read

Information can be read from any block, identifier codes or status register independent of the VPP voltage. #RESET can be at VIH.

The first task is to write the appropriate read mode command (Read Array, Read Identifier Codes or Read Status Register) to the CUI. Upon initial device power-up or after exit from reset mode, the device automatically resets to read array mode. Six control pins dictate the data flow in and out of the component: #CE, #OE, #BYTE, #WE, #RESET and #WP. #CE and #OE must be driven active to obtain data at the outputs. #CE is the device selection control, and when active enables the selected memory device. #OE is the data output (DQ0 – DQ15) control and when active drives the selected memory data onto the I/O bus. #BYTE is the device I/O interface mode control. #WE must be at VIH, #RESET must be at VIH, and #BYTE and #WP must be at VIL or VIH. Figure 14, 15 illustrates read cycle.

### Output Disable

With #OE at a logic-high level (VIH), the device outputs are disabled. Output pins (DQ0-DQ15) are placed in a high-impedance state.

### Standby

#CE at a logic-high level (VIH) places the device in standby mode which substantially reduces device power consumption. DQ0 – DQ15 outputs are placed in a high impedance state independent of #OE. If deselected during block erase, full chip erase, word/byte write or lock-bit configuration, the device continues functioning, and consuming active power until the operation completes.

### Reset

#RESET at VIL initiates the reset mode.

In read modes, #RESET-low deselects the memory, places output drivers in a high-impedance state and turns off all internal circuits. #RESET must be held low for a minimum of 100 nS. Time tPHQV is required after return from reset mode until initial memory access outputs are valid. After this wake-up interval, normal operation is restored. The CUI is reset to read array mode and status register is set to 80H.

During block erase, full chip erase, word/byte write or lock-bit configuration modes, #RESET-low will abort the operation. RY/#BY remains low until the reset operation is complete. Memory contents being altered are no longer valid; the data may be partially erased or written. Time tPHWL is required after #RESET goes to logic-high (VIH) before another command can be written.

As with any automated device, it is important to assert #RESET during system reset. When the system comes out of reset, it expects to read from the flash memory. Automated flash memories provide status information when accessed during block erase, full chip erase, word/byte write or lock-bit configuration modes. If a CPU reset occurs with no flash memory reset, proper CPU initialization may not occur because the flash memory may be providing status information instead of array data. WINBOND's flash memories allow proper CPU initialization following a system reset through the use of



the #RESET input. In this application, #RESET is controlled by the same #RESET signal that resets the system CPU.

## Read Identifier Codes

The read identifier codes operation outputs the manufacturer code, device code, block lock configuration codes for each block and the permanent lock configuration code (see Figure 4). Using the manufacturer and device codes, the system CPU can automatically match the device with its proper algorithms. The block lock and permanent lock configuration codes identify locked and unlocked blocks and permanent lock-bit setting.

## Write

Writing commands to the CUI enable reading of device data and identifier codes. They also control inspection and clearing of the status register. When  $V_{DD} = 2.7V - 3.6V$  and  $V_{PP} = V_{PPH1/2}$ , the CUI additionally controls block erase, full chip erase, word/byte write and lock-bit configuration.

The Block Erase command requires appropriate command data and an address within the block to be erased. The Full Chip Erase command requires appropriate command data and an address within the device. The Word/Byte Write command requires the command and address of the location to be written. Set Permanent and Block Lock-Bit commands require the command and address within the device (Permanent Lock) or block within the device (Block Lock) to be locked. The Clear Block Lock-Bits command requires the command and address within the device.

The CUI does not occupy an addressable memory location. It is written when #WE and #CE are active. The address and data needed to execute a command are latched on the rising edge of #WE or #CE (whichever goes high first). Standard microprocessor write timings are used.

Figures 16 and 17 illustrate #WE and #CE controlled write operations.

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Top Boot		Bottom Boot	
[A <sub>19</sub> :A <sub>0</sub> ]*		[A <sub>19</sub> :A <sub>0</sub> ]*	
FFFF	Reserved for Future Implementation	FFFF	Reserved for Future Implementation
FF003		F8003	
FF002	Boot Block 0 Lock Configuration Code	F8002	Main Block 30 Lock Configuration Code
FF001	Reserved for Future Implementation	F8001	Reserved for Future Implementation
FF000	Boot Block 0	F8000	Main Block 30
FEFFF	Reserved for Future Implementation	F7FFF	(Main Blocks 1 through 29)
FE003		10000	
FE002	Boot Block 1 Lock Configuration Code	0FFFF	Reserved for Future Implementation
FE001	Reserved for Future Implementation	08003	
FE000	Boot Block 1	08002	Main Block 0 Lock Configuration Code
FDFFF	Reserved for Future Implementation	08001	Reserved for Future Implementation
FD003		08000	Main Block 0
FD002	Parameter Block 0 Lock Configuration Code	07FFF	Reserved for Future Implementation
FD001	Reserved for Future Implementation	07003	
FD000	Parameter Block 0	07002	Parameter Block 5 Lock Configuration Code
FCFFF	(Parameter Blocks 1 through 4)	07001	Reserved for Future Implementation
F9000		07000	Parameter Block 5
F8FFF	Reserved for Future Implementation	06FFF	(Parameter Blocks 1 through 4)
F8003		03000	
F8002	Parameter Block 5 Lock Configuration Code	02FFF	Reserved for Future Implementation
F8001	Reserved for Future Implementation	02003	
F8000	Parameter Block 5	02002	Parameter Block 0 Lock Configuration Code
F7FFF	Reserved for Future Implementation	02001	Reserved for Future Implementation
F0003		02000	Parameter Block 0
F0002	Main Block 0 Lock Configuration Code	01FFF	Reserved for Future Implementation
F0001	Reserved for Future Implementation	01003	
F0000	Main Block 0	01002	Boot Block 1 Lock Configuration Code
EFFFF	(Main Blocks 1 through 29)	01001	Reserved for Future Implementation
08000		01000	Boot Block 1
07FFF	Reserved for Future Implementation	00FFF	Reserved for Future Implementation
00004		00004	
00003	Permanent Lock Configuration Code	00003	Permanent Lock Configuration Code
00002	Main Block 30 Lock Configuration Code	00002	Boot Block 0 Lock Configuration Code
00001	Device Code	00001	Device Code
00000	Manufacturer Code Main Block 30	00000	Manufacturer Code Boot Block 0

\* Address A-1 don't care.

Figure 4. Device Identifier Code Memory Map



## 9. COMMAND DEFINITIONS

When the VPP voltage VPPLK, read operations from the status register, identifier codes, or blocks are enabled. Placing VPPH1/2 on VPP enables successful block erase, full chip erase, word/byte write and lock-bit configuration operations.

Device operations are selected by writing specific commands into the CUI. Table 3 defines these commands.

**Table 2.1. Bus Operations (#BYTE = VIH) (note 1, 2)**

MODE	#RESET	#CE	#OE	#WE	ADDRESS	VPP	DQ0 - 15	RY/#BY(3)
Read (note 8)	VIH	VIL	VIL	VIH	X	X	DOUT	X
Output Disable	VIH	VIL	VIH	VIH	X	X	High Z	X
Standby	VIH	VIH	X	X	X	X	High Z	X
Reset (note 4)	VIL	X	X	X	X	X	High Z	High Z
Read Identifier Codes	VIH	VIL	VIL	VIH	See Figure 4	X	Note 5	High Z
Write (note 6,7,8)	VIH	VIL	VIH	VIL	X	X	DIN	X

**Table 2.2. Bus Operations (#BYTE = VIL) (note 1, 2)**

MODE	#RESET	#CE	#OE	#WE	ADDRESS	VPP	DQ0 - 15	RY/#BY(3)
Read (note 8)	VIH	VIL	VIL	VIH	X	X	DOUT	X
Output Disable	VIH	VIL	VIH	VIH	X	X	High Z	X
Standby	VIH	VIH	X	X	X	X	High Z	X
Reset (note 4)	VIL	X	X	X	X	X	High Z	High Z
Read Identifier Codes	VIH	VIL	VIL	VIH	See Figure 4	X	Note 5	High Z
Write (note 6, 7, 8)	VIH	VIL	VIH	VIL	X	X	DIN	X

Notes:

1. Refer to DC Characteristics. When VPP VPPLK, memory contents can be read, but not altered.
2. X can be VIL or VIH for control pins and addresses, and VPPLK or VPPH1/2 for VPP. See DC Characteristics for VPPLK voltages.
3. RY/#BY is VOL when the WSM is executing internal block erase, full chip erase, word/byte write or lock-bit configuration algorithms. It is High Z during when the WSM is not busy, in block erase suspend mode (with word/byte write inactive), word/byte write suspend mode or reset mode.
4. #RESET at Vss ±0.2V ensures the lowest power consumption.
5. See Read Identifier Codes Command section for details.
6. Command writes involving block erase, full chip erase, word/byte write or lock-bit configuration are reliably executed when VPP = VPPH1/2 and VDD = 2.7V – 3.6V.
7. Refer to Table 3 for valid DIN during a write operation.
8. Never hold #OE low and #WE low at the same timing.



**Table 3. Command Definitions(10)**

COMMAND	BUS CYCLES REQD.	FIRST BUS CYCLE			SECOND BUS CYCLE		
		Oper(1)	Addr(2)	Data(3)	Oper(1)	Addr(2)	Data(3)
Read Array/Reset	1	Write	X	FFH			
Read Identifier Codes	≥2 (note 4)	Write	X	90H	Read	IA	ID
Read Status Register	2	Write	X	70H	Read	X	SRD
Clear Status Register	1	Write	X	50H			
Block Erase	2 (note 5)	Write	X	20H	Write	BA	D0H
Full Chip Erase	2	Write	X	30H	Write	X	D0H
Word/Byte Write	2 (note5, 6)	Write	X	40H or 10H	Write	WA	WD
Block Erase and Word/Byte Write Suspend	1 (note 5)	Write	X	B0H			
Block Erase and Word/Byte Write Resume	1 (note 5)	Write	X	D0H			
Set Block Lock-Bit	2 (note 8)	Write	X	60H	Write	BA	01H
Clear Block Lock-Bits	2 (note 7, 8)	Write	X	60H	Write	X	D0H
Set Permanent Lock-Bit	2 (note 9)	Write	X	60H	Write	X	F1H

Notes:

- BUS operations are defined in Table 2.1 and Table 2.2.
- X = Any valid address within the device.  
IA = Identifier Code Address: see Figure 4.  
BA = Address within the block being erased.  
WA = Address of memory location to be written.
- SRD = Data read from status register. See Table 6 for a description of the status register bits.  
WD = Data to be written at location WA. Data is latched on the rising edge of #WE or #CE (whichever goes high first).  
ID = Data read from identifier codes.
- Following the Read Identifier Codes command, read operations access manufacturer, device, block lock configuration and permanent lock configuration codes. See Read Identifier Codes Command section for details.
- If #WP is  $V_{IL}$ , boot blocks are locked without block lock-bits state. If #WP is  $V_{IH}$ , boot blocks are locked by block lockbits. The parameter and main blocks are locked by block lock-bits without #WP state.
- Either 40H or 10H are recognized by the WSM as the word/byte write setup.
- The clear block lock-bits operation simultaneously clears all block lock-bits.
- If the permanent lock-bit is set, Set Block Lock-Bit and Clear Block Lock-Bits commands can not be done.
- Once the permanent lock-bit is set, permanent lock-bit reset is unable.
- Commands other than those shown above are reserved by WINBOND for future device implementations and should not be used.

## Read Array Command

Upon initial device power-up and after exit from reset mode, the device defaults to read array mode. This operation is also initiated by writing the Read Array command. The device remains enabled for reads until another command is written. Once the internal WSM has started a block erase, full chip erase, word/byte write or lock-bit configuration the device will not recognize the Read Array command until the WSM completes its operation unless the WSM is suspended via an Erase Suspend or



Word/Byte Write Suspend command. The Read Array command functions independently of the VPP voltage and #RESET can be VIH.

## Read Identifier Codes Command

The identifier code operation is initiated by writing the Read Identifier Codes command. Following the command write, read cycles from addresses shown in Figure 4 retrieve the manufacturer, device, block lock configuration and permanent lock configuration codes (see Table 4 for identifier code values). To terminate the operation, write another valid command. Like the Read Array command, the Read Identifier Codes command functions independently of the VPP voltage and #RESET can be VIH. Following the Read Identifier Codes command, the following information can be read:

**Table 4. Identifier Codes**

CODE	ADDRESS(2) [A19 - A0]	DATA(3) [DQ7 - DQ0]
Manufacture Code	00000H	B0H
Device Code	00001H	E8H
Block Lock Configuration	BA(1)+2	
• Block is Unlocked		DQ0 = 0
• Block is Locked		DQ0 = 1
• Reserved for Future Use		DQ1 - 7
Permanent Lock Configuration	00003H	
• Device is Unlocked		DQ0 = 0
• Device is Locked ed		DQ0 = 1
• Reserved for Future Use		DQ1 - 7

## Read Status Register Command

The status register may be read to determine when a block erase, full chip erase, word/byte write or lock-bit configuration is complete and whether the operation completed successfully. It may be read at any time by writing the Read Status Register command. After writing this command, all subsequent read operations output data from the status register until another valid command is written. The status register contents are latched on the falling edge of #OE or #CE, whichever occurs. #OE or #CE must toggle to VIH before further reads to update the status register latch. The Read Status Register command functions independently of the VPP voltage. #RESET can be VIH.

## Clear Status Register Command

Status register bits SR.5, SR.4, SR.3 or SR.1 are set to "1"s by the WSM and can only be reset by the Clear Status Register command. These bits indicate various failure conditions (see Table 6). By allowing system software to reset these bits, several operations (such as cumulatively erasing multiple blocks or writing several words/bytes in sequence) may be performed. The status register may be polled to determine if an error occurred during the sequence.



To clear the status register, the Clear Status Register command (50H) is written. It functions independently of the applied VPP Voltage. #RESET can be VIH. This command is not functional during block erase or word/byte write suspend modes.

## Block Erase Command

Erase is executed one block at a time and initiated by a two-cycle command. A block erase setup is first written, followed by a block erase confirm. This command sequence requires appropriate sequencing and an address within the block to be erased (erase changes all block data to FFFFH/FFH). Block preconditioning, erase, and verify are handled internally by the WSM (invisible to the system). After the two-cycle block erase sequence is written, the device automatically outputs status register data when read (see Figure 5). The CPU can detect block erase completion by analyzing the output data of the RY/#BY pin or status register bit SR.7.

When the block erase is complete, status register bit SR.5 should be checked. If a block erase error is detected, the status register should be cleared before system software attempts corrective actions. The CUI remains in read status register mode until a new command is issued.

This two-step command sequence of set-up followed by execution ensures that block contents are not accidentally erased. An invalid Block Erase command sequence will result in both status register bits SR.4 and SR.5 being set to "1". Also, reliable block erasure can only occur when  $V_{DD} = 2.7V - 3.6V$  and  $V_{PP} = V_{PPH1/2}$ . In the absence of this high voltage, block contents are protected against erasure. If block erase is attempted while  $V_{PP} = V_{PPLK}$ , SR.3 and SR.5 will be set to "1". Successful block erase requires for boot blocks that #WP is VIH and the corresponding block lock-bit be cleared. In parameter and main blocks case, it must be cleared the corresponding block lock-bit. If block erase is attempted when the excepting above conditions, SR.1 and SR.5 will be set to "1".

## Full Chip Erase Command

This command followed by a confirm command erases all of the unlocked blocks. A full chip erase setup (30H) is first written, followed by a full chip erase confirm (D0H). After a confirm command is written, device erases the all unlocked blocks block by block. This command sequence requires appropriate sequencing. Block preconditioning, erase and verify are handled internally by the WSM (invisible to the system). After the two-cycle full chip erase sequence is written, the device automatically outputs status register data when read (see Figure 6). The CPU can detect full chip erase completion by analyzing the output data of the RY/#BY pin or status register bit SR.7.

When the full chip erase is complete, status register bit SR.5 should be checked. If erase error is detected, the status register should be cleared before system software attempts corrective actions. The CUI remains in read status register mode until a new command is issued. If error is detected on a block during full chip erase operation, WSM stops erasing. Full chip erase operation start from lower address block, finish the higher address block. Full chip erase can not be suspended.

This two-step command sequence of set-up followed by execution ensures that block contents are not accidentally erased. An invalid Full Chip Erase command sequence will result in both status register bits SR.4 and SR.5 being set to "1". Also, reliable full chip erasure can only occur when  $V_{DD} = 2.7V - 3.6V$  and  $V_{PP} = V_{PPH1/2}$ . In the absence of this high voltage, block contents are protected against erasure. If full chip erase is attempted while  $V_{PP} = V_{PPLK}$ , SR.3 and SR.5 will be set to "1". Successful full chip erase requires for boot blocks that #WP is VIH and the corresponding block lock-bit be cleared. In parameter and main blocks case, it must be cleared the corresponding block lock-bit. If all blocks are locked, SR.1 and SR.5 will be set to "1".





## Word/Byte Write Command

Word/Byte write is executed by a two-cycle command sequence. Word/Byte write setup (standard 40H or alternate 10H) is written, followed by a second write that specifies the address and data (latched on the rising edge of #WE). The WSM then takes over, controlling the word/byte write and write verify algorithms internally. After the word/byte write sequence is written, the device automatically outputs status register data when read (see Figure 7). The CPU can detect the completion of the word/byte write event by analyzing the RY/#BY pin or status register bit SR.7.

When word/byte write is complete, status register bit SR.4 should be checked. If word/byte write error is detected, the status register should be cleared. The internal WSM verify only detects errors for "1"s that do not successfully write to "0"s. The CUI remains in read status register mode until it receives another command.

Reliable word/byte writes can only occur when  $V_{DD} = 2.7V - 3.6V$  and  $V_{PP} = V_{PPH1/2}$ . In the absence of this high voltage, memory contents are protected against word/byte writes. If word/byte write is attempted while  $V_{PP} < V_{PPLK}$ , status register bits SR.3 and SR.4 will be set to "1". Successful word/byte write requires for boot blocks that #WP is  $V_{IH}$  and the corresponding block lockbit be cleared. In parameter and main blocks case, it must be cleared the corresponding block lock-bit. If word/byte write is attempted when the excepting above conditions, SR.1 and SR.4 will be set to "1".

## Block Erase Suspend Command

The Block Erase Suspend command allows block-erase interruption to read or word/byte write data in another block of memory. Once the block erase process starts, writing the Block Erase Suspend command requests that the WSM suspend the block erase sequence at a predetermined point in the algorithm. The device outputs status register data when read after the Block Erase Suspend command is written. Polling status register bits SR.7 and SR.6 can determine when the block erase operation has been suspended (both will be set to "1"). RY/#BY will also transition to High Z. Specification tWHRZ2 defines the block erase suspend latency.

When Block Erase Suspend command write to the CUI, if block erase was finished, the device places read array mode. Therefore, after Block Erase Suspend command write to the CUI, Read Status Register command (70H) has to write to CUI, then status register bit SR.6 should be checked for places the device in suspend mode. At this point, a Read Array command can be written to read data from blocks other than that which is suspended.

A Word/Byte Write command sequence can also be issued during erase suspend to program data in other blocks. Using the Word/Byte Write Suspend command (see Word/Byte Write Suspend Command section), a word/byte write operation can also be suspended. During a word/byte write operation with block erase suspended, status register bit SR.7 will return to "0" and the RY/#BY output will transition to VOL. However, SR.6 will remain "1" to indicate block erase suspend status.

The only other valid commands while block erase is suspended are Read Status Register and Block Erase Resume. After a Block Erase Resume command is written to the flash memory, the WSM will continue the block erase process. Status register bits SR.6 and SR.7 will automatically clear and RY/#BY will return to VOL. After the Erase Resume command is written, the device automatically outputs status register data when read (see Figure 8).  $V_{PP}$  must remain at  $V_{PPH1/2}$  (the same  $V_{PP}$  level used for block erase) while block erase is suspended. #RESET must also remain at  $V_{IH}$ . #WP must also remain at  $V_{IL}$  or  $V_{IH}$  (the same #WP level used for block erase). Block erase cannot resume until word/byte write operations initiated during block erase suspend have completed.



If the period of from Block Erase Resume command write to the CUI till Block Erase Suspend command write to the CUI be short and done again and again, erase time be prolonged.

## Word/Byte Write Suspend Command

The Word/Byte Write Suspend command allows word/byte write interruption to read data in other flash memory locations. Once the word/byte write process starts, writing the Word/Byte Write Suspend command requests that the WSM suspend the Word/Byte write sequence at a predetermined point in the algorithm. The device continues to output status register data when read after the Word/Byte Write Suspend command is written. Polling status register bits SR.7 and SR.2 can determine when the word/byte write operation has been suspended (both will be set to "1"). RY/#BY will also transition to High Z. Specification tWHRZ1 defines the word/byte write suspend latency.

When Word/Byte Write Suspend command write to the CUI, if word/byte write was finished, the device places read array mode. Therefore, after Word/Byte Write Suspend command write to the CUI, Read Status Register command (70H) has to write to CUI, then status register bit SR.2 should be checked for places the device in suspend mode.

At this point, a Read Array command can be written to read data from locations other than that which is suspended. The only other valid commands while word/byte write is suspended are Read Status Register and Word/Byte Write Resume. After Word/Byte Write Resume command is written to the flash memory, the WSM will continue the word/byte write process. Status register bits SR.2 and SR.7 will automatically clear and RY/#BY will return to VOL. After the Word/Byte Write Resume command is written, the device automatically outputs status register data when read (see Figure 9). VPP must remain at VPPH1/2 (the same VPP level used for word/byte write) while in word/byte write suspend mode. #RESET must also remain at VIH. #WP must also remain at VIL or VIH (the same #WP level used for word/byte write).

If the period of from Word/Byte Write Resume command write to the CUI till Word/Byte Write Suspend command write to the CUI be short and done again and again, write time be prolonged.

## Set Block and Permanent Lock-Bit Commands

A flexible block locking and unlocking scheme is enabled via a combination of block lock-bits, a permanent lock-bit and #WP pin. The block lock-bits and #WP pin gates program and erase operations while the permanent lock-bit gates block-lock bit modification. With the permanent lock-bit not set, individual block lock-bits can be set using the Set Block Lock-Bit command. The Set Permanent Lock-Bit command, sets the permanent lock-bit. After the permanent lock-bit is set, block lock-bits and locked block contents cannot altered. See Table 5 for a summary of hardware and software write protection options.

Set block lock-bit and permanent lock-bit are executed by a two-cycle command sequence. The set block or permanent lock-bit setup along with appropriate block or device address is written followed by either the set block lock-bit confirm (and an address within the block to be locked) or the set permanent lock-bit confirm (and any device address). The WSM then controls the set lock-bit algorithm. After the sequence is written, the device automatically outputs status register data when read (see Figure 10). The CPU can detect the completion of the set lock-bit event by analyzing the RY/#BY pin output or status register bit SR.7.

When the set lock-bit operation is complete, status register bit SR.4 should be checked. If an error is detected, the status register should be cleared. The CUI will remain in read status register mode until a new command is issued.



This two-step sequence of set-up followed by execution ensures that lock-bits are not accidentally set. An invalid Set Block or Permanent Lock-Bit command will result in status register bits SR.4 and SR.5 being set to "1". Also, reliable operations occur only when  $V_{DD} = 2.7V - 3.6V$  and  $V_{PP} = V_{PPH1/2}$ . In the absence of this high voltage, lock-bit contents are protected against alteration.

A successful set block lock-bit operation requires that the permanent lock-bit be cleared. If it is attempted with the permanent lock-bit set, SR.1 and SR.4 will be set to "1" and the operation will fail.

## Clear Block Lock-Bits Command

All set block lock-bits are cleared in parallel via the Clear Block Lock-Bits command. With the permanent lock-bit not set, block lock-bits can be cleared using only the Clear Block Lock-Bits command. If the permanent lock-bit is set, block lock-bits cannot be cleared. See Table 5 for a summary of hardware and software write protection options.

Clear block lock-bits operation is executed by a two-cycle command sequence. A clear block lock-bits setup is first written. After the command is written, the device automatically outputs status register data when read (see Figure 11). The CPU can detect completion of the clear block lock-bits event by analyzing the RY/#BY Pin output or status register bit SR.7.

When the operation is complete, status register bit SR.5 should be checked. If a clear block lock-bit error is detected, the status register should be cleared. The CUI will remain in read status register mode until another command is issued.

This two-step sequence of set-up followed by execution ensures that block lock-bits are not accidentally cleared. An invalid Clear Block Lock-Bits command sequence will result in status register bits SR.4 and SR.5 being set to "1". Also, a reliable clear block lock-bits operation can only occur when  $V_{DD} = 2.7V - 3.6V$  and  $V_{PP} = V_{PPH1/2}$ . If a clear block lock-bits operation is attempted while  $V_{PP}$   $V_{PPLK}$ , SR.3 and SR.5 will be set to "1". In the absence of this high voltage, the block lock-bits content are protected against alteration. A successful clear block lock-bits operation requires that the permanent lock-bit is not set. If it is attempted with the permanent lock-bit set, SR.1 and SR.5 will be set to "1" and the operation will fail.

If a clear block lock-bits operation is aborted due to  $V_{PP}$  or  $V_{DD}$  transitioning out of valid range or #RESET active transition, block lock-bit values are left in an undetermined state. A repeat of clear block lock-bits is required to initialize block lock-bit contents to known values. Once the permanent lock-bit is set, it cannot be cleared.

## Block Locking by the #WP

This Boot Block Flash memory architecture features two hardware-lockable boot blocks so that the kernel code for the system can be kept secure while other blocks are programmed or erased as necessary.

The lockable two boot blocks are locked when #WP =  $V_{IL}$ ; any program or erase operation to a locked block will result in an error, which will be reflected in the status register. For top configuration, the top two boot blocks are lockable. For the bottom configuration, the bottom two boot blocks are lockable. If #WP is  $V_{IH}$  and block lockbit is not set, boot block can be programmed or erased normally (Unless  $V_{PP}$  is below  $V_{PPLK}$ ). #WP is valid only two boot blocks, other blocks are not affected.

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**Table 5. Write Protection Alternatives**

OPERATION	V <sub>PP</sub>	#RESET	PERMANENT LOCK-BIT	BLOCK LOCK-BIT	#WP	EFFECT
Block Erase or Word/Byte Write	≤V <sub>PPLK</sub>	X	X	X	X	All Blocks Locked.
	>V <sub>PPLK</sub>	V <sub>IL</sub>	X	X	X	All Blocks Locked.
		V <sub>IH</sub>	X	0	V <sub>IL</sub>	2 Boot Blocks Locked.
					V <sub>IH</sub>	Block Erase and Word/Byte Write Enabled.
				1	V <sub>IL</sub>	Block Erase and Word/Byte Write Disabled.
					V <sub>IH</sub>	Block Erase and Word/Byte Write Disabled.
Full Chip Erase	≤V <sub>PPLK</sub>	X	X	X	X	All Blocks Locked.
	>V <sub>PPLK</sub>	V <sub>IL</sub>	X	X	X	All Blocks Locked.
		V <sub>IH</sub>	X	X	V <sub>IL</sub>	All Unlocked Blocks are Erased. 2 Boot Blocks and Locked Blocks are NOT Erased.
					V <sub>IH</sub>	All Unlocked Blocks are Erased. Locked Blocks are NOT Erased.
Set Block Lock-Bit	≤V <sub>PPLK</sub>	X	X	X	X	Set Block Lock-Bit Disabled.
	>V <sub>PPLK</sub>	V <sub>IL</sub>	X	X	X	Set Block Lock-Bit Disabled.
		V <sub>IH</sub>	0	X	X	Set Block Lock-Bit Enabled.
			1	X	X	Set Block Lock-Bit Disabled.
Clear Block Lock-Bits	≤V <sub>PPLK</sub>	X	X	X	X	Clear Block Lock-Bits Disabled.
	>V <sub>PPLK</sub>	V <sub>IL</sub>	X	X	X	Clear Block Lock-Bits Disabled.
		V <sub>IH</sub>	0	X	X	Clear Block Lock-Bits Enabled.
			1	X	X	Clear Block Lock-Bits Disabled.
Set Permanent Lock-Bit	≤V <sub>PPLK</sub>	X	X	X	X	Set Permanent Lock-Bit Disabled.
	>V <sub>PPLK</sub>	V <sub>IL</sub>	X	X	X	Set Permanent Lock-Bit Disabled.
		V <sub>IH</sub>	X	X	X	Set Permanent Lock-Bit Enabled.

**Table 6. Status Register Definition**

WSMS	BESS	ECBLBS	WBWSLBS	VPPS	WBWSS	DPS	R
7	6	5	4	3	2	1	0

<p>SR.7 = WRITE STATE MACHINE STATUS (WSMS) 1 = Ready 0 = Busy</p> <p>SR.6 = BLOCK ERASE SUSPEND STATUS (BESS) 1 = Block Erase Suspended 0 = Block Erase in Progress/Completed</p> <p>SR.5 = ERASE AND CLEAR BLOCK LOCK-BITS STATUS (ECBLBS) 1 = Error in Block Erase, Full Chip Erase or Clear Block Lock-Bits 0 = Successful Block Erase, Full Chip Erase or Clear Block Lock-Bits</p> <p>SR.4 = WORD/BYTE WRITE AND SET LOCK-BIT STATUS (WBWSLBS) 1 = Error in Word/Byte Write or Set Block/Permanent Lock-Bit 0 = Successful Word/Byte Write or Set Block/Permanent Lock-Bit</p> <p>SR.3 = VPP STATUS (VPPS) 1 = VPP Low Detect, Operation Abort 0 = VPP OK</p> <p>SR.2 = WORD/BYTE WRITE SUSPEND STATUS (WBWSS) 1 = Word/Byte Write Suspended 0 = Word/Byte Write in Progress/Completed</p> <p>SR.1 = DEVICE PROTECT STATUS (DPS) 1 = Block Lock-Bit, Permanent Lock-Bit and/or #WP Lock Detected, Operation Abort 0 = Unlock</p> <p>SR.0 = RESERVED FOR FUTURE ENHANCEMENTS (R)</p>	<p><b>NOTES:</b></p> <p>Check RY/#BY or SR.7 to determine block erase, full chip erase, word/byte write or lock-bit configuration completion. SR.6-0 are invalid while SR.7 = "0".</p> <p>If both SR.5 and SR.4 are "1"s after a block erase, full chip erase or lock-bit configuration attempt, an improper command sequence was entered.</p> <p>SR.3 does not provide a continuous indication of VPP level. The WSM interrogates and indicates the VPP level only after Block Erase, Full Chip Erase, Word/Byte Write or Lock-Bit Configuration command sequences. SR.3 is not guaranteed to reports accurate feedback only when <math>V_{PPH1/2}</math>.</p> <p>SR.1 does not provide a continuous indication of permanent and block lock-bit and #WP values. The WSM interrogates the permanent lock-bit, block lock-bit and #WP only after Block Erase, Full Chip Erase, Word/Byte Write or Lock-Bit Configuration command sequences. It informs the system, depending on the attempted operation, if the block lock-bit is set, permanent lock-bit is set and/or #WP is VIL. Reading the block lock and permanent lock configuration codes after writing the Read Identifier Codes command indicates permanent and block lock-bit status.</p> <p>SR.0 is reserved for future use and should be masked out when polling the status register.</p>
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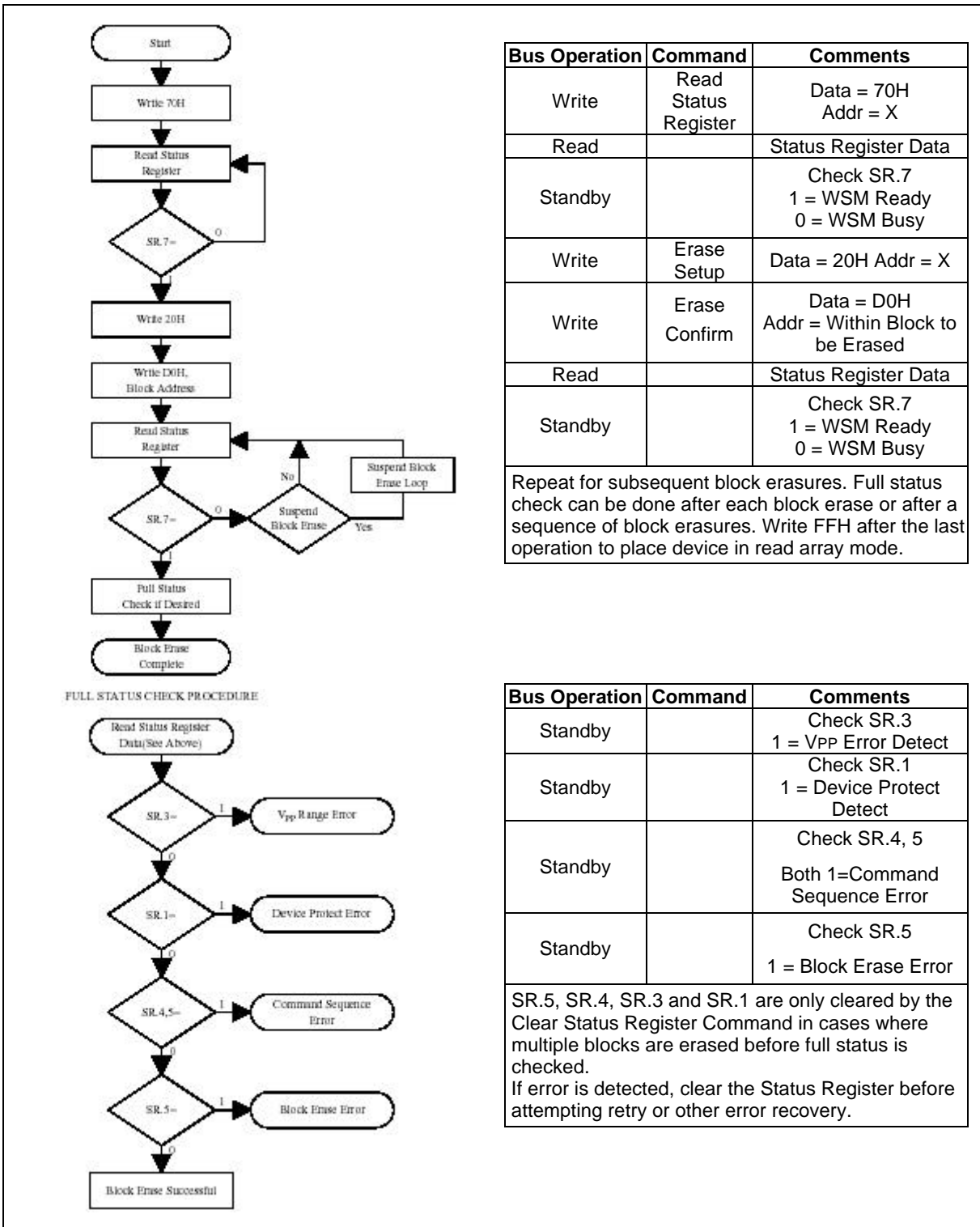


Figure 5. Automated Block Erase Flowchart

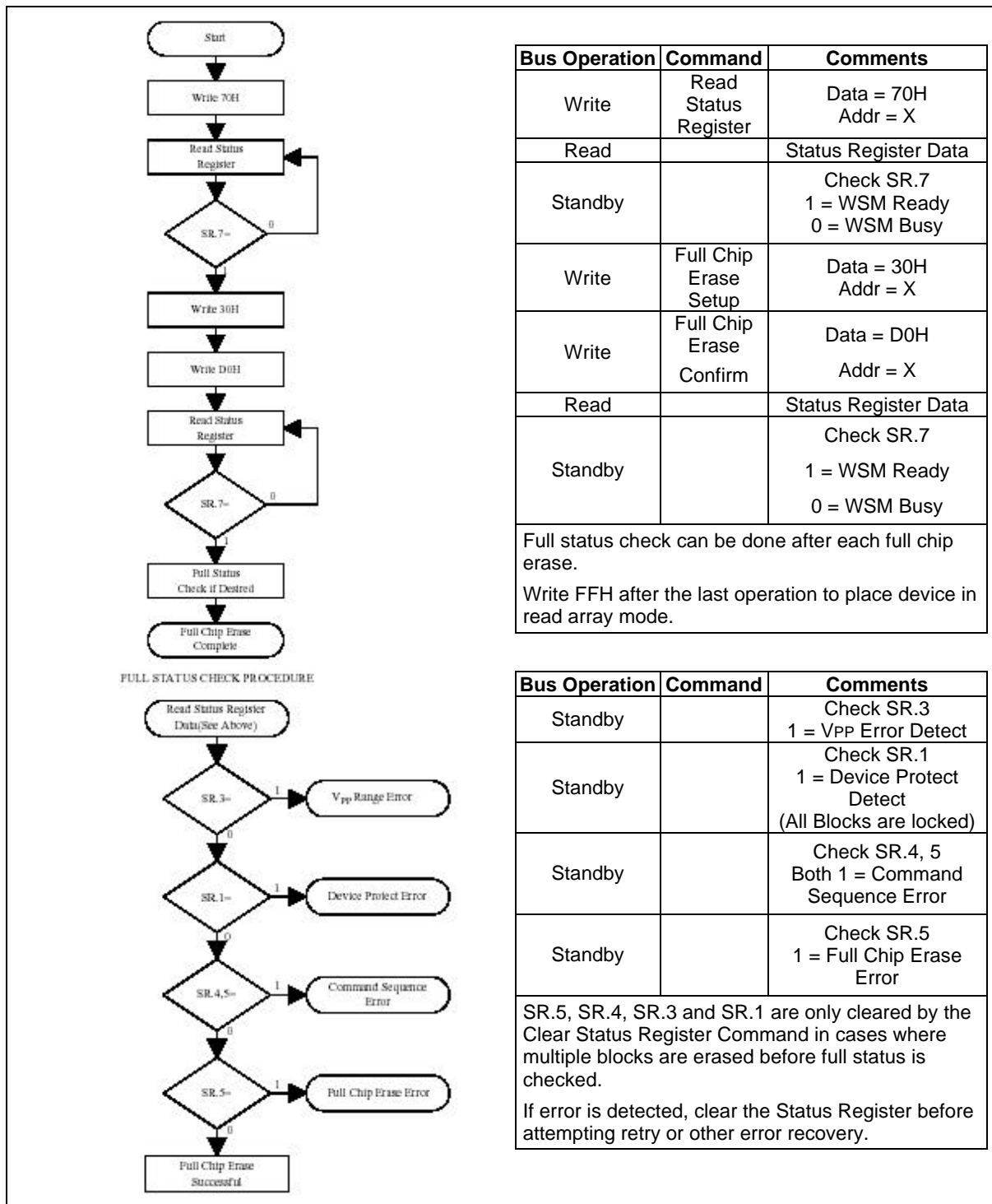


Figure 6. Automated Full Chip Erase Flowchart



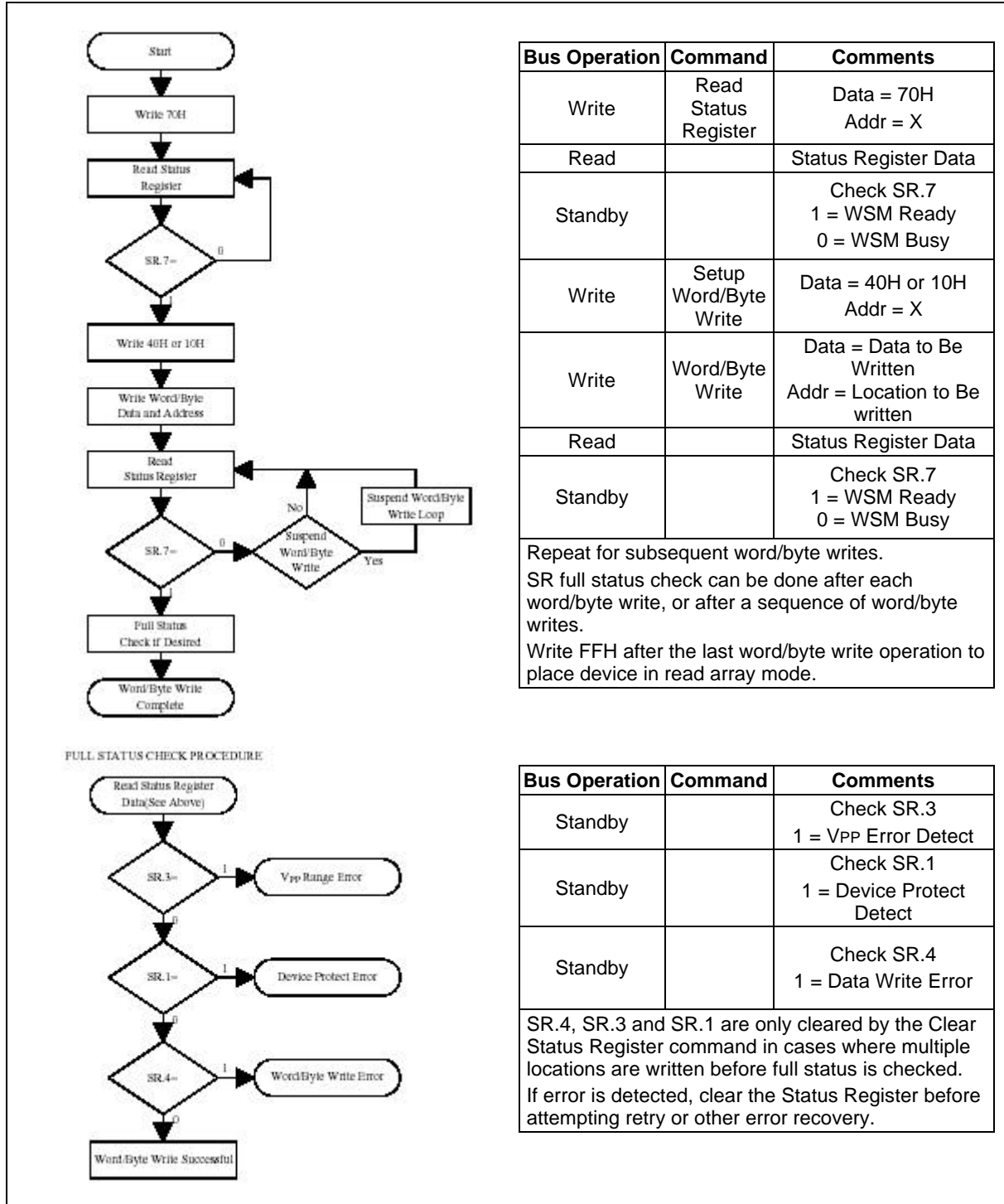


Figure 7. Automated Word/Byte Write Flowchart



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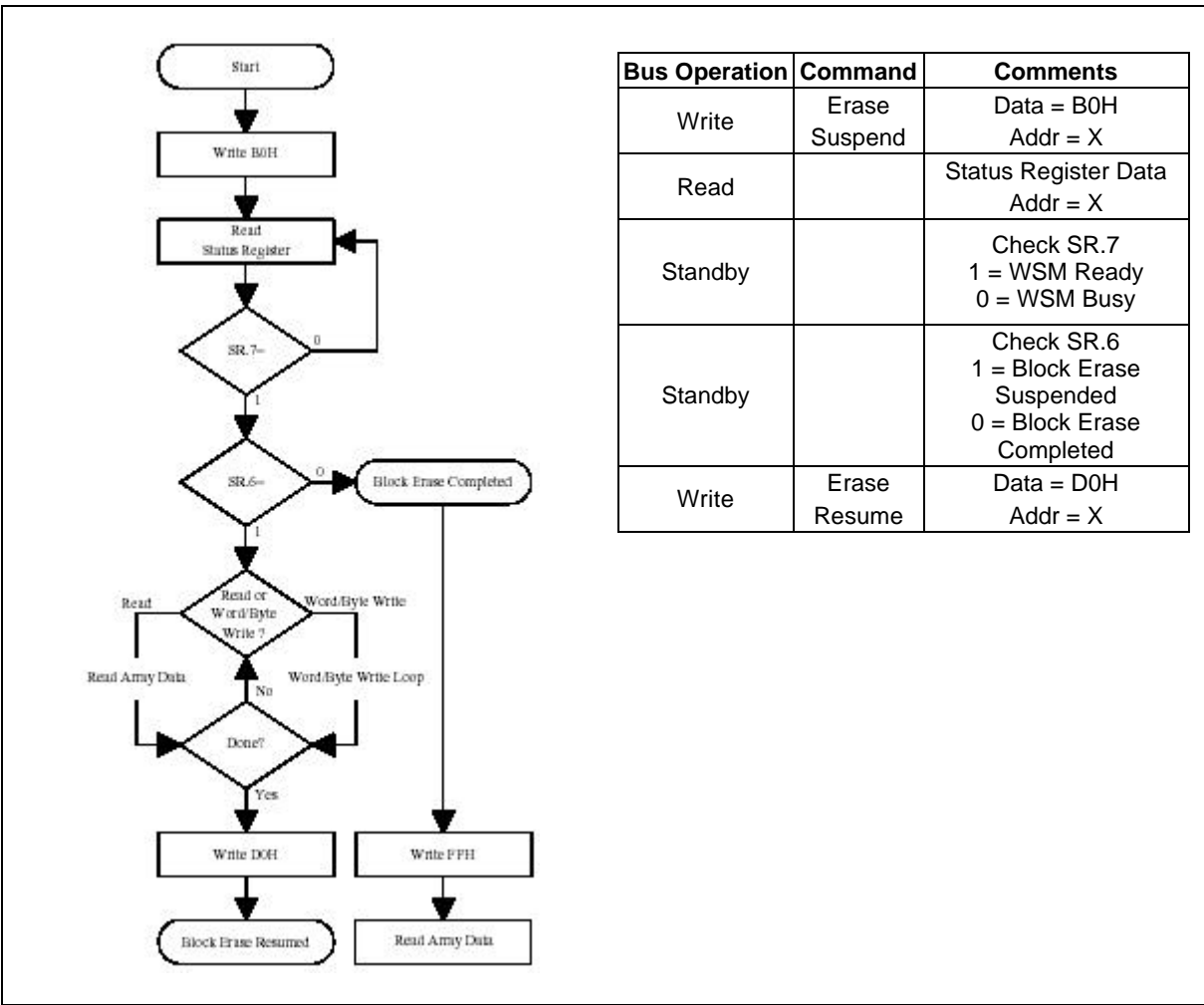


Figure 8. Block Erase Suspend/Resume Flowchart

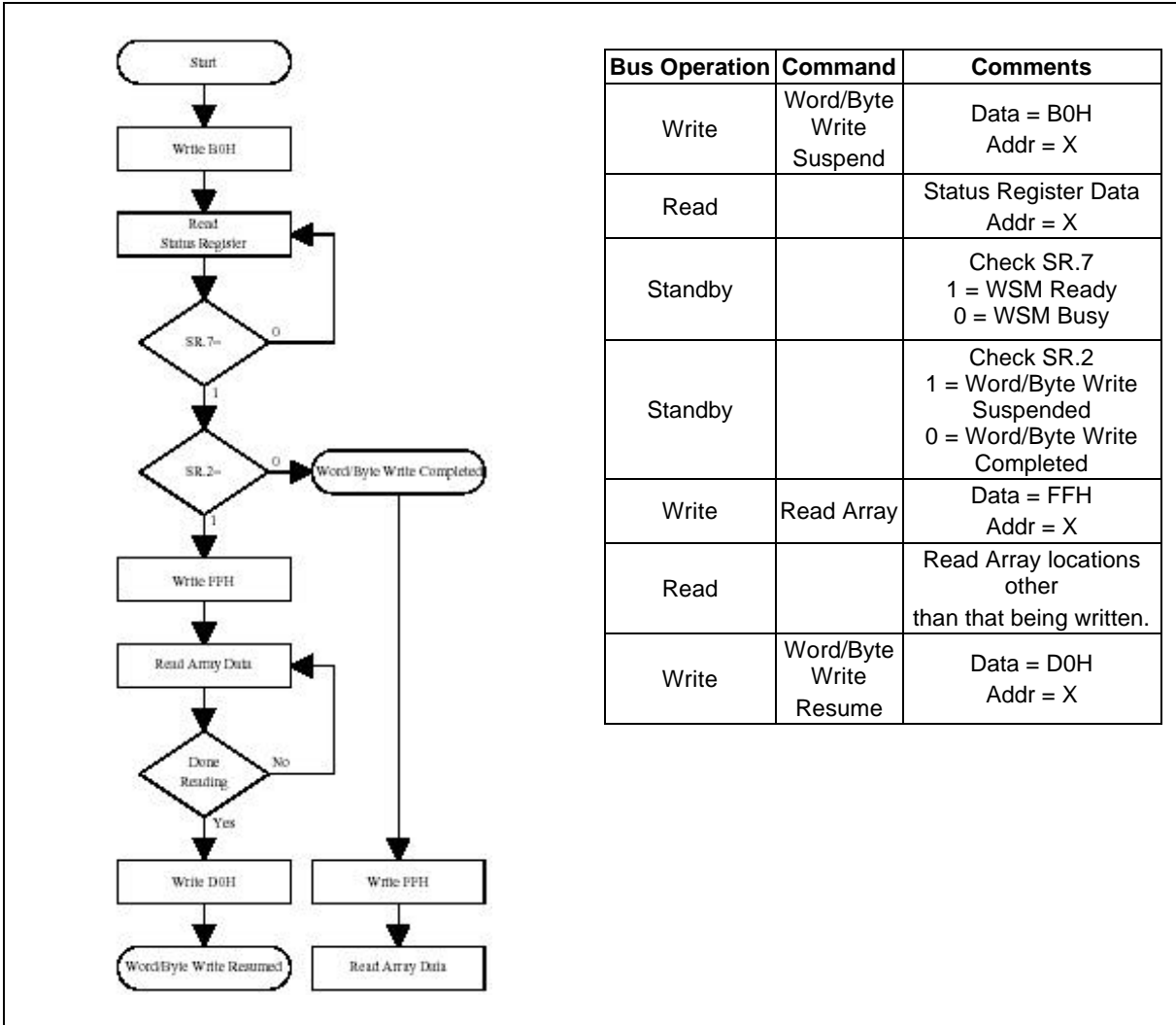


Figure 9. Word/Byte Write Suspend/Resume Flowchart

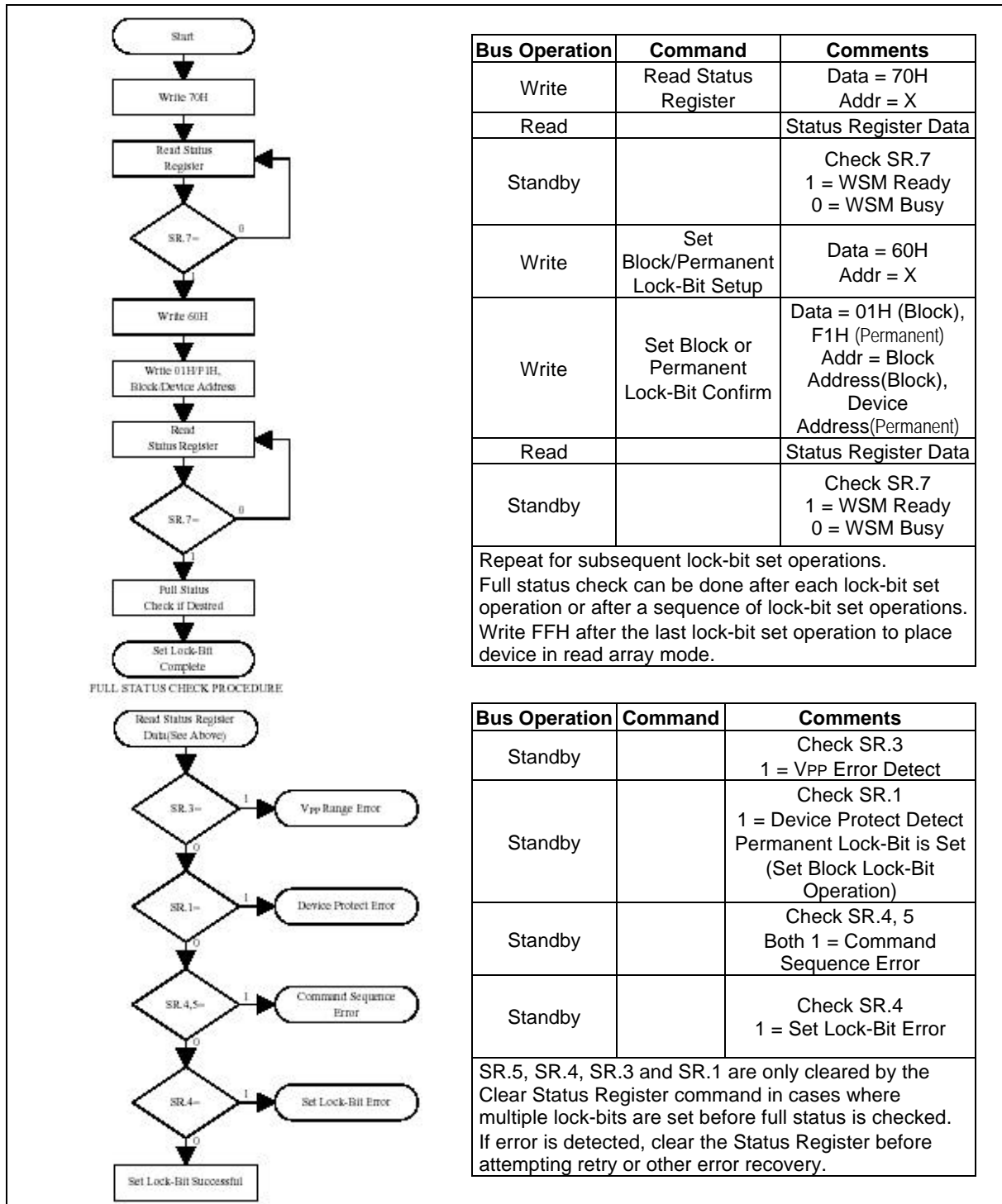
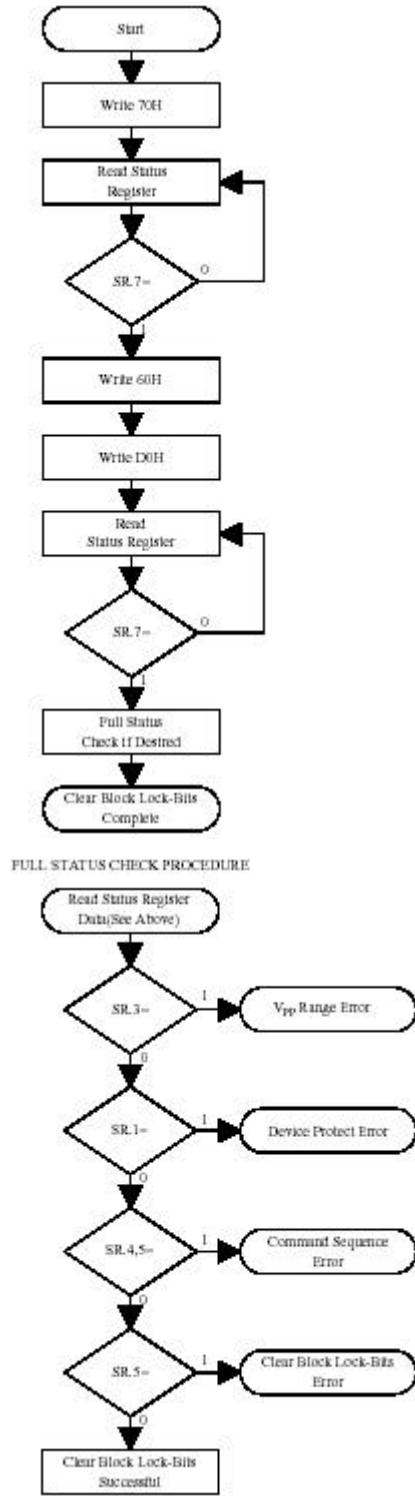


Figure 10. Set Block and Permanent Lock-Bit Flowchart



Bus Operation	Command	Comments
Write	Read Status Register	Data = 70H Addr = X
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Write	Clear Block Lock-Bits Setup	Data = 60H Addr = X
Write	Clear Block Lock-Bits Confirm	Data = D0H Addr = X
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy

Write FFH after the Clear Block Lock-Bits operation to place device in read array mode.

Bus Operation	Command	Comments
Standby		Check SR.3 1 = VPP Error Detect
Standby		Check SR.1 1 = Device Protect Detect Permanent Lock-Bit is Set
Standby		Check SR.4, 5 Both 1=Command Sequence Error
Standby		Check SR.5 1 = Clear Block Lock-Bits Error

SR.5, SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register command. If error is detected, clear the Status Register before attempting retry or other error recovery.

Figure 11. Clear Block Lock-Bits Flowchart



## 10. DESIGN CONSIDERATIONS

### Three-line Output Control

The device will often be used in large memory arrays. WINBOND provides three control inputs to accommodate multiple memory connections. Three-line control provides for:

- a. Lowest possible memory power dissipation.
- b. Complete assurance that data bus contention will not occur.

To use these control inputs efficiently, an address decoder should enable #CE while #OE should be connected to all memory devices and the system's #READ control line. This assures that only selected memory devices have active outputs while deselected memory devices are in standby mode. #RESET should be connected to the system POWERGOOD signal to prevent unintended writes during system power transitions. POWERGOOD should also toggle during system reset.

### RY/#BY and WSM Polling

RY/#BY is an open drain output that should be connected to VDD by a pull up resistor to provides a hardware method of detecting block erase, full chip erase, word/byte write and lock-bit configuration completion. It transitions low after block erase, full chip erase, word/byte write or lockbit configuration commands and returns to VOH (while RY/#BY is pull up) when the WSM has finished executing the internal algorithm.

RY/#BY can be connected to an interrupt input of the system CPU or controller. It is active at all times. RY/#BY is also High Z when the device is in block erase suspend (with word/byte write inactive), word/byte write suspend or reset modes.

### Power Supply Decoupling

Flash memory power switching characteristics require careful device decoupling. System designers are interested in three supply current issues; standby current levels, active current levels and transient peaks produced by falling and rising edges of #CE and #OE. Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks.

Each device should have a 0.1  $\mu$ F ceramic capacitor connected between its VDD and Vss and between its VPP and Vss. These high-frequency, low inductance capacitors should be placed as close as possible to package leads. Additionally, for every eight devices, a 4.7  $\mu$ F electrolytic capacitor should be placed at the array's power supply connection between VDD and Vss. The bulk capacitor will overcome voltage slumps caused by PC board trace inductance.

### VPP Trace on Printed Circuit Boards

Updating flash memories that reside in the target system requires that the printed circuit board designer pay attention to the VPP Power supply trace. The VPP pin supplies the memory cell current for word/byte writing and block erasing. Use similar trace widths and layout considerations given to the VDD power bus. Adequate VPP supply traces and decoupling will decrease VPP voltage spikes and overshoots.

### VDD, VPP, #RESET Transitions

Block erase, full chip erase, word/byte write and lock-bit configuration are not guaranteed if VPP falls outside of a valid VPPH1/2 range, VDD falls outside of a valid 2.7V – 3.6V range, or #RESET  $\neq$  VIH. If



VPP error is detected, status register bit SR.3 is set to "1" along with SR.4 or SR.5, depending on the attempted operation. If #RESET transitions to VIL during block erase, full chip erase, word/byte write or lock-bit configuration, RY/#BY will remain low until the reset operation is complete. Then, the operation will abort and the device will enter reset mode. The aborted operation may leave data partially altered. Therefore, the command sequence must be repeated after normal operation is restored. Device power-off or #RESET transitions to VIL clear the status register.

The CUI latches commands issued by system software and is not altered by VPP or #CE transitions or WSM actions. Its state is read array mode upon power-up, after exit from reset mode or after VDD transitions below VLKO.

## Power-up/Down Protection

The device is designed to offer protection against accidental block erase, full chip erase, word/byte write or lock-bit configuration during power transitions. Upon power-up, the device is indifferent as to which power supply (VPP or VDD) powers-up first. Internal circuitry resets the CUI to read array mode at power-up.

A system designer must guard against spurious writes for VDD voltages above VLKO when VPP is active. Since both #WE and #CE must be low for a command write, driving either to VIH will inhibit writes. The CUI's two step command sequence architecture provides added level of protection against data alteration.

In-system block lock and unlock capability prevents inadvertent data alteration. The device is disabled while #RESET = VIL regardless of its control inputs state.

## Power Dissipation

When designing portable systems, designers must consider battery power consumption not only during device operation, but also for data retention during system idle time. Flash memory's nonvolatility increases usable battery life because data is retained when system power is removed.

## Data Protection Method

Noises having a level exceeding the limit specified in the specification may be generated under specific operating conditions on some systems. Such noises, when induced onto #WE signal or power supply, may be interpreted as false commands, causing undesired memory updating. To protect the data stored in the flash memory against unwanted overwriting, systems operating with the flash memory should have the following write protect designs, as appropriate:

### 1) Protecting data in specific block

When a lock bit is set, the corresponding block (includes the 2 boot blocks) is protected against overwriting. By setting a #WP to low, only the 2 boot blocks can be protected against overwriting. By using this feature, the flash memory space can be divided into the program section (locked section) and data section (unlocked section). The permanent lock bit can be used to prevent false block bit setting. For further information on setting/resetting lock-bit, refer to the specification.

### 2) Data protection through VPP

When the level of VPP is lower than VPPLK (lockout voltage), write operation on the flash memory is disabled. All blocks are locked and the data in the blocks are completely write protected. For the lockout voltage, refer to the specification.

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## 3) Data protection through #RESET

When the #RESET is kept low during read mode, the flash memory will be reset mode, then write protecting all blocks. When the #RESET is kept low during power up and power down sequence such as voltage transition, write operation on the flash memory is disabled, write protecting all blocks. For the details of #RESET control, refer to the specification.

## 11. ELECTRICAL SPECIFICATIONS

### Absolute Maximum Ratings\*

Operating Temperature	
During Read, Block Erase, Full Chip Erase, Word/Byte Write	
and Lock-Bit Configuration .....	-40 to +85° C (1)
.....	0 to +70° C (1)
Storage Temperature	
During under Bias .....	
During non Bias .....	
Voltage On Any Pin	
(except VDD and VPP) .....	
VDD Supply Voltage.....	
VPP Supply Voltage.....	
Output Short Circuit Current.....	

*\*WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

#### Notes:

1. -40 to +85° C operating temperature is for extended temperature product defined by this specification.  
(for W28J160BT/TT90C)  
0 to +70° C operating temperature is for commercial temperature product defined by this specification.  
(for W28J160BT/TT90L)
2. All specified voltages are with respect to Vss. Minimum DC voltage is -0.5V on input/output pins and -0.2V on VDD and VPP pins. During transitions, this level may undershoot to -2.0V for periods <20 nS. Maximum DC voltage on input/output pins are VDD +0.5V which, during transitions, may overshoot to VDD +2.0V for periods <20 nS.
3. Maximum DC voltage on VPP may overshoot to +13.0V for periods <20 nS. Applying 12V ±0.3V to VPP during erase/write can only be done for a maximum of 1000 cycles on each block. VPP may be connected to 12V ±0.3V for a total of 80 hours maximum.
4. Output shorted for no more than one second. No more than one output shorted at a time.

## Operating Conditions

### Temperature and VDD Operating Conditions

SYMBOL	PARAMETER		MIN.	MAX.	UNIT	TEST CONDITION
TA	Operating Temperature	W28J160BT/TT90C	0	+70	°C	Ambient Temperature
		W28J160BT/TT90L	-40	+85		
VDD	VDD Supply Voltage (2.7V – 3.6V)		2.7	3.6	V	

## Capacitance(1)

$T_A = +25^\circ\text{C}$ ,  $f = 1\text{ MHz}$

PARAMETER	SYMBOL	TYP.	MAX.	UNIT	CONDITION
Input Capacitance	$C_{IN}$	7	10	pF	$V_{IN} = 0.0\text{V}$
Output Capacitance	$C_{OUT}$	9	12	pF	$V_{OUT} = 0.0\text{V}$

Note: Sampled, not 100% tested.

## AC Input/Output Test Conditions

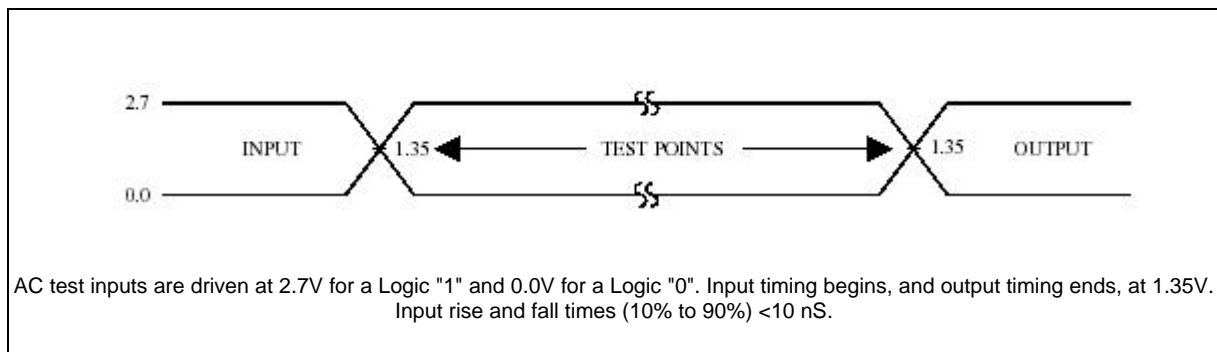


Figure 12. Transient Input/Output Reference Waveform for  $V_{DD} = 2.7\text{V} - 3.6\text{V}$

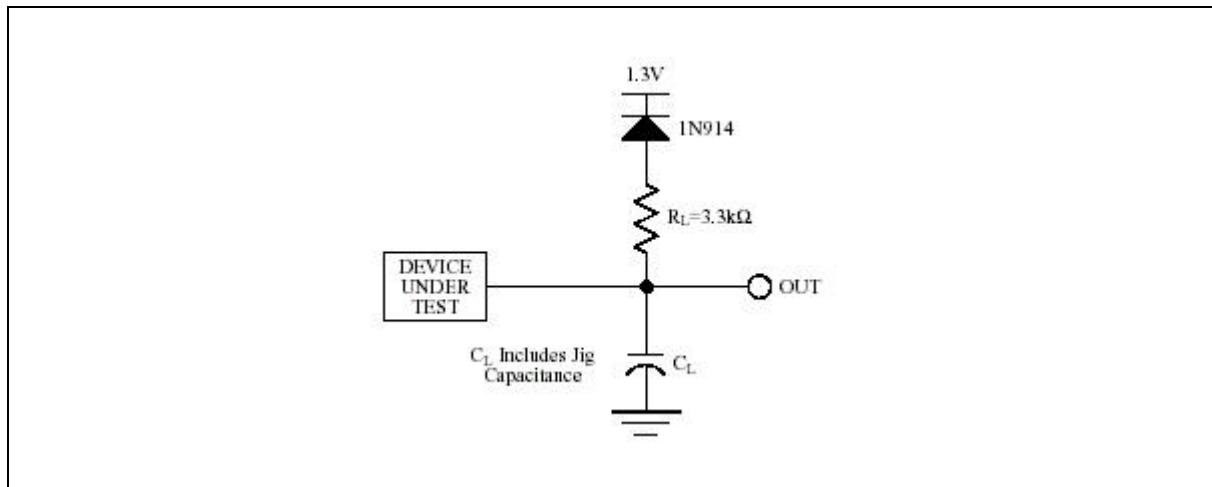


Figure 13. Transient Equivalent Testing Load Circuit

## Test Configuration Capacitance Loading Value

Test Configuration	$C_L(\text{pF})$
$V_{DD} = 2.7\text{V} - 3.6\text{V}$	50



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## DC Characteristics

PARAMETER	SYM.	TEST CONDITIONS	VDD = 2.7V - 3.6V		UNIT
			Typ.	Max.	
Input Load Current (note1)	ILI	VDD = VDD Max. VIN = VDD or Vss		±0.5	μA
Output Leakage Current (note 1)	ILO	VDD = VDD Max. VOUT = VDD or Vss		±0.5	μA
VDD Standby Current (note 1, 3, 6)	ICCS	CMOS Level Inputs VDD = VDD Max. #CE = #RESET = VDD ±0.2V	2	15	μA
		TTL Level Inputs VDD = VDD Max. #CE = #RESET = VIH	0.2	2	mA
VDD Auto Power-Save Current (note 1, 5, 6)	ICCAS	CMOS Level Inputs VDD = VDD Max. #CE = Vss ±0.2V	2	15	μA
VDD Reset Power-Down Current (note 1)	ICCD	#RESET = Vss ±0.2V IOUT(RY/#BY) = 0 mA CMOS Level Inputs	2	15	μA
VDD Read Current (note 1, 6)	ICCR	VDD = VDD Max., #CE = Vss, f = 5 MHz, IOUT = 0 mA	15	25	mA
		TTL Level Inputs VDD = VDD Max., #CE = Vss, f = 5 MHz, IOUT = 0 mA		30	mA
VDD Word/Byte Write or Set Lock- Bit Current (note 1, 7)	ICCW	VPP = 2.7V - 3.6V	5	17	mA
		VPP = 11.7V - 12.3V	5	12	mA
VDD Block Erase, Full Chip Erase or Clear Block Lock-Bits Current (note 1, 7)	ICCE	VPP = 2.7V - 3.6V	4	17	mA
		VPP = 11.7V - 12.3V	4	12	mA
VDD Word/Byte Write or Block Erase Suspend Current (note 1, 2)	ICCWS ICCES	#CE = VIH	1	6	mA
VPP Standby or Read Current (note 1)	ICCWS ICCW	VPP ≤ VDD	±2	±15	μA
		VPP > VDD	10	200	μA
VPP Auto Power-Save Current (note 1, 5, 6)	ICCWAS	CMOS Level Inputs VDD = VDD Max. #CE = Vss ±0.2V	0.1	5	μA
VPP Reset Power-Down Current (note1)	ICPWD	#RESET = Vss ±0.2V	0.1	5	μA
VPP Word/Byte Write or Set Lock- Bit Current (note 1, 7)	ICCW	VPP = 2.7V - 3.6V	12	40	mA
		VPP = 11.7V - 12.3V		30	mA
VPP Block Erase, Full Chip Erase or Clear Block Lock-Bits Current (note 1, 7)	ICCWE	VPP = 2.7V - 3.6V	8	25	mA
		VPP = 11.7V - 12.3V		20	mA
VPP Word/Byte Write or Block Erase Suspend Current (note 1)	ICCWWS ICCWES	VPP = VPPH1/2	10	200	μA

DC Characteristics (Continued)

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PARAMETER	SYM.	TEST CONDITIONS	VDD = 2.7V - 3.6V		UNIT
			Min.	Max.	
Input Low Voltage (note7)	V <sub>IL</sub>		-0.5	0.8	V
Input High Voltage (note7)	V <sub>IH</sub>		2.0	VDD +0.5	V
Output Low Voltage (note 3,7)	V <sub>OL</sub>	VDD = VDD Min. I <sub>OL</sub> = 2.0 mA		0.4	V
Output High Voltage (TTL) (note 7)	V <sub>OH1</sub>	VDD = VDD Min. I <sub>OH</sub> = -2.0 mA	2.4		V
Output High Voltage (CMOS) (note 7)	V <sub>OH2</sub>	VDD = VDD Min. I <sub>OH</sub> = -2.5 mA	0.85 VDD		V
			VDD -0.4		V
VPP Lockout during Normal Operations (note 4, 7)	V <sub>PPLK</sub>	VDD = VDD Min. I <sub>OH</sub> = -100 $\mu$ A		1.0	V
VPP during Block Erase, Full Chip Erase, Word/Byte Write or Lock-Bit Configuration Operations	V <sub>PPH1</sub>		2.7	3.6	V
VPP during Block Erase, Full Chip Erase, Word/Byte Write or Lock-Bit Configuration Operations (note 8)	V <sub>PPH2</sub>		11.7	12.3	V
VDD Lockout Voltage	V <sub>LKO</sub>		2.0		V

## Notes:

1. All currents are in RMS unless otherwise noted. Typical values at nominal VDD voltage and TA = +25° C.
2. ICCWS and ICCES are specified with the device de-selected. If read or word/byte written while in erase suspend mode, the device's current draw is the sum of ICCWS or ICCES and ICCR or ICCW, respectively.
3. Includes RY/#BY.
4. Block erases, full chip erase, word/byte writes and lock-bit configurations are inhibited when VPP = V<sub>PPLK</sub>, and not guaranteed in the range between V<sub>PPLK</sub> (max.) and V<sub>PPH1</sub> (min.), between V<sub>PPH1</sub> (max.) and V<sub>PPH2</sub> (min.) and above V<sub>PPH2</sub> (max.).
5. The Automatic Power Savings (APS) feature is placed automatically power save mode that addresses not switching more than 300 nS while read mode.
6. About all of pin except describe Test Conditions, CMOS level inputs are either VDD  $\pm$ 0.2V or Vss  $\pm$ 0.2V, TTL level inputs are either V<sub>IL</sub> or V<sub>IH</sub>.
7. Sampled, not 100% tested.
8. Applying 12V  $\pm$ 0.3V to VPP during erase/write can only be done for a maximum of 1000 cycles on each block. VPP may be connected to 12V  $\pm$ 0.3V for a total of 80 hours maximum.

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## AC Characteristics - Read-only Operations(1)

V<sub>DD</sub> = 2.7V – 3.6V, T<sub>A</sub> = 0 to +70° C for W28J160BT/TT90L; T<sub>A</sub> = -40 to +85° C for W28J160BT/TT90C

PARAMETER	SYM.	T <sub>A</sub> = 0 to +70° C		T <sub>A</sub> = -40 to +85° C		UNIT
		Min.	Max.	Min.	Max.	
Read Cycle Time	tAVAV	90		90		nS
Address to Output Delay	tAVQV		90		90	nS
#CE to Output Delay (note 2)	tELQV		90		90	nS
#RESET High to Output Delay	tPHQV		600		600	nS
#OE to Output Delay (note 2)	tGLQV		40		50	nS
#CE to Output in Low Z (note 3)	tELQX	0		0		nS
#CE High to Output in High Z (note 3)	tEHQZ		40		55	nS
#OE to Output in Low Z (note 3)	tGLQX	0		0		nS
#OE High to Output in High Z (note 3)	tGHQZ		15		20	nS
Output Hold from Address, #CE or #OE Change, Whichever Occurs First (note 3)	tOH	0		0		nS
#BYTE to Output Delay (note3)	tFVQV		90		90	nS
#BYTE Low to Output in High Z (note 3)	tFLQZ		25		30	nS
#CE to #BYTE High or Low (note 3, 4)	tELFV		5		5	nS

Notes:

1. See AC Input/Output Reference Waveform for maximum allowable input slew rate.
2. #OE may be delayed up to tELQV – tGLQV after the falling edge of #CE without impact on tELQV.
3. Sampled, not 100% tested.
4. If #BYTE transfer during reading cycle, exist the regulations separately.

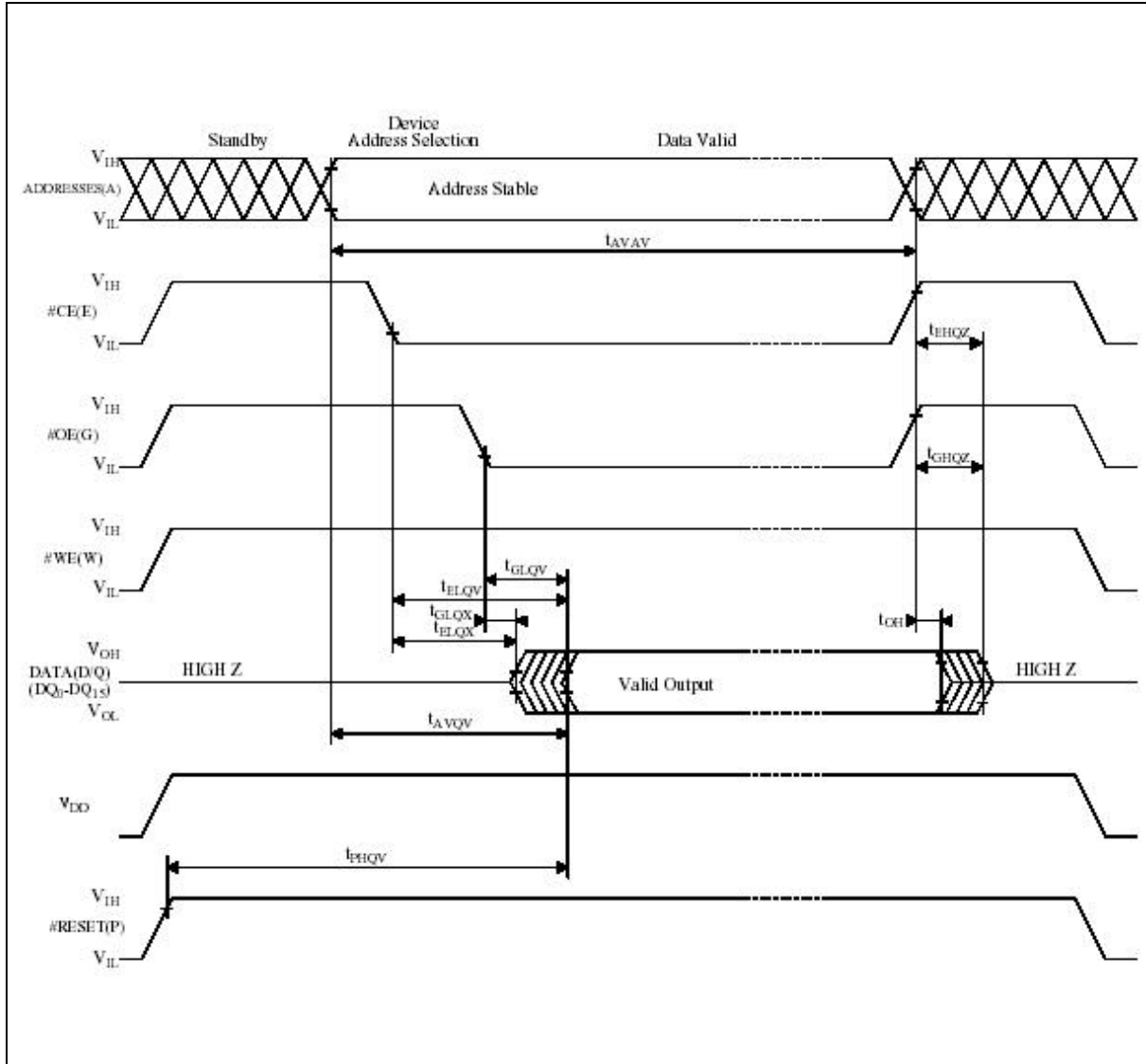


Figure 14. AC Waveform for Read Operations

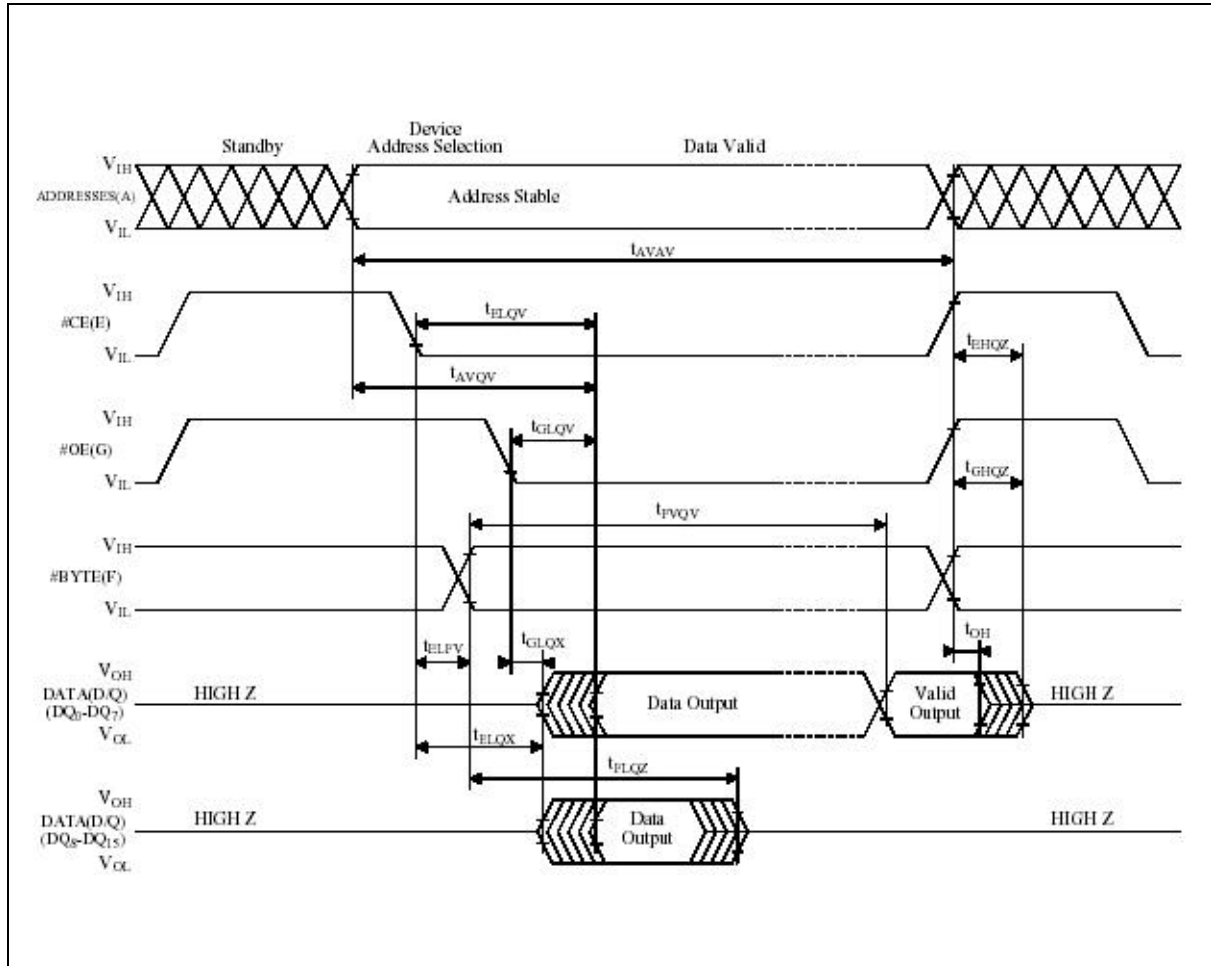


Figure 15. #BYTE Timing Waveform

# Preliminary W28J160B/T



## AC Characteristics - Write Operations(1)

V<sub>DD</sub> = 2.7V – 3.6V, T<sub>A</sub> = 0 to +70° C for W28J160BT/TT90L; T<sub>A</sub> = -40 to +85° C for W28J160BT/TT90C

PARAMETER	SYM.	MIN.	MAX.	UNIT
Write Cycle Time	tAVAV	90		nS
#RESET High Recovery to #WE Going Low (note 2)	tPHWL	1		μS
#CE Setup to #WE Going Low	tELWL	10		nS
#WE Pulse Width	tWLWH	50		nS
#WPVIH Setup to #WE Going High (note 2)	tSHWH	100		nS
VPP Setup to #WE Going High (note 2)	tVPWH	100		nS
Address Setup to #WE Going High (note 3)	tAVWH	50		nS
Data Setup to #WE Going High (note 3)	tDVWH	50		nS
Data Hold from #WE High	tWHDX	0		nS
Address Hold from #WE High	tWHAX	0		nS
#CE Hold from #WE High	tWHEH	10		nS
#WE Pulse Width High	tWHWL	30		nS
#WE High to RY/#BY Going Low or SR.7 Going "0"	tWHRL		100	nS
Write Recovery before Read	tWHGL	0		nS
VPP Hold from Valid SRD, RY/#BY High Z (note 2, 4)	tQVVL	0		nS
#WP VIH Hold from Valid SRD, RY/#BY High Z (note 2, 4)	tQVSL	0		nS
#BYTE Setup to #WE Going High (note 5)	tFVWH	50		nS
#BYTE Hold from #WE High (note 5)	tWHFV	90		nS

Notes:

1. Read timing characteristics during block erase, full chip erase, word/byte write and lock-bit configuration operations are the same as during read-only operations. Refer to AC Characteristics for read-only operations.
2. Sampled, not 100% tested.
3. Refer to Table 4 for valid AIN and DIN for block erase, full chip erase, word/byte write or lock-bit configuration.
4. VPP should be held at VPPH1/2 until determination of block erase, full chip erase, word/byte write or lock-bit configuration success (SR.1/3/4/5 = 0).
5. If #BYTE switch during reading cycle, exist the regulations separately.

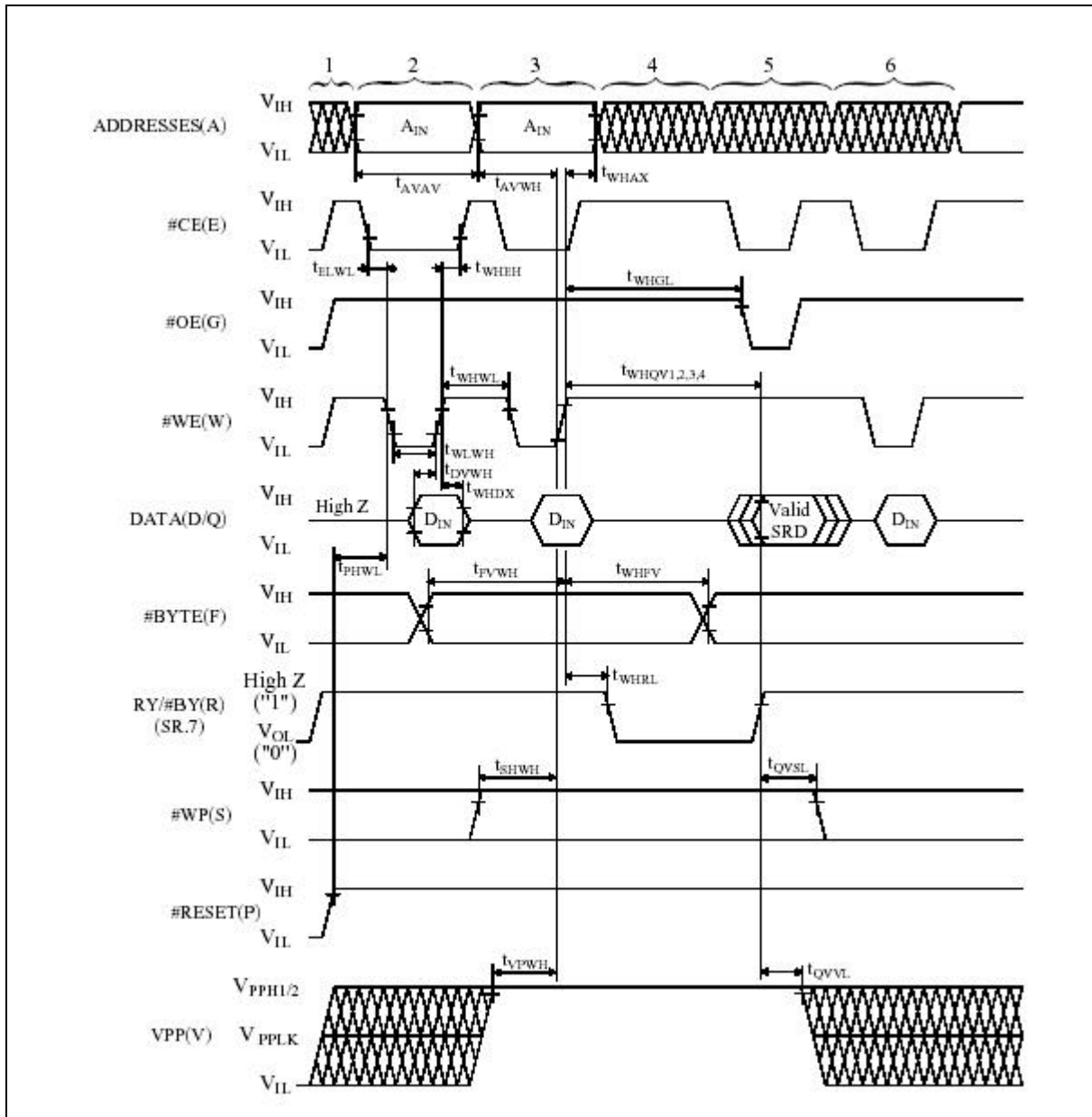


Figure 16. AC Waveform for #WE-Controlled Write Operations

Notes:

1. VDD power-up and standby.
2. Write each setup command.
3. Write each confirm command or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. Write Read Array command.

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## Alternative #CE-Controlled Writes(1)

V<sub>DD</sub> = 2.7V – 3.6V, T<sub>A</sub> = 0 to +70° C for W28J160BT/TT90L; T<sub>A</sub> = -40 to +85° C for W28J160BT/TT90C

PARAMETER	SYM.	MIN.	MAX.	UNIT
Write Cycle Time	tAVAV	90		nS
#RESET High Recovery to #CE Going Low (note 2)	tPHEL	1		μS
#WE Setup to #CE Going Low	tWLEL	0		nS
#CE Pulse Width	tELEH	65		nS
#WPVIH Setup to #CE Going High (note 2)	tSHEH	100		nS
V <sub>PP</sub> Setup to #CE Going High (note 2)	tVPEH	100		nS
Address Setup to #CE Going High (note 3)	tAVEH	50		nS
Data Setup to #CE Going High (note 3)	tDVEH	50		nS
Data Hold from #CE High	tEHDH	0		nS
Address Hold from #CE High	tEHAX	0		nS
#WE Hold from #CE High	tEHWL	0		nS
#CE Pulse Width High	tEHEL	25		nS
#CE High to RY/#BY Going Low or SR.7 Going "0"	tEHRL		100	nS
Write Recovery before Read	tEHGL	0		nS
V <sub>PP</sub> Hold from Valid SRD, RY/#BY High Z (note 2, 4)	tQVVL	0		nS
#WP VIH Hold from Valid SRD, RY/#BY High Z (note 2, 4)	tQVSL	0		nS
#BYTE Setup to #CE Going High (note 5)	tFVEH	50		nS
#BYTE Hold from #CE High (note 5)	tEHFV	90		nS

Notes:

1. In systems where #CE defines the write pulse width (within a longer #WE timing waveform), all setup, hold, and inactive #WE times should be measured relative to the #CE waveform.
2. Sampled, not 100% tested.
3. Refer to Table 4 for valid AIN and DIN for block erase, full chip erase, word/byte write or lock-bit configuration.
4. V<sub>PP</sub> should be held at V<sub>PPH1/2</sub> until determination of block erase, full chip erase, word/byte write or lock-bit configuration success (SR.1/3/4/5 = 0).
5. If #BYTE switch during reading cycle, exist the regulations separately.



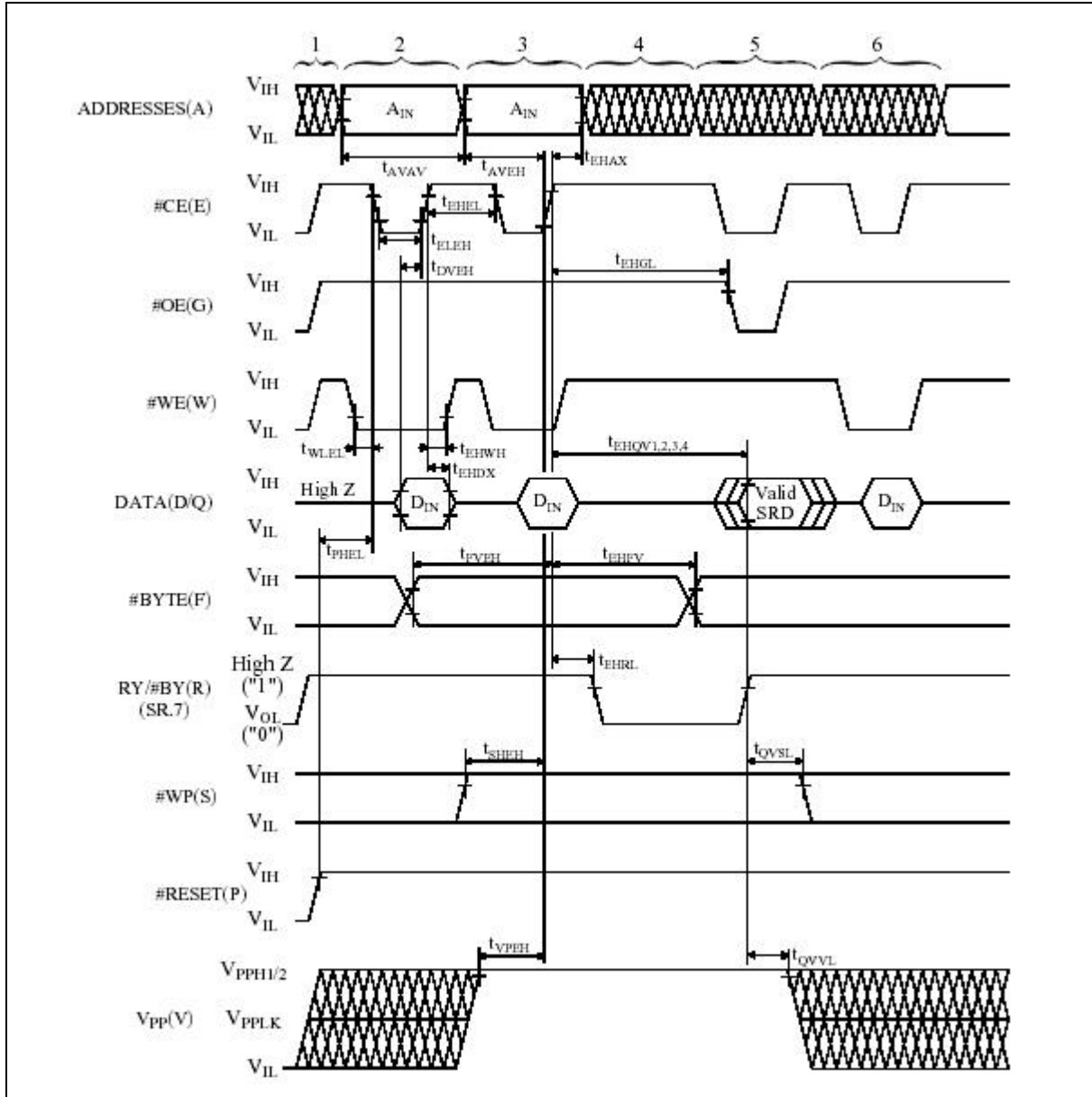


Figure 17. AC Waveform for #CE-Controlled Write Operations

Notes:

1. VDD power-up and standby.
2. Write each setup command.
3. Write each confirm command or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. Write Read Array command.

## Reset Operations

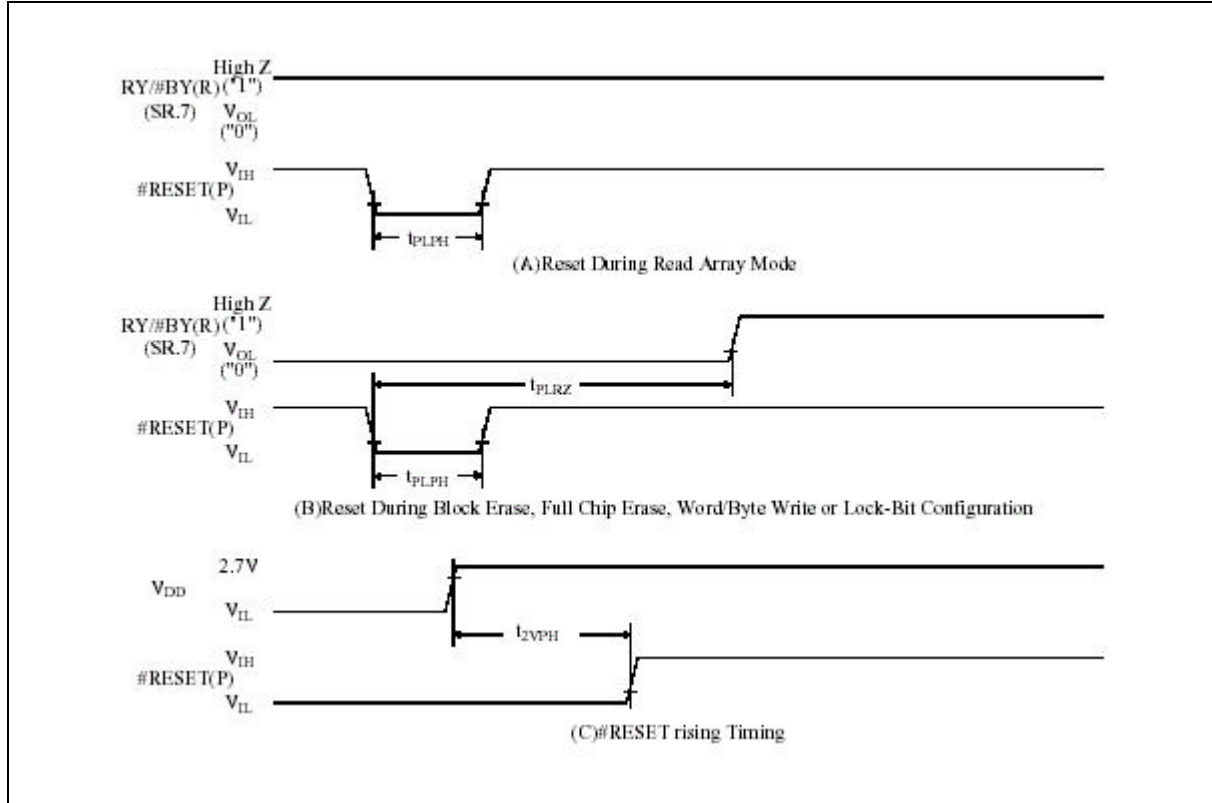


Figure 18. AC Waveform for Reset Operation

## Reset AC Specifications

PARAMETER	SYM.	MIN.	MAX.	UNIT
#RESET Pulse Low Time (note 2)	t <sub>PLPH</sub>	100		nS
#RESET Low to Reset during Block Erase, Full Chip Erase, Word/Byte Write or Lock-Bit Configuration (note 1, 2)	t <sub>PLRZ</sub>		30	μS
V <sub>DD</sub> 2.7V to #RESET High (note 2, 3)	t <sub>2VPH</sub>	100		nS

### Notes:

1. If #RESET is asserted while a block erase, full chip erase, word/byte write or lock-bit configuration operation is not executing, the reset will complete within 100 nS.
2. A reset time, t<sub>PHQV</sub>, is required from the later of RY/#BY(SR.7) going High Z("1") or #RESET going high until outputs are valid. Refer to AC Characteristics - Read-Only Operations for t<sub>PHQV</sub>.
3. When the device power-up, holding #RESET low minimum 100ns is required after V<sub>DD</sub> has been in predefined range and also has been in stable there.

# Preliminary W28J160B/T



## Block Erase, Full Chip Erase, Word/Byte Write And Lock-Bit Configuration Performance(3)

V<sub>DD</sub> = 2.7V – 3.6V, T<sub>A</sub> = 0 to +70° C for W28J160BT/TT90L; T<sub>A</sub> = -40 to +85° C for W28J160BT/TT90C

SYMBOL	PARAMETER		NOTES	V <sub>PP</sub> = 2.7V – 3.6V		V <sub>PP</sub> = 11.7V – 12.3V		UNIT
				Typ.(1)	Max.	Typ.(1)	Max.	
t <sub>WHQV1</sub> t <sub>EHQV1</sub>	Word Write Time	32K word Block	2	33	200	20		μS
		4K word Block	2	36	200	27		μS
	Byte Write Time	64K byte Block	2	31	200	19		μS
		8K byte Block	2	32	200	26		μS
	Block Write Time (In word mode)	32K word Block	2	1.1	4	0.66		S
		4K word Block	2	0.15	0.5	0.12		S
	Block Write Time (In byte mode)	64K byte Block	2	2.2	7	1.4		S
		8K byte Block	2	0.3	1	0.25		S
t <sub>WHQV2</sub> t <sub>EHQV2</sub>	Block Erase Time	32K word Block 64K byte Block	2	1.2	6	0.9		S
		4K word Block 8K byte Block	2	0.6	5	0.5		S
	Full Chip Erase Time	T <sub>A</sub> = 0 to +70° C	2	42	210	32		S
		T <sub>A</sub> = -40 to +85° C	2	22.8	114	17.5		
t <sub>WHQV3</sub> t <sub>EHQV3</sub>	Set Lock-Bit Time		2	56	200	42		μS
t <sub>WHQV4</sub> t <sub>EHQV4</sub>	Clear Block Lock-Bits Time		2	1	5	0.69		S
t <sub>WHRZ1</sub> t <sub>EHRZ1</sub>	Word/Byte Write Suspend Latency Time to Read		4	6	15	6	15	μS
t <sub>WHRZ2</sub> t <sub>EHRZ2</sub>	Block Erase Suspend Latency Time to Read		4	16	30	16	30	μS

Notes:

1. Typical values measured at T<sub>A</sub> = +25 C and V<sub>DD</sub> = 3.0V, V<sub>PP</sub> = 3.0V or 12.0V. Assumes corresponding lock-bits are not set. Subject to change based on device characterization.
2. Excludes system-level overhead.
3. Sampled but not 100% tested.
4. A latency time is required from issuing suspend command(#WE or #CE going high) until RY/#BY going High Z or SR.7 going "1".

## 12. ADDITIONAL INFORMATION

### Block Erase Suspend and Resume Command

If the time between writing the Block Erase Resume command and writing the Block Erase Suspend command is shorter than 15ms and both commands are written repeatedly, a longer time is required than standard block erase until the completion of the operation.

### Recommended Operating Conditions

#### At Device Power-up

AC timing illustrated in Figure 19 is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.

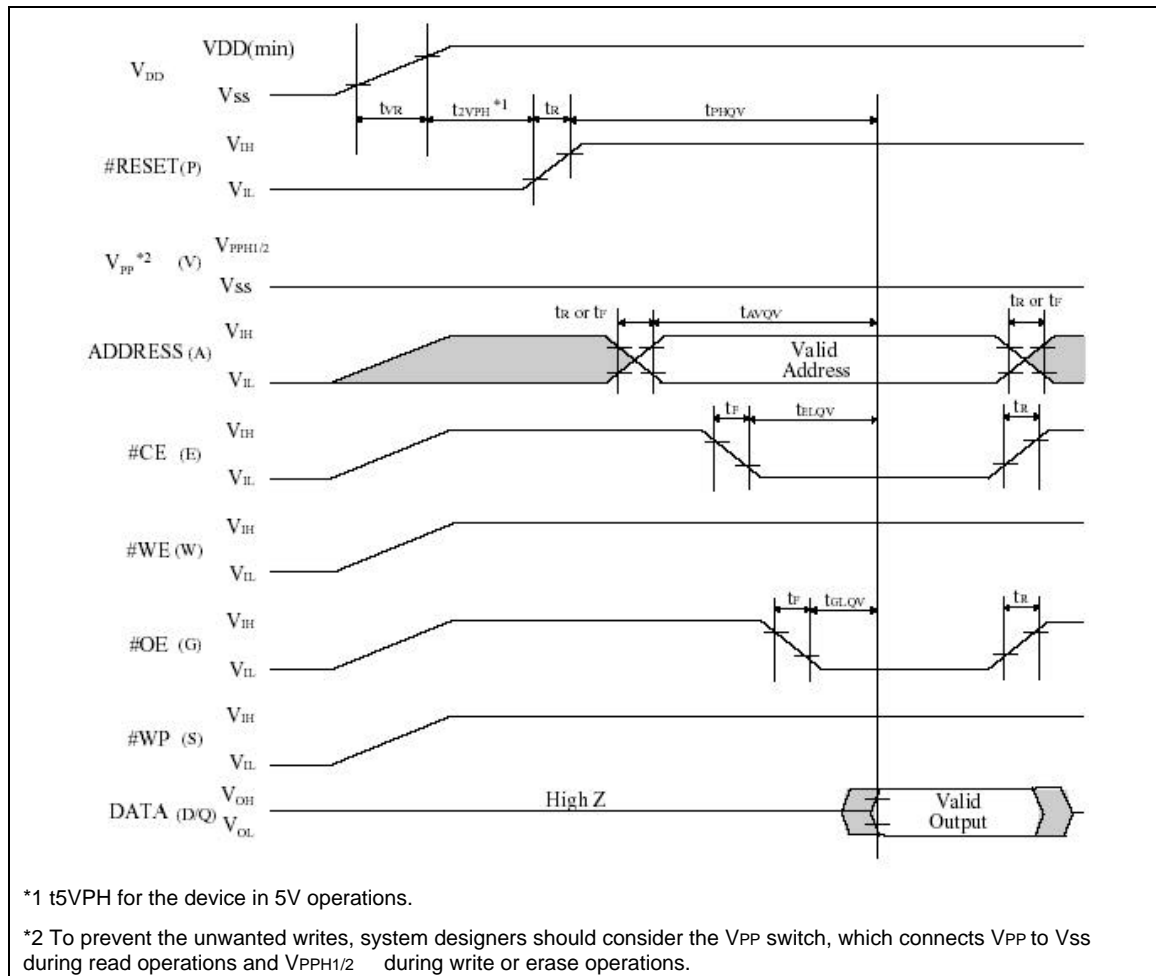


Figure 19. AC Timing at Device Power-up

For the AC specifications  $t_{VR}$ ,  $t_R$ ,  $t_F$  in the figure, refer to the next page. See the "ELECTRICAL SPECIFICATIONS" described in specifications for the supply voltage range, the operating temperature and the AC specifications not shown in the next page.

## Rise and Fall Time

PARAMETER		SYMBOL	MIN.	MAX.	UNIT
V <sub>DD</sub> Rise Time (note 1)		t <sub>VR</sub>	0.5	30000	μS/ V
Input Signal	Rise Time (note 1, 2)	t <sub>R</sub>		1	μS/ V
Input Signal	Fall Time (note 1, 2)	t <sub>F</sub>		1	μS/ V

Notes:

1. Sampled, not 100% tested.
2. This specification is applied for not only the device power-up but also the normal operations. t<sub>R</sub>(Max.) and t<sub>F</sub>(Max.) for #RESET are 50 μS/V

## Glitch Noises

Do not input the glitch noises which are below V<sub>IH</sub> (Min.) or above V<sub>IL</sub> (Max.) on address, data, reset, and control signals, as shown in Figure 20 (b). The acceptable glitch noises are illustrated in Figure 20 (a).

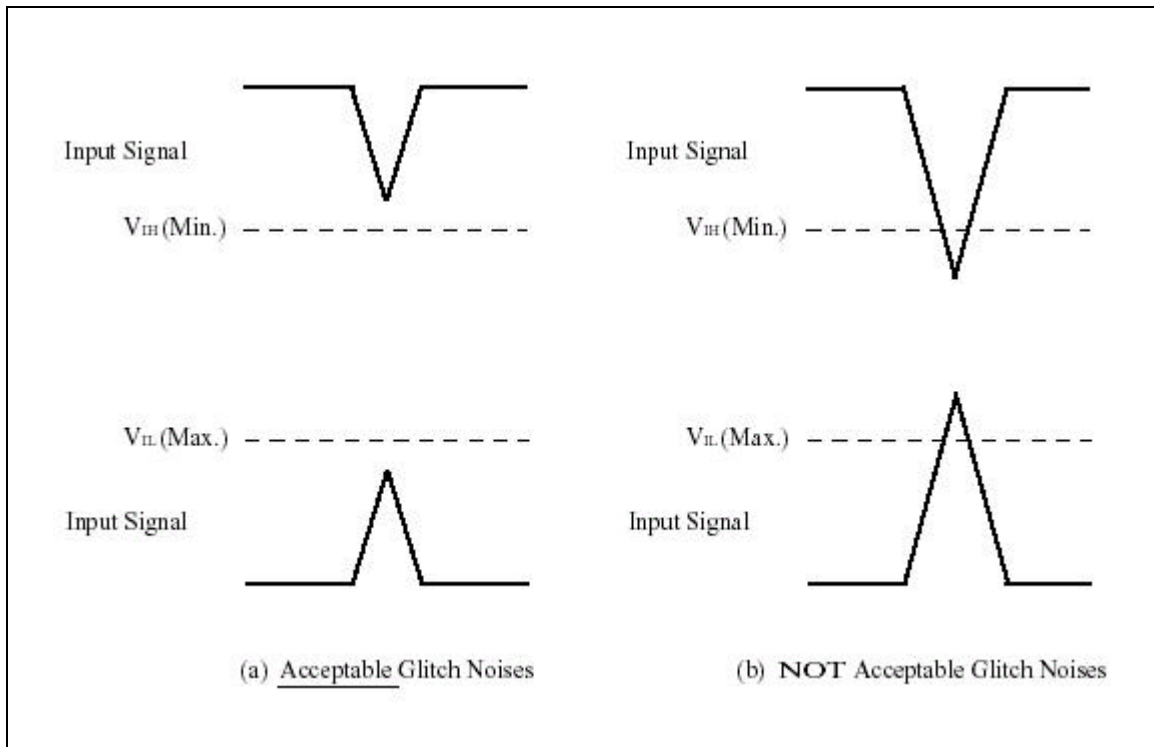


Figure 20. Waveform for Glitch Noises

See the "DC CHARACTERISTICS" described in specifications for V<sub>IH</sub> (Min.) and V<sub>IL</sub> (Max.).

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### 13. ORDERING INFORMATION

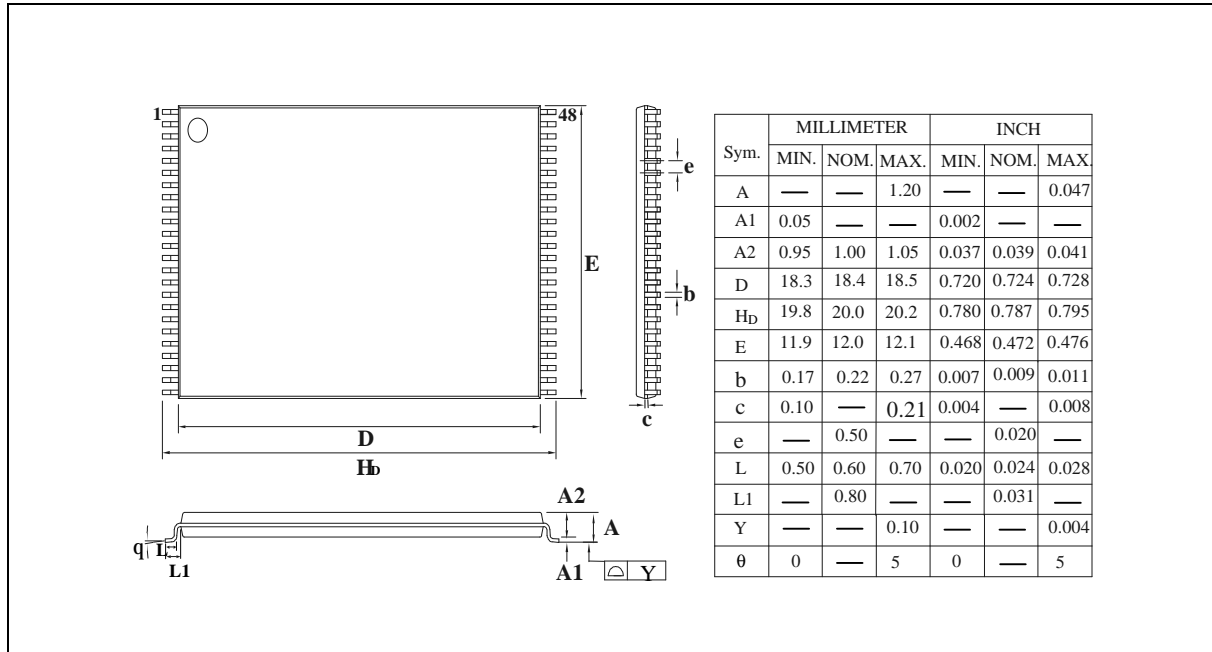
PART NO.	ACCESS TIME (nS)	OPERATING TEMPERATURE (°C)	BOOT BLOCK	PACKAGE
W28J160BT90C	90	0° C to 70° C	Bottom Boot	48L TSOP
W28J160TT90C	90	0° C to 70° C	Top Boot	48L TSOP
W28J160BT90L	90	-40° C to 85° C	Bottom Boot	48L TSOP
W28J160TT90L	90	-40° C to 85° C	Top Boot	48L TSOP

Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

## 14. PACKAGE DIMENSION

### 48-Lead Standard Thin Small Outline Package (measured in millimeters)





# Preliminary W28J160B/T



## 15. VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	May 21, 2002	-	Initial Issued



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