Winbond Electronics Corp.

2M ´ 4 BANKS ´ 16 BIT SDRAM

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1. GENERAL DESCRIPTION

W987Y6CB is a high-speed synchronous dynamic random access memory (SDRAM), organized as 2M words × 4 banks × 16 bits. Using pipelined architecture and 0.175 μm process technology, W987Y6CB delivers a data bandwidth of up to 125M words per second (-8). For different application, W987Y6CB is sorted into two speed grades: -75 and -8. The -75 is compliant to the 133 MHz/ CL3 specification; the -8 is compliant to the 125 MHz/ CL3 specification. For handheld device application, these parts are specially designed with several power saving mechanisms to achieve extremely low Self Refresh Current.

Accesses to the SDRAM are burst oriented. Consecutive memory location in one page can be accessed at a burst length of 1, 2, 4, 8 or full page when a bank and row is selected by an ACTIVE command. Column addresses are automatically generated by the SDRAM internal counter in burst operation. Random column read is also possible by providing its address at each clock cycle. The multiple bank nature enables interleaving among internal banks to hide the precharging time.

By having a programmable Mode Register, the system can change burst length, latency cycle, interleave or sequential burst to maximize its performance. W987Y6CB is ideal for main memory in high performance applications.

2. FEATURES

- Power supply V_{DD} = 2.5V ±0.2V
- V_{DDQ} = 2.5V
- Standard Self Refresh Mode
- Power Down Mode
- CAS Latency: 2 and 3
- Burst Length: 1, 2, 4, 8, and full page
- 4K Refresh Cycles / 64 mS
- Interface: LVTTL
- Packaged in 54 balls FBGA
- Operating Temperature Range
- Commercial Temperature (0° C – 70° C)
- Industrial Temperature (-40° C – 85° C)

3. AVAILABLE PART NUMBER

PART NUMBER	SPEED	SELF REFRESH CURRENT (MAX.)	TEMPERATURE RANGE	LEAD-FREE PACKAGE
W987Y6CBN75	133 MHz/ CL3	400 μA	0° C – 70° C	No
W987Y6CBG75	133 MHz/ CL3	400 μA	0° C – 70° C	Yes
W987Y6CBN80	125 MHz/ CL3	400 μA	0° C – 70° C	No
W987Y6CBG80	125 MHz/ CL3	400 μA	0° C – 70° C	Yes

4. BALL CONFIGRUATION

(TOP VIEW)

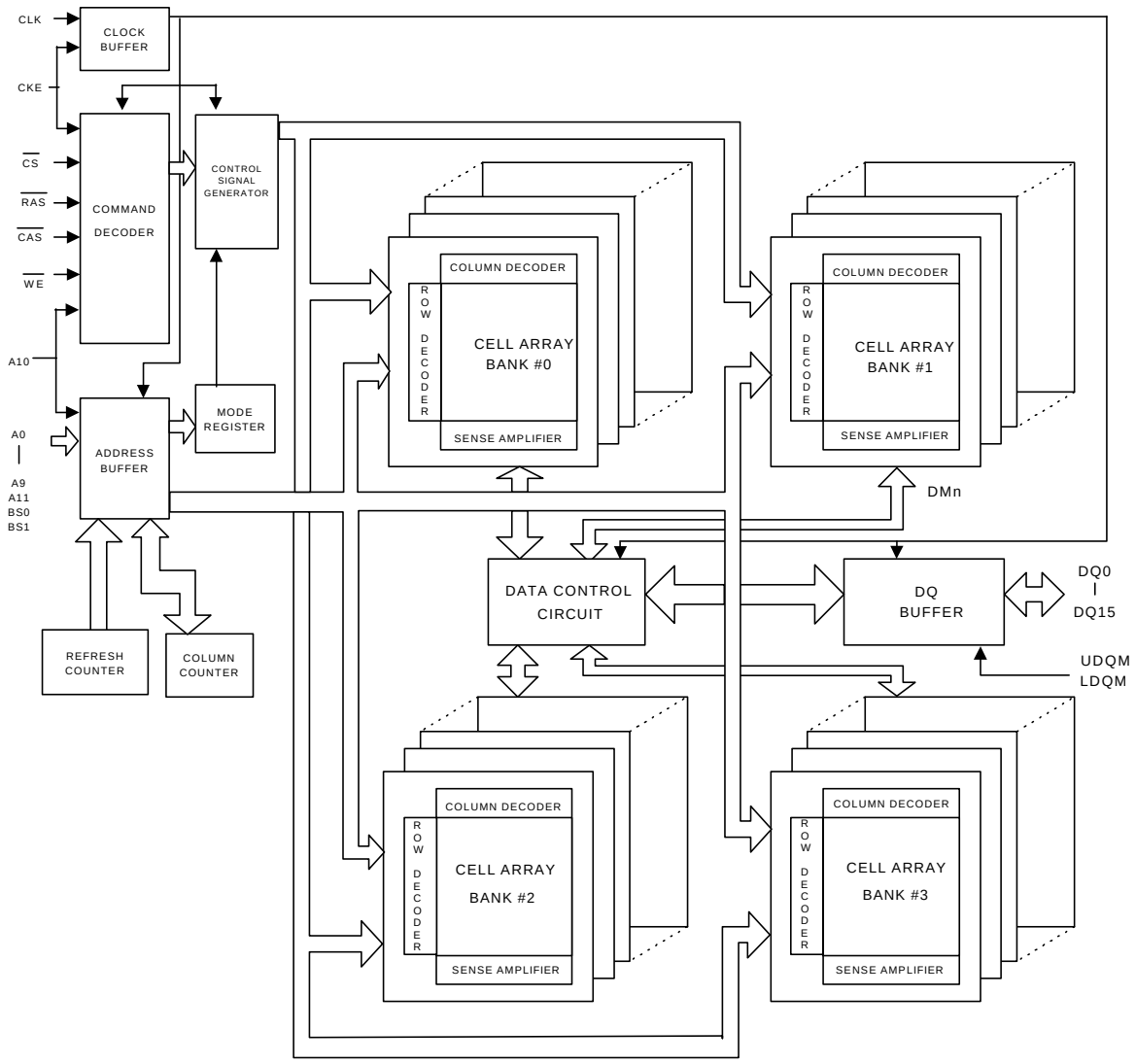
1	2	3	4	5	6	7	8	9	
Vss	DQ15	VSSQ				VDDQ	DQ0	VDD	A
DQ14	DQ13	VDDQ				VSSQ	DQ2	DQ1	B
DQ12	DQ11	VSSQ				VDDQ	DQ4	DQ3	C
DQ10	DQ9	VDDQ				VSSQ	DQ6	DQ5	D
DQ8	NC	Vss				VDD	LDQM	DQ7	E
UDQM	CLK	CKE				CAS	RAS	WE	F
NC	A11	A9				BA0	BA1	CS	G
A8	A7	A6				A0	A1	A10/ AP	H
Vss	A5	A4				A3	A2	VDD	J

Package Dimension 8mm x 9 mm

5. BALL DESCRIPTION

PIN NUMBER	BALL NAME	FUNCTION	DESCRIPTION
H7, H8, J8, J7, J3, J2, H3, H2, H1, G3, H9, G2	A0 – A11	Address	Multiplexed pins for row and column address. Row address: A0 – A11. Column address: A0 – A8.
G7, G8	BS0, BS1	Bank Select	Select bank to activate during row address latch time, or bank to read/write during address latch time.
A8, B9, B8, C9, C8, D9, D8, E9, E1, D2 D1, C2, C1, B2, B1, A2	DQ0 – DQ15	Data Input/ Output	Multiplexed pins for data output and input.
G9	$\overline{CS}$	Chip Select	Disable or enable the command decoder. When command decoder is disabled, new command is ignored and previous operation continues.
F8	$\overline{RAS}$	Row Address Strobe	Command input. When sampled at the rising edge of the clock, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ define the operation to be executed.
F7	$\overline{CAS}$	Column Address Strobe	Referred to $\overline{RAS}$
F9	$\overline{WE}$	Write Enable	Referred to $\overline{RAS}$
F1, E8	UDQM LDQM	Input/Output Mask	The output buffer is placed at Hi-Z (with latency of 2) when DQM is sampled high in read cycle. In write cycle, sampling DQM high will block the write operation with zero latency.
F2	CLK	Clock Inputs	System clock used to sample inputs on the rising edge of clock.
F3	CKE	Clock Enable	CKE controls the clock activation and deactivation. When CKE is low, Power Down mode, Suspend mode or Self Refresh mode is entered.
A9, E7, J9	V_{DD}	Power	Power for input buffers and logic circuit inside DRAM.
A1, E3, J1	V_{SS}	Ground	Ground for input buffers and logic circuit inside DRAM.
A7, B3, C7, D3	V_{DDQ}	Power for I/O Buffer	Separated power from V_{CC}, used for output buffers to improve noise.
A3, B7, C3, D7	V_{SSQ}	Ground for I/O Buffer	Separated ground from V_{SS}, used for output buffers to improve noise.
E2, G1	NC	No Connection	No connection

6. BLOCK DIAGRAM



Note: The cell array configuration is 4096 * 512 * 16.

7. ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Input/Output Voltage	V_{IN}, V_{OUT}	-0.3 – V_{DD} +0.3	V	1
Power Supply Voltage	V_{DD}, V_{DDQ}	-0.3 – 3.6	V	1
Operating Temperature (Commercial parts)	T_{OPR}	0 – 70	°C	1
Operating Temperature (Industrial parts)	T_{OPR}	-40 – 85	°C	1
Storage Temperature	T_{STG}	-55 – 150	°C	1
Soldering Temperature (10s)	T_{SOLDER}	260	°C	1
Power Dissipation	PD	1	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

8. DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(T_A = 0°C to 70°C for commercial parts, T_A = -40°C to 85°C for Industrial parts)

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}	2.3	2.5	2.7	V
Supply Voltage (for I/O Buffer)	V_{DDQ}	2.3	2.5	2.7	V
Input High level Voltage	V_{IH}	0.8*V_{DDQ}	-	V_{DDQ} +0.3	V
Input Low level Voltage	V_{IL}	-0.3	-	0.2*V_{DDQ}	V
LVTTL Output "H" Level Voltage (I_{OUT} = -0.1 mA)	V_{OH}	V_{DDQ} – 0.2	-	-	V
LVTTL Output "L" Level Voltage (I_{OUT} = +0.1 mA)	V_{OL}	-	-	0.2	V
Input Leakage Current (0V ≤ V_{IN} ≤ V_{DD}, all other pins not under test = 0V)	$I_{I(L)}$	-5	-	5	µA
Output Leakage Current (Output disable , 0V ≤ V_{OUT} ≤ V_{CCQ})	$I_{O(L)}$	-5	-	5	µA

Note: V_{IH} (max.) = V_{DD}/ V_{DDQ} +1.2V for pulse width ≤ 5 nS
V_{IL} (min.) = V_{SS}/ V_{SSQ} -1.2V for pulse width ≤ 5 nS

9. CAPACITANCE

(V_{DD} = 2.5V, f = 1 MHz, T_A = 25° C)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance (A0 to A11, BS0, BS1, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM, CKE)	CI	-	3.8	pF
Input Capacitance (CLK)	CCLK	-	3.5	pF
Input/Output Capacitance	CIO	-	6.5	pF

Note: These parameters are periodically sampled and not 100% tested.

10. OPERATING CURRENT

(V_{DD} = 2.5V ±0.2V, T_A = 0° C to 70° C for commercial parts, T_A = -40° C to 85° C for Industrial parts)

PARAMETER		SYM.	-75/75I	-8/-8I	UNIT	NOTES
			MAX.	MAX.		
Operating Current t_{CK} = min., t_{RC} = min. Active precharge command cycling without burst operation	1 bank operation	I_{CC1}	65	60	mA	3
Standby Current t_{CK} = min, $\overline{CS}$ = V_{IH} V_{IH} / $_L$ = V_{IH} (min.)/ V_{IL} (max.) Bank: Inactive state	CKE = V_{IH}	I_{CC2}	15	15		3
	CKE = V_{IL} (Power Down mode)	I_{CC2P}	0.5	0.5		3
Standby Current CLK = V_{IL}, $\overline{CS}$ = V_{IH} V_{IH} / $_L$ = V_{IH} (min.)/ V_{IL} (max.) BANK: Inactive state	CKE = V_{IH}	I_{CC2S}	10	10		
	CKE = V_{IL} (Power down mode)	I_{CC2PS}	0.35	0.35		
No Operating Current t_{CK} = min., $\overline{CS}$ = V_{IH} (min.) BANK: Active state (4 banks)	CKE = V_{IH}	I_{CC3}	20	20		
	CKE = V_{IL} (Power down mode)	I_{CC3P}	2	2		
Burst Operating Current t_{CK} = min. Read/ Write command cycling		I_{CC4}	90	85		3, 4
Auto Refresh Current t_{CK} = min. Auto refresh command cycling		I_{CC5}	150	140		3
Self Refresh Current Self Refresh Mode CKE = 0.2V		I_{CC6}	400	400	µA	
Deep Power Down Mode Current		I_{CC7}	10	10	µA	

11. AC CHARACTERISTICS AND OPERATING CONDITION

(Vcc = 2.5V ± 0.2V, T_A = 0° to 70°C for commercial parts ,T_A = -40°C to 85°C for Industrial parts; Notes: 5, 6, 7, 8)

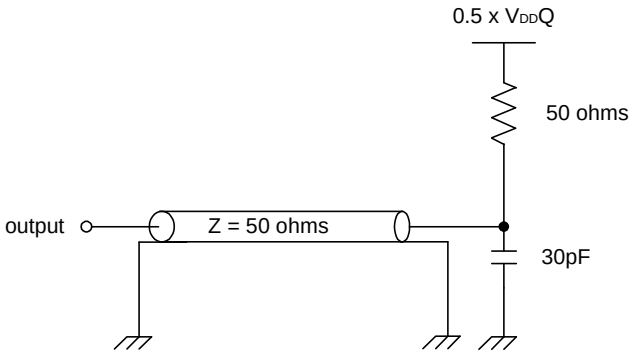
PARAMETER	SYM.	-75/75I		-8/-8I		UNIT
		MIN.	MAX.	MIN.	MAX.	
Ref/Active to Ref/Active Command Period	t_{RC}	65		68		nS
Active to precharge Command Period	t_{RAS}	45	100000	48	100000	
Active to Read/Write Command Delay Time	t_{RCD}	20		20		
Read/Write(a) to Read/Write(b)Command Period	t_{CCD}	1		1		Cycle
Precharge to Active Command Period	t_{RP}	20		20		nS
Active(a) to Active(b) Command Period	t_{RRD}	15		16		
Write Recovery Time CL* = 2	t_{WR}	10		10		
Write Recovery Time CL* = 3		7.5		8		
CLK Cycle Time CL* = 2	t_{CK}	10		10		
CLK Cycle Time CL* = 3		7.5		8		
CLK High Level width	t_{CH}	2.5		3		
CLK Low Level width	t_{CL}	2.5		3		
Access Time from CLK CL* = 2	t_{AC}		6		6	
Access Time from CLK CL* = 3			5.4		6	
Output Data Hold Time	t_{OH}	3		3		
Output Data High Impedance Time	t_{HZ}	3	7.5	3	8	
Output Data Low Impedance Time	t_{LZ}	0		0		
Power Down Mode Entry Time	t_{SB}	0	7.5	0	8	
Transition Time of CLK (Rise and Fall)	t_T	0.3	10	0.3	10	
Data-in Set-up Time	t_{DS}	1.5		2		
Data-in Hold Time	t_{DH}	1		1		
Address Set-up Time	t_{AS}	1.5		2		
Address Hold Time	t_{AH}	1		1		
CKE Set-up Time	t_{CKS}	1.5		2		
CKE Hold Time	t_{CKH}	1		1		
Command Set-up Time	t_{CMS}	1.5		2		
Command Hold Time	t_{CMH}	1		1		
Refresh Time	t_{REF}		64		64	mS
Mode Register Set Cycle Time	t_{RSC}	15		16		nS

*CL = CAS Latency

Notes:

1. Operation exceeds "ABSOLUTE MAXIMUM RATING" may adversely affect the life and reliability of the devices.
2. All voltages are referenced to V_{SS}
3. These parameters depend on the cycle rate and listed values are measured at a cycle rate with the minimum values of t_{CK} and t_{RC}.
4. These parameters depend on the output loading conditions. specified values are obtained with output open.
5. Power up sequence is further described in the "Functional Description" section.
6. AC Testing Conditions

Output Reference Level	0.5 * V_{DDQ}
Output Load	See diagram below
Input Signal Levels	0.8* V_{DDQ} / 0.2* V_{DDQ}
Transition Time (Rise and Fall) of Input Signal	1 nS
Input Reference Level	0.5 * V_{DDQ}



AC TEST LOAD

7. Transition times are measured between V_{IH} and V_{IL}.
8. t_{HZ} defines the time at which the outputs achieve the open circuit condition and is not referenced to output level.
9. The value that shown on table are based on silicon simulation result. It will be changed according to real product characteristic.

Operation Mode

Fully synchronous operations are performed to latch the commands at the positive edges of CLK. Table 1 shows the truth table for the operation commands.

Table 1 Truth Table (Note (1), (2))

COMMAND	DEVICE STATE	CKEn-1	CKEn	DQM	BS0, 1	A10	A0 - A9 A11	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$
Bank Active	Idle	H	x	x	v	v	v	L	L	H	H
Bank Precharge	Any	H	x	x	v	L	x	L	L	H	L
Precharge All	Any	H	x	x	x	H	x	L	L	H	L
Write	Active (3)	H	x	x	v	L	v	L	H	L	L
Write with Autoprecharge	Active (3)	H	x	x	v	H	v	L	H	L	L
Read	Active (3)	H	x	x	v	L	v	L	H	L	H
Read with Autoprecharge	Active (3)	H	x	x	v	H	v	L	H	L	H
Mode Register Set	Idle	H	x	x	v	v	v	L	L	L	L
No - Operation	Any	H	x	x	x	x	x	L	H	H	H
Burst Stop	Active (4)	H	x	x	x	x	x	L	H	H	L
Device Deselect	Any	H	x	x	x	x	x	H	x	x	x
Auto - Refresh	Idle	H	H	x	x	x	x	L	L	L	H
Self - Refresh Entry	Idle	H	L	x	x	x	x	L	L	L	H
Self Refresh Exit	idle (S.R.)	L L	H H	x x	x x	x x	x x	H L	x H	x H	x x
Clock Suspend Entry	Active	H	L	x	x	x	x	x	x	x	x
Power Down Entry	Idle Active (5)	H H	L L	x x	x x	x x	x x	H L	x H	x H	x x
Clock Suspend Exit	Active	L	H	x	x	x	x	x	x	x	x
Power Down Exit	Any (power down)	L L	H H	x x	x x	x x	x x	H L	x H	x H	x x
Deep Power Down Entry	Idle	H	L	x	x	x	x	L	H	H	L
Deep Power Down Exit	DPDM	L	H	x	x	x	x	x	x	x	x
Data write/Output Enable	Active	H	x	L	x	x	x	x	x	x	x
Data write/Output Disable	Active	H	x	H	x	x	x	x	x	x	x

Notes:

1. V = Valid X = Don't care L = Low Level H = High Level
2. CKEn signal is input level when commands are provided. CKEn-1 signal is the input level one clock cycle before the command is issued.
3. These are state of bank designated by BS0, BS1 signals.
4. Device state is full page burst operation.
5. Power Down Mode can not be entered in the burst cycle. When this command asserts in the burst cycle, device state is clock suspend mode.

12. FUNCTIONAL DESCRIPTION

Power Up Sequence

The default power up state of the mode register is unspecified. The following power up and initialization sequence need to be followed to guarantee the device being preconditioned to each user specific needs.

During power up, all V_{DD} and V_{DDQ} pins must be ramp up simultaneously to the specified voltage when the input signals are held in the "NOP" state. The power up voltage must not exceed V_{DD} +0.3V on any of the input pins or V_{DD} supplies. After power up, an initial pause of 200 µS is required followed by a precharge of all banks using the precharge command. To prevent data contention on the DQ bus during power up, it is required that the DQM and CKE pins be held high during the initial pause period. Once all banks have been precharged, the Mode Register Set Command must be issued to initialize the Mode Register. An additional eight Auto Refresh cycles (CBR) are also required before or after programming the Mode Register to ensure proper subsequent operation.

Command Function

Bank Activate command

($\overline{RAS}$ = "L", $\overline{CAS}$ = "H", $\overline{WE}$ ="H", BS0, BS1 = Bank, A0 to A11 = Row Address)

The Bank Activate command activates the bank designated by the BS (Bank select) signal. Row addresses are latched on A0 to A11 when this command is issued and the cell data is read out of the sense amplifiers. The maximum time that each bank can be held in the active state is specified as $t_{RAS\ (max)}$. After this command is issued, Read or Write operation can be executed.

Bank Precharge command

($\overline{RAS}$ ="L", $\overline{CAS}$ ="H", $\overline{WE}$ ="L", BS0, BS1 = Bank, A10 ="L", A0 to A9, A11 = Don't care)

The Bank Precharge command percharges the bank designated by BS. The precharged bank is switched from the active state to the idle state.

Precharge All command

($\overline{RAS}$ ="L", $\overline{CAS}$ ="H", $\overline{WE}$ ="L", BS0, BS1 = Don't care, A10 = "H", A0 to A9, A11 = Don't care)

The Precharge All command precharges all banks simultaneously. Then all banks are switched to the idle state.

Write command

($\overline{RAS}$ ="H", $\overline{CAS}$ ="L", $\overline{WE}$ ="L", BS0, BS1 = Bank, A10 ="L", A0 to A8 = Column Address)

The write command performs a Write operation to the bank designated by BS. The write data are latched at rising edge of CLK. The length of the write data (Burst Length) and column access sequence (Addressing Mode) must be programmed in the Mode Register at power-up prior to the Write operation.

Write with Auto Precharge command

($\overline{RAS}$ ="H", $\overline{CAS}$ ="L", $\overline{WE}$ ="L", BS0, BS1 = Bank, A10="H", A0 to A8 = Column Address)

The Write with Auto Precharge command performs the Precharge operation automatically after the Write operation. This command must not be interrupted by any other commands.

Read command

($\overline{RAS}$ ="H", $\overline{CAS}$ ="L", $\overline{WE}$ ="H", BS0, BS1 = Bank, A10 ="L", A0 to A8 = Column Address)

The Read command performs a Read operation to the bank designated by BS. The length of read data (Burst Length), Addressing Mode and $\overline{CAS}$ Latency (access time from $\overline{CAS}$ command in a clock cycle) must be programmed in the Mode Register at power-up prior to the Read operation.

Read with Auto Precharge command

($\overline{RAS}$ ="H", $\overline{CAS}$ ="L", $\overline{WE}$ ="H", BS0, BS1 = Bank, A10 ="H", A0 to A8 = Column Address)

The Read with Auto precharge command automatically performs the Precharge operation after the Read operation. This command must not be interrupted by any other command.

Mode Register Set command

($\overline{RAS}$ ="L", $\overline{CAS}$ ="L", $\overline{WE}$ ="L", BS0 ="L", BS1 ="L", A0 to A11 = Register Data)

The Mode Register Set command programs the values of Burst Length, Addressing Mode, $\overline{CAS}$ latency and Write Mode in the Mode Register. The default values in the Mode Register after power-up are undefined, therefore this command must be issued during the power-up sequence. Also, this command can be issued while all banks are in the idle state. Refer to the table for specific codes.

Extended Mode Register Set command

($\overline{RAS}$ ="L", $\overline{CAS}$ ="L", $\overline{WE}$ ="L", BS0 ="L", BS1 ="H", A0 to A11 = Register data)

The Extended Mode Register Set command programs the values of Driver Strength, Temperature Compensated Self Refresh and Partial Array Self Refresh. The default value of the extended mode register is Full Driver Strength, 70 degrees C and All banks Refreshed

No-Operation command

($\overline{RAS}$ ="H", $\overline{CAS}$ ="H", $\overline{WE}$ ="H")

The No-Operation command simply performs no operation (same command as Device Deselect).

Burst Read stop command

($\overline{RAS}$ ="H", $\overline{CAS}$ ="H", $\overline{WE}$ ="L")

The Burst stop command is used to stop the burst operation. This command is only valid during a Burst Read operation.

Device Deselect command

($\overline{CS}$ ="H")

The Device Deselect command disables the command decoder so that the $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and Address inputs are ignored. This command is similar to the No-Operation command.

Auto Refresh command

($\overline{RAS}$ ="L", $\overline{CAS}$ ="L", $\overline{WE}$ ="H", CKE ="H", BS0, BS1, A0 to A11 = Don't care)

The Auto Refresh command is used to refresh the row address provided by the internal refresh counter. The Refresh operation must be performed 4096 times within 64ms. The next command can be issued after t_{RC} from the end of the Auto Refresh command. When the Auto Refresh command is used, all banks must be in the idle state.

Self Refresh Entry command

($\overline{RAS}$ ="L", $\overline{CAS}$ ="L", $\overline{WE}$ ="H", CKE="L", BS0, BS1, A0 to A11 = don't care)

The Self Refresh Entry command is used to enter Self Refresh mode. While the device is in Self Refresh mode, all input and output buffer (except the CKE buffer) are disabled and the Refresh operation is automatically performed. Self Refresh mode is exited by taking CKE "high" (the Self Refresh Exit command).

Self Refresh Exit command

(CKE = "H" during SDRAM in Self Refresh Mode)

This command is used to exit from Self Refresh mode. Any subsequent commands can be issued after t_{RC} from the end of this command.

Deep Power Down Mode Entry command

($\overline{RAS}$ ="H", $\overline{CAS}$ ="H", $\overline{WE}$ ="L", CKE ="L", BS0, BS1, A0 to A11 = don't care)

The Deep Power Down Mode Entry command is used to enter Deep Power Down mode. While the device is in Deep Power Down mode, all internal circuits (except the CKE buffer) are disabled in order to 10uA current consumption.

Deep Power Down Mode Exit command

(CKE= "H" during SDRAM in Deep Power Down Mode)

This command is used to exit from Deep Power Down mode. Full initialization is required when the device exits from Deep Power Down Mode.

Data Write Enable /Disable command

(LDQM, UDQM ="L/H")

During a Write cycle, the LDQM or UDQM signal functions as Data Mask and can control every word of the input data. The LDQM signal controls DQ0 to DQ7 and UDQM signal controls DQ8 to DQ15.

Read Operation

Issuing the Bank Activate command to the idle bank puts it into the active state. When the Read command is issued after t_{RCD} from the Bank Activate command, the data is read out sequentially. The address inputs determine the starting column address for the burst. The initial read data becomes available after $\overline{CAS}$ latency from the issuing of the Read command. The $\overline{CAS}$ latency must be set in the Mode Register at power-up.

When the Precharge Operation is performed on a bank during a Burst Read and operation, the Burst operation is terminated.

When the Read with Auto Precharge command is issued, the Precharge operation is performed automatically after the Read cycle, then the bank is switched to the idle state. This command cannot be interrupted by any other commands. Refer to the diagrams for Read operation.

Write Operation

Issuing the Write command after t_{RCD} from the bank activate command. The address inputs determine the starting column address. Data for the first burst write cycle must be applied on the DQ pins on the same clock cycle that the Write Command is issued. The remaining data inputs must be supplied on each subsequent rising clock edge until the burst length is completed. Data supplied to the DQ pins after burst finishes will be ignored. The burst length of the Write data (Burst Length) and Addressing Mode must be set in the Mode Register at power-up.

When the Precharge operation is performed in a bank during a Burst Write operation, the Burst operation is terminated.

When the Write with Auto Precharge command is issued, the Precharge operation is performed automatically after the Write cycle, then the bank is switched to the idle state, The Write with Auto Precharge command cannot be interrupted by any other command for the entire burst data duration.

Precharge

The Precharge Command is used to precharge or close a bank that has been activated. The Precharge Command is entered when CS, RAS and WE are low and CAS is high at the rising edge of the clock. The Precharge Command can be used to precharge each bank separately or all banks simultaneously. Three address bits, A10, BS0, and BS1, are used to define which bank(s) is to be precharged when the command is issued. After the Precharge Command is issued, the precharged bank must be reactivated before a new read or write access can be executed. The delay between the Precharge Command and the Activate Command must be greater than or equal to the Precharge time (t_{RP}).

Burst Termination

When the Precharge command is used for a bank in a Burst cycle, the Burst operation is terminated. When Burst Read cycle is interrupted by the Precharge command, read operation is disabled after clock cycle of ($\overline{CAS}$ latency) from the Precharge command. When the Burst Write cycle is interrupted by the Precharge command . the input circuit is reset at the same clock cycle at which the precharge command is issued. In this case, the DQM signal must be asserted "high" during t_{WR} to prevent writing the invalided data to the cell array.

When the Burst Read Stop command is issued for the bank in a Burst Read cycle, the Burst Read operation is terminated. The Burst read Stop command is not supported during a write burst operation.

Interruption

Read Interrupted by a Read

A Burst Read may be interrupted by another Read Command. When the previous burst is interrupted, the remaining addresses are overridden by the new read address with the full burst length. The data from the first Read Command continues to appear on the outputs until the CAS latency from the interrupting Read Command the is satisfied.

Read Interrupted by a Write

To interrupt a burst read with a Write Command, DQM may be needed to place the DQs (output drivers) in a high impedance state to avoid data contention on the DQ bus. If a Read Command will issue data on the first and second clocks cycles of the write operation, DQM is needed to insure the DQs are tri-stated. After that point the Write Command will have control of the DQ bus and DQM masking is no longer needed.

Write Interrupted by a Write

A burst write may be interrupted before completion of the burst by another Write Command. When the previous burst is interrupted, the remaining addresses are overridden by the new address and data will be written into the device until the programmed burst length is satisfied.

Write Interrupted by a Read

A Read Command will interrupt a burst write operation on the same clock cycle that the Read Command is activated. The DQs must be in the high impedance state at least one cycle before the new read data appears on the outputs to avoid data contention. When the Read Command is activated, any residual data from the burst write cycle will be ignored.

Refresh Operation

Two types of Refresh operation can be performed on the device: Auto Refresh and Self Refresh. By repeating the Auto Refresh cycle, each bank in turn refreshed automatically. The Refresh operation must be performed 4096 times (rows) within 64ms. The period between the Auto Refresh command and the next command is specified by t_{RC}.

The Self Refresh Mode is entered by issuing the Self Refresh Entry Command at the rising edge of the clock. All banks must be idle prior to issuing the Self Refresh Entry Command. Once the command is registered, CKE must be held low to keep the device in Self Refresh mode. When the SDRAM has entered Self Refresh mode all of the external control signals, except CKE, are disabled. The clock is internally disabled during Self Refresh Operation to save power. The device will exit Self Refresh operation after CKE is returned high. A minimum delay time is required when the device exits Self Refresh Operation and before the next command can be issued. This delay is equal to the t_{RC} cycle time plus the Self Refresh exit time.

If, during normal operation, AUTO REFRESH cycles are issued in bursts (as opposed to being evenly distributed), a burst of 4,096 AUTO REFRESH cycles should be completed just prior to entering and just after exiting the self refresh mode.

Power Down Mode

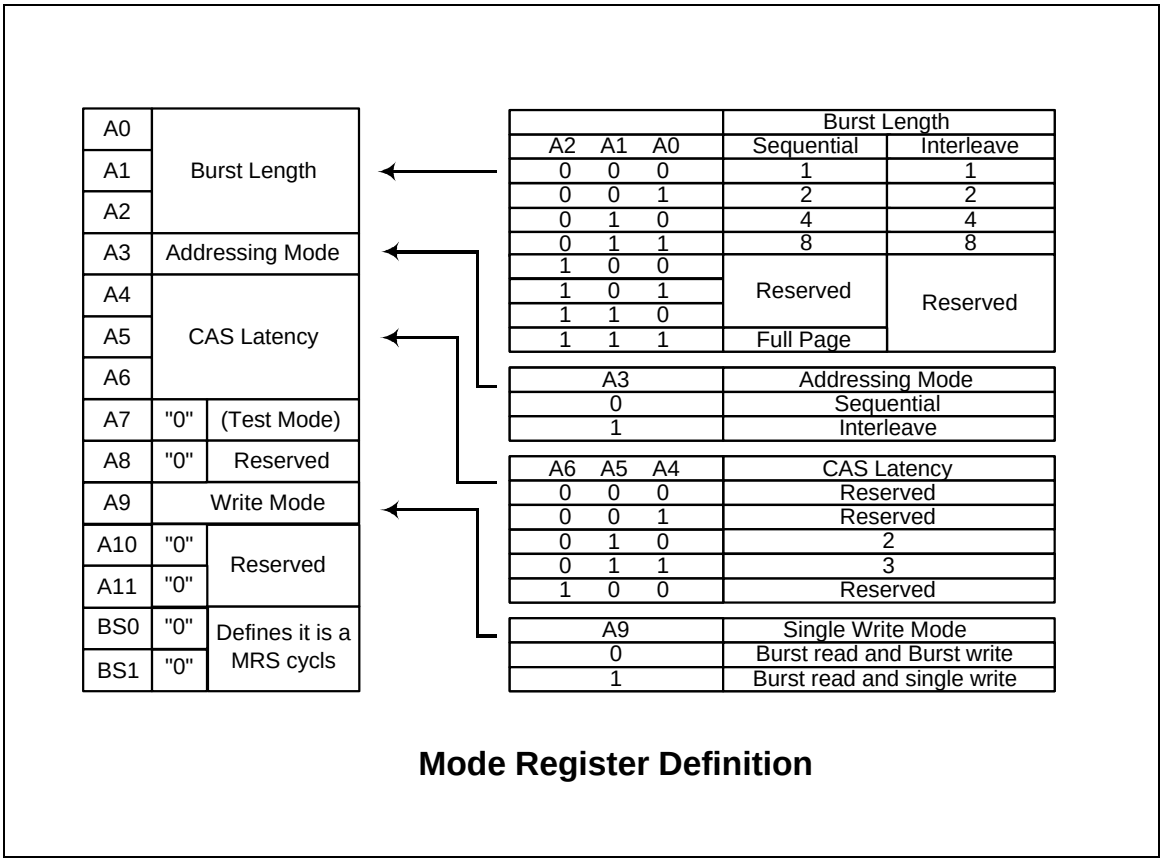
The Power Down mode is initiated by holding CKE low. All of the receiver circuits except CKE are gated off to reduce the power. The Power Down mode does not perform any refresh operations, therefore the device can not remain in Power Down mode longer than the Refresh period (t_{REF}) of the device.

Mode Register Set Operation

The mode register is programmed by the Mode Register Set command (MRS/EMRS) when all banks are in the idle state. The data to be set in the Mode Register is transferred using the Address pins of A0 to A11 inputs. The combination of BS0, BS1 detains this cycle is MRS or EMRS.

Mode Register Description

The Mode Register designates the operation mode for the read or write cycle. The register is divided into four fields; (1) Burst Length field sets the length of burst data (2) Addressing Mode selection bit to designate the column access sequence in a Burst cycle (3) CAS Latency field sets the access time in clock cycle (4) Single Write Mode selection bit to designate write operation in burst or single write.



Mode Register Definition

- **Address sequence of Sequential mode**

  A column access is performed by incrementing the column address input to the device. The address is varied by the Burst Length as the following.

Addressing Sequence of Sequential Mode

DATA	ACCESS ADDRESS	BURST LENGTH
Data 0	n	2 words (address bits is A0)
Data 1	n + 1	No carried from A0 to A1
Data 2	n + 2	4 words (address bit A0, A1)
Data 3	n + 3	Not carried from A1 to A2
Data 4	n + 4	
Data 5	n + 5	8 words(address bits A2, A1 and A0)
Data 6	n + 6	Not carried from A2 to A3
Data 7	n + 7	

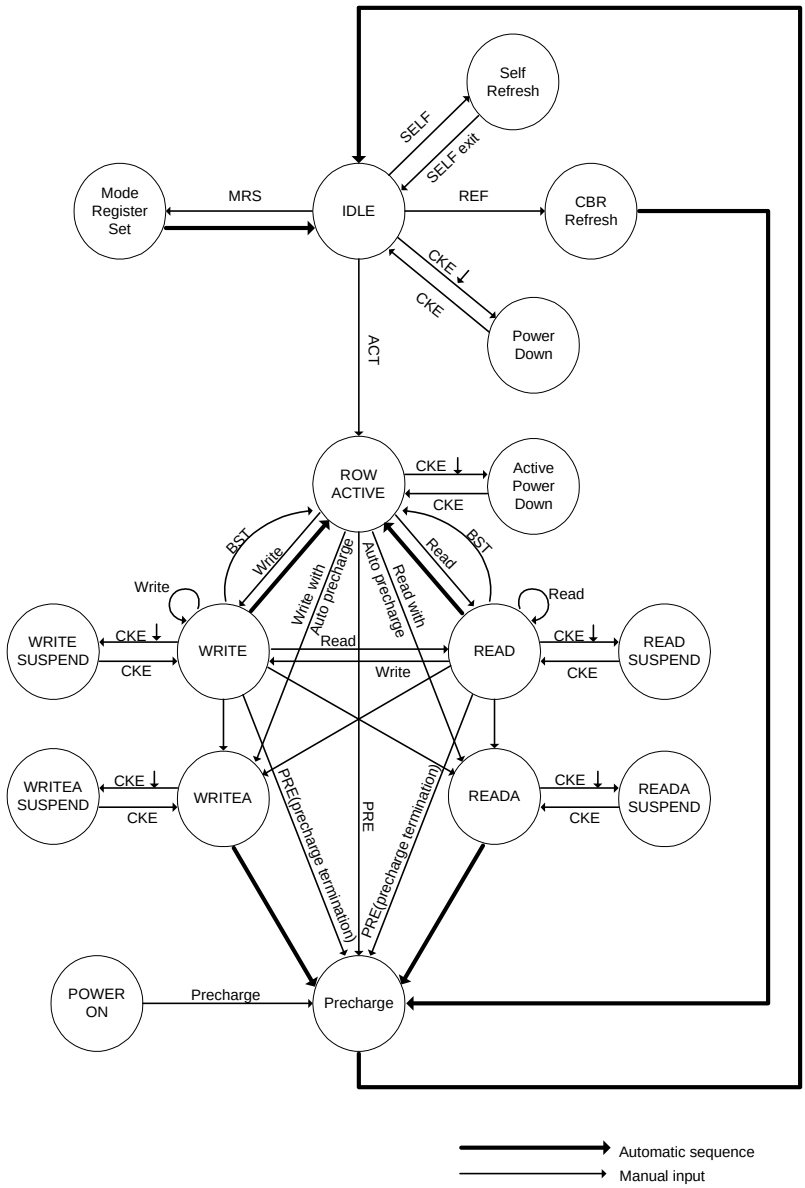
- **Addressing sequence of Interleave mode**

  A Column access is started from the inputted column address and is performed by interleaving the address bits in the sequence shown as the following.

Address Sequence for Interleave Mode

DATA	ACCESS ADDRESS	BURST LENGTH
Data 0	A8 A7 A6 A5 A4 A3 A2 A1 A0	2 words
Data 1	A8 A7 A6 A5 A4 A3 A2 A1 $\overline{A0}$	
Data 2	A8 A7 A6 A5 A4 A3 A2 $\overline{A1}$ A0	4 words
Data 3	A8 A7 A6 A5 A4 A3 A2 $\overline{A1}$ $\overline{A0}$	
Data 4	A8 A7 A6 A5 A4 A3 $\overline{A2}$ A1 A0	8 words
Data 5	A8 A7 A6 A5 A4 A3 $\overline{A2}$ A1 $\overline{A0}$	
Data 6	A8 A7 A6 A5 A4 A3 $\overline{A2}$ $\overline{A1}$ A0	
Data 7	A8 A7 A6 A5 A4 A3 $\overline{A2}$ $\overline{A1}$ $\overline{A0}$	

Simplified State Diagram

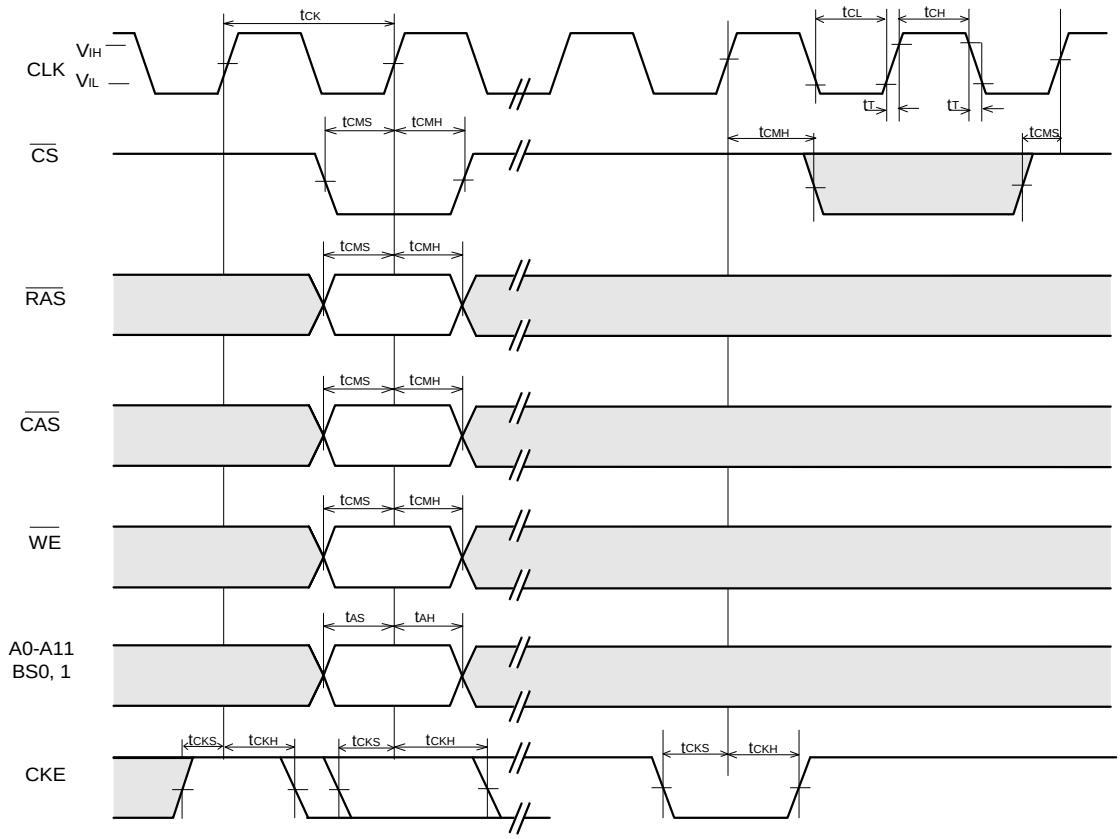


Notes:

MRS = Mode Register Set
REF = Refresh
ACT = Active
PRE = Precharge
WRITEA = Write with Auto precharge
READA = Read with Auto precharge

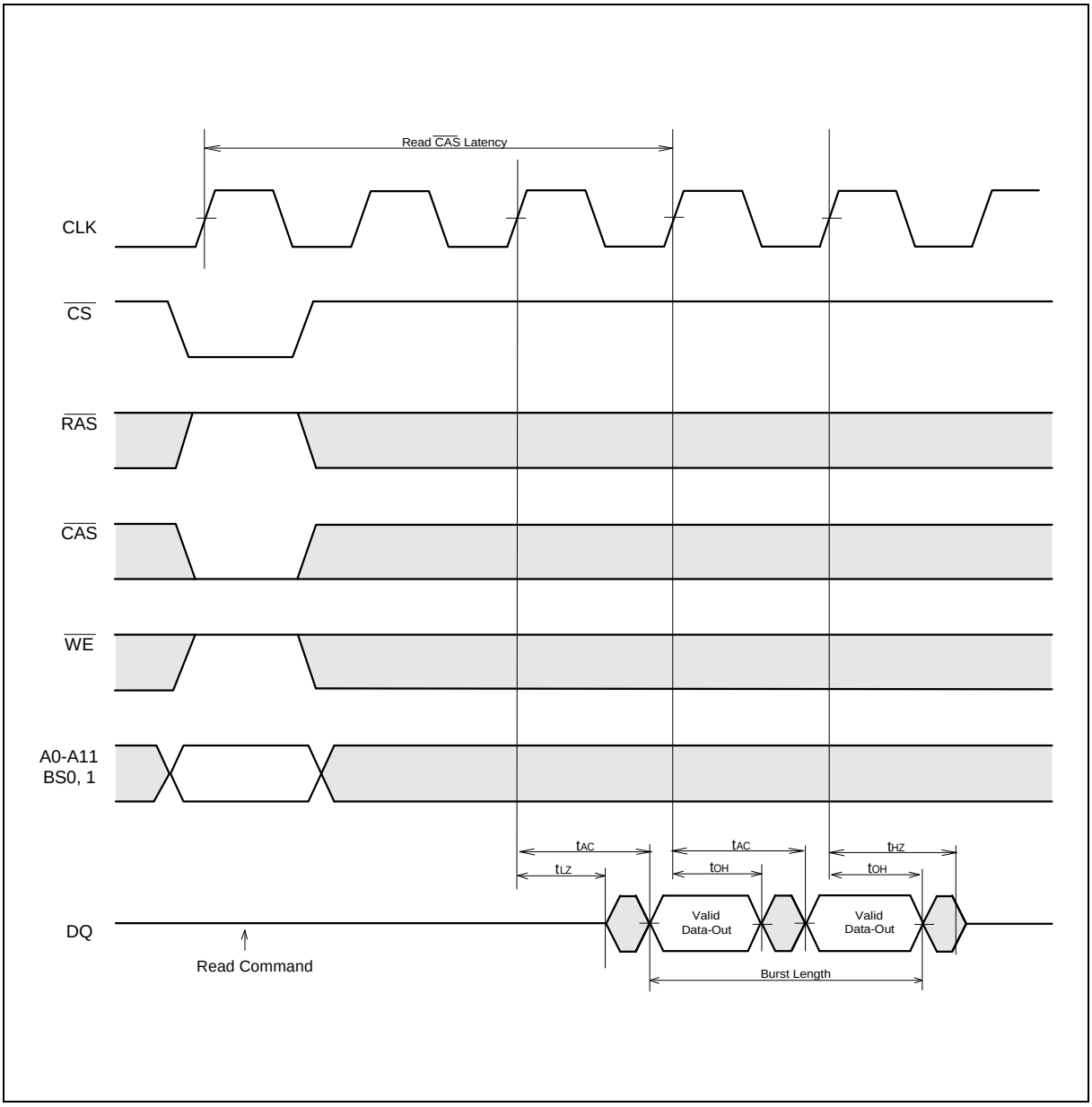
13. TIMING WAVEFORMS

Command Input Timing



Timing Waveforms, continued

Read Timing

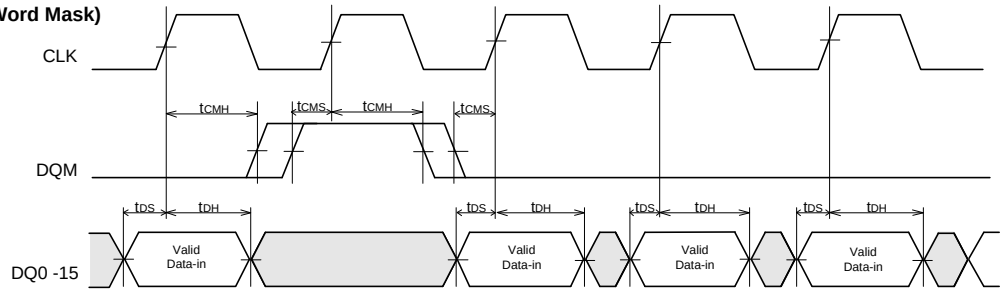


Timing Waveforms, continued

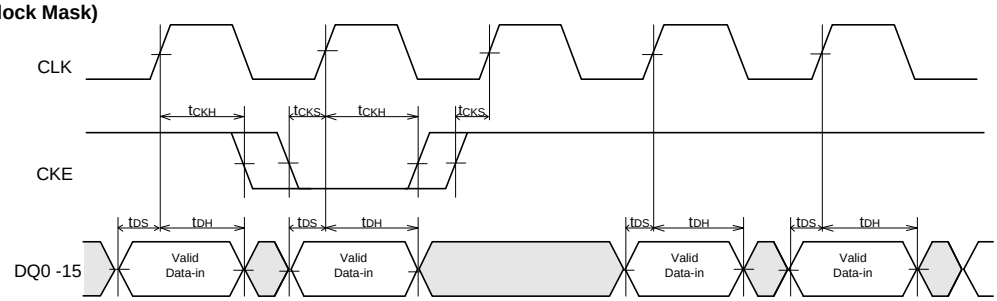
Control Timing of Input / Output Data

Control Timing of Input Data

(Word Mask)

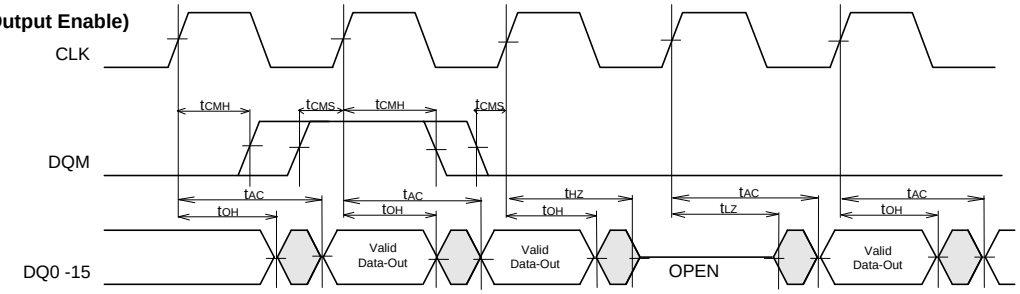


(Clock Mask)

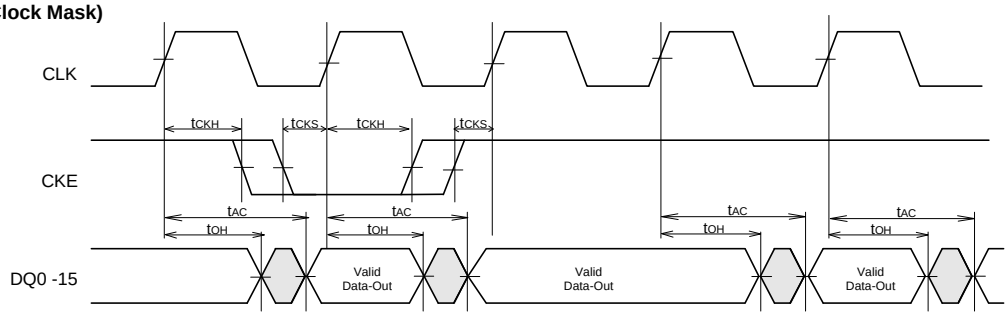


Control Timing of Output Data

(Output Enable)

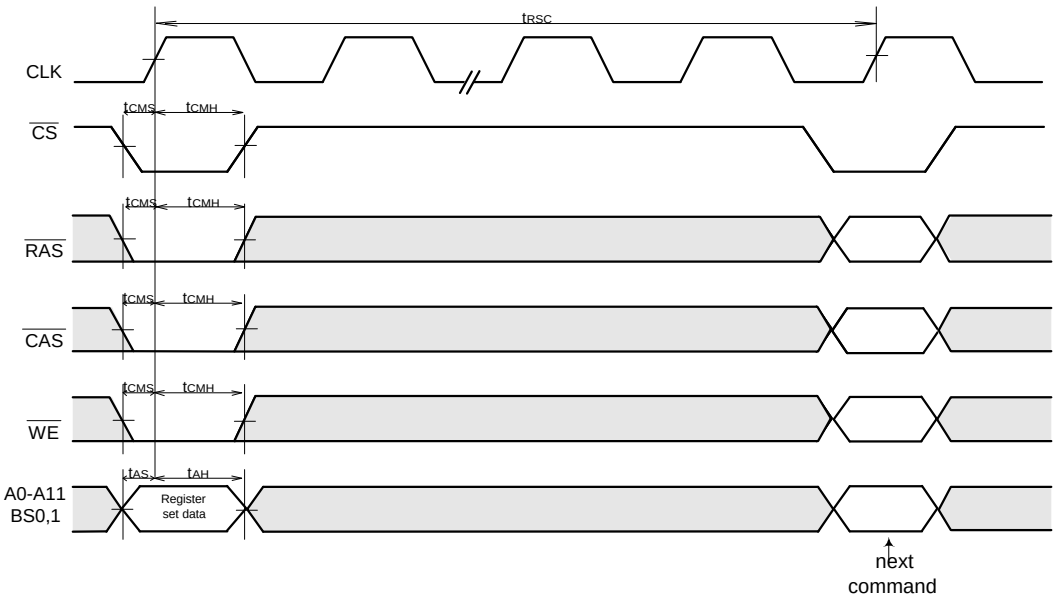


(Clock Mask)



Timing Waveforms, continued

Mode Register Set Cycle



A0	Burst Length	
A1		
A2		
A3	Addressing Mode	
A4	CAS Latency	
A5		
A6		
A7	"0"	(Test Mode)
A8	"0"	Reserved
A9	Write Mode	
A10	"0"	Reserved
A11	"0"	
BS0	"0"	
BS1	"0"	

			Burst Length	
A2	A1	A0	Sequential	Interleave
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1		
1	1	0		
1	1	1	Full Page	

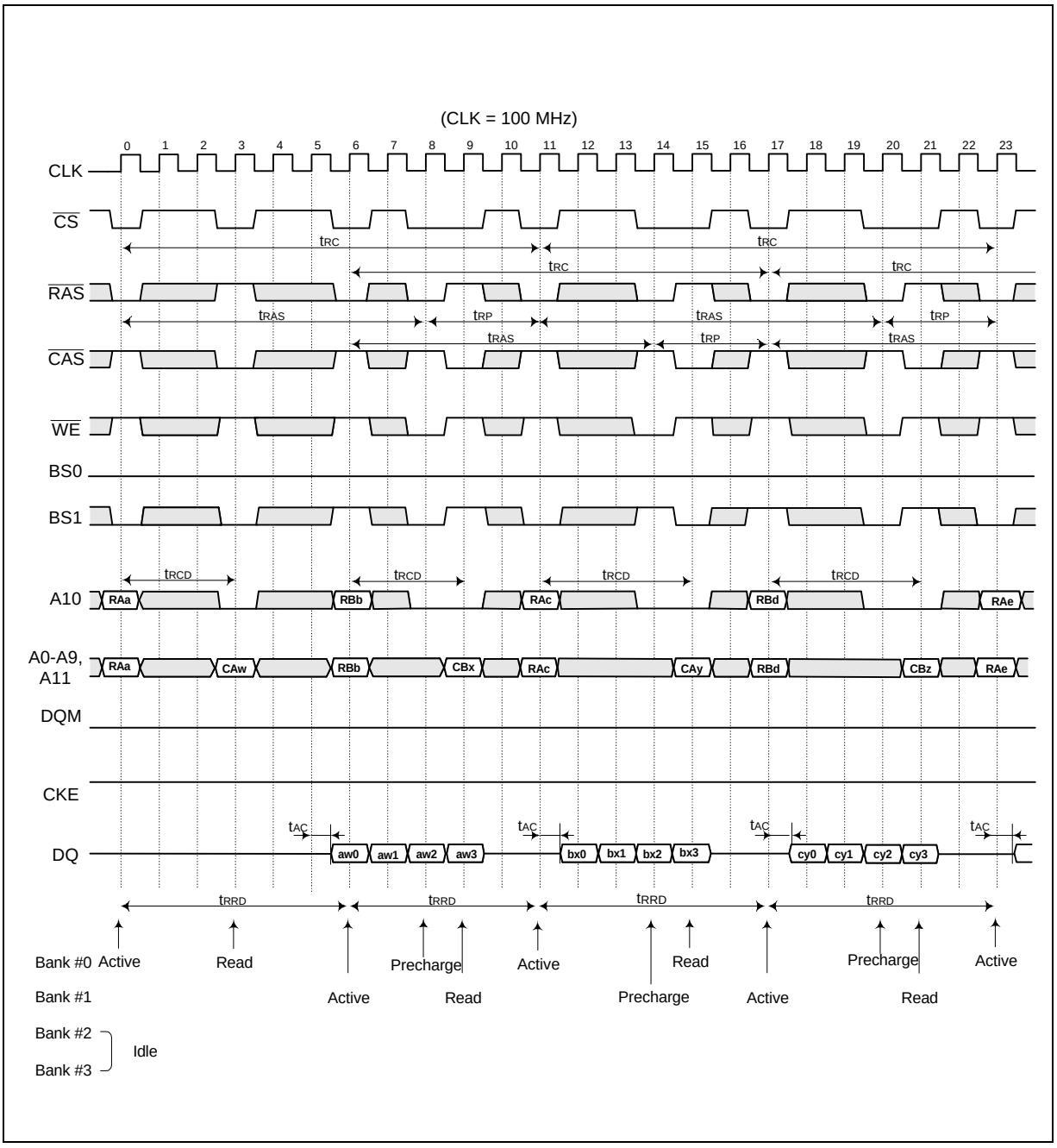
A3	Addressing Mode
0	Sequential
1	Interleave

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved

A9	Single Write Mode
0	Burst read and Burst write
1	Burst read and single write

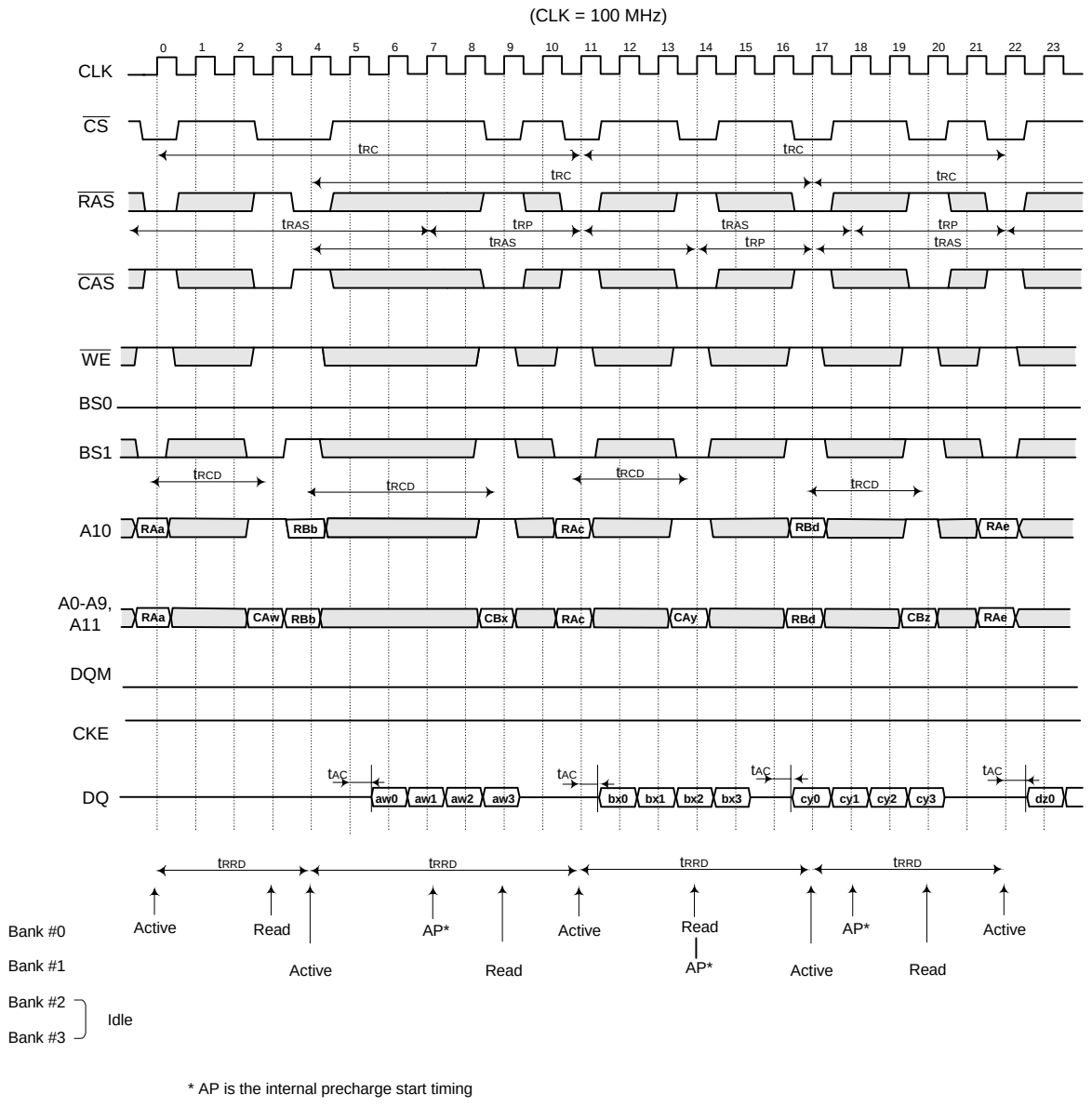
14. OPERATING TIMING EXAMPLE

Interleaved Bank Read (Burst Length = 4, CAS Latency = 3)



Operating Timing Example, contined

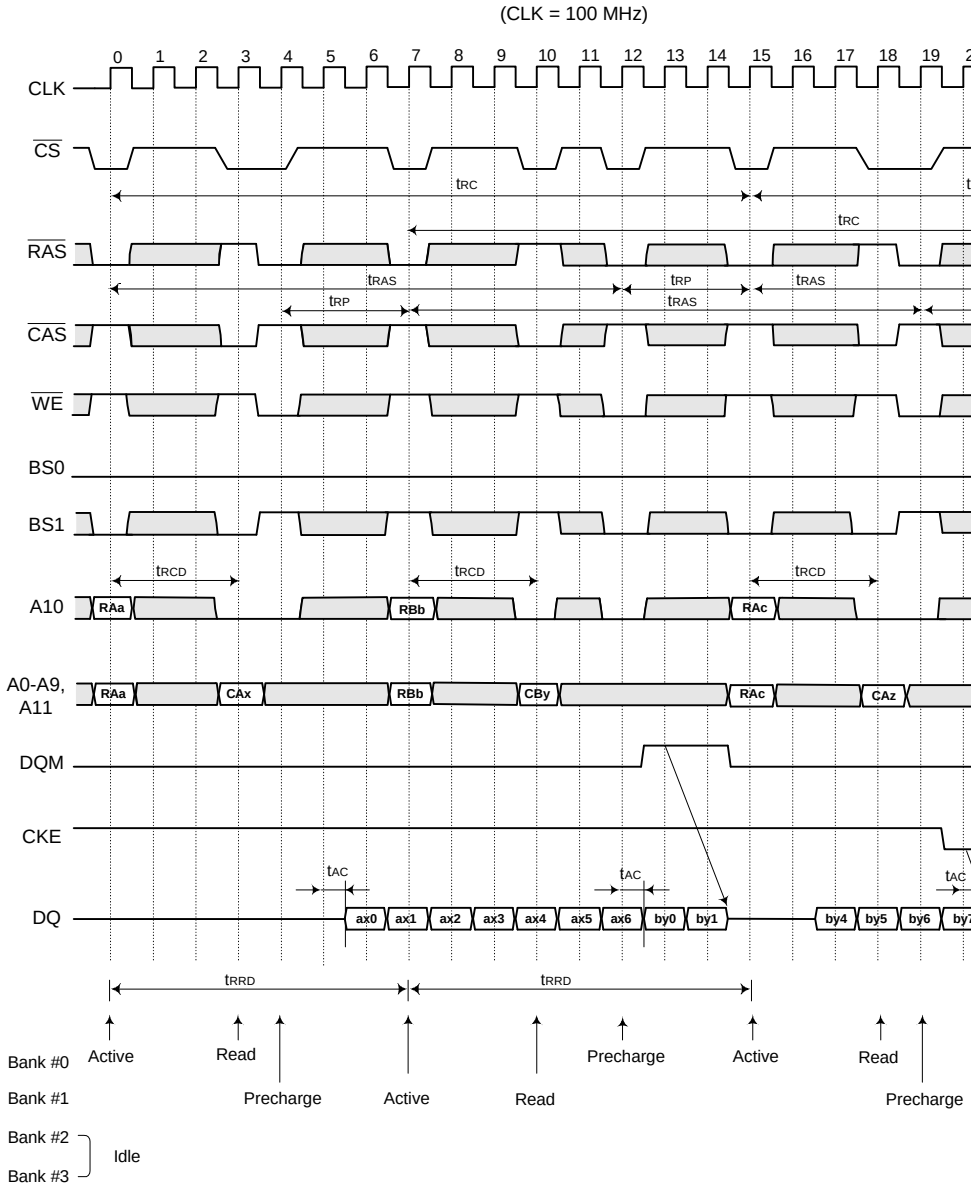
Interleaved Bank Read (Burst Length = 4, CAS Latency = 3, Autoprecharge)



* AP is the internal precharge start timing

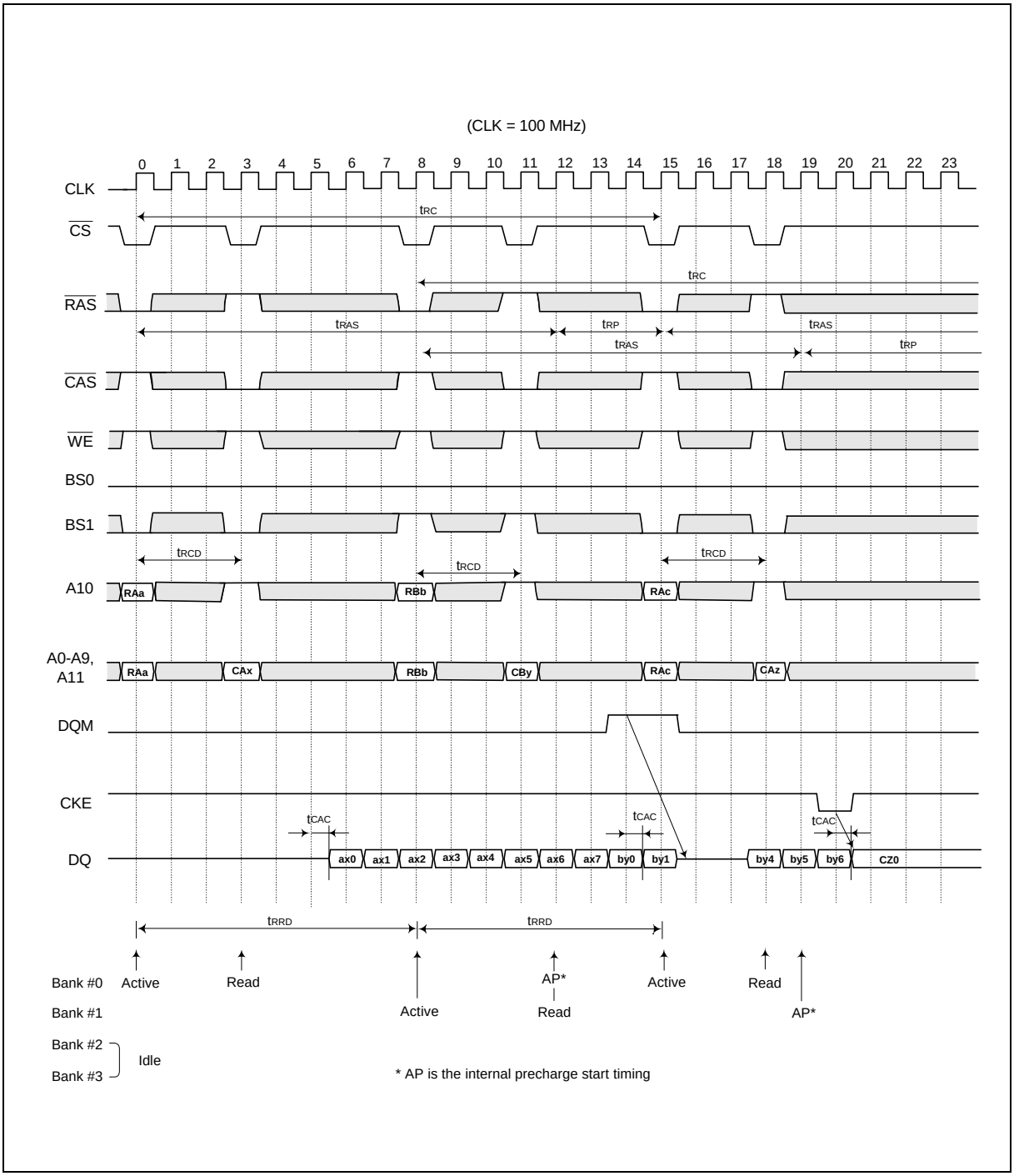
Operating Timing Example, contined

Interleaved Bank Read (Burst Length = 8, CAS Latency = 3)



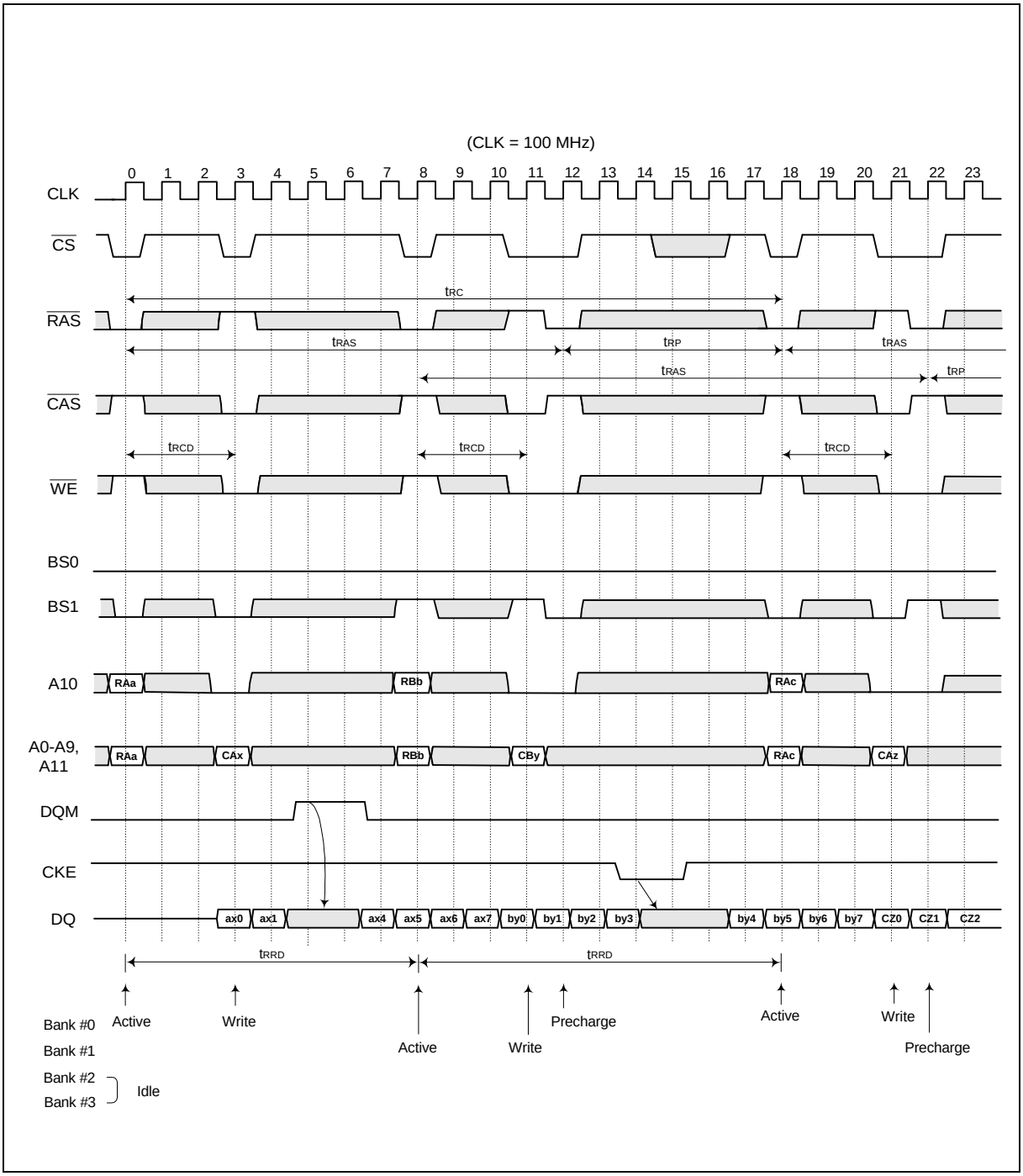
Operating Timing Example, contined

Interleaved Bank Read (Burst Length = 8, CAS Latency = 3, Autoprecharge)



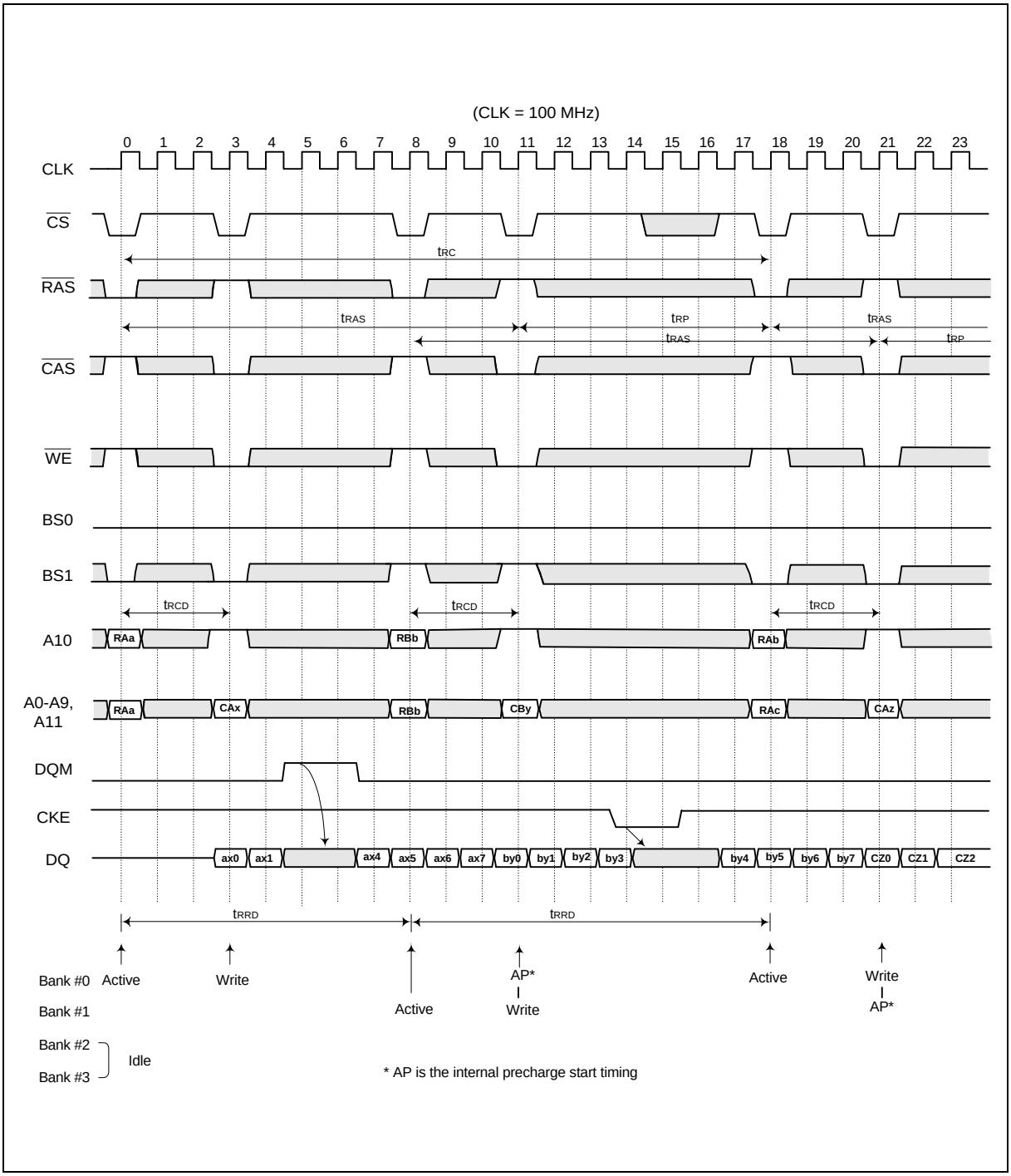
Operating Timing Example, contined

Interleaved Bank Write (Burst Length = 8)



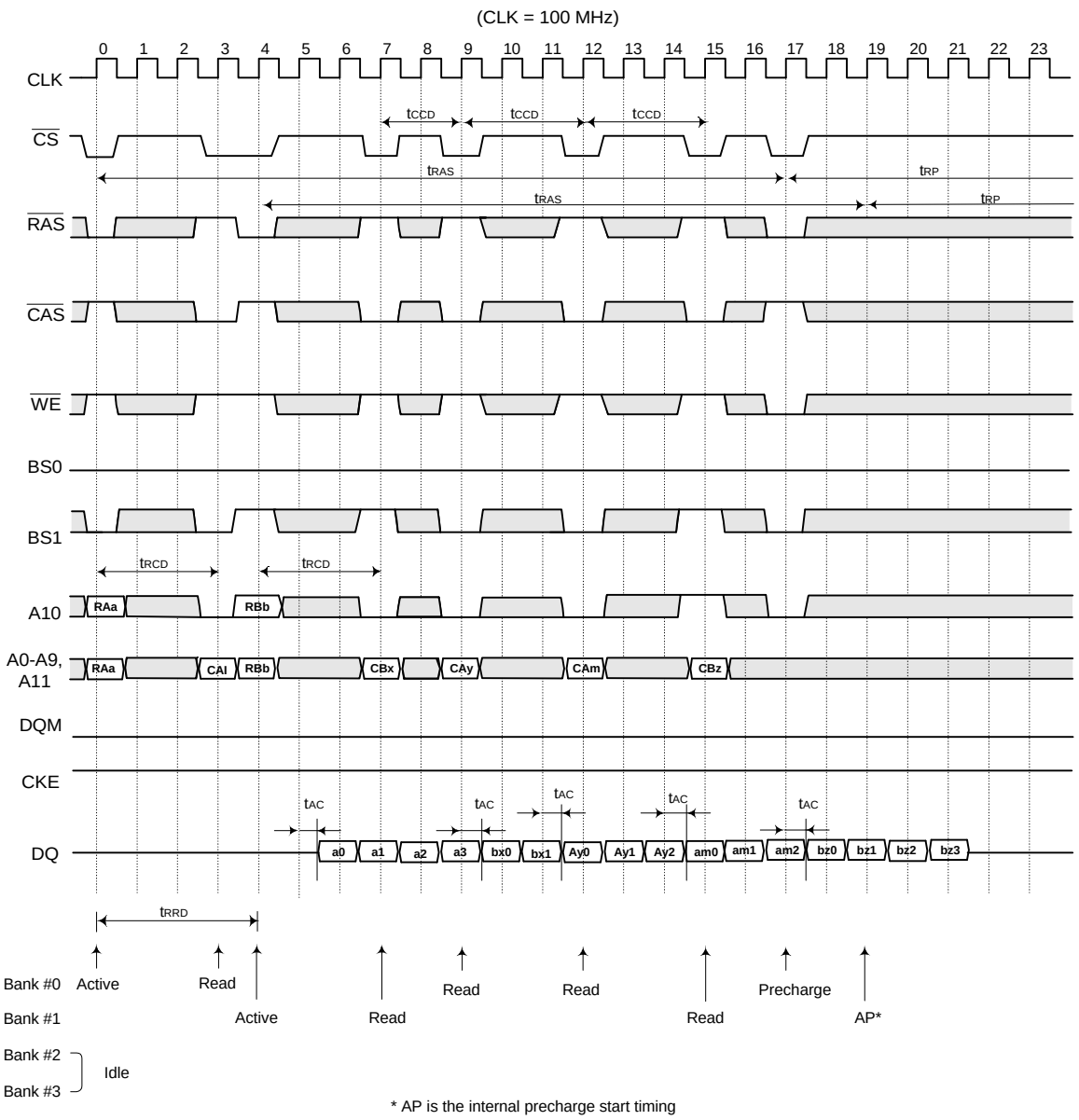
Operating Timing Example, contined

Interleaved Bank Write (Burst Length = 8, Autoprecharge)



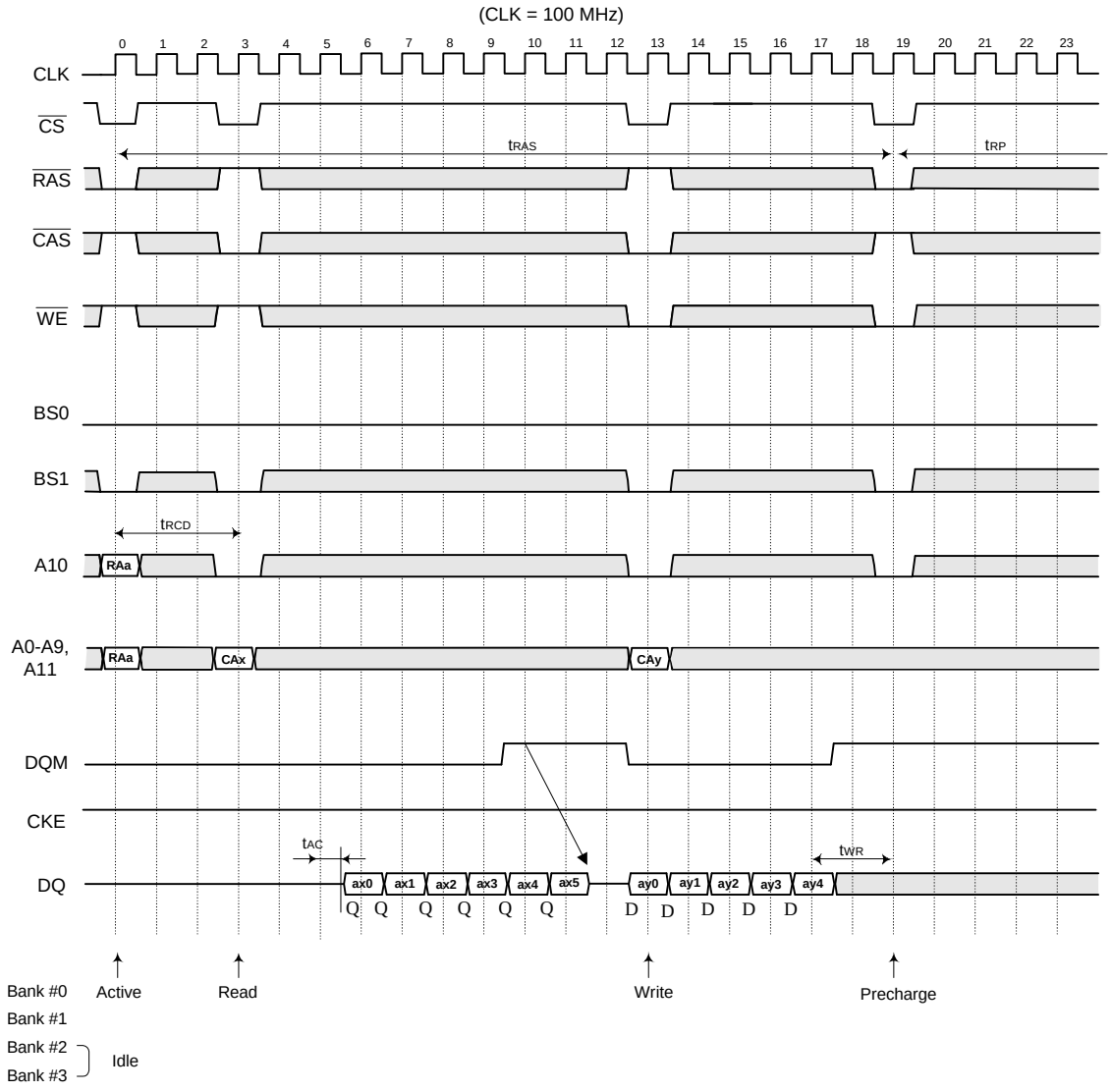
Operating Timing Example, contined

Page Mode Read (Burst Length = 4, CAS Latency = 3)



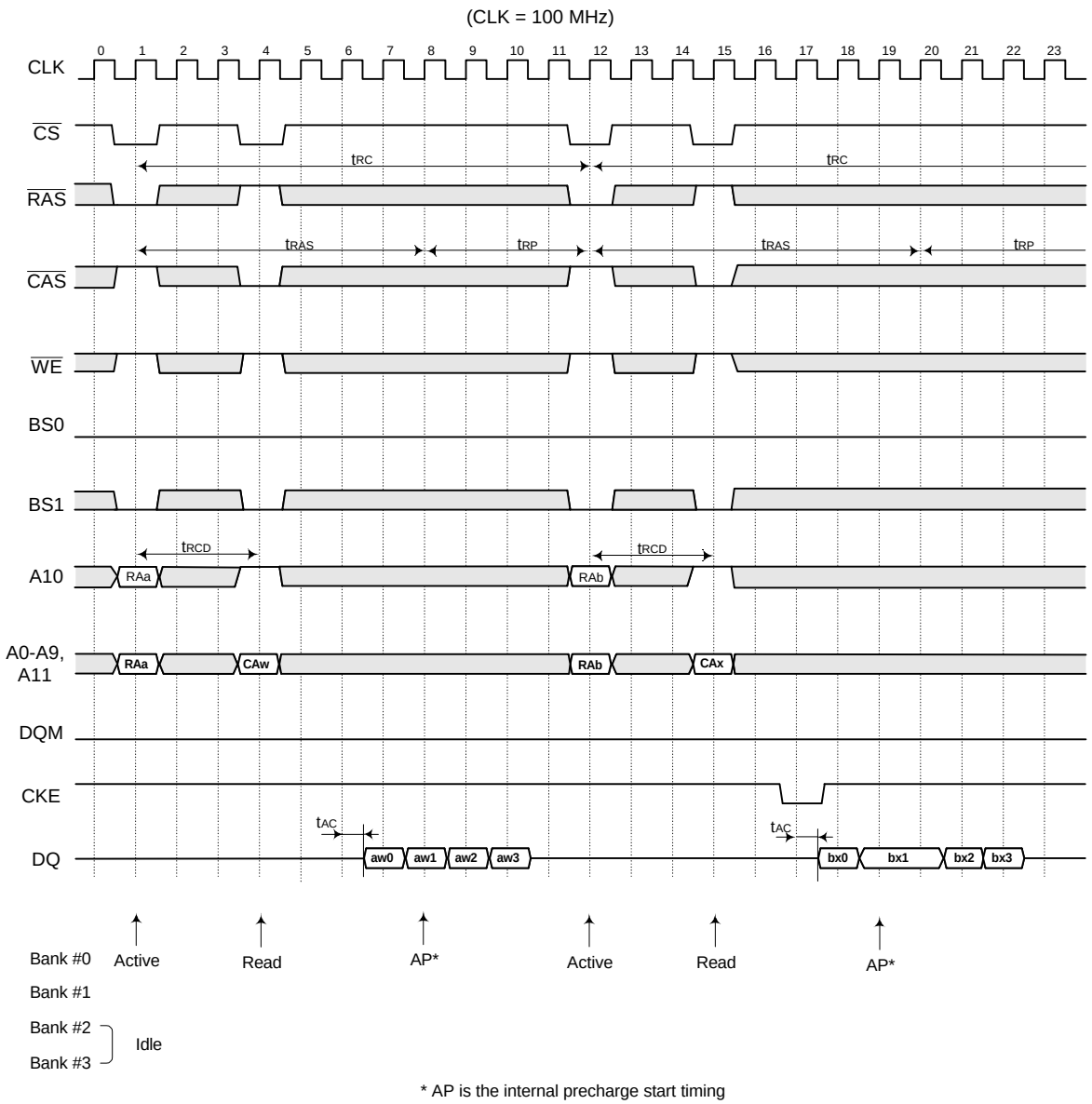
Operating Timing Example, contined

Page Mode Read / Write (Burst Length = 8, CAS Latency = 3)



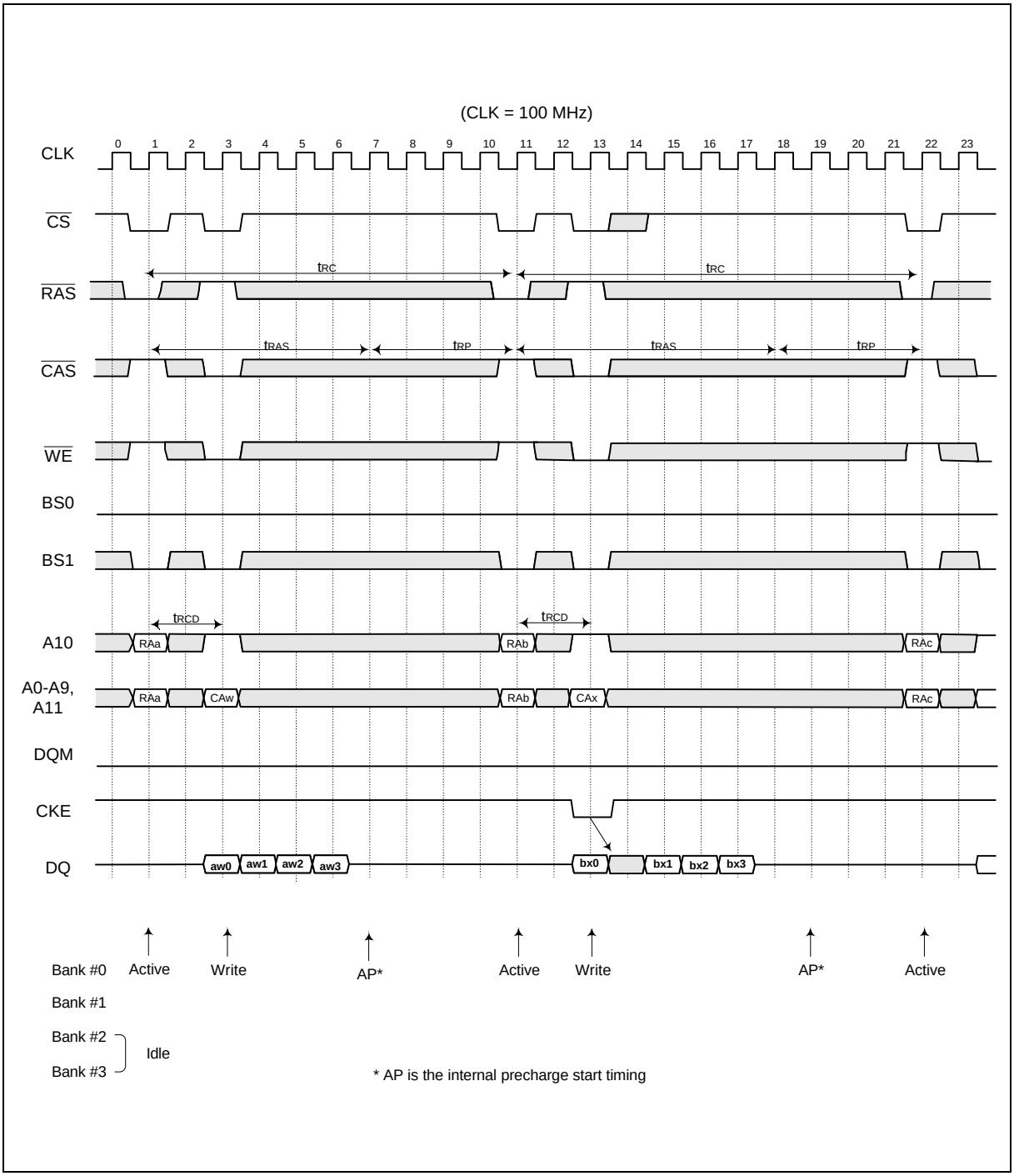
Operating Timing Example, contined

Auto Precharge Read (Burst Length = 4, CAS Latency = 3)



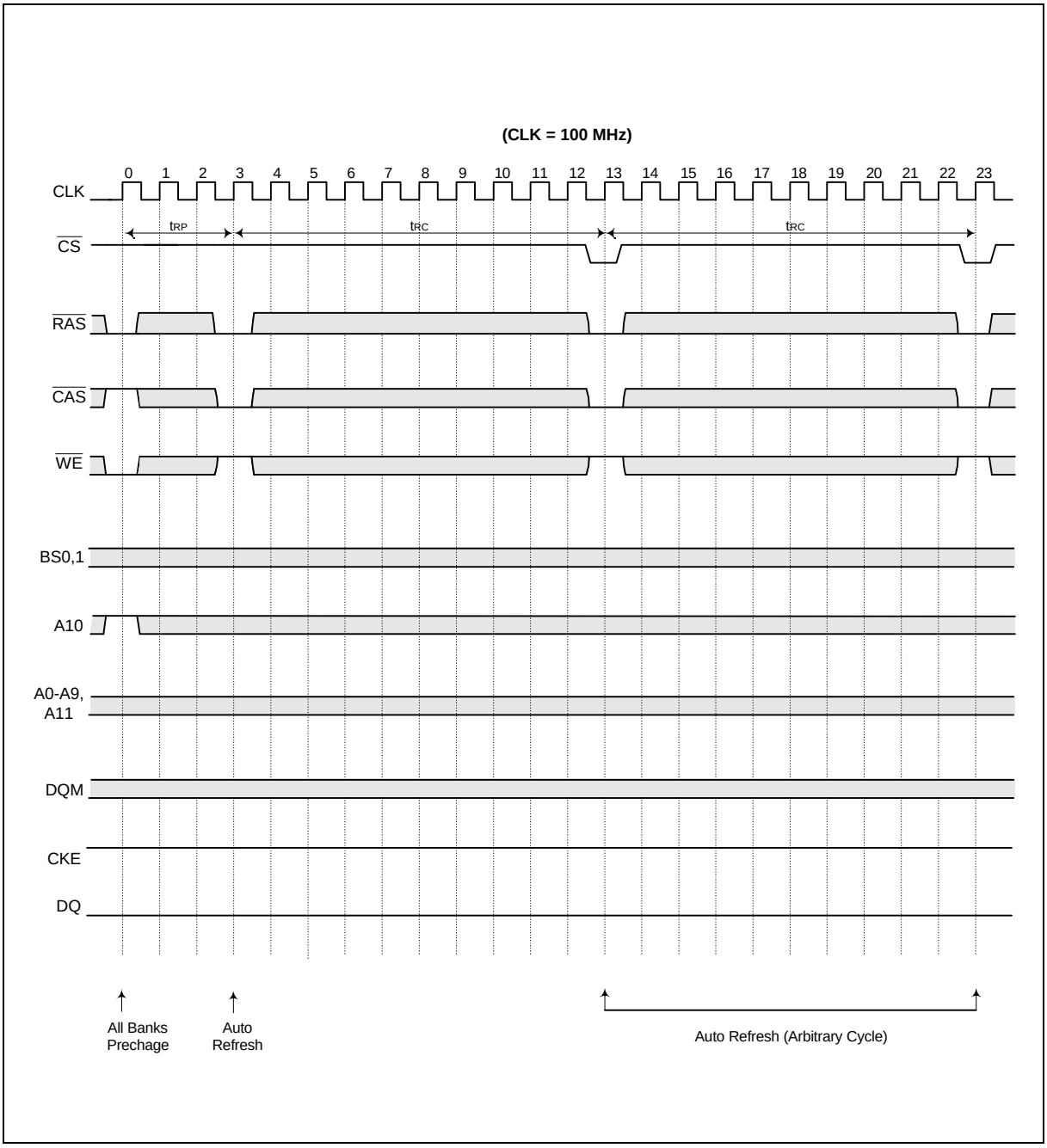
Operating Timing Example, contined

Auto Precharge Write (Burst Length = 4)



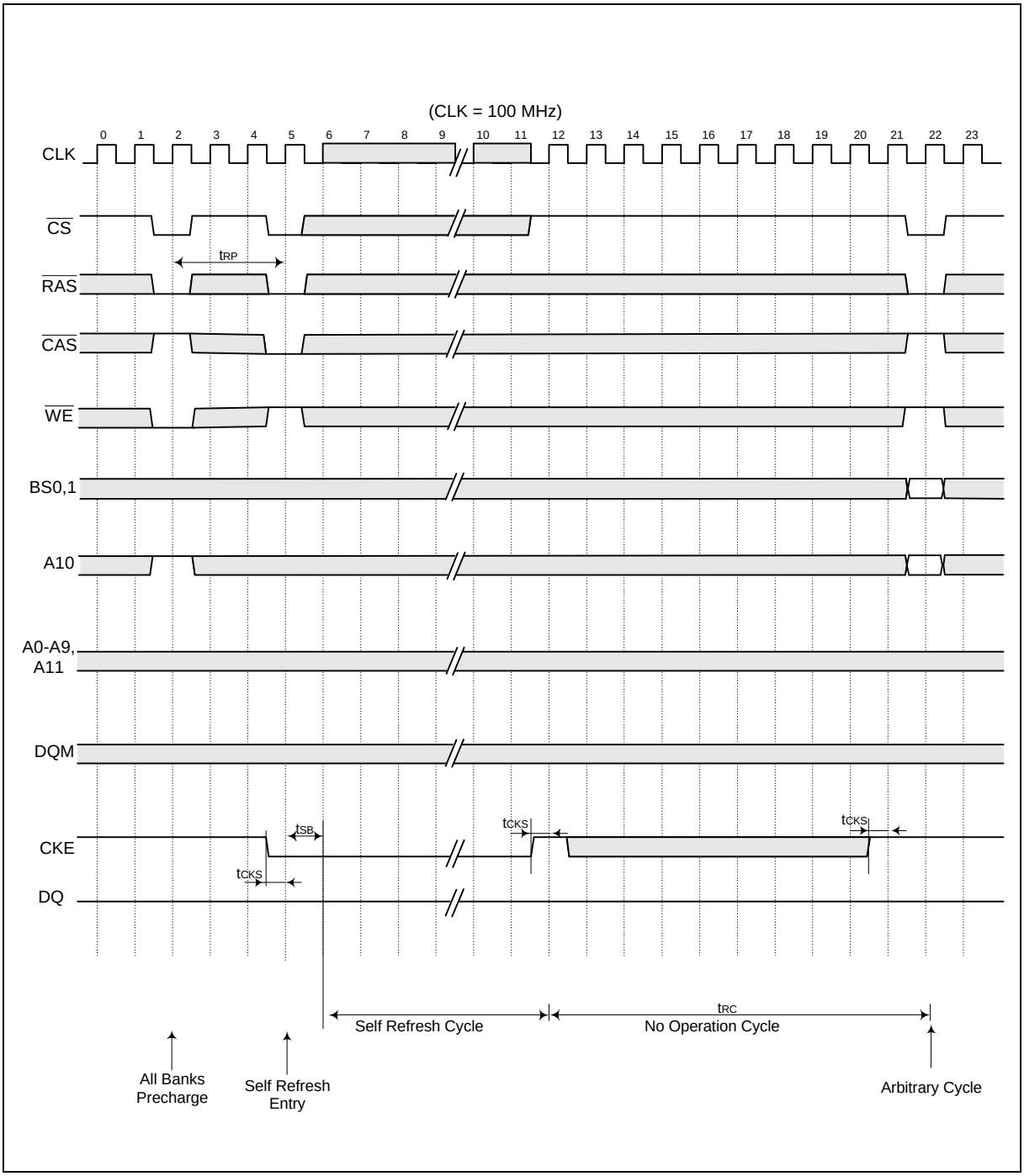
Operating Timing Example, contined

Auto Refresh Cycle



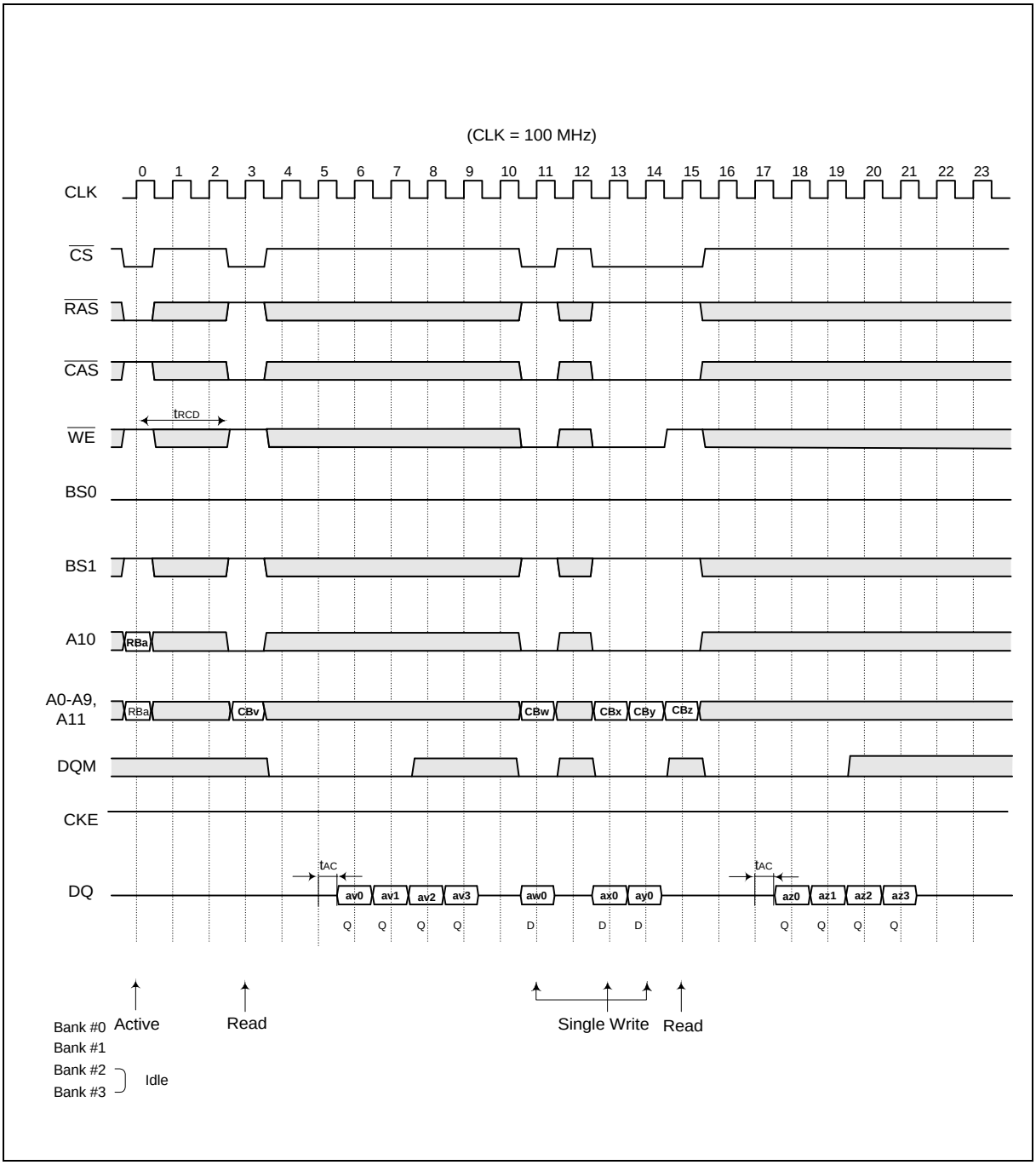
Operating Timing Example, contined

Self Refresh Cycle



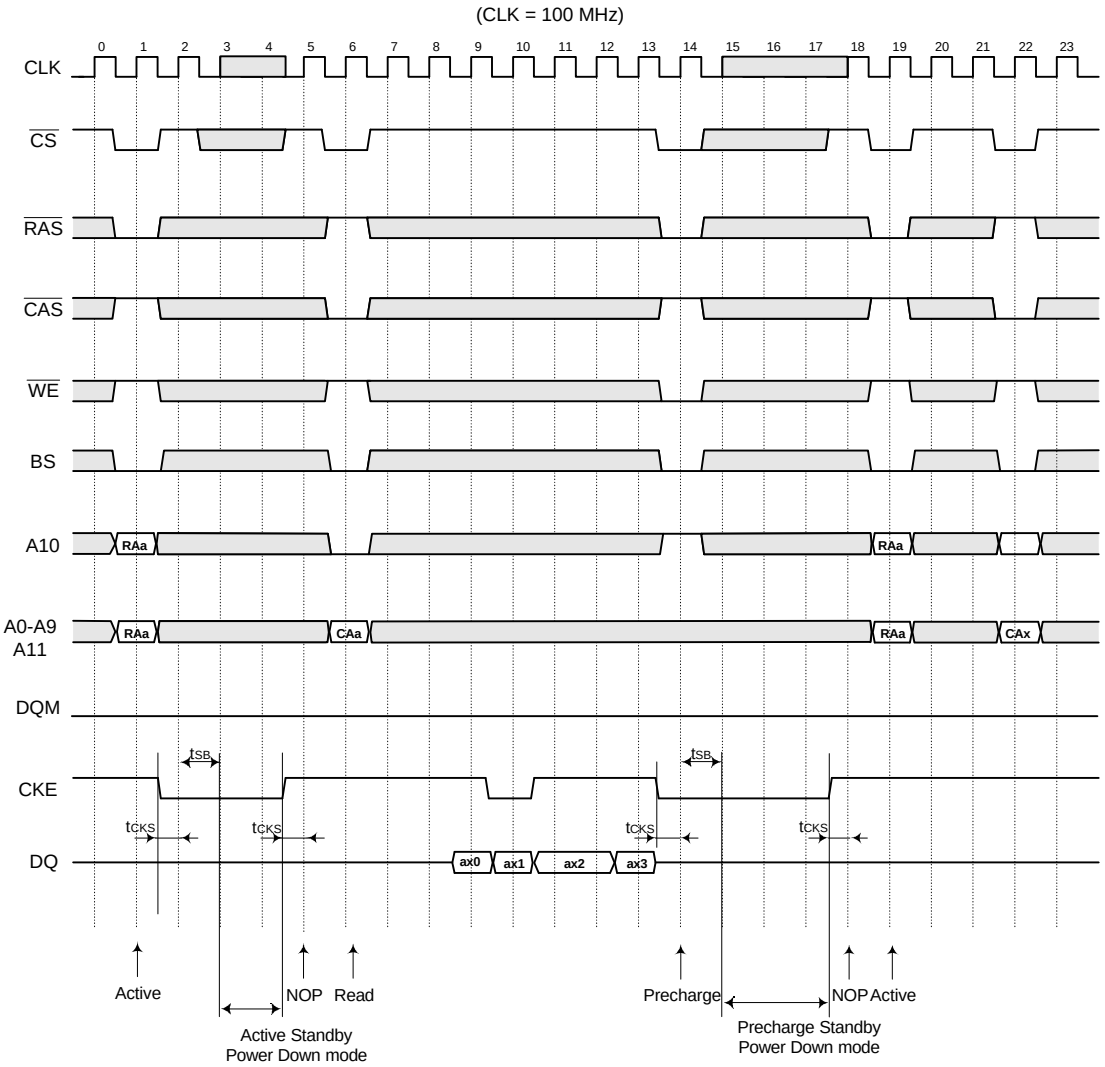
Operating Timing Example, contined

Burst Read and Single Write (Burst Length = 4, CAS Latency = 3)



Operating Timing Example, contined

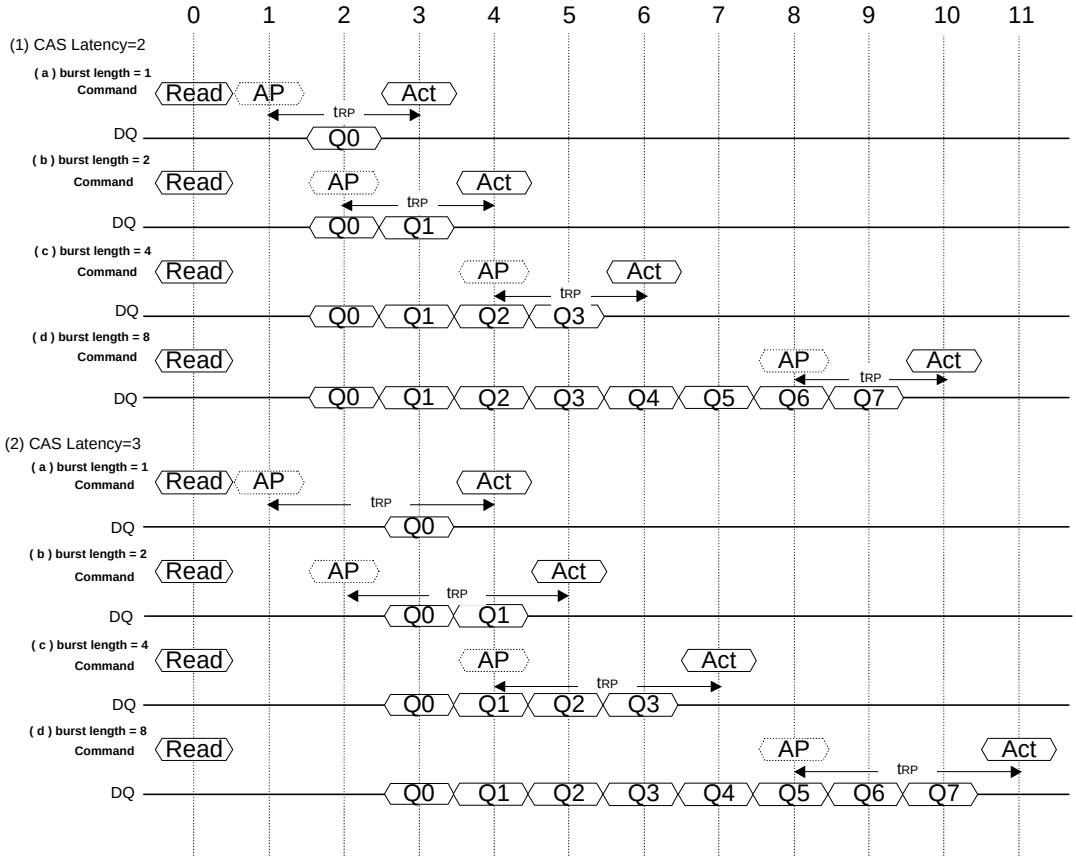
PowerDown Mode



Note: The PowerDown Mode is entered by asserting CKE "low".
All Input/Output buffers (except CKE buffers) are turned off in the PowerDown mode.
When CKE goes high, command input must be No operation at next CLK rising edge.

Operating Timing Example, contined

Autoprecharge Timing (Read Cycle)



Note)

Read represents the Read with Auto precharge command.

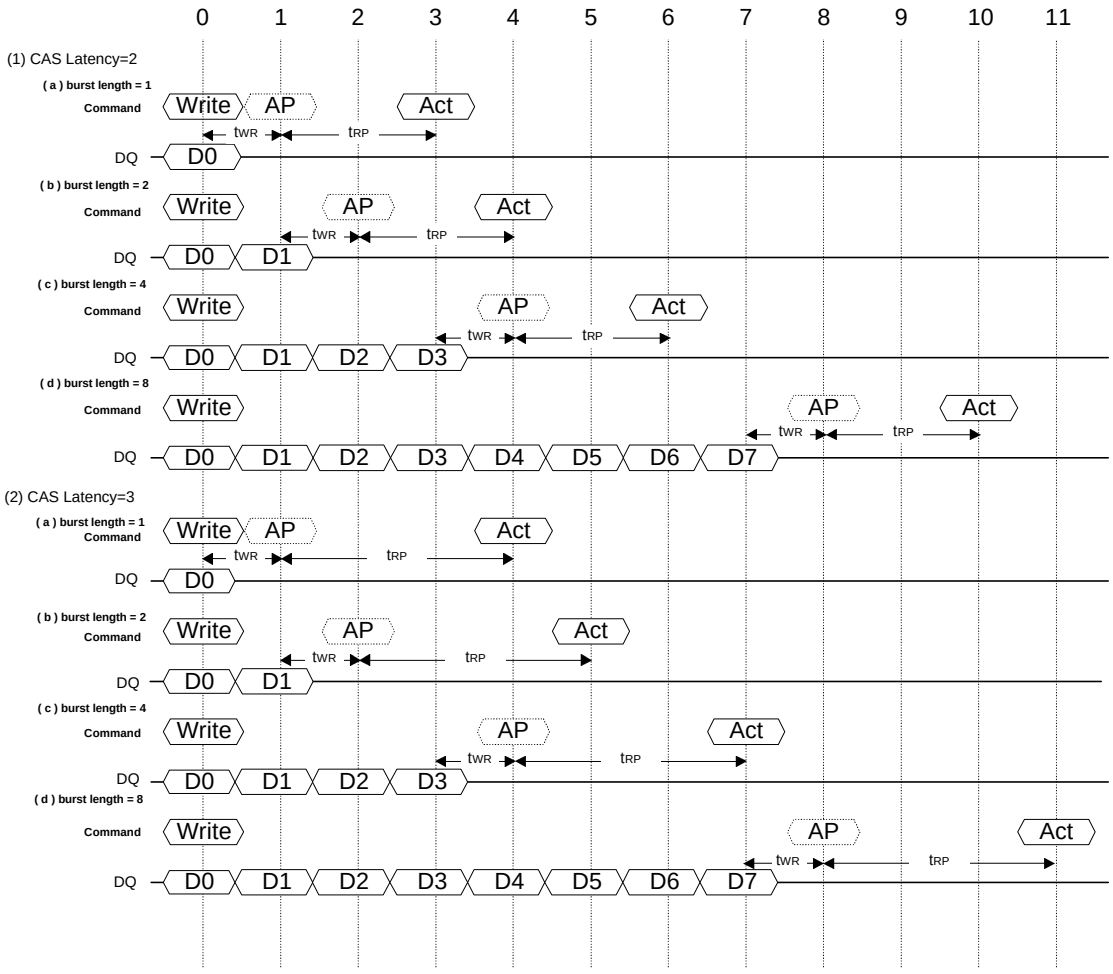
AP represents the start of internal precharging.

Act represents the Bank Activate command.

When the Auto precharge command is asserted, the period from Bank Activate command to the start of internal precgarging must be at least t_{RAS}(min).

Operating Timing Example, contined

Autoprecharge Timing (Write Cycle)



Note)

Write represents the Write with Auto precharge command.

AP represents the start of internal precharging.

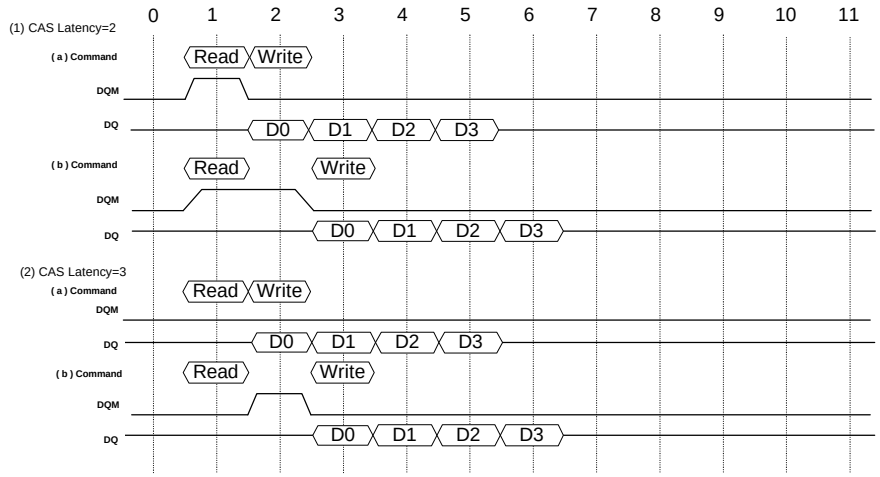
Act represents the Bank Activate command.

When the Auto precharge command is asserted, the period from Bank Activate command to the start of internal precgarging must be at least tRAS (min).

Operating Timing Example, contined

Timing Chart of Read to Write Cycle

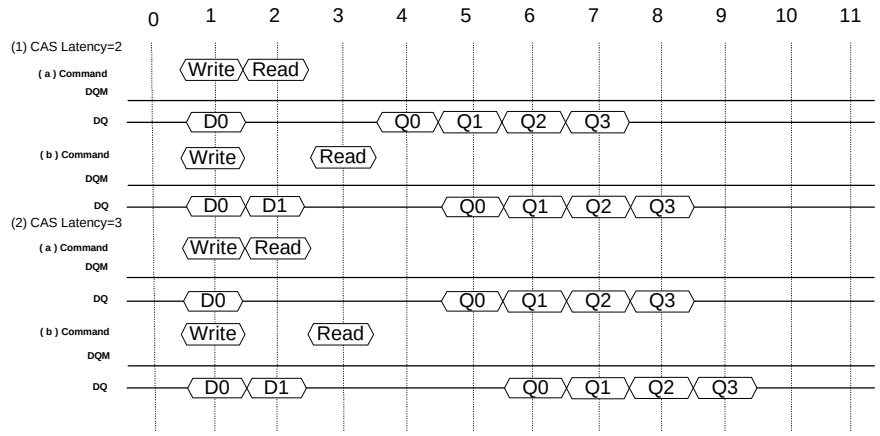
In the case of Burst Length = 4



Note: The Output data must be masked by DQM to avoid I/O conflict

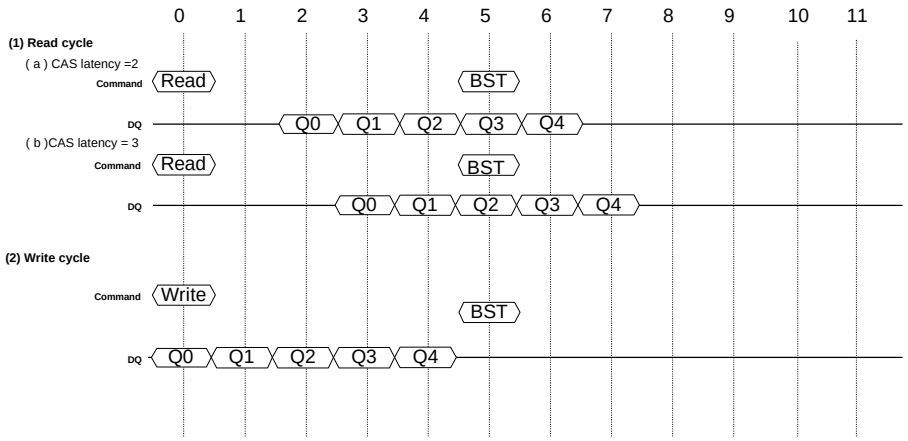
Timing Chart of Write to Read Cycle

In the case of Burst Length=4



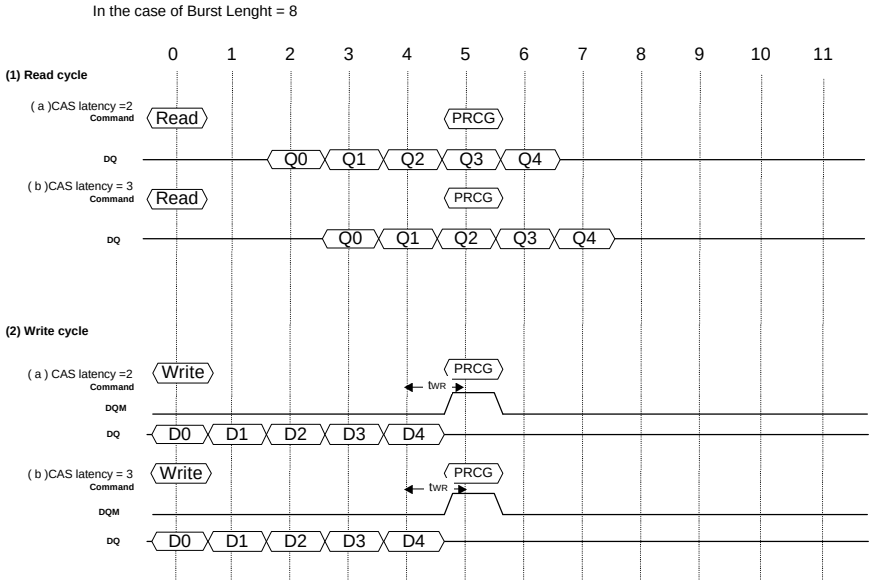
Operating Timing Example, contined

Timing Chart of Burst Stop Cycle (Burst Stop Command)



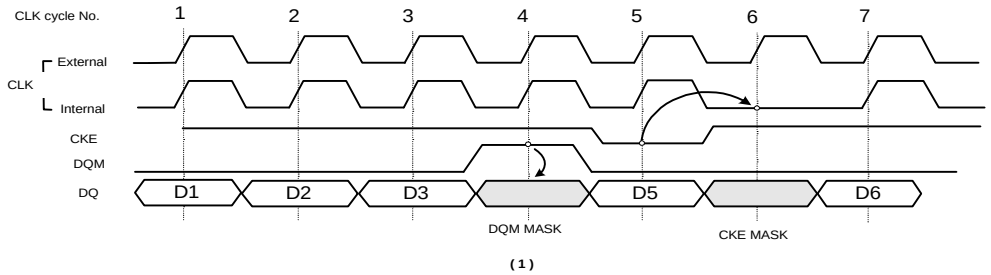
Note: BST represents the Burst stop command

Timing Chart of Burst Stop Cycle (Precharge Command)

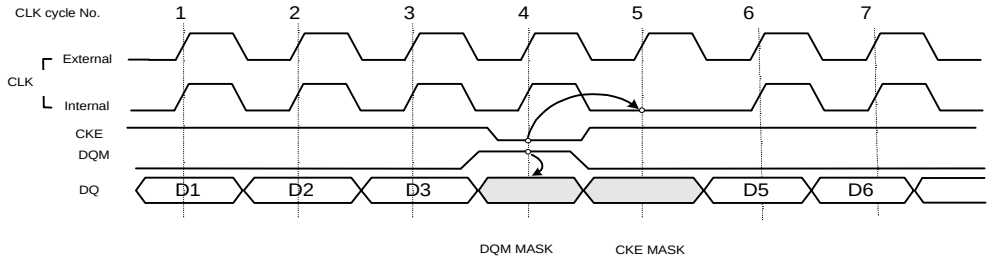


Operating Timing Example, contined

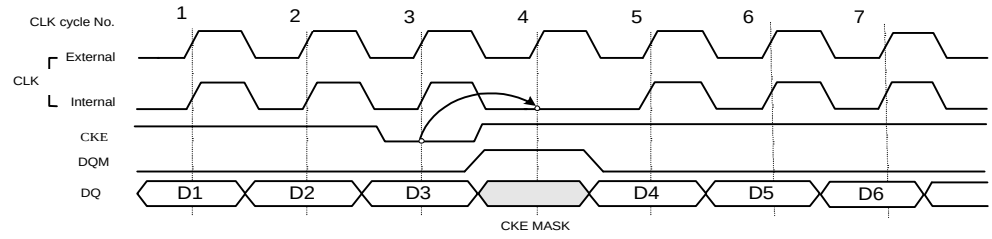
CKE/DQM Input Timing (Write Cycle)



(1)



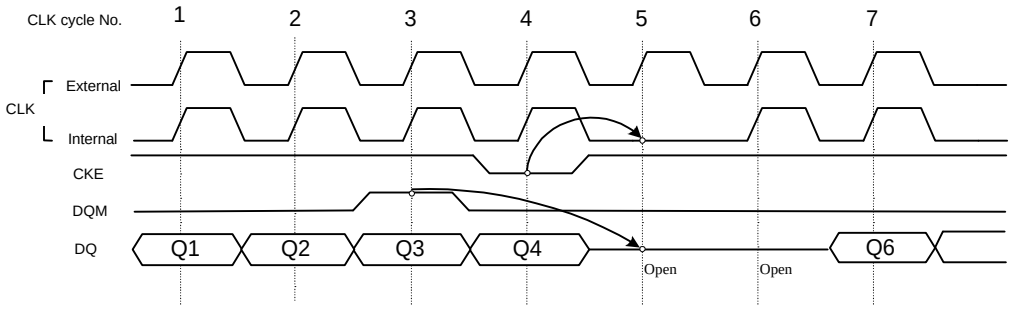
(2)



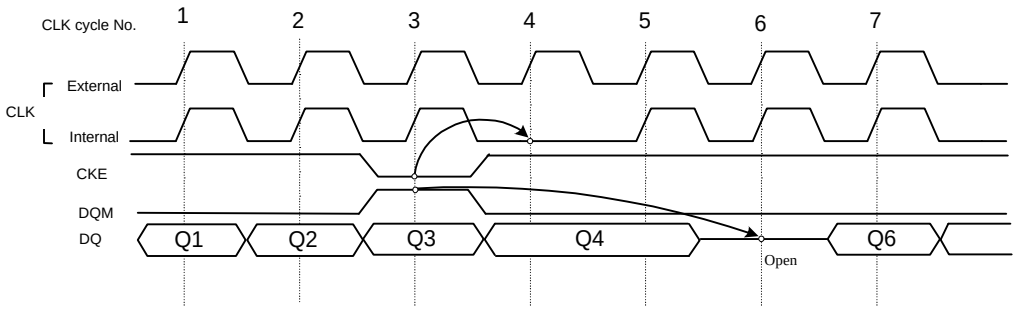
(3)

Operating Timing Example, contined

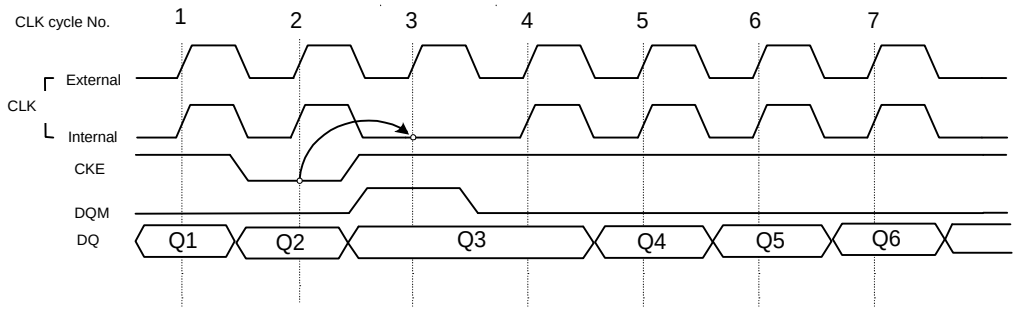
CKE/DQM Input Timing (Read Cycle)



(1)



(2)



(3)

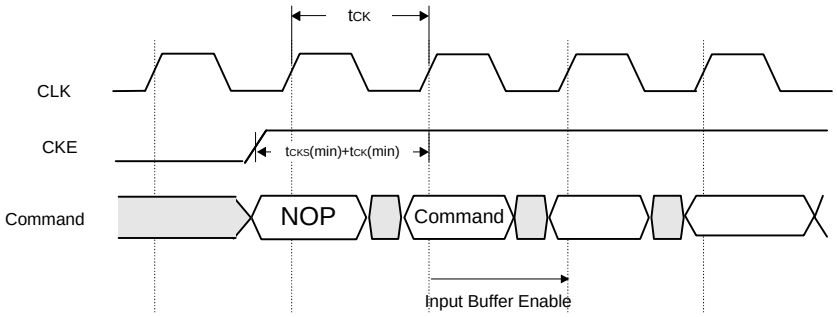
Operating Timing Example, contined

Self Refresh/Power Down Mode Exit Timing

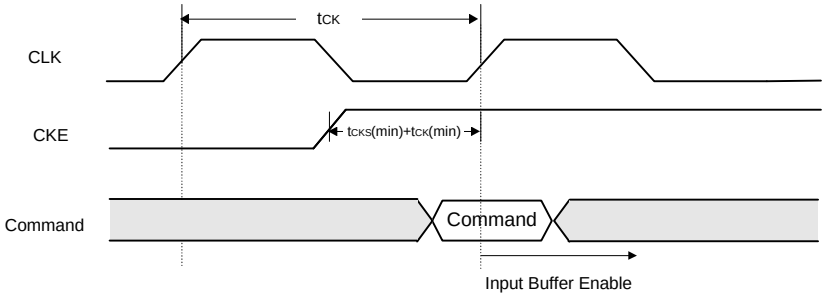
Asynchronous Control

Input Buffer turn on time (Power down mode exit time) is specified by tCKS(min) + tCK(min)

A) tCK < tCKS(min)+tCK(min)



B) tCK >= tCKS(min) + tCK (min)



Note)

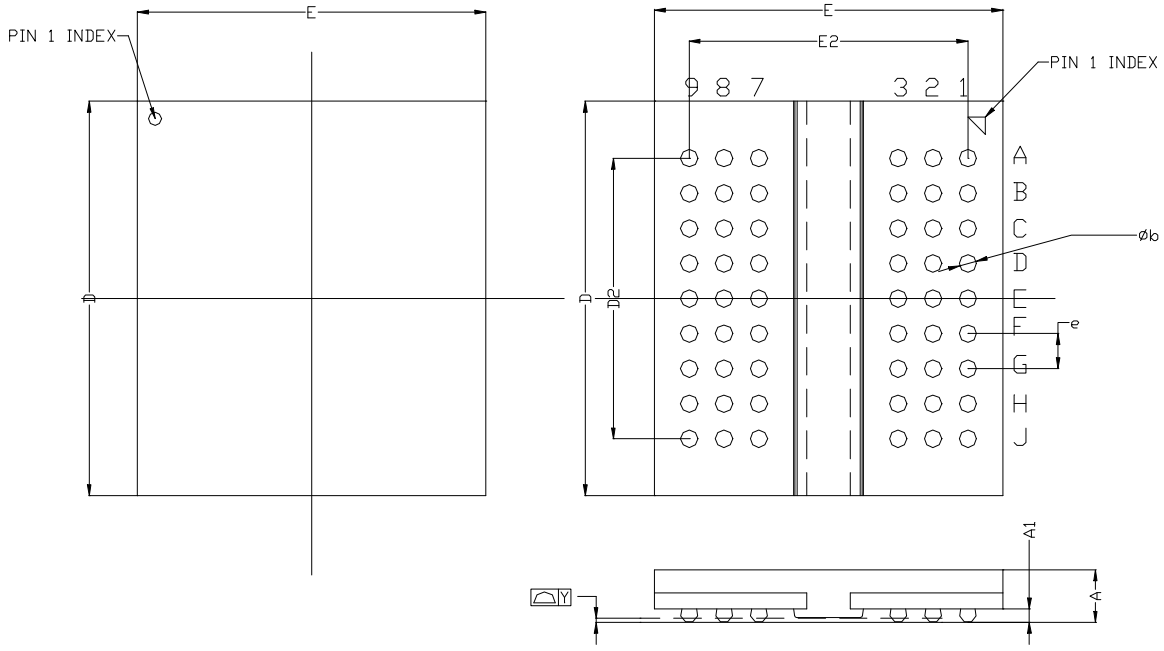
All Input Buffer(Include CLK Buffer) are turned off in the Power Down mode and Self Refresh mode

NOP — Represents the No-Operation command

Command — Represents one command

15. PACKAGE DIMENSION

FBGA 54 Balls (8 x 9 x 1.2 mm^3, Ø = 0.40 mm)



SYMBOL	DIMENSION (MM)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.97	1.1	1.2	0.038	0.043	0.047
A1	0.25	0.30	0.35	0.001	0.012	0.014
D	8.9	9.0	9.1	0.350	0.354	0.358
D2		6.4 BSC.			0.252 BSC.	
E	7.9	8.0	8.1	0.311	0.315	0.319
E2		6.40 BSC.			0.252 BSC.	
b	0.35	–	0.45	0.014	–	0.018
ccc		0.10			0.004	
e		0.8 BSC.			0.031 BSC.	

16. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	May 21, 2002	-	Initial Issued

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