

Preliminary W26B041



256K ´ 16 CMOS STATIC RAM

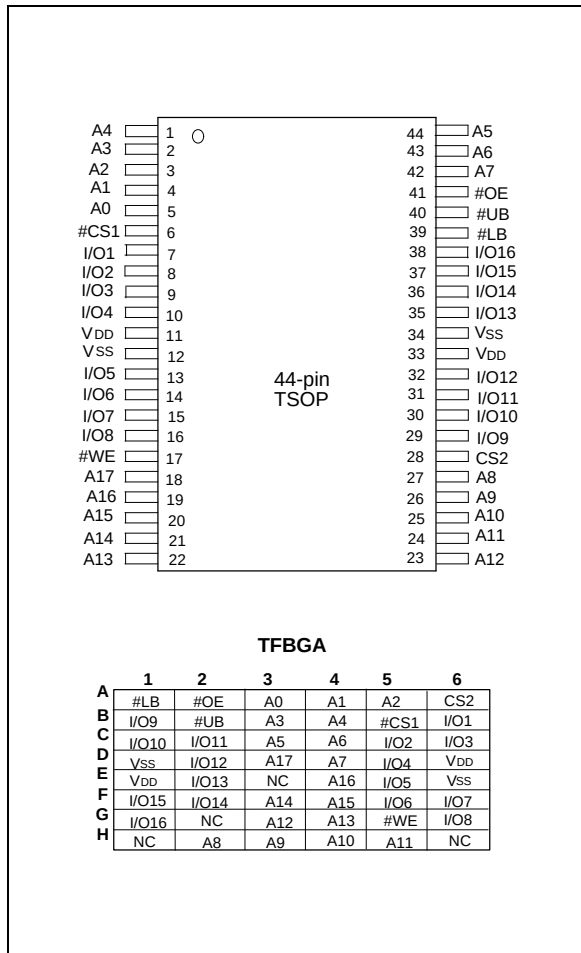
GENERAL DESCRIPTION

The W26B041 is a normal-speed, very low-power CMOS static RAM organized as 262144 × 16 bits that operates on a wide voltage range from 2.7V to 3.6V power supply. The W26B041, W26B041-LE and W26B041-LI, can meet the requirement of various operating temperature. This device is manufactured using Winbond's high performance CMOS technology.

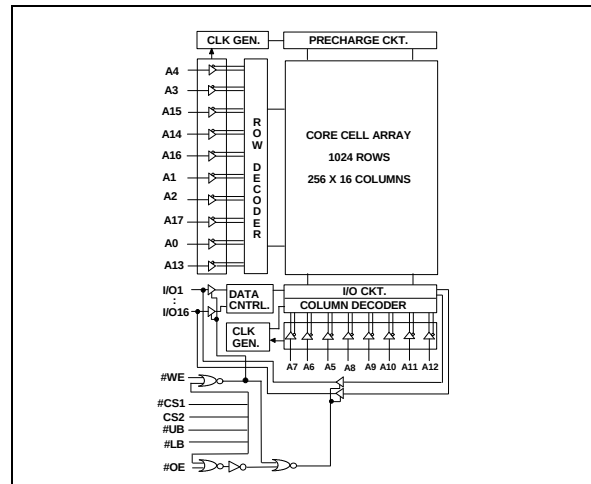
FEATURES

- Low power consumption
- Access time: 70 nS
- 2.7V to 3.6V supply voltage
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three-state outputs
- Battery back-up operation capability
- Data retention voltage: 1.5V (min.)
- Data byte control
 - #LB (I/O1 – I/O8), #UB (I/O9 – I/O16)
- Available packages: 44-pin type two TSOP, and TFBGA

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 – A17	Address Inputs
I/O1 – I/O16	Data Inputs/Outputs
#CS1	Chip Select Input 1, Low Active
CS2	Chip Select Input 2, High Active
#WE	Write Enable Input
#LB	Lower byte select
#UB	Upper byte select
#OE	Output Enable Input
VDD	Power Supply
VSS	Ground
NC	No Connection

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TRUTH TABLE

#CS1	CS2	#OE	#WE	#LB	#UB	MODE	I/O1 - I/O8	I/O9 - I/O16	VDD CURRENT
H	X	X	X	X	X	Not Selected	High Z	High Z	ISB, ISB1
X	L	X	X	X	X	Not Selected	High Z	High Z	ISB, ISB1
X	X	X	X	H	H	Not Selected	High Z	High Z	ISB, ISB1
L	H	H	H	X	X	Output Disable	High Z	High Z	IDD
L	H	L	H	L	L	2 Bytes Read	DOUT	DOUT	IDD
L	H	L	H	L	H	Lower Byte Read	DOUT	High Z	IDD
L	H	L	H	H	L	Upper Byte Read	High Z	DOUT	IDD
L	H	X	L	L	L	2 Bytes Write	DIN	DIN	IDD
L	H	X	L	L	H	Lower Byte Write	DIN	High Z	IDD
L	H	X	L	H	L	Upper Byte Write	High Z	DIN	IDD

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DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER		RATING	UNIT
Supply Voltage to Vss Potential		-0.5 to +4.6	V
Input/Output to Vss Potential		-0.5 to V _{DD} +0.5	V
Allowable Power Dissipation		1.0	W
Storage Temperature		-65 to +150	°C
Operating Temperature	LE	-20 to 85	°C
	LI	-40 to 85	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

Operating Characteristics

(V_{SS} = 0V; T_A (°C) = -20 to 85 for LE, -40 to 85 for LI)

PARAMETER	SYM.	TEST CONDITIONS	W26B041		UNIT
			MIN.	MAX.	
Operating Power Voltage	V _{DD}	-	2.7	3.6	V
Input Low Voltage	V _{IL}	-	-0.2	+0.4	V
Input High Voltage	V _{IH}	-	+2.2	V _{DD} +0.3	V
Input Leakage Current	I _{LI}	V _{IN} = V _{SS} to V _{DD}	-1	+1	μA
Output Leakage Current	I _{LO}	V _{I/O} = V _{SS} to V _{DD} ; #CS1 = V _{IH} (min.) or CS2 = V _{IL} (max.) or #OE = V _{IH} (min.) or #WE = V _{IL} (max.)	-1	+1	μA
Output Low Voltage	V _{OL}	I _{OL} = +2.1 mA	-	0.4	V
Output High Voltage	V _{OH}	I _{OH} = -1.0 mA	2.4	-	V
Operating Power Supply Current	I _{DD}	#CS1 = V _{IL} (max.) and CS2 = V _{IH} (min.), I/O = 0 mA; Cycle = min. Duty = 100%	-	40	mA
Standby Power Supply Current	I _{SB}	#CS1 = V _{IH} (min.) or CS2 = V _{IL} (max.)	-	0.3	mA
	I _{SB1}	#CS1 ≥ V _{DD} - 0.2V, CS2 ≥ V _{DD} - 0.2V or #CS1 ≤ 0.2V, CS2 ≤ 0.2V	-	10	μA



CAPACITANCE

($T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

PARAMETER	SYM.	CONDITIONS	MAX.	UNIT
Input Capacitance	C_{IN}	$V_{IN} = 0V$	8	pF
Input/Output Capacitance	$C_{I/O}$	$V_{OUT} = 0V$	10	pF

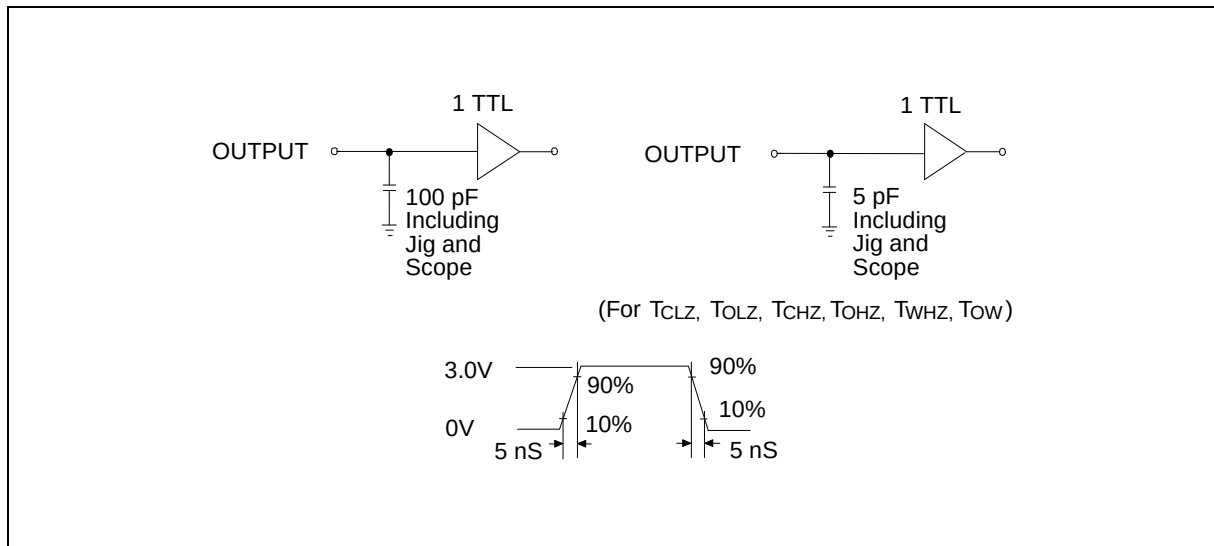
Note: These parameters are sampled but not 100% tested.

AC CHARACTERISTICS

AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5 nS
Input and Output Timing Reference Level	1.5V
Output Load	See the drawing below

AC Test Loads and Waveform



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AC Characteristics, continued

(V_{SS} = 0V; T_A (°C) = -20 to 85 for LE, -40 to 85 for LI)

Read Cycle

PARAMETER	SYMBOL	W26B041		UNIT
		MIN.	MAX.	
Read Cycle Time	TRC	70	-	nS
Address Access Time	TAA	-	70	nS
Chip Select Access Time	TACS	-	70	nS
Output Enable to Output Valid	TAOE	-	35	nS
#UB, #LB Access Tim	TBA	-	70	nS
Chip Selection to Output in Low Z	TCLZ*	10	-	nS
Output Enable to Output in Low Z	TOLZ*	5	-	nS
#UB, #LB Enable to Output in Low Z	TBLZ*	5	-	nS
Chip Deselection to Output in High Z	TCHZ*	-	30	nS
Output Disable to Output in High Z	TOHZ*	-	30	nS
#UB, #LB Disable to Output in High Z	TBHZ*	-	30	nS
Output Hold from Address Change	TOH	10	-	nS

*These parameters are sampled but not 100% tested

Write Cycle

PARAMETER		SYMBOL	W26B041		UNIT
			MIN.	MAX.	
Write Cycle Time		TWC	70	-	nS
Chip Selection to End of Write		TcW	60	-	nS
Address Valid to End of Write		TAW	60	-	nS
#UB, #LB Select to End of Write		TBW	60	-	nS
Address Setup Time		TAS	0	-	nS
Write Pulse Width		TWP	55	-	nS
Write Recovery Time	#CS1, CS2, #WE	TWR	0	-	nS
Data Valid to End of Write		TdW	40	-	nS
Data Hold from End of Write		TdH	0	-	nS
Write to Output in High Z		TWHZ*	-	30	nS
Output Disable to Output in High Z		TOHZ*	-	30	nS
Output Active from End of Write		TOW	5	-	nS

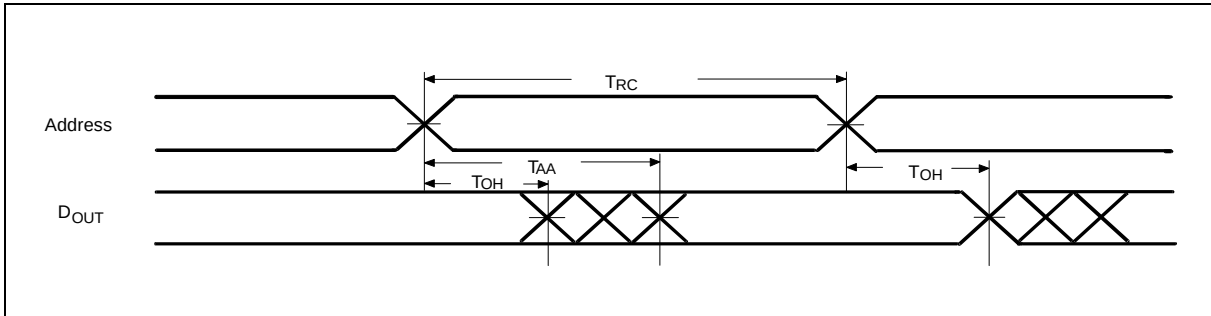
*These parameters are sampled but not 100% tested



TIMING WAVEFORMS

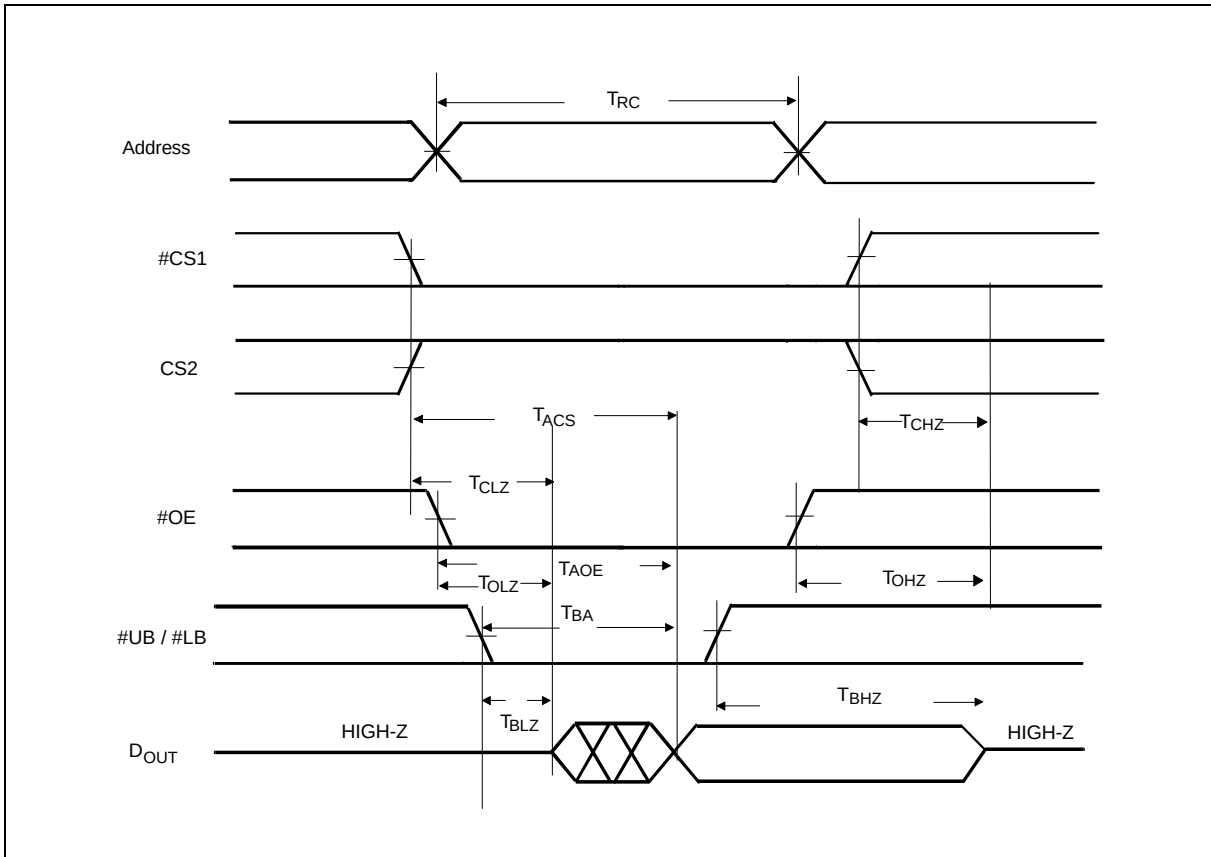
Read Cycle 1

(Address Controlled)



Read Cycle 2

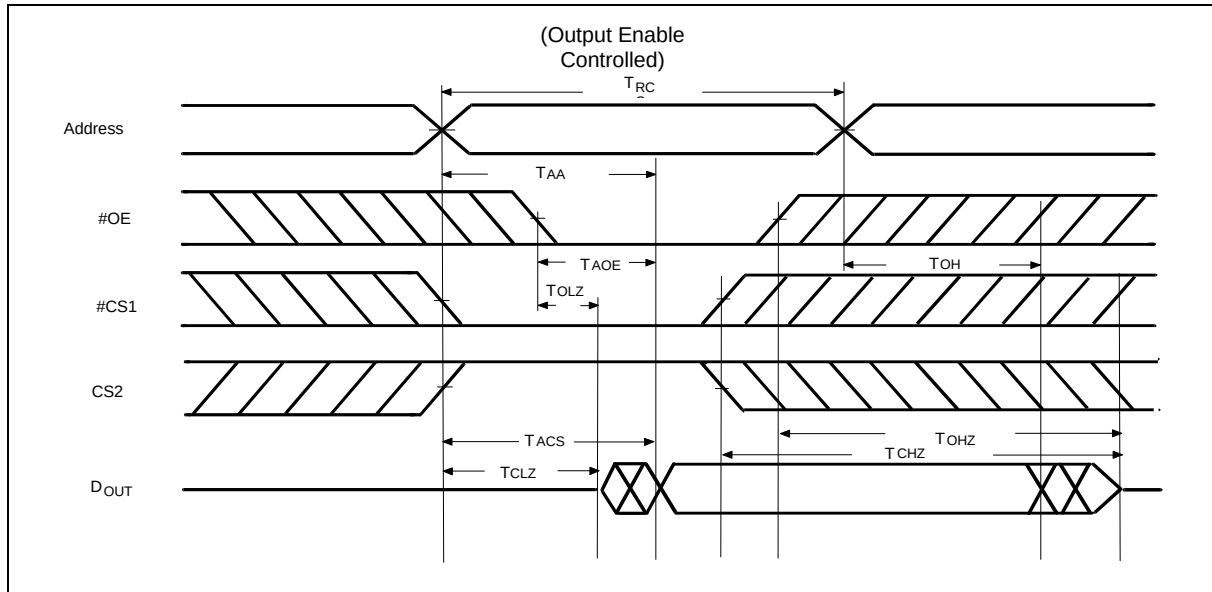
(Chip Select Controlled, #OE = V_{IL}, #WE = V_{IH})





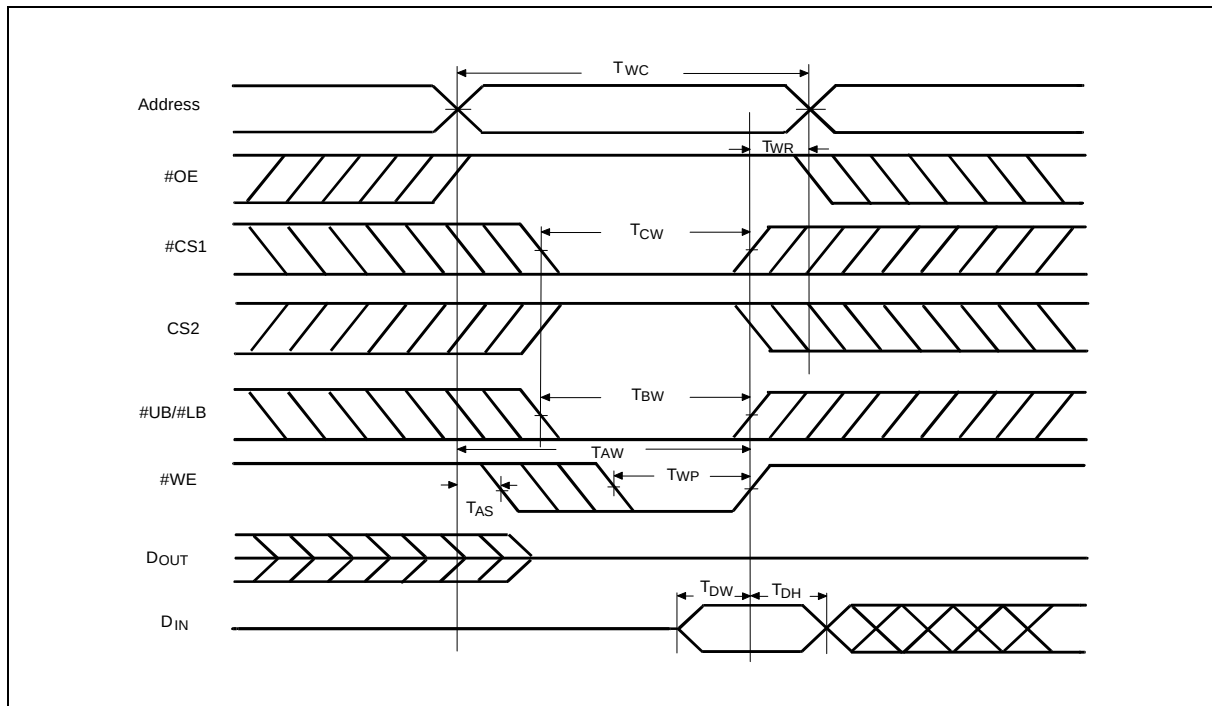
Timing Waveforms, continued

Read Cycle 3



Write Cycle 1

(#OE Clock)

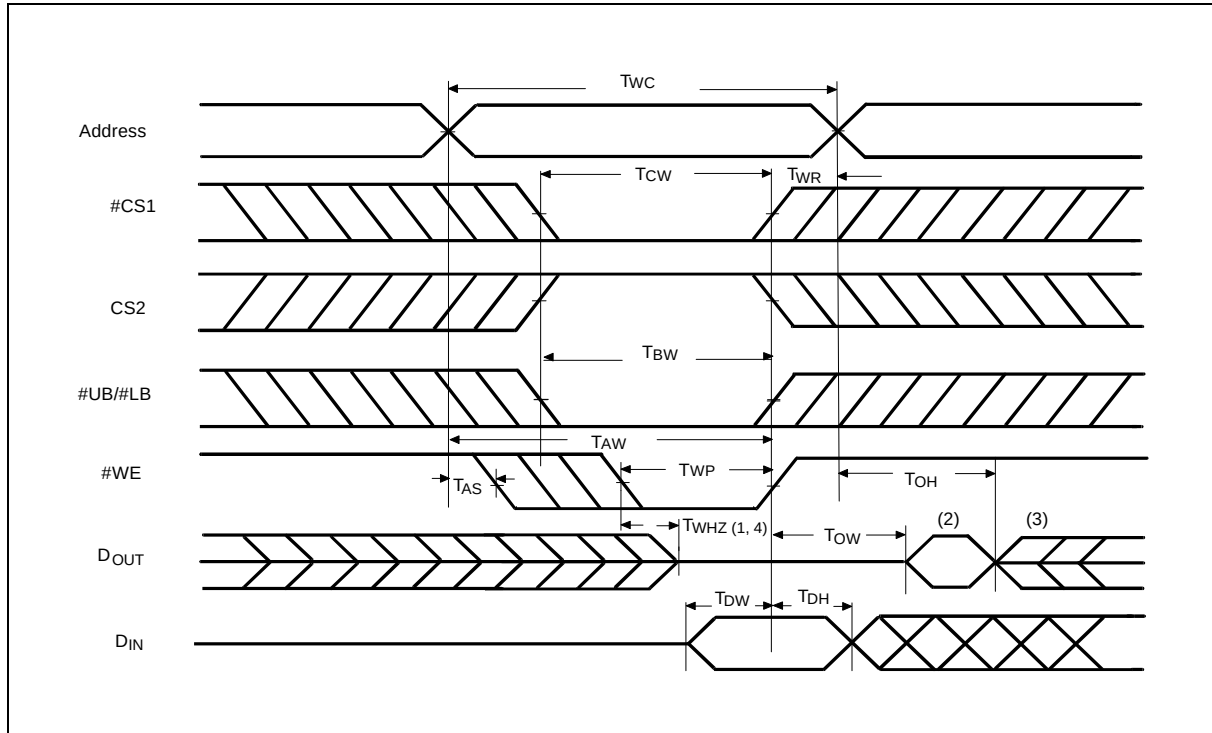




Timing Waveforms, continued

Write Cycle 2

(#OE = V_{IL} Fixed)



Notes:

1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from D_{OUT} are the same as the data written to D_{IN} during the write cycle.
3. D_{OUT} provides the read data for the next address.
4. Transition is measured ± 500 mV from steady state with $C_L = 5$ pF. This parameter is guaranteed but not 100% tested.



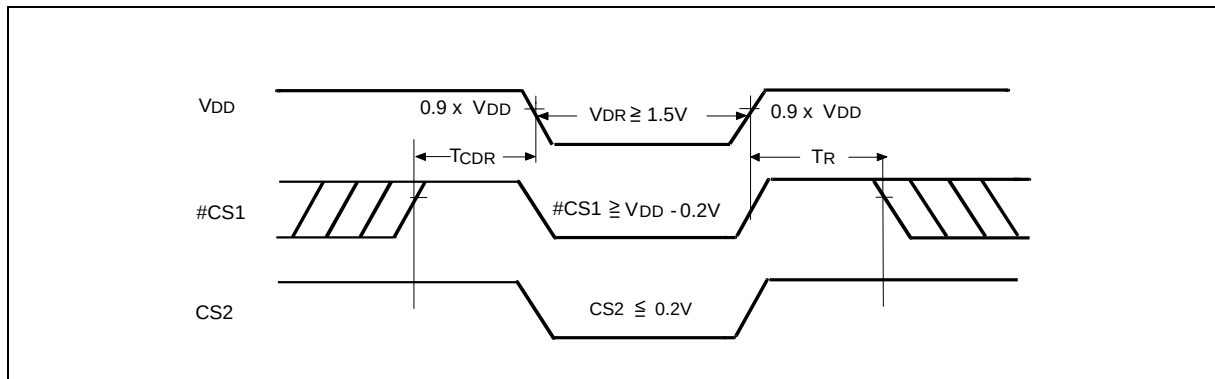
DATA RETENTION CHARACTERISTICS

(T_A (°C) = -20 to 85 for LE; -40 to 85 for LI)

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{DD} for Data Retention	V _{DR}	#CS1 ≥ V _{DD} - 0.2V or CS2 ≤ 0.2V	1.5	-	-	V
Data Retention Current	I _{DDDR}	#CS1 ≥ V _{DD} - 0.2V or CS2 ≤ 0.2V, V _{DD} = 3.0V	-	-	10	μA
Chip Deselect to Data Retention Time	T _{CDR}	See data retention waveform	0	-	-	nS
Operation Recovery Time	T _R		T _{RC} *	-	-	nS

* Read Cycle Time

DATA RETENTION WAVEFORM



ORDERING INFORMATION

PART NO.	ACCESS TIME (nS)	OPERATING VOLTAGE (V) STANDBY CURRENT (μA)	OPERATING TEMPERATURE (°C)	PACKAGE
W26B041B70LE	70	3V/10 μA	-20 to 85	TFBGA
W26B041H70LE	70	3V/10 μA	-20 to 85	TSOP(II)
W26B041B70LI	70	3V/10 μA	-40 to 85	TFBGA
W26B041H70LI	70	3V/10 μA	-40 to 85	TSOP(II)

Notes:

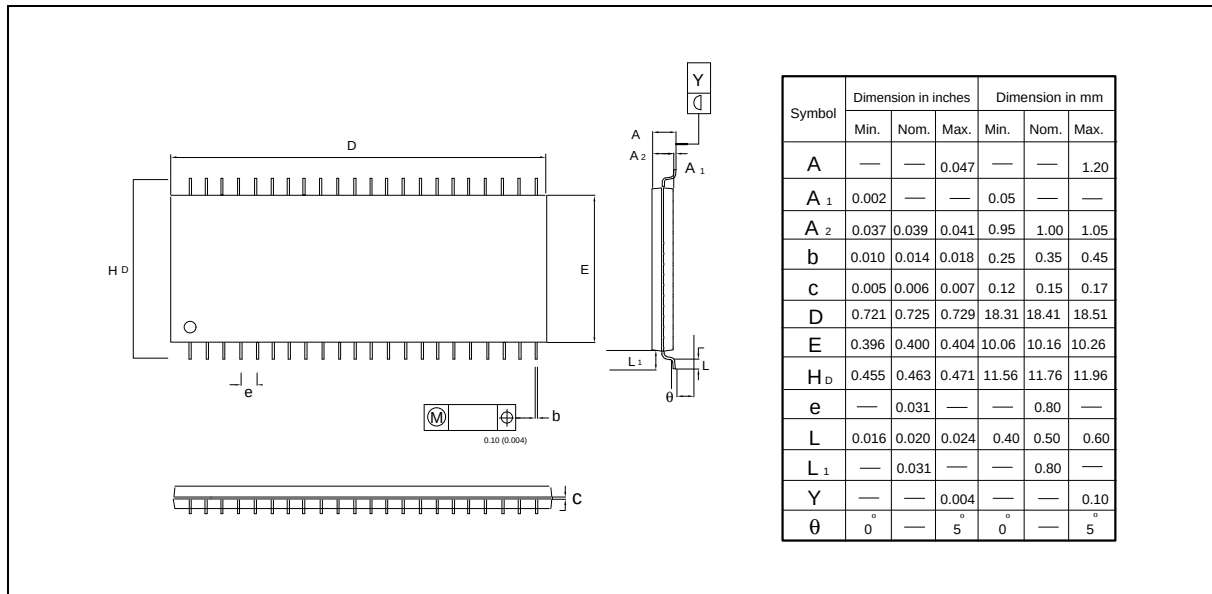
- Winbond reserves the right to make changes to its products without prior notice.
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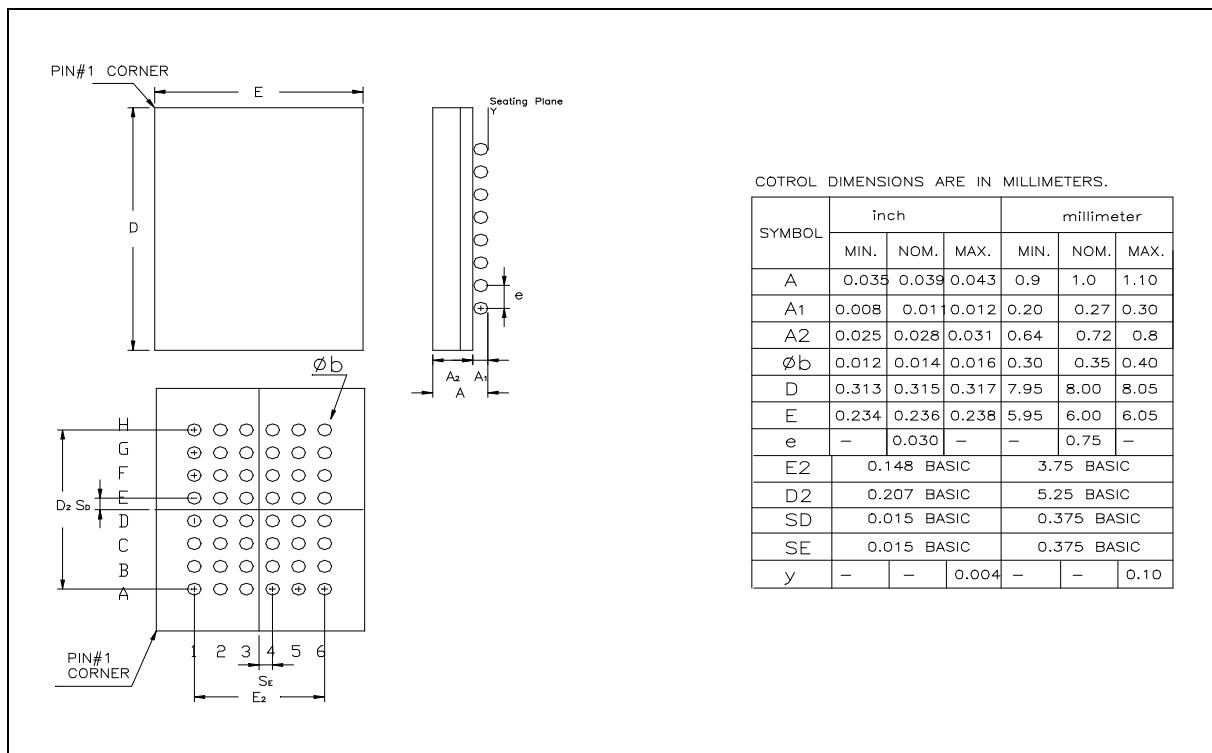


PACKAGE DIMENSIONS

44-pin Standard Type Two TSOP



TFBGA



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VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Apr. 22, 2002	-	Initial Issued



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