Winbond Electronics Corp.

128K ´ 16 CMOS STATIC RAM

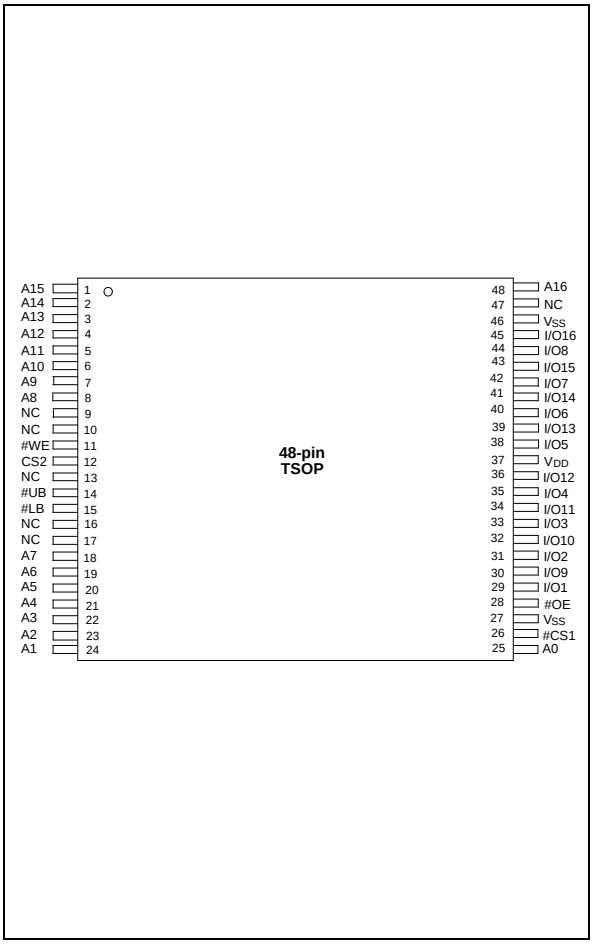
GENERAL DESCRIPTION

The W26B021 is a normal speed, very low-power CMOS static RAM organized as 131,072 × 16 bits that operates on a wide voltage range from 2.2V to 3.6V power supply. The W26B021T-LL, W26B021T-LE and W26B021T-LI, can meet the requirement of various operating temperature. This device is manufactured using Winbond's high performance CMOS technology.

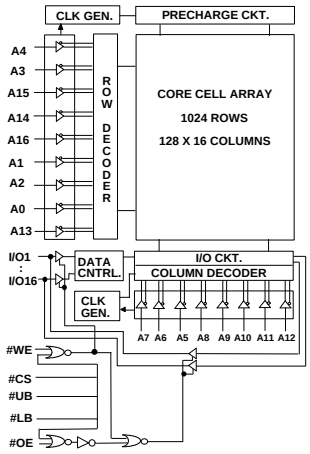
FEATURES

- Low power consumption
- Access time: 70, 100 nS
- 2.2V to 3.6V supply voltage
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three-state outputs
- Battery back-up operation capability
- Data retention voltage: 1.5V (min.)
- Data byte control
  - #LB (I/O1 – I/O8), #UB (I/O9 – I/O16)
- Available packages: 48-pin TSOP

PIN CONFIGURATION



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 – A16	Address Inputs
I/O1 – I/O16	Data Inputs/Outputs
#CS1	Chip Select Input 1, Low Active
CS2	Chip Select Input 2, High Active
#WE	Write Enable Input
#LB	Lower byte select
#UB	Upper byte select
#OE	Output Enable Input
VDD	Power Supply
VSS	Ground
NC	No Connection

TRUTH TABLE

#CS1	CS2	#OE	#WE	#LB	#UB	MODE	I/O1 - I/O8	I/O9 - I/O16	VDD CURRENT
H	X	X	X	X	X	Not Selected	High Z	High Z	ISB, ISB1
X	L	X	X	X	X	Not Selected	High Z	High Z	ISB, ISB1
X	X	X	X	H	H	Not Selected	High Z	High Z	ISB, ISB1
L	H	H	H	X	X	Output Disable	High Z	High Z	IDD
L	H	L	H	L	L	2 Bytes Read	DOUT	DOUT	IDD
L	H	L	H	L	H	Lower Byte Read	DOUT	High Z	IDD
L	H	L	H	H	L	Upper Byte Read	High Z	DOUT	IDD
L	H	X	L	L	L	2 Bytes Write	DIN	DIN	IDD
L	H	X	L	L	H	Lower Byte Write	DIN	High Z	IDD
L	H	X	L	H	L	Upper Byte Write	High Z	DIN	IDD

DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER		RATING	UNIT
Supply Voltage to V_{SS} Potential		-0.5 to +4.6	V
Input/Output to V_{SS} Potential		-0.5 to V_{DD} +0.5	V
Allowable Power Dissipation		1.0	W
Storage Temperature		-65 to +150	°C
Operating Temperature	LL	0 to 70	°C
	LE	-20 to 85	°C
	LI	-40 to 85	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

Operating Characteristics

(V_{SS} = 0V; T_A (°C) = 0 to 70 for LL, -20 to 85 for LE, -40 to 85 for LI)

PARAMETER	SYM.	TEST CONDITIONS	W26B021		UNIT
			MIN.	MAX.	
Operating Power Voltage	V_{DD}	-	2.2	3.6	V
Input Low Voltage	V_{IL}	-	-0.3	+0.4	V
Input High Voltage	V_{IH}	V_{DD} = 2.7V to 3.6V	+2.4	V_{DD} +0.4	V
		V_{DD} = 2.2V to 2.7V	+2.0	V_{DD} +0.3	
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{DD}	-1	+1	µA
Output Leakage Current	I_{LO}	$V_{I/O}$ = V_{SS} to V_{DD}; #CS1 = V_{IH} (min.) or CS2 = V_{IL} (max.) or #OE = V_{IH} (min.) or #WE = V_{IL} (max.)	-1	+1	µA
Output Low Voltage	V_{OL}	I_{OL} = +1.0 mA, V_{DD} = 2.7V to 3.6V	-	0.4	V
		I_{OL} = +1.0 mA, V_{DD} = 2.2V to 2.7V	-	0.4	
Output High Voltage	V_{OH}	I_{OH} = -0.5 mA, V_{DD} = 2.7V to 3.6V	2.4	-	V
		I_{OH} = -0.5 mA, V_{DD} = 2.2V to 2.7V	1.8	-	
Operating Power Supply Current	I_{DD}	#CS1 = V_{IL} (max.) and CS2 = V_{IH} (min.), I/O = 0 mA; Cycle = min. Duty = 100%	-	20	mA
Standby Power Supply Current	I_{SB}	#CS1 = V_{IH} (min.) or CS2 = V_{IL} (max.)	-	0.3	mA
	I_{SB1}	#CS1 ≥ V_{DD} -0.2V, CS2 ≥ V_{DD} -0.2V or #CS1 ≤ 0.2V, CS2 ≤ 0.2V	-	5	µA

CAPACITANCE

(T_A = 25° C, f = 1 MHz)

PARAMETER	SYM.	CONDITIONS	MAX.	UNIT
Input Capacitance	C_{IN}	V_{IN} = 0V	8	pF
Input/Output Capacitance	$C_{I/O}$	V_{OUT} = 0V	10	pF

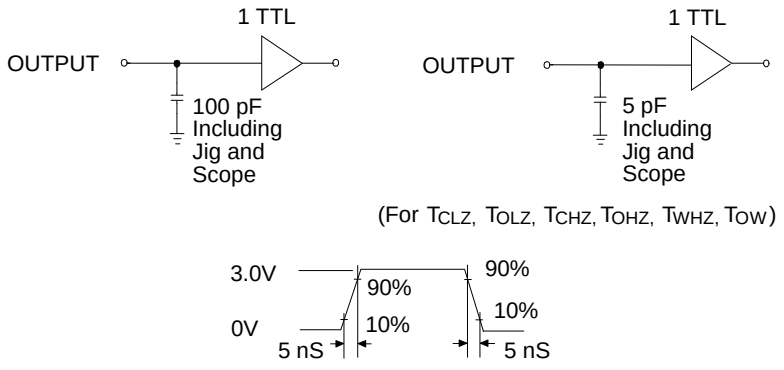
Note: These parameters are sampled but not 100% tested.

AC CHARACTERISTICS

AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5 nS
Input and Output Timing Reference Level	1.5V
Output Load	See the drawing below

AC Test Loads and Waveform



AC Characteristics, continued

(V_{SS} = 0V; T_A (°C) = -20 to 85 for LE, -40 to 85 for LI)

Read Cycle

PARAMETER	SYM.	W26B021-70		W26B021-10		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	T_{RC}	70	-	100	-	nS
Address Access Time	T_{AA}	-	70	-	100	nS
Chip Select Access Time	T_{ACS}	-	70	-	100	nS
Output Enable to Output Valid	T_{AOE}	-	35	-	50	nS
#UB, #LB Access Tim	T_{BA}	-	70	-	100	nS
Chip Selection to Output in Low Z	T_{CLZ}*	10	-	10	-	nS
Output Enable to Output in Low Z	T_{OLZ}*	5	-	5	-	nS
#UB, #LB Enable to Output in Low Z	T_{BLZ}*	5	-	5	-	nS
Chip Deselection to Output in High Z	T_{CHZ}*	-	30	-	35	nS
Output Disable to Output in High Z	T_{OHZ}*	-	30	-	35	nS
#UB, #LB Disable to Output in High Z	T_{BHZ}*	-	30	-	35	nS
Output Hold from Address Change	T_{OH}	10	-	10	-	nS

∗These parameters are sampled but not 100% tested

Write Cycle

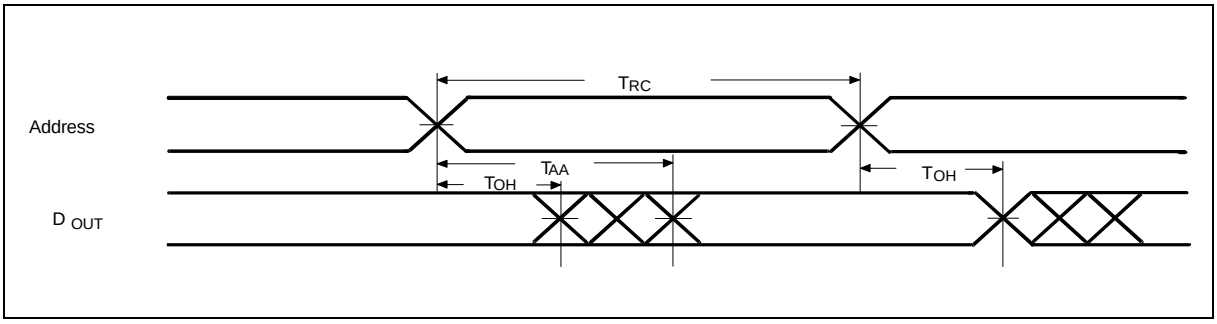
PARAMETER		SYM.	W26B021-70		W26B021-10		UNIT
			MIN.	MAX.	MIN.	MAX.	
Write Cycle Time		T_{WC}	70	-	100	-	nS
Chip Selection to End of Write		T_{CW}	60	-	80	-	nS
Address Valid to End of Write		T_{AW}	60	-	80	-	nS
#UB, #LB Select to End of Write		T_{BW}	60	-	80	-	nS
Address Setup Time		T_{AS}	0	-	0	-	nS
Write Pulse Width		T_{WP}	55	-	60	-	nS
Write Recovery Time	#CS1, CS2, #WE	T_{WR}	0	-	0	-	nS
Data Valid to End of Write		T_{DW}	40	-	40	-	nS
Data Hold from End of Write		T_{DH}	0	-	0	-	nS
Write to Output in High Z		T_{WHZ}*	-	30	-	35	nS
Output Disable to Output in High Z		T_{OHZ}*	-	30	-	35	nS
Output Active from End of Write		T_{OW}	5	-	5	-	nS

∗These parameters are sampled but not 100% tested

TIMING WAVEFORMS

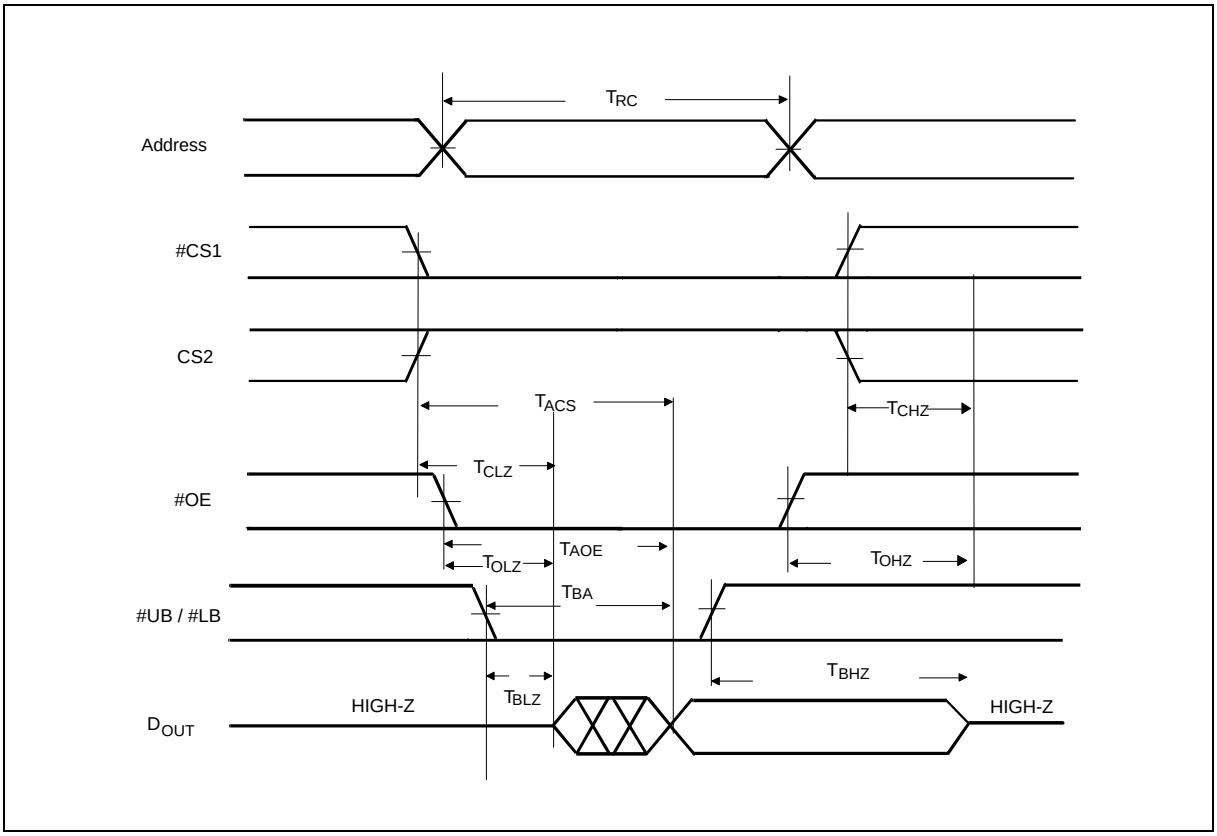
Read Cycle 1

(Address Controlled)



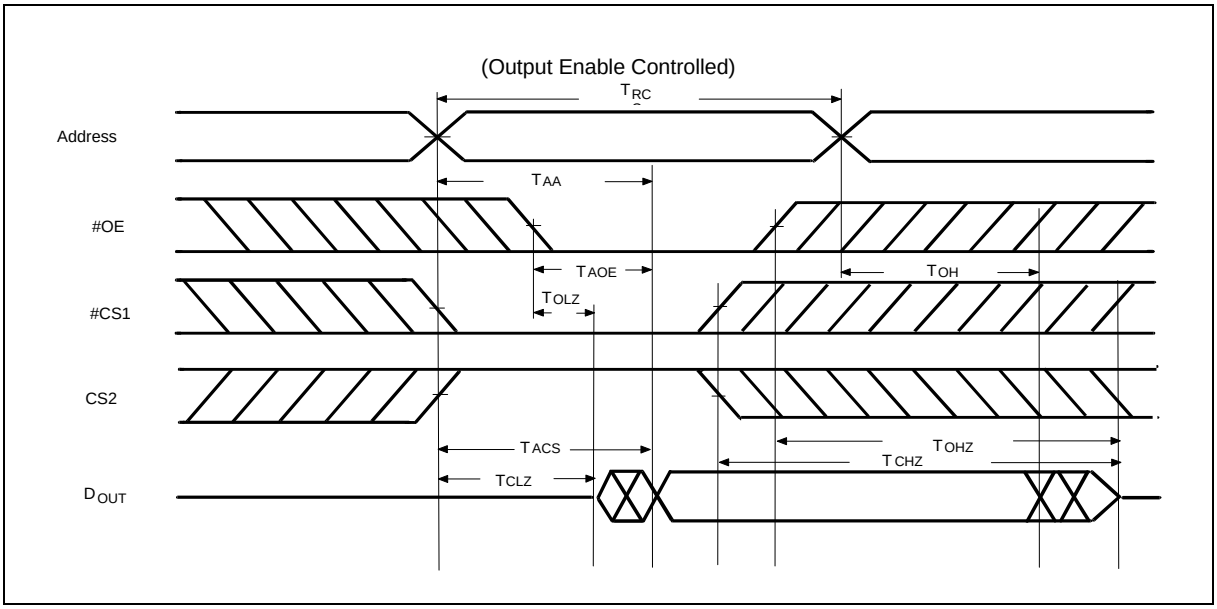
Read Cycle 2

(Chip Select Controlled, #OE = VIL, **#WE**= VIH**)**



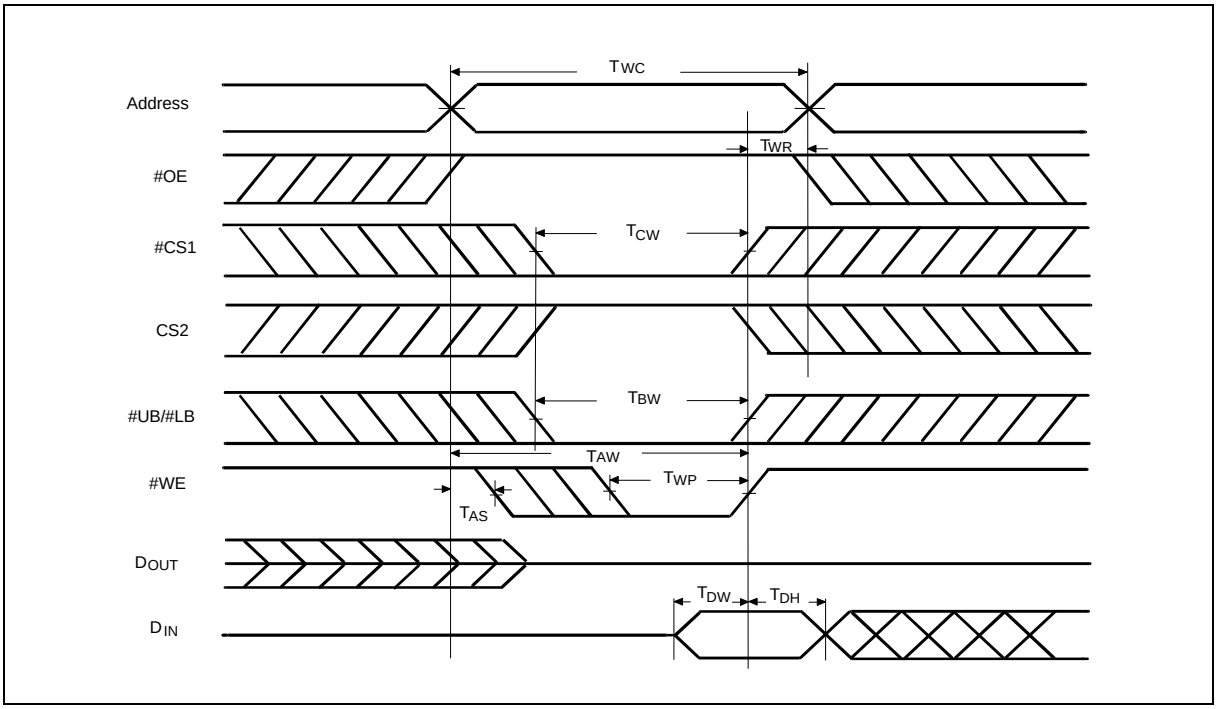
Timing Waveforms, continued

Read Cycle 3



Write Cycle 1

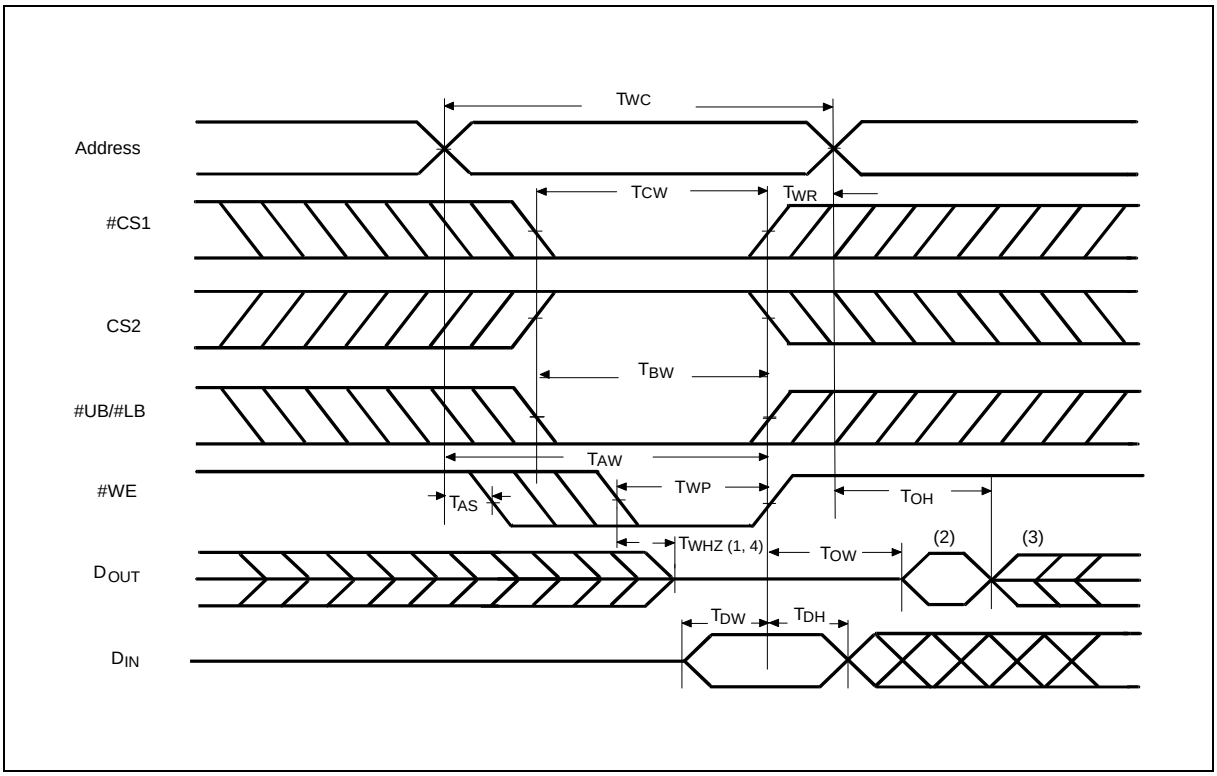
(#OE Clock)



Timing Waveforms, continued

Write Cycle 2

(#OE = VIL Fixed)



Notes:

1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from DOUT are the same as the data written to DIN during the write cycle.
3. DOUT provides the read data for the next address.
4. Transition is measured ±500 mV from steady state with CL = 5 pF. This parameter is guaranteed but not 100% tested.

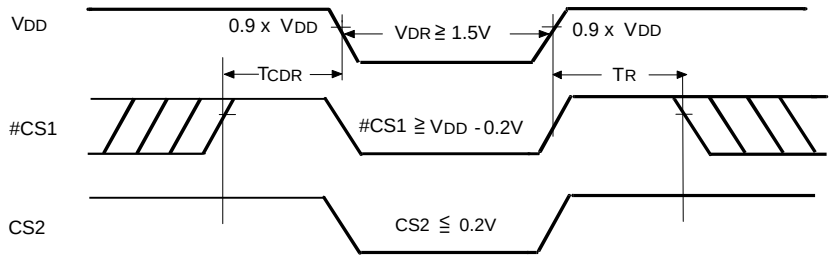
DATA RETENTION CHARACTERISTICS

(T_A (°C) = -20 to 85 for LE; -40 to 85 for LI)

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD} for Data Retention	V_{DR}	#CS1 ≥ V_{DD}-0.2V or CS2 ≤ 0.2V	1.5	-	-	V
Data Retention Current	I_{DDDR}	#CS1 ≥ V_{DD} -0.2V or CS2 ≤ 0.2V, V_{DD} = 3.0V	-	-	5	µA
Chip Deselect to Data Retention Time	T_{CDR}	See data retention waveform	0	-	-	nS
Operation Recovery Time	T_R		T_{RC}*	-	-	nS

* Read Cycle Time

DATA RETENTION WAVEFORM



ORDERING INFORMATION

PART NO.	ACCESS TIME (nS)	OPERATING VOLTAGE (V) STANDBY CURRENT (μA)	OPERATING TEMPERATURE (°C)	PACKAGE
W26B021T70LL	70	3V/5 μA	0 to 70	48L TSOP-I
W26B021T70LE	70	3V/5 μA	-20 to 85	48L TSOP-I
W26B021T70LI	70	3V/5 μA	-40 to 85	48L TSOP-I
W26B021T10LL	70	3V/5 μA	0 to 70	48L TSOP-I
W26B021T10LE	100	3V/5 μA	-20 to 85	48L TSOP-I
W26B021T10LI	100	3V/5 μA	-40 to 85	48L TSOP-I

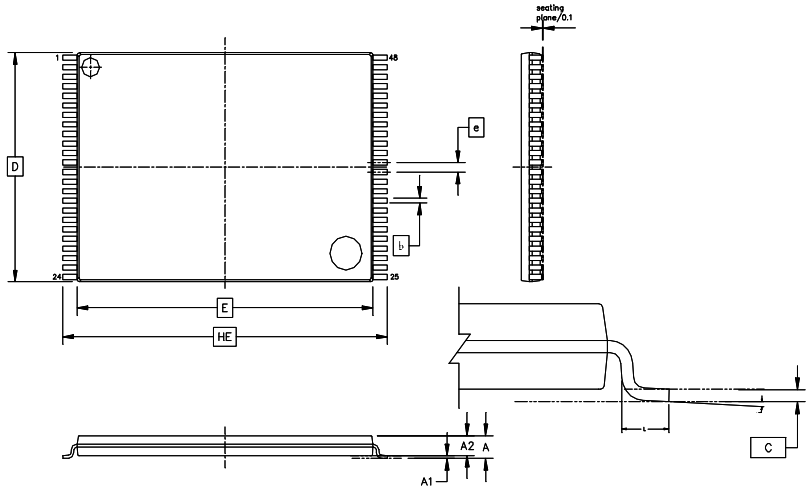
Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

PACKAGE DIMENSION

TSOP48

48-Pin Standard Thin Small Outline Package (measured in millimeters)



SYMBOL	MILLIMETER			INCH		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	–	–	1.20	–	–	0.047
A_1	0.05	–	0.15	0.002	–	0.0059
A_2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.1	–	0.21	0.039	–	0.008
D	12.00 BSC			0.472 BSC		
E	16.40 BSC			0.646 BSC		
H_E	18.00 BSC			0.709 BSC		
e	0.50 BSC			0.020 BSC		
L	0.50	0.60	0.70	0.020	0.024	0.028
θ	0°	5°	8°	0°	5°	8°

VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Apr. 19, 2002	-	Initial Issued

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