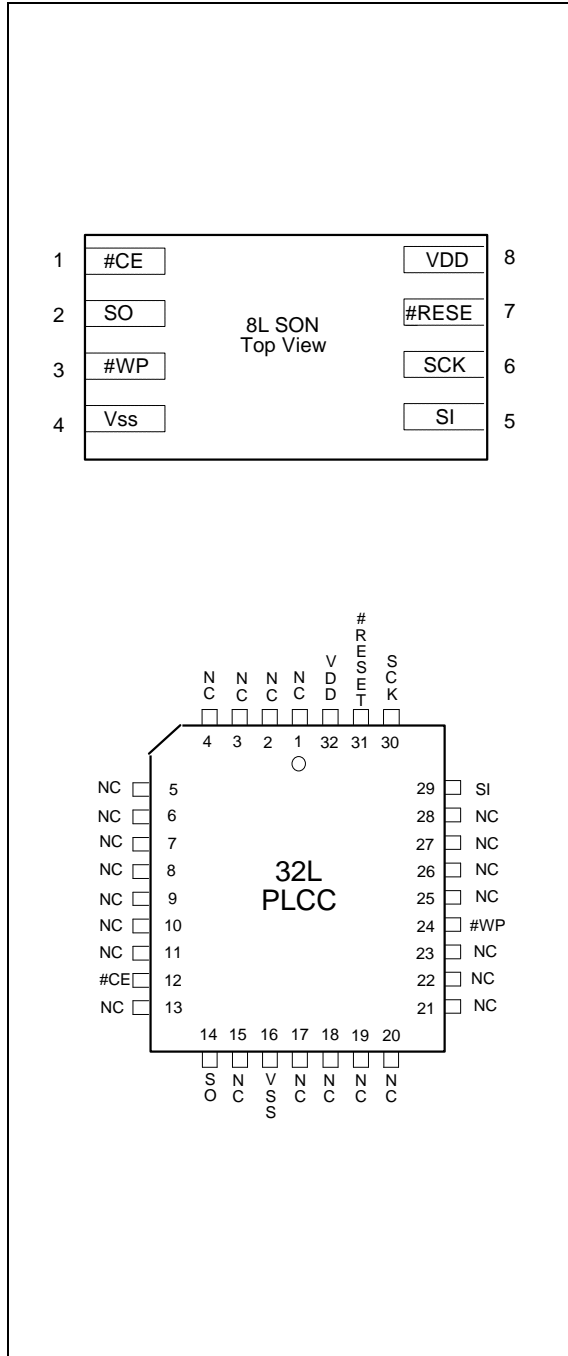**Winbond**
Electronics Corp.

# 512K ´ 1 SERIAL FLASH

## GENERAL DESCRIPTION

The W45B512 is manufactured with Winbond's high performance CMOS WinFlash technology. The Serial Flash is organized as 16 sectors of 4096 Bytes for the W45B512. The memory is accessed for Read or Erase/Program by the SPI bus compatible serial protocol. The bus signals are: serial data input (SI), serial data output (SO), serial clock (SCK), write protect (#WP), chip enable (#CE), and hardware reset (#RESET). This device is offered in 8L SON and 32L PLCC package.
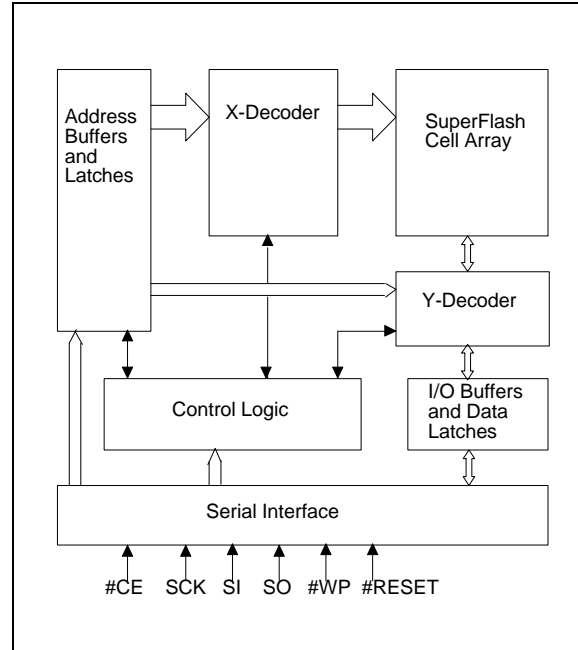
## FEATURES

- Single 2.7 – 3.6V Read and Write Operations
- Serial Interface Architecture
  - SPI Compatible: Mode 0 and Mode 3
- Byte Serial Read with Single Command
- Superior Reliability
  - Endurance: 10,000 Cycles (Typ.)
  - 20 years Data Retention
- Low Power Consumption
  - Active Current: 30 mA (Max.)
  - Standby Current: 15 µA (Max.)
- Sector or Chip-erase Capability
  - Uniform 4 KByte sectors
- Fast Erase and Byte-program
  - Chip-erase Time: 100 mS (Max.)
  - Sector-erase Time: 25 mS (Max.)
  - Byte-program Time: 50 µS (Max.)

- Automatic Write Timing
  - Internal $V_{PP}$ Generation
- End-of-Write Detection
  - Software Status
- 20 MHz Max Clock Frequency
- Hardware Reset Pin (#RESET)
  - Resets the device to Standby Mode
- TTL Compatibility
- Hardware Data Protection
  - Protects/Unprotects the device from Write operation
- Packages Available
  8L SON (5 x 6 mm), 32L PLCC

**Winbond**
Electronics Corp.

## PIN CONFIGURATIONS

| | | 8L SON Top View | | |
|---|---|---|---|---|
| 1 | #CE | | VDD | 8 |
| 2 | SO | | #RESE | 7 |
| 3 | #WP | | SCK | 6 |
| 4 | Vss | | SI | 5 |

32L PLCC

Top pins (left to right): NC, NC, NC, NC, VDD, #RESET, SCK — pins 4, 3, 2, 1, 32, 31, 30

Left side:
NC 5
NC 6
NC 7
NC 8
NC 9
NC 10
NC 11
#CE 12
NC 13

Right side:
29 SI
28 NC
27 NC
26 NC
25 NC
24 #WP
23 NC
22 NC
21 NC

Bottom (14–20): SO, NC, VSS, NC, NC, NC, NC

## BLOCK DIAGRAM

Address Buffers and Latches → X-Decoder → SuperFlash Cell Array

Y-Decoder

Control Logic

I/O Buffers and Data Latches

Serial Interface

#CE   SCK   SI   SO   #WP   #RESET

## PIN DESCRIPTION

| SYMBOL | PIN NAME |
|---|---|
| #CE | Chip Enable |
| SI | Serial Data Input |
| SO | Serial Data Output |
| SCK | Serial Clock |
| #WP | Write Protect |
| #RESET | Reset |
| VDD | Power Supply |
| VSS | Ground |

## PRODUCT IDENTIFICATION

| | BYTE | DATA |
|---|---|---|
| Manufacturer's ID | 0000 h | DA h |
| Device ID: W45B512 | 0001 h | 98 h |

## FUNCTIONAL DESCRIPTION

### Device Operation

The W45B512 uses bus cycles of 8 bits each for commands, data, and addresses to execute operations. The operation instructions are listed in the table below. All instructions are synchronized off a high to low transition of #CE. The first low to high transition on SCK will initiate the instruction sequence. Inputs will be accepted on the rising edge of SCK starting with the most significant bit. Any low to high transition on #CE before the input instruction completes will terminate any instruction in progress and return the device to the standby mode.

### Read

The Read operation outputs the data in order from the initial accessed address. While SCK is input, the address will be incremented automatically until end (top) of the address space, then the internal address pointer automatically increments to beginning (bottom) of the address space (00000h), and data out stream will continue. The read data stream is continuous through all addresses until terminated by a low to high transition on #CE.

### Sector/Chip-erase Operation

The Sector-Erase operation clears all bits in the selected sector to 'FF'. The Chip -Erase instruction clears all bits in the device to 'FF'.

### Byte-program Operation

The Byte-Program operation programs the bits in the selected byte to the desired data. The selected byte must be in the erased state ('FF') when initiating a Program operation. The data is input from bit 7 to bit 0 in order.

### Software Status Operation

The Status operation determines if an Erase or Program operation is in progress. If bit 0 is at a '0' an Erase or Program operation is in progress, the device is busy. If bit 0 is at a '1' the device is ready for any valid operation. The status read is continuous with ongoing clock cycles until terminated by a low to high transition on #CE.

### Reset

Reset will terminate any operation, e.g., Read, Erase and Program, in progress. It is activated by a high to low transition on the #RESET pin. The device will remain in reset condition as long as #RESET is low. Minimum reset time is 10 $\mu$S. See Figure 14 for reset timing diagram. #RESET is internally pulled-up and could remain unconnected during normal operation. After reset, the device is in standby mode, a high to low transition on #CE is required to start the next operation. An internal power-on reset circuit protects against accidental data writes. Applying a logic level low to #RESET during the power-on process then changing to a logic level high when V$_{DD}$ has reached the correct voltage level will provide additional protection against accidental writes during power on.

### Read WINBOND ID/Read Device ID

The Read Manufacturer ID and Read Device ID operations read the JEDEC assigned manufacturer identification and the manufacturer assigned device identification codes. These codes may be used to determine the actual device resident in the system.

**Winbond**
Electronics Corp.

## Write Protect

The #WP pin provides inadvertent write protection. The #WP pin must be held high for any Erase or Program operation. The #WP pin is "dont care" for all other operations. In typical use, the #WP pin is connected to $V_{SS}$ with a standard pull-down resistor. #WP is then driven high whenever an Erase or Program operation is required. If the #WP pin is tied to $V_{DD}$ with a pull-up resistor, then all operations may occur and the write protection feature is disabled. The #WP pin has an internal pull-up and could remain unconnected when not used.

## DEVICE OPERATION INSTRUCTION

| BUS CYCLE | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| Operation/Type | Command | Address [1] | Address | Address | Data | Dummy | Data |
| Read | FFh | $A_{23} - A_{16}$ | $A_{15} - A_8$ | $A_7 - A_0$ | X | X | Dout |
| Sector-erase [2] | 20h | $A_{23} - A_{16}$ | $A_{15} - A_8$ | X | Dout | X | |
| Chip-erase | 60h | X | X | X | Dout | X | |
| Byte-program | 10h | $A_{23} - A_{16}$ | $A_{15} - A_8$ | $A_7 - A_0$ | Din | X | |
| Software-status | 9Fh | Dout | | | | | |
| Read Manufacture ID | 90h | X | X | $A_0 = 0$ | DAh | | |
| Read Device ID [3] | 90h | X | X | $A_0 = 1$ | 98h | | |

Notes:

1. $A_{23} - A_{16}$ are 'Don't Care" for device.

2. $A_{15} - A_{12}$ are used to determine sector address, $A_{11} - A_8$ are don't care.

3. With $A_{15} - A_1 = 0$, W45B512 Device ID = 98h, is read with $A_0 = 1$.

## DEVICE OPERATION TABLE

| OPERATION | SI | SO | #CE[1] | #WP | #RESET |
|---|---|---|---|---|---|
| Read | X | Dout | Low | X | High |
| Sector-erase | X | X | Low | High | High |
| Chip-erase | X | X | Low | High | High |
| Byte-program | Din | X | Low | High | High |
| Software-status | X | Dout | Low | X | High |
| Reset[2] | X | X | X | X | Low |
| Read Manufacture ID | X | Dout | Low | X | High |
| Read Device ID | X | Dout | Low | X | High |

Notes:

1. A high to low transition on #CE will be required to start any device operation except for Reset.

2. The #RESET low will return the device to standby and terminate any Erase or Program operation in progress.

![Winbond Electronics Corp. logo]

## DC CHARACTERISTICS

### Absolute Maximum Stress Ratings

(Applied conditions greater than those listed under "Absolute maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

| PARAMETER | RATING | UNIT |
|---|---|---|
| Temperature Under Bias | -55 to +125 | °C |
| Storage Temperature | -65 to +150 | °C |
| D. C. Voltage on Any Pin to Ground Potential | -0.5 to $V_{DD}$ +0.5 | V |
| Transient Voltage (<20 nS) on Any Pin to Ground Potential | -1.0 to $V_{DD}$ +1.0 | V |
| Package Power Dissipation Capability ($T_A$ = 25° C) | 1.0 | W |
| Surface Mount Lead Soldering Temperature (3 Seconds) | 240 | °C |
| Output Short Circuit Current 1 | 50 | mA |

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

### DC Operating Characteristics

($V_{DD}$ =2.7V – 3.6V, $V_{SS}$ = 0V, $T_A$ = 0 to 70° C)

| PARAMETER | SYM. | TEST CONDITION | | LIMITS | | |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | UNITS |
| Power Supply Current | $I_{DD}$ | f = 20 MHz #CE = $V_{IL}$, $V_{DD}$ = $V_{DD}$ Max. | Program/Erase | - | 30 | mA |
| | | | Read | - | 20 | mA |
| Standby Current | $I_{SB}$ | #CE = $V_{IHC}$, $V_{DD}$ = $V_{DD}$ Max. | | - | 15 | µA |
| Input Leakage | $I_{LI}$ | $V_{IN}$ = GND to $V_{DD}$, $V_{DD}$ = $V_{DD}$ Max. | | - | 2 | µA |
| Output Leakage | $I_{LO}$ | $V_{OUT}$ = GND to $V_{DD}$, $V_{DD}$ = $V_{DD}$ Max. | | | 2 | µA |
| Input Low Voltage | $V_{IL}$ | | | -0.2 | 0.6 | V |
| Input High Voltage | $V_{IH}$ | | | 2.0 | $V_{DD}$ +0.3 | V |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 1.6 mA | | - | 0.4 | V |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -0.4 mA | | 2.4 | - | V |

Note: Outputs shorted for no more than one second. No more than one output shorted at a time.

## CAPACITANCE

($V_{DD}$ = 2.7V ~ 3.6V, $T_A$ = 25° C, f = 1 MHz)

| PARAMETER | SYMBOL | CONDITIONS | MAX. | UNIT |
|---|---|---|---|---|
| Output Pin Capacitance | $C_{OUT}$[1] | $V_{DQ}$ = 0V | 12 | pF |
| Input Pin Capacitance | $C_{IN}$[1] | $V_{IN}$ = 0V | 6 | pF |

## AC CHARACTERISTICS

### AC Test Conditions

($V_{DD}$ = 2.7V ~ 3.6V)

| PARAMETER | CONDITIONS |
|---|---|
| Input Rise/Fall Time | <5 nS |
| Input/Output Timing Level | 0.5 $V_{DD}$ / 0.5 $V_{DD}$ |
| Output Load | $C_L$ = 30 pF |

### AC Test Load and Waveform
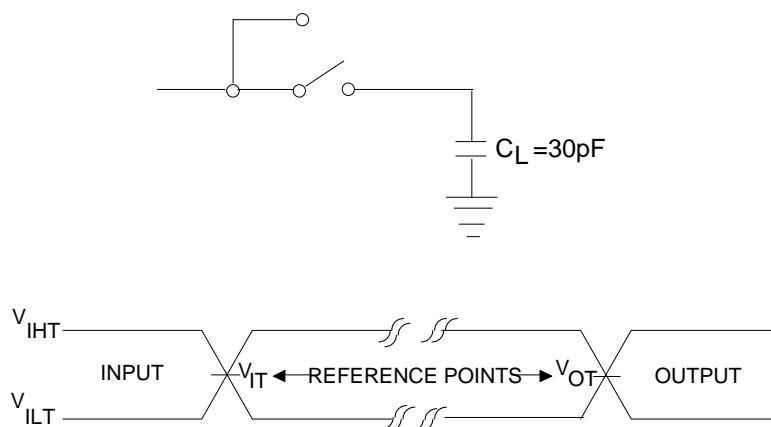


AC test inputs are driven at $V_{IHT}$ (0.9 $V_{DD}$) for a logic "1" and $V_{ILT}$ (0.1 $V_{DD}$) for a logic "0". Measurement reference points for inputs and outputs are at $V_{IT}$ (0.5 $V_{DD}$) and $V_{OT}$ (0.5 $V_{DD}$) Input rise and fall times (10% ↔ 90%) are <5 nS.

Note: $V_{IT}$: VINPUT Test; $V_{OT}$: VOUTPUT Test; $V_{IHT}$: VINPUT HIGH Test; $V_{ILT}$; VINPUT LOW Test

## AC Operating Characteristics
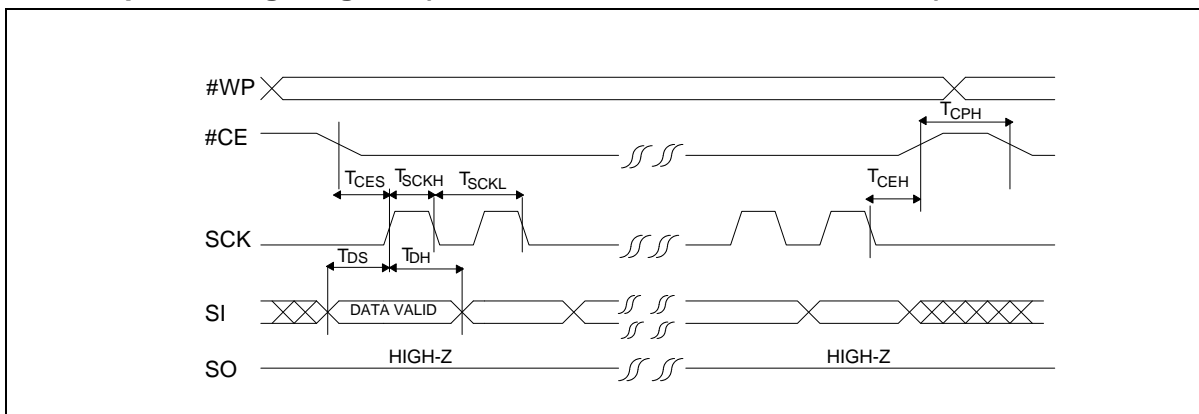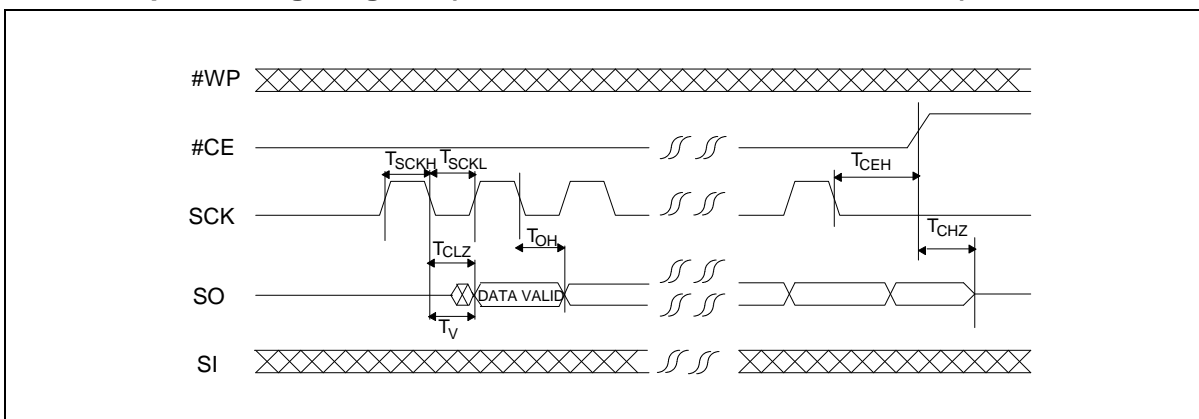
($V_{DD}$ = 2.7V ~ 3.6V)

| PARAMETER | SYMBOL | LIMITS | | |
|---|---|---|---|---|
| | | MIN. | MAX. | UNITS |
| Serial Clock Frequency | $F_{CLK}$ | | 20 | MHz |
| Serial Clock High Time | $T_{SCKH}$ | 22 | - | nS |
| Serial Clock Low Time | $T_{SCKL}$ | 22 | - | nS |
| #CE Setup Time | $T_{CES}$ | 10 | - | nS |
| #CE Hold Time | $T_{CEH}$ | 10 | - | nS |
| #CE High Time | $T_{CPH}$ | 50 | - | nS |
| #CE High to High-Z Output | $T_{CHZ}$ | - | 20 | nS |
| #CE Low to Low-Z Output | $T_{CLZ}$ | 0 | - | nS |
| #RESET Low to High-Z Output | $T_{RLZ}$ | - | 20 | nS |
| Data In Setup Time | $T_{DS}$ | 5 | - | nS |
| Data In Hold Time | $T_{DH}$ | 5 | - | nS |
| Output Hold from SCK Change | $T_{OH}$ | 0 | - | nS |
| Output Valid from SCK | $T_{V}$ | - | 25 | nS |
| Write Protect Setup Time | $T_{WPS}$ | 10 | - | nS |
| Write Protect Hold Time | $T_{WPH}$ | 10 | - | nS |
| Sector-erase | $T_{SE}$ | - | 25 | mS |
| Chip-erase | $T_{SCE}$ | - | 100 | mS |
| Byte-program | $T_{BP}$ | - | 50 | $\mu$S |
| Reset Pulse Width | $T_{RST}$ | 10 | - | $\mu$S |
| Reset Recovery Time | $T_{REC}$ | - | 1 | $\mu$S |
| Reset Time After Power-up | $T_{PURST}$ | 10 | - | $\mu$S |

## TIMING WAVEFORMS

### Serial Input Timing Diagram (Inactive Serial Clock Low - Mode 0)

#WP

#CE

$T_{CPH}$

$T_{CES}$  $T_{SCKH}$  $T_{SCKL}$

$T_{CEH}$

SCK

$T_{DS}$  $T_{DH}$

SI

DATA VALID

SO

HIGH-Z

HIGH-Z

### Serial Output Timing Diagram (Inactive Serial Clock Low - Mode 0)

#WP

#CE

$T_{SCKH}$  $T_{SCKL}$

$T_{CEH}$

SCK

$T_{CLZ}$  $T_{OH}$

$T_{CHZ}$

SO

DATA VALID

$T_V$

SI

### Serial Input Timing Diagram (Inactive Serial Clock High - Mode 3)

#WP

#CE

$T_{CPH}$

$T_{CES}$  $T_{SCKH}$  $T_{SCKL}$

SCK

$T_{CEH}$

$T_{DS}$  $T_{DH}$

SI

DATA VALID

SO

HIGH-Z

HIGH-Z
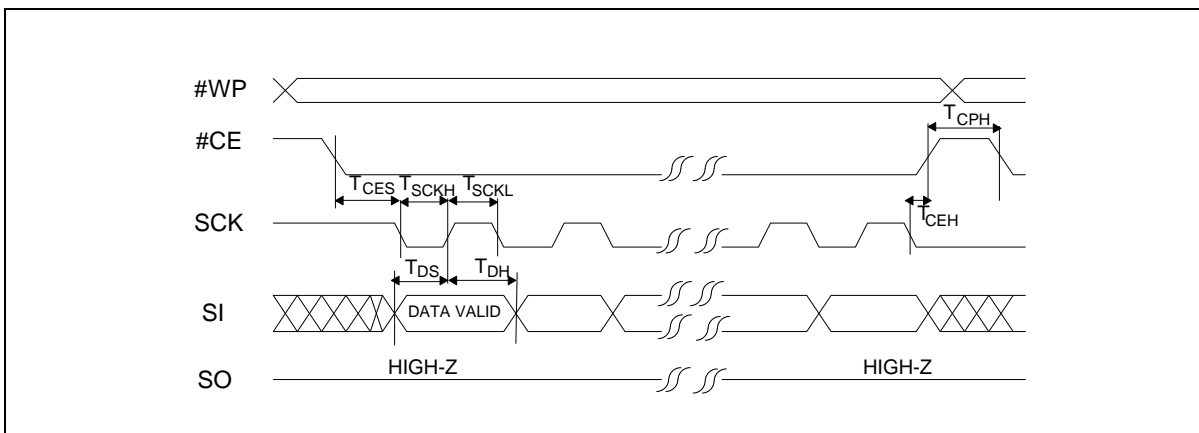
Timing Waveforms, continued

## Serial Output Timing Diagram (Inactive Serial Clock High - Mode 3)
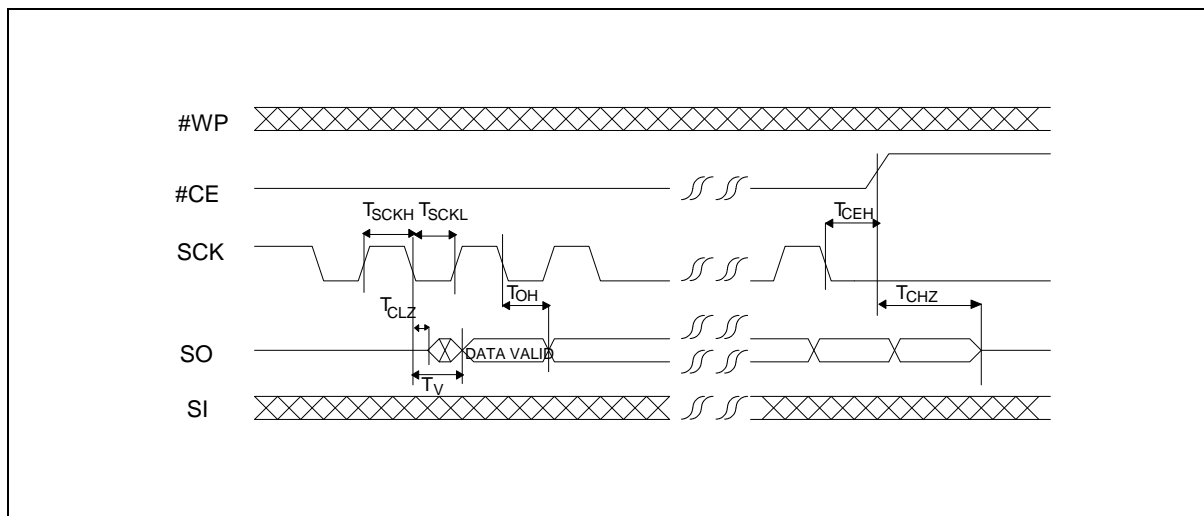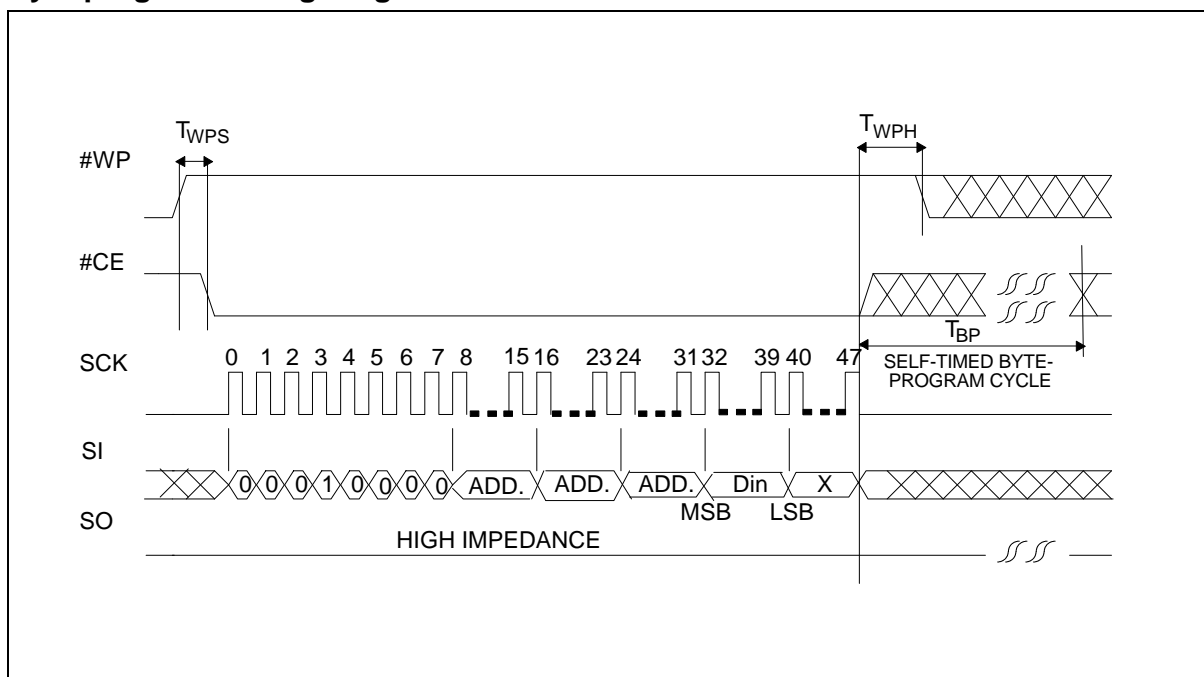


## Sector-erase Timing Diagram
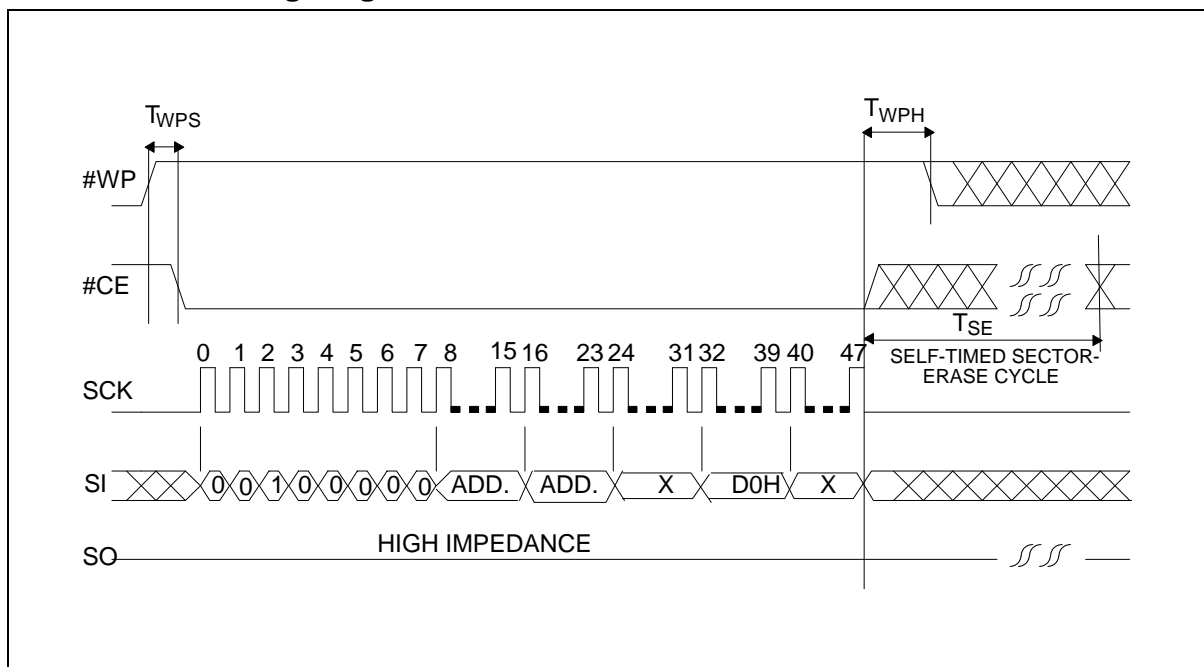
Timing Waveforms, continued

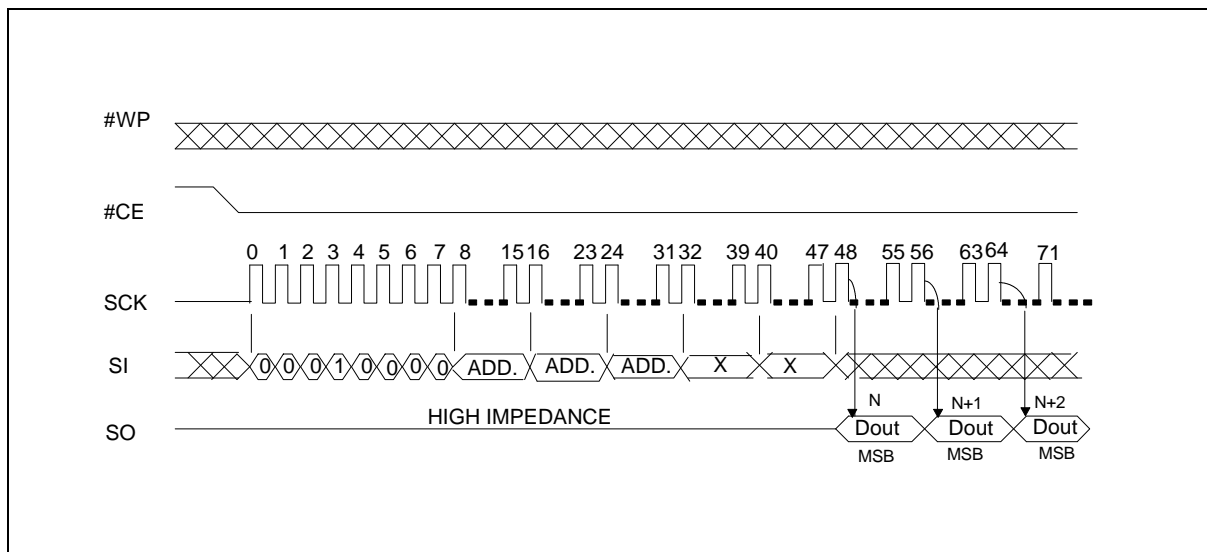## Chip-erase Timing Diagram
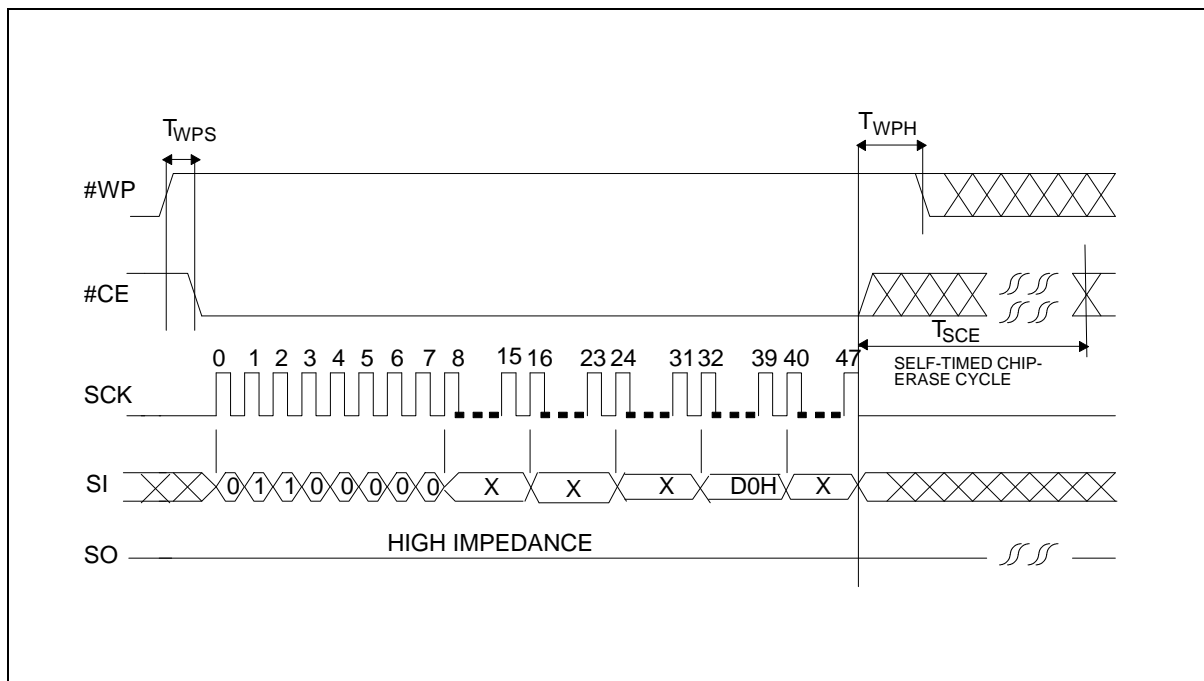


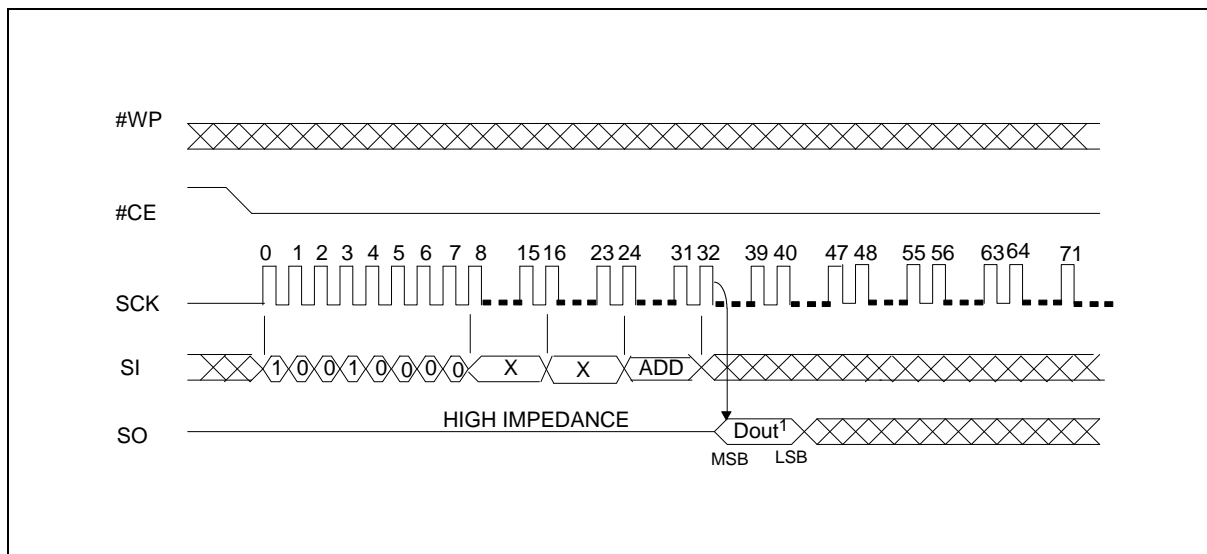## Byte-program Timing Diagram

Timing Waveforms, continued

## Read Timing Diagram
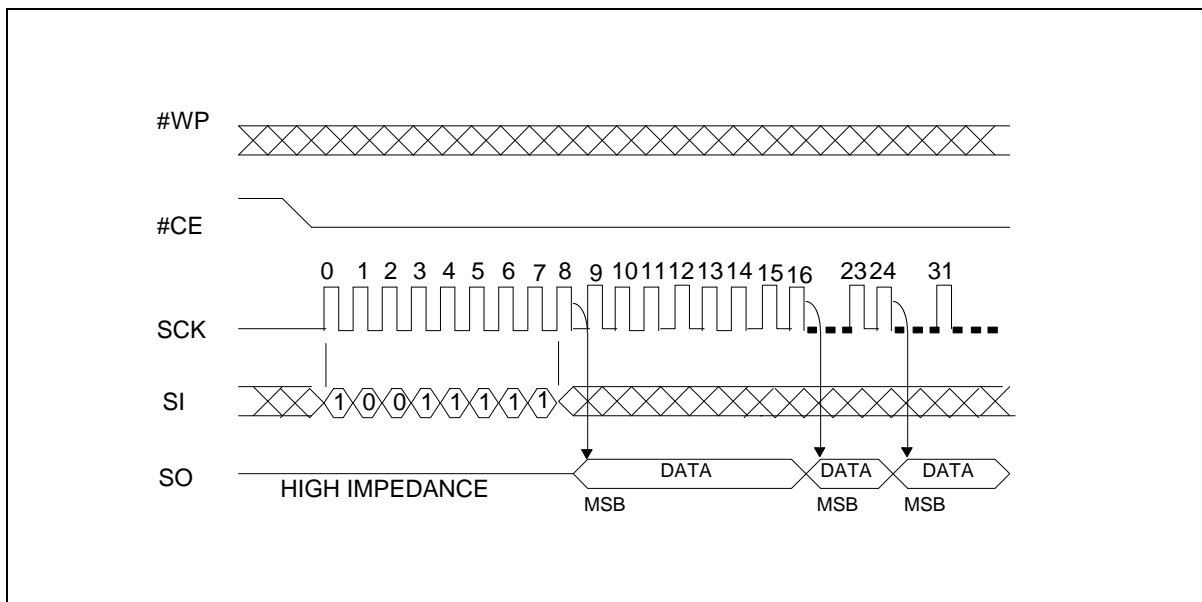


## Read-Id Timing Diagram



Note: 1. Manufacturer's ID = DAh is read with A 0 = 0
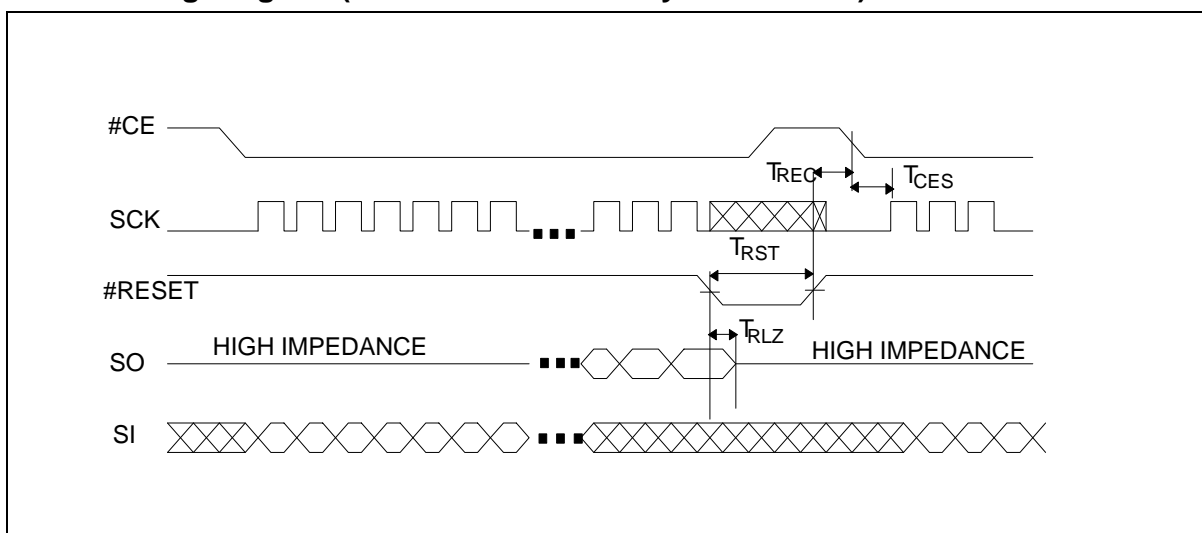
   Device ID = 98h is read with A 0 = 1

Timing Waveforms, continued

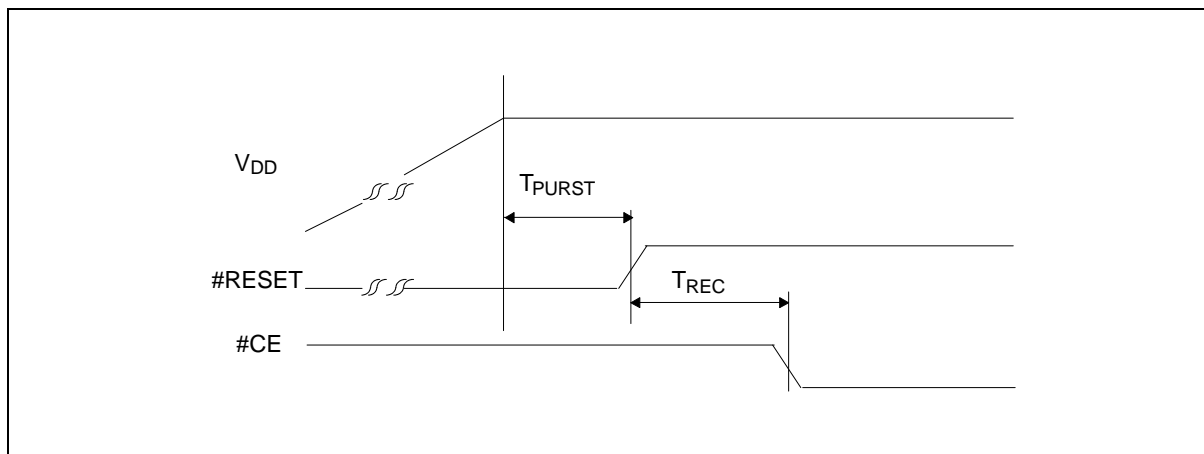## Software-Status Timing Diagram



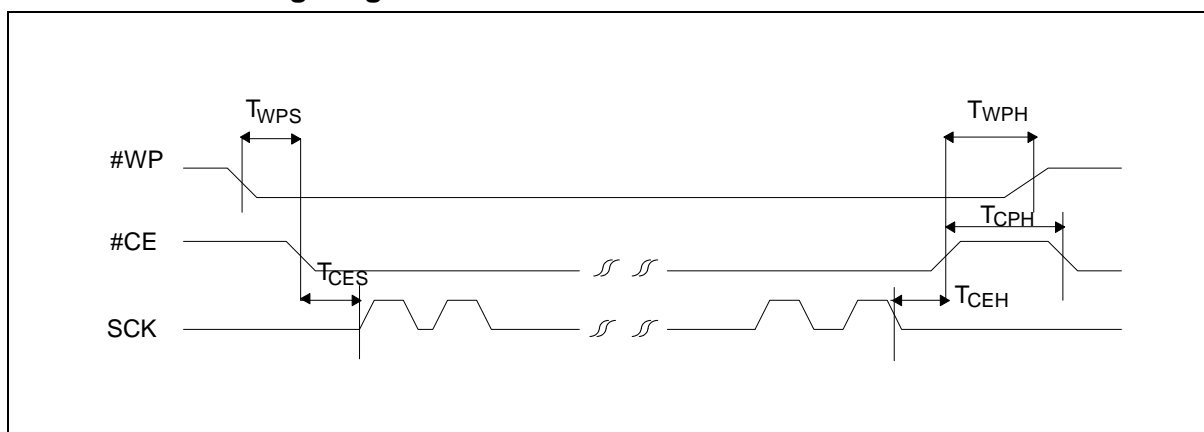## Reset Timing Diagram (Inactive Clock Polarity Low Shown)

Timing Waveforms, continued

## Power-on Reset Timing Diagram



## Write Protect Timing Diagram

**Winbond**
Electronics Corp.

## ORDERING INFORMATION

| PART NO. | OPERATING VOLTAGE (V) | POWER SUPPLY CURRENT MAX. (mA) | STANDBY $V_{DD}$ CURRENT MAX. (mA) | PACKAGE | CYCLING | OPERATING TEMP. (°C) |
|---|---|---|---|---|---|---|
| W45B512Z | 2.7V – 3.6V | 30 | 15 | 8L SON (5 x 6 mm) | 10K | 0°C – 70°C |
| W45B512P | 2.7V – 3.6V | 30 | 15 | 32L PLCC | 10K | 0°C – 70°C |

Notes:

1. Winbond reserves the right to make changes to its products without prior notice.

2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

## HOW TO READ THE TOP MARKING

Example: The top marking of 32L-PLCC W45B512

**Winbond**
Electronics Corp.

W45B512Z

2138977A-A12

149OBSA

$1^{st}$ line: winbond logo

$2^{nd}$ line: the part number: W45B512Z

$3^{rd}$ line: the lot number

$4^{th}$ line: the tracking code: 149 O B SA

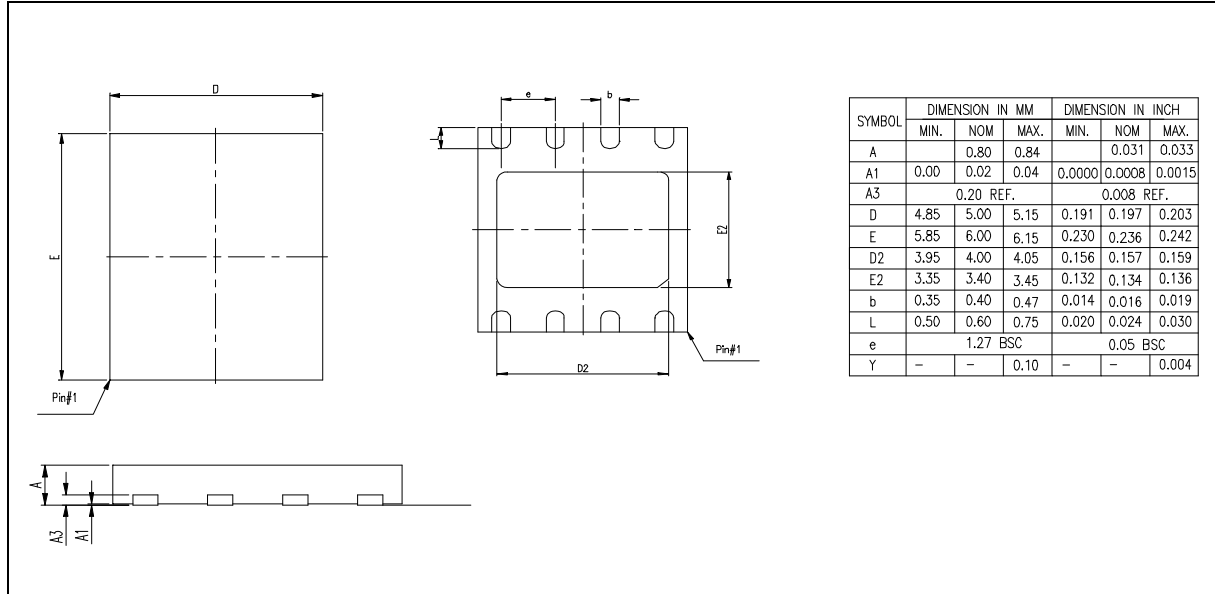        149: Packages made in 01, week 49

        O: Assembly house ID: A means ASE, O means OSE, ... etc.

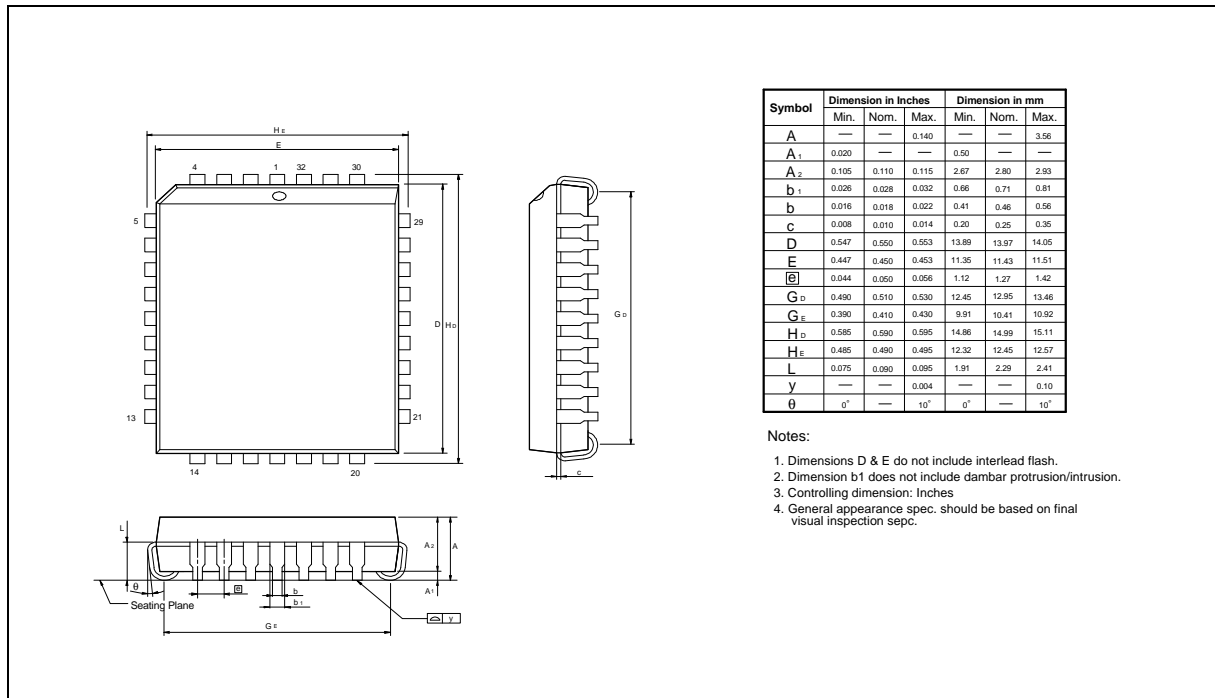        B: IC revision; A means version A, H means version H, ... etc.

        SA: Process code

## PACKAGE DIMENSIONS

### 8L SON (5 x 6 mm)



| SYMBOL | DIMENSION IN MM | | | DIMENSION IN INCH | | |
|--------|------|------|------|------|------|------|
| | MIN. | NOM | MAX. | MIN. | NOM | MAX. |
| A | | 0.80 | 0.84 | | 0.031 | 0.033 |
| A1 | 0.00 | 0.02 | 0.04 | 0.0000 | 0.0008 | 0.0015 |
| A3 | 0.20 REF. | | | 0.008 REF. | | |
| D | 4.85 | 5.00 | 5.15 | 0.191 | 0.197 | 0.203 |
| E | 5.85 | 6.00 | 6.15 | 0.230 | 0.236 | 0.242 |
| D2 | 3.95 | 4.00 | 4.05 | 0.156 | 0.157 | 0.159 |
| E2 | 3.35 | 3.40 | 3.45 | 0.132 | 0.134 | 0.136 |
| b | 0.35 | 0.40 | 0.47 | 0.014 | 0.016 | 0.019 |
| L | 0.50 | 0.60 | 0.75 | 0.020 | 0.024 | 0.030 |
| e | 1.27 BSC | | | 0.05 BSC | | |
| Y | – | – | 0.10 | – | – | 0.004 |

### 32L PLCC



| Symbol | Dimension in Inches | | | Dimension in mm | | |
|--------|------|------|------|------|------|------|
| | Min. | Nom. | Max. | Min. | Nom. | Max. |
| A | — | — | 0.140 | — | — | 3.56 |
| A1 | 0.020 | — | — | 0.50 | — | — |
| A2 | 0.105 | 0.110 | 0.115 | 2.67 | 2.80 | 2.93 |
| b1 | 0.026 | 0.028 | 0.032 | 0.66 | 0.71 | 0.81 |
| b | 0.016 | 0.018 | 0.022 | 0.41 | 0.46 | 0.56 |
| c | 0.008 | 0.010 | 0.014 | 0.20 | 0.25 | 0.35 |
| D | 0.547 | 0.550 | 0.553 | 13.89 | 13.97 | 14.05 |
| E | 0.447 | 0.450 | 0.453 | 11.35 | 11.43 | 11.51 |
| e | 0.044 | 0.050 | 0.056 | 1.12 | 1.27 | 1.42 |
| GD | 0.490 | 0.510 | 0.530 | 12.45 | 12.95 | 13.46 |
| GE | 0.390 | 0.410 | 0.430 | 9.91 | 10.41 | 10.92 |
| HD | 0.585 | 0.590 | 0.595 | 14.86 | 14.99 | 15.11 |
| HE | 0.485 | 0.490 | 0.495 | 12.32 | 12.45 | 12.57 |
| L | 0.075 | 0.090 | 0.095 | 1.91 | 2.29 | 2.41 |
| y | — | — | 0.004 | — | — | 0.10 |
| θ | 0° | — | 10° | 0° | — | 10° |

Notes:

1. Dimensions D & E do not include interlead flash.
2. Dimension b1 does not include dambar protrusion/intrusion.
3. Controlling dimension: Inches
4. General appearance spec. should be based on final visual inspection sepc.

## VERSION HISTORY

| VERSION | DATE | PAGE | DESCRIPTION |
|---|---|---|---|
| A1 | Feb. 21, 2002 | - | Initial Issued |