W83972D

AC'97 2.1 AUDIO CODEC

W83972D Data Sheet Revision History

	Pages	Dates	Version	Version on Web	Main Contents
1	n.a.	09/20/2001	0.5	0.5	First published.
2					
3					
4					
5					
6					
7					
8					
9					
10					

Please note that all data and specifications are subject to change without notice. All the trade marks of products and companies mentioned in this data sheet belong to their respective owners.

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.

TABLE OF CONTENTS

Winbond Electronics Corp.

PRELIMINARY

1. GENERAL DESCRIPTION

The Winbond W83972D is a high performance codec compliant with Audio Codec'97 rev.2.1 requirements, in addition to 3D stereo enhancement. The definition of AC Link serial interface allows the W83972D to be used with DC97 controller as well as various digital controller has AC Link interface.

Packaged in a small 48-pin LQFP, the W83972D can be placed on the motherboard, CNR card, daughter board, add-on cards, PCMCIA cards, or outside the main chassis such as in speakers.

2. FEATURE LIST

- AC'97 2.1 compliant
- 16-bit stereo full-duplex codec with variable sampling rate
- S/N ratio: 85dB (analog to analog), 80dB(analog to digital), 90dB(digital to analog)
- Four analog line-level stereo inputs for connection from LINE IN, CD, VIDEO, and AUX
- Two analog line-level mono inputs for speakerphone and PC BEEP
- Mono mic input switchable from two external sources
- High quality pseudo-differential CD input
- Stereo line-level output
- Mono output for speakerphone
- 3D stereo enhancement
- Multiple Codec Support
- Power management support
- External AMP power down control output support
- Analog 5V, digital 3.3V
- Package: 48-pin LQFP

Ordering Information

Part Number	Package Type	Production Flow
W83972D	48-PIN LQFP	Commercial, 0°C to +70°C

3. FUNCTIONAL BLOCK DIAGRAM

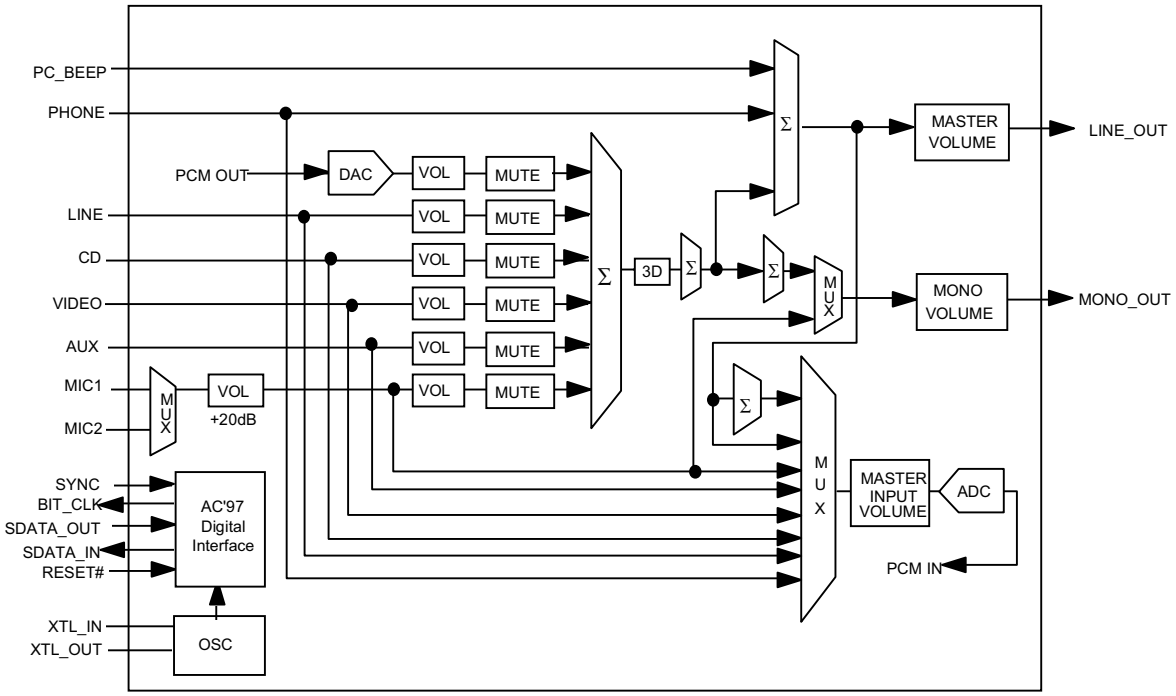


Figure 3.1: W83972D Function Block Diagram

4. PIN-OUT AND PIN LIST

4.1 Pin-Out

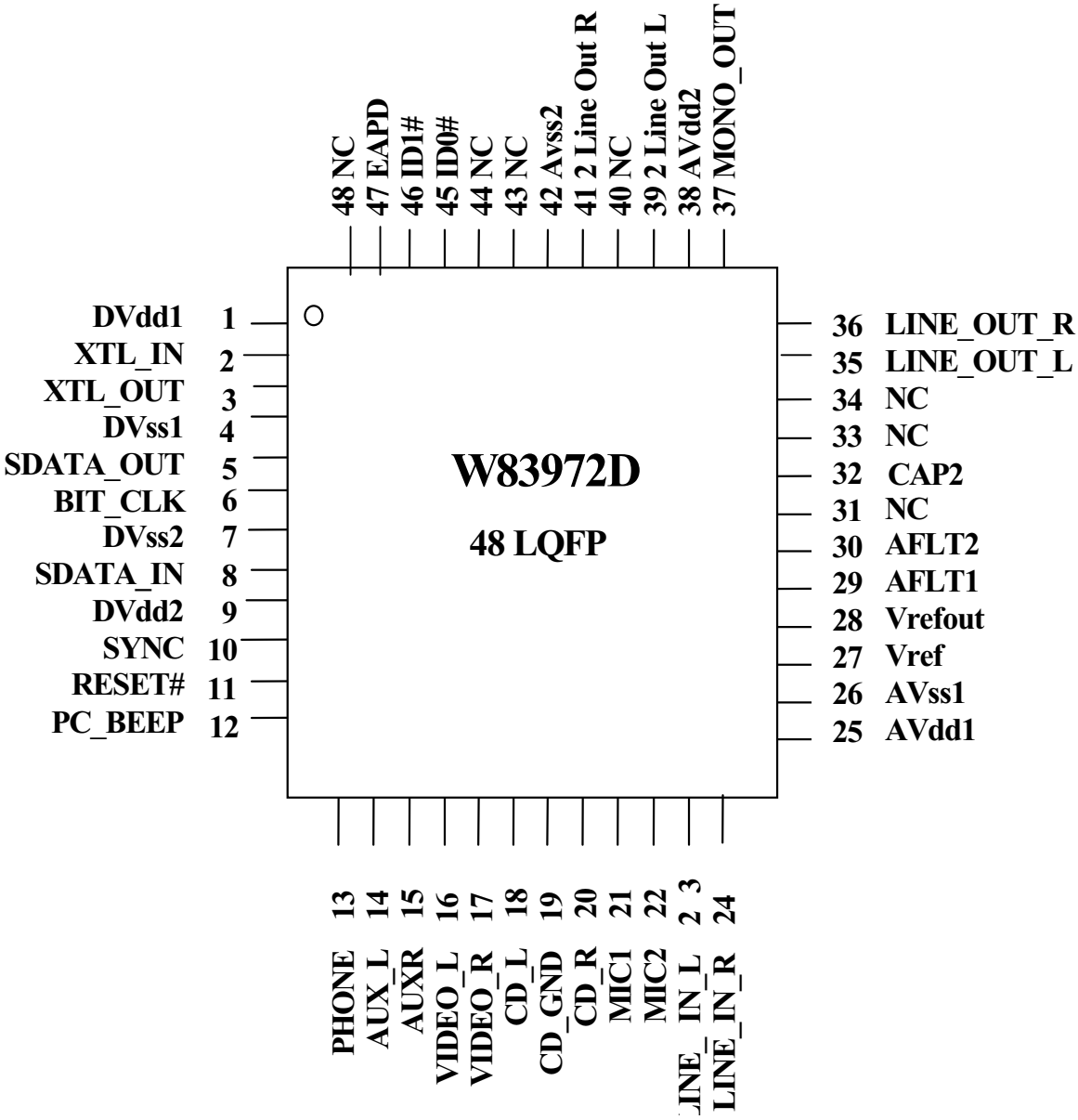


Figure 4.1: W83972D Pin-Out

4.2 W83972D 48-LQFP Pin List

Pin#	Signal Name	Pin#	Signal Name	Pin#	Signal Name	Pin#	Signal Name
1	DVdd1	13	PHONE	25	AVdd1	37	MONO_OUT
2	XTL_IN	14	AUX_L	26	AVss1	38	AVdd2
3	XTL_OUT	15	AUX_R	27	Vref	39	2nd LINE_OUT_L
4	DVss1	16	VIDEO_L	28	Vrefout	40	NC
5	SDATA_OUT	17	VIDEO_R	29	AFLT1	41	2nd LINE_OUT_R
6	BIT_CLK	18	CD_L	30	AFLT2	42	AVss2
7	DVss2	19	CD_GND	31	NC	43	NC
8	SDATA_IN	20	CD_R	32	CAP2	44	NC
9	DVdd2	21	MIC1	33	NC	45	ID0#
10	SYNC	22	MIC2	34	NC	46	ID1#
11	RESET#	23	LINE_IN_L	35	LINE_OUT_L	47	EAPD
12	PC_BEEP	24	LINE_IN_R	36	LINE_OUT_R	48	NC

5. PIN DESCRIPTION

5.1 Digital I/O

Signal Name	Type	Description
RESET#	I	AC'97 Master Reset
XTL_IN	I	24.576 MHz Crystal
XTL_OUT	O	24.576 MHz Crystal
SYNC	I	48 kHz Fixed Rate Sync Pulse
BIT_CLK	I/O	12.288 MHz Serial Data Clock
SDATA_OUT	I	AC'97 Serial Data Input Stream
SDATA_IN	O	AC'97 Serial Data Output Stream
EAPD	O	External AMP Power Down Control

5.2 Analog I/O

Signal Name	Type	Description
PC_BEEP	I	PC Speaker Beep Pass Through
PHONE	I	Telephony Subsystem Speakerphone
MIC1	I	Desktop Microphone
MIC2	I	Second Microphone
LINE_IN_L	I	Line In Left Channel
LINE_IN_R	I	Line In Right Channel
CD_L	I	CD Audio Left Channel
CD_GND	I	CD Audio Analog Ground
CD_R	I	CD Audio Right Channel
VIDEO_L	I	Video Left Channel
VIDEO_R	I	Video Right Channel
AUX_L	I	Auxiliary Left Channel
AUX_R	I	Auxiliary Right Channel
LINE_OUT_L	O	Line Out Left Channel
LINE_OUT_R	O	Line Out Right Channel
2nd LINE_OUT_L	O	Second Line Out Left Channel
2nd LINE_OUT_R	O	Second Line Out Right Channel
MONO_OUT	O	Mono Output

5.3 Filter and Reference Pins

Signal Name	Type	Description
Vref	I	Reference Voltage
Vrefout	O	Reference Voltage Output
CAP2	I	Reference Voltage
AFLT1	I	Left Channel Anti-Aliasing Filter Capacitor
AFLT2	I	Right Channel Anti-Aliasing Filter Capacitor

5.4 Power Supplies

Signal Name	Type	Description
AVdd1	I	Analog Supply Voltage, 5V
AVdd2	I	Analog Supply Voltage, 5V
AVss1	I	Analog Ground
AVss2	I	Analog Ground
DVdd1	I	Digital Supply Voltage, 3.3V
DVdd2	I	Digital Supply Voltage, 3.3V
DVss1	I	Digital Ground
DVss2	I	Digital Ground

6. REGISTER DESCRIPTION

6.1 Register Map

Reg#	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	Reset	x	SE4	SE3	SE2	SE1	SE0	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	6C00h
02h	Master Volume	Mute	x	ML5	ML4	ML3	ML2	ML1	ML0	x	x	MR5	MR4	MR3	MR2	MR1	MR0	8000h
04h	2nd Volume	Mute	x	SL5	SL4	SL3	SL2	SL1	SL0	x	x	SR5	SR4	SR3	SR2	SR1	SR0	8000h
06h	Master Volume Mono	Mute	x	x	x	x	x	x	x	x	x	MM5	MM4	MM3	MM2	MM1	MM0	8000h
0Ah	PC_BEEP Volume	Mute	x	x	x	x	x	x	x	x	x	x	PV3	PV2	PV1	PV0	x	0000h
0Ch	Phone Volume	Mute	x	x	x	x	x	x	x	x	x	x	GN4	GN3	GN2	GN1	GN0	8008h
0Eh	Mic Volume	Mute	x	x	x	x	x	x	x	x	20db	x	GN4	GN3	GN2	GN1	GN0	8008h
10h	Line in Volume	Mute	x	x	GL4	GL3	GL2	GL1	GL0	x	x	x	GR4	GR3	GR2	GR1	GR0	8808h
12h	CD Volume	Mute	x	x	GL4	GL3	GL2	GL1	GL0	x	x	x	GR4	GR3	GR2	GR1	GR0	8808h
14h	Video Volume	Mute	x	x	GL4	GL3	GL2	GL1	GL0	x	x	x	GR4	GR3	GR2	GR1	GR0	8808h
16h	Aux Volume	Mute	x	x	GL4	GL3	GL2	GL1	GL0	x	x	x	GR4	GR3	GR2	GR1	GR0	8808h
18h	PCM Out Volume	Mute	x	x	GL4	GL3	GL2	GL1	GL0	x	x	x	GR4	GR3	GR2	GR1	GR0	8808h
1Ah	Record Select	x	x	x	x	x	SL2	SL1	SL0	x	x	x	x	x	SR2	SR1	SR0	0000h
1Ch	Record Gain	Mute	x	x	x	GL3	GL2	GL1	GL0	x	x	x	x	GR3	GR2	GR1	GR0	8000h
20h	General Purpose	x	x	3D	x	x	x	MIX	MS	LPBK	x	x	x	x	x	x	x	0000h
22h	3D Control	x	x	x	x	x	x	x	x	x	x	x	x	DP3	DP2	DP1	DP0	0000h
26h	Pwrdwn Control/Status	EAPD	x	PR5	PR4	PR3	PR2	PR1	PR0	x	x	x	x	REF	ANL	DAC	ADC	000Fh
28h	Extended Audio ID	ID1	ID0	x	x	x	x	x	x	x	x	x	x	x	x	x	VRA	0000h
2Ah	Extended Audio Control	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	VRE	0000h
2Ch	DAC Sample Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
32h	ADC Sample Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
.,	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..
..	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..
5Eh	Enhanced Function	x	LP_CD	E_C	DAM	x	x	x	x	x	x	x	x	x	x	x	x	0000h
..	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..
..	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..
7Ah	Vendor Reserved	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
7Ch	Vendor ID1	F7	F6	F5	F4	F3	F2	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0	5745h
7Eh	Vendor ID2	T7	T6	T5	T4	T3	T2	T1	T0	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0	4302h

Table 1: Mixer Register

6.2 Reset Register (Index 00h)

Reg#	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	0	1	1	0	1	1		0	0	0	0	0	0	0	0	0	0000h

The Reset register is used to configure the hardware to a known state or is used to read the status of the current hardware configuration. Writing data to this register will set all the mixer registers to their default values. Reading data from this register will return the ID code for the device.

Register Map: Register Write: sets all mixer registers to default value
Register Read: returns ID code for device
D10~D13: 3D stereo enhancement ID

6.3 Stereo Output Control Register (Index 02h)

Reg#	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
02h	Mute		ML5	ML4	ML3	ML2	ML1	ML0			MR5	MR4	MR3	MR2	MR1	MR0	8000h

6.3.1 Mute Stereo Output Mute Control

"1" : Mute enabled

"0" : Mute disabled

6.3.2 ML[5:0] Master Output (Left Channel) Volume Control

These six bits select the level of attenuation applied to the Left channel of the Stereo Output signal. The level of attenuation is programmable from 0dB to -94.5dB in 1.5dB increments, providing a total of 64 programmable levels.

6.3.3 MR[5:0] Master Output (Right Channel) Volume Control

These six bits select the level of attenuation applied to the Right channel of the Stereo Output signal. The level of attenuation is programmable from 0dB to -94.5dB in 1.5dB increments, providing a total of 64 programmable levels.

6.3.4 Output Volume Control Map

	MR0	MR1	MR2	MR3	MR4	MR5	Level(dB)
0	0	0	0	0	0	0	0.0
1	0	0	0	0	0	1	-1.5
2	0	0	0	0	1	0	-3.0
3	0	0	0	0	1	1	-4.5

4	0	0	0	1	0	0	-6.0
5	0	0	0	1	0	1	-7.5
..	..	..	..	..	..	..	..
..	..	..	..	..	..	..	..
60	1	1	1	1	0	0	-90.0
61	1	1	1	1	0	1	-91.5
62	1	1	1	1	1	0	-93.0
63	1	1	1	1	1	1	-94.5

6.4. Second Stereo Output Control Register (Index 04h)

Reg#	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
04h	Mute		SL5	SL4	SL3	SL2	SL1	SL0			SR5	SR4	SR3	SR2	SR1	SR0	8000h

We support the second line_out pair for notebook or home theater application.

6.4.1. Mute the Second Stereo Output Mute Control

“1” : Mute enable

“0” : Mute disable

6.4.2. SL[5:0] The Second Output (Left Channel) Volume Control

These six bits select the level of attenuation applied to the Left channel of the second Stereo Output signal. The level of attenuation is programmable from 0dB to -94.5dB in 1.5dB increments, providing a total of 64 programmable levels.

6.4.3. SR[5:0] The Second Output (Right Channel) Volume Control

These six bits select the level of attenuation applied to the Right channel of the second Stereo Output signal. The level of attenuation is programmable from 0dB to -94.5dB in 1.5dB increments, providing a total of 64 programmable levels.

The attenuation map is the same as the master Stereo Output control.

6.4 Mono Output Control Register (Index 06h)

Reg#	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
06h	Mute										MM5	MM4	MM3	MM2	MM1	MM0	8000h

6.4.1 Mute Mono Output Mute Control

"1" : Mute enabled

"0" : Mute disabled

6.4.2 MM[5:0] Mono Output Volume Control

These six bits select the level of attenuation applied to the Mono Output signal. The level of attenuation is programmable from 0dB to -94.5dB in 1.5dB increments, providing a total of 64 programmable levels. Please refer to **Stereo and Mono Output Attenuation.**

6.4.3 Stereo and Mono Output Attenuation

	MM0	MM1	MM2	MM3	MM4	MM5	Level(dB)
0	0	0	0	0	0	0	0.0
1	0	0	0	0	0	1	-1.5
2	0	0	0	0	1	0	-3.0
3	0	0	0	0	1	1	-4.5
4	0	0	0	1	0	0	-6.0
5	0	0	0	1	0	1	-7.5
..	..	..	..	..	..	..	..
..	..	..	..	..	..	..	..
60	1	1	1	1	0	0	-90.0
61	1	1	1	1	0	1	-91.5
62	1	1	1	1	1	0	-93.0
63	1	1	1	1	1	1	-94.5

6.5 PC_BEEP Input Volume Control Register (Index 0Ah)

Reg#	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0Ah												PV3	PV2	PV1	PV0		0000h

6.5.1 Mute PC Beep Input Mute Control

"1" : Mute enabled

"0" : Mute disabled

6.5.2 PV[3:0] PC Beep Input Volume Control

These four bits select the level of attenuation applied to the PC beep input signal. The level of attenuation is programmable from 0dB to -45dB in 3dB increments, providing a total of 16 programmable levels. The beep gain is set at 0dB when PV[3:0] = 0h.

6.6 Phone Input Volume Control Register (Index 0Ch)

Reg#	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0Ch	Mute											GN4	GN3	GN2	GN1	GN0	8008h

6.6.1 Mute Phone Input Mute Control

"1" : Mute enabled

"0" : Mute disabled

6.6.2 GN[4:0] PC Phone Input Volume Control

These five bits select the gain applied to the Phone Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Programmable Input and Output Gain Levels .**

6.6.3 Programmable Input and Output Gain Levels

	G4	G3	G2	G1	G0	Level(dB)
0	0	0	0	0	0	12.0
1	0	0	0	0	1	10.5
2	0	0	0	1	0	9.0
3	0	0	0	1	1	7.5
4	0	0	1	0	0	6.0
5	0	0	1	0	1	4.5
6	0	0	1	1	0	3.0
7	0	0	1	1	1	1.5
8	0	1	0	0	0	0.0
9	0	1	0	0	1	-1.5
10	0	1	0	1	0	-3.0
11	0	1	0	1	1	-4.5
12	0	1	1	0	0	-6.0
13	0	1	1	0	1	-7.5
14	0	1	1	1	0	-9.0
15	0	1	1	1	1	-10.5
16	1	0	0	0	0	-12.0
17	1	0	0	0	1	-13.5
18	1	0	0	1	0	-15.0
19	1	0	0	1	1	-16.5
20	1	0	1	0	0	-18.0
21	1	0	1	0	1	-19.5
22	1	0	1	1	0	-21.0
23	1	0	1	1	1	-22.5
24	1	1	0	0	0	-24.0
25	1	1	0	0	1	-25.5
26	1	1	0	1	0	-27.0
27	1	1	0	1	1	-28.5
28	1	1	1	0	0	-30.0
29	1	1	1	0	1	-31.5
30	1	1	1	1	0	-33.0
31	1	1	1	1	1	-34.5

6.7 Mic Input Volume Control Register (Index 0Eh)

Reg#	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0Eh	Mute									20dB		GN4	GN3	GN2	GN1	GN0	8008h

6.7.1 Mute Mic Input Mute Control

"1" : Mute enabled

"0" : Mute disabled

6.7.2 20dB Mic Boost Control

"1" :Fixed 20dB gain enabled

"0" : Fixed 20dB gain disabled

6.7.3 GN[4:0] Mic Input Volume Control

These five bits select the gain applied to the Mic Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Programmable Input and Output Gain Levels .**

6.8 Line Input Control Register (Index 10h)

Reg#	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
10h	Mute			GL4	GL3	GL2	GL1	GL0				GR4	GR3	GR2	GR1	GR0	8808h

6.8.1 Mute Line Input Mute Control

"1" : Mute enabled

"0" : Mute disabled

6.8.2 GL[4:0] Left Channel Gain Control

These five bits select the gain applied to the LEFT channel of the Line Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Programmable Input and Output Gain Levels .**

6.8.3 GR[4:0] Right Channel Gain Control

These five bits select the gain applied to the RIGHT channel of the Line Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Programmable Input and Output Gain Levels.**

6.9 CD Input Control Register (Index 12h)

Reg#	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
12h	Mute			GL4	GL3	GL2	GL1	GL0				GR4	GR3	GR2	GR1	GR0	8808h

6.9.1 Mute Line Input Mute Control

"1" : Mute enabled

"0" : Mute disabled

6.9.2 GL[4:0] Left Channel Gain Control

These five bits select the gain applied to the LEFT channel of the Line Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Programmable Input and Output Gain Levels .**

6.9.3 GR[4:0] Right Channel Gain Control

These five bits select the gain applied to the RIGHT channel of the Line Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 3: Programmable Input and Output Gain Levels .**

6.10 Video Input Control Register (Index 14h)

Reg#	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
14h	Mute			GL4	GL3	GL2	GL1	GL0				GR4	GR3	GR2	GR1	GR0	8808h

6.10.1 Mute Line Input Mute Control

"1" : Mute enabled

"0" : Mute disabled

6.10.2 GL[4:0] Left Channel Gain Control

These five bits select the gain applied to the LEFT channel of the Line Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Programmable Input and Output Gain Levels .**

6.10.3 GR[4:0] Right Channel Gain Control

These five bits select the gain applied to the RIGHT channel of the Line Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Programmable Input and Output Gain Levels .**

6.11 Auxiliary Input Control Register (Index 16h)

Reg#	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
16h	Mute			GL4	GL3	GL2	GL1	GL0				GR4	GR3	GR2	GR1	GR0	8808h

6.11.1 Mute Line Input Mute Control

"1" : Mute enabled

"0" : Mute disabled

6.11.2 GL[4:0] Left Channel Gain Control

These five bits select the gain applied to the LEFT channel of the Line Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Programmable Input and Output Gain Levels .**

6.11.3 GR[4:0] Right Channel Gain Control

These five bits select the gain applied to the RIGHT channel of the Line Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Programmable Input and Output Gain Levels .**

6.12 PCM Output Control Register (Index 18h)

Reg#	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
18h	Mute			GL4	GL3	GL2	GL1	GL0				GR4	GR3	GR2	GR1	GR0	8808h

6.12.1 Mute Line Input Mute Control

"1" : Mute enabled

"0" : Mute disabled

6.12.2 GL[4:0] Left Channel Gain Control

These five bits select the gain applied to the LEFT channel of the Line Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Programmable Input and Output Gain Levels .**

6.12.3 GR[4:0] Right Channel Gain Control

These five bits select the gain applied to the RIGHT channel of the Line Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Programmable Input and Output Gain Levels .**

6.13 Record Select Register (Index 1Ah)

Reg#	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
1Ah						SL2	SL1	SL0						SR2	SR1	SR0	0000h

6.13.1 Record Source Select(Left Channel)

SL<2:0>	Left Record Source
<000>	Mic
<001>	CD_L
<010>	Video In_L
<011>	Aux In_L
<100>	Line In_L
<101>	Stereo Mix_L
<110>	Mono Mix
<111>	Phone

Record Source Select(Right Channel)

SR<2:0>	Right Record Source
<000>	Mic
<001>	CD_R
<010>	Video In_R
<011>	Aux In_R
<100>	Line In_R
<101>	Stereo Mix_R
<110>	Mono Mix
<111>	Phone

6.14 Record Gain Control Register (Index 1Ch)

Reg#	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
1Ch	Mute				GL3	GL2	GL1	GL0					GR3	GR2	GR1	GR0	8000h

6.14.1 Mute Record Mute Control

"1" : Mute enabled

"0" : Mute disabled

6.14.2 GL[3:0] Record Gain Control (Left Channel)

These four bits select the gain applied to the LEFT channel recording source. The gain is programmable from 0dB to 22.5dB in 1.5dB increments, providing a total of 16 programmable levels. The gain is set at 0dB when GL[3:0] = 0h.

6.14.3 GR[3:0] Record Gain Control (Right Channel)

These four bits select the gain applied to the RIGHT channel recording source. The gain is programmable from 0dB to 22.5dB in 1.5dB increments, providing a total of 16

6.15 General Purpose Register (Index 20h)

Reg#	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
20h			3D				MIX	MS	LPBK					DAM	LPM _CD	ECHO	0000h

6.15.1 3D Stereo Enhancement

"1" : Enabled

"0" : Disabled

6.15.2 MIX Mono Output Mode

"1" : Mic Output

"0" : Mono mix output

6.15.3 MS Microphone Select

"1" : Microphone 2

"0" : Microphone 1

6.15.4 LPBK Loopback Mode

"1" : DAC/ADC Loopback enabled

"0" : DAC/ADC Loopback disabled

6.15.5 Digital Audio Mode

"1" : DAM enabled. DAC outputs bypass analog mixer and pass through the codec

“0” : Default value

6.15.6 Low Power Mixer for CD

"1" : LPX_CD enabled. Keeps CD to Line_out path alive

“0” : Default value

6.15.7 LPBK Loopback Mode

"1" : DAC/ADC Loopback enabled

"0" : DAC/ADC Loopback disabled

6.16 3D Control Register (Index 22h)

Reg#	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
22h													DP3	DP2	DP1	DP0	0000h

This Register is used to control the depth of the 3D stereo enhancement function built into of the AC’97 controller.

6.16.1 Depth of 3D Control Level

DP3 ... DP0	Depth
0	0%
1	6.67%
...	...
14	93.33%
15	100%

6.17 Power Down and Status Register (Index 26h)

Reg#	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
26h	EAPD		PR5	PR4	PR3	PR2	PR1	PR0					REF	ANL	DAC	ADC	0000h

6.17.1 EAPD External Amplifier Power Down Bit

This D15 is used to power down external amplifier. It is a read/write bit.

6.17.2 PR[5:0] Power Down Mode Bits

These read/write bits are used to control the power down states of the W83972D. Each power down function bit is enabled by setting the respective bit high. The power down modes controlled by each bit is described in the table below:

6.17.3 Status (READ Only) bits

These bits are used to monitor the readiness of some sections of the W83972D. Reading a "1" from any of these bits would be an indication of a "ready" state.

D<3:0>	Status Read Only Bits
REF	Vref at Nominal Levels
ANL	Mixers, Mux & Volume Controls Ready
DAC	DAC Ready to Accept Data
ADC	ADC Ready to Transmit Data

PR<5:0>	Power Down Mode Bits
PR0	ADC & Mux Power down
PR1	DAC Power down
PR2	Mixer (Vref on) Power down
PR3	Mixer (Vref off) Power down
PR4	AC-Link (BIT_CLK off) Power down
PR5	Internal Clock Disable

6.18 Extended Audio ID Register (Index 28h)

Reg#	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
28h	ID1	ID0														VRA	0001h

It is a read only register.

6.18.1 ID[1:0] Audio ID bits

ID1, ID0 is a 2-bit field which indicates the Codec configuration : Primary is 00; Secondary is 01, 10, or 11.

6.18.2 VRA bit

VRA=1 indicates optional Varaible Rate PCM Audio is supported. The default value is one.

6.19 Extended Audio Status and Control Register (Index 2Ah)

Reg#	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
2Ah																VRE	0000h

VRE=1 enables Varaible Rate Audio mode. It is a read/write bit and its default value is zero.

6.20 DAC Sample Rate Control Register (Index 2Ch)

Reg#	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
2Ch	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h

6.20.1 SR[15:0] DAC Sample Rate bits

These bits are read/write bits and used to control DAC sample rate. They can only be written as the VRE bit(in 2Ah) is set. Their default value is BB80h which indicates that DAC operates in 48K sample rate.

Sample rate	D15-D0
8,000	1F40
11,025	2B11
16,000	3E80
22,050	5622
32,000	7D00
44,100	AC44
48,000	BB80

6.21 ADC Sample Rate Control Register (Index 32h)

Reg#	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
32h	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h

6.21.1 SR[15:0] DAC Sample Rate bits

These bits are read/write bits and used to control ADC sample rate. They can only be written as the VRE bit(in 2Ah) is set. Their default value is BB80h which indicates that DAC operates in 48K sample rate.

Sample rate	D15-D0
8,000	1F40
11,025	2B11
16,000	3E80
22,050	5622
32,000	7D00
44,100	AC44
48,000	BB80

6.22 Enhanced Function register (Index 5Eh)(76h)

Reg#	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
5Eh		LPM_CD	ECHO	DAM													0000h

LPM_CD : “1” to keep CD to LINE_OUT path alive in low power mode.

ECHO : “1” to offer the data for echo cancellation; microphone signal is put in left channel of ADC in, and stereo signal is put in right channel of ADC in.

DAM : “1” to enable that DAC directly output to line_out and bypass analog mixer.

6.23 Vendor Identification Registers (Index 7Ch, 7Eh)

Reg#	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
7Ch	0	1	0	1	0	1	1	1	0	1	0	0	0	1	0	1	5745h
7Eh	0	1	0	0	0	0	1	1	0	0	0	0	0	0	1	0	4302h

The upper and lower byte of this register (index 7Ch), in conjunction with the upper byte of index register 7Eh, make up the vendor identification code for the W83972. The Vendor ID Code (in ASCII format) is equal to WEC(Winbond Elec. Inc. ,), where:

F[7:0] Upper Byte (Index 7Ch) D[15:8] = W

S[7:0] Lower Byte (Index 7Ch) D[7:0] = E

T[15:8] Upper Byte (Index 7Eh) D[15:8] = C

The upper byte of this register is used in conjunction with index register 7Ch to make up the Vendor ID code for the W83972. The lower byte identifies the revision code of the W83972.

T[15:8] See description in Vendor Identification Register.

REV[7:0] Revision ID "02"” as Revision Number.

7. MULTIPLE CODEC EXTENSION

One primary and a maximum of three secondary codecs may be supported as an option.

7.1 Multiple Codec Mode Select

ID0	ID1	Codec Mode
NC	NC	Primary Codec
pull down	NC	Secondary Codec 1
NC	pull down	Secondary Codec 2
pull down	pull down	Secondary Codec 3

Note: Digital Controller supports four DATA_IN pins to support one primary and three secondary codecs. BIT_CLK is an output for the primary codec and an input pin for the controller and secondary codecs.

7.2 Multiple Codec Example

One primary codec and three secondary codecs, with ID0 and ID1 defining which codec is primary and the order of the secondary codecs. Note that the ID0 and ID1 are internally pulled up; therefore, when left floating they configure Codec as Primary. Note: 1 = pull up. 0 = pull down.

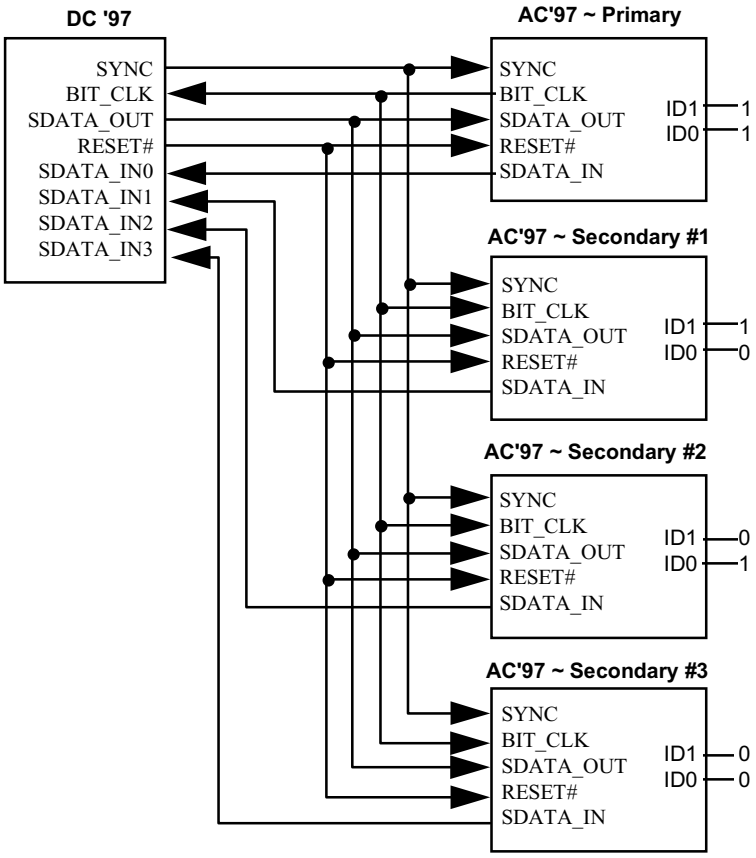


Figure 7.1: Multiple Codec Example

8. ELECTRICAL SPECIFICATIONS

8.1 DC Characteristics:

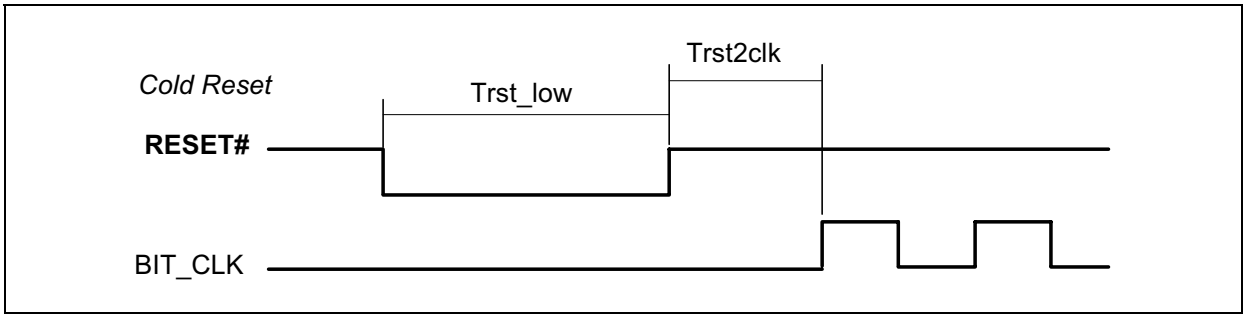
Ta = 25°C, DVdd = 5.0V or 3.3V +/- 5%; AVss = DVss = 0V; 50pF load

Parameters	Symbol	Min	Typ	Max	Units
Input Voltage Range	Vin	-0.3		Vdd + 0.3	v
Input Voltage (low)	Vil			0.3 x Vdd	v
Input Voltage (high)	Vih	0.4 x Vdd			v
Output Voltage (low)	Vol			0.2 x Vdd	v
Output Voltage (high)	Voh	0.5 x Vdd			v
Input Leakage Current (AC-Link)		-10		10	uA
Output Leakage Current (AC-Link and Hi-Z)		-10		10	uA
Output Buffer Drive Current			5		mA

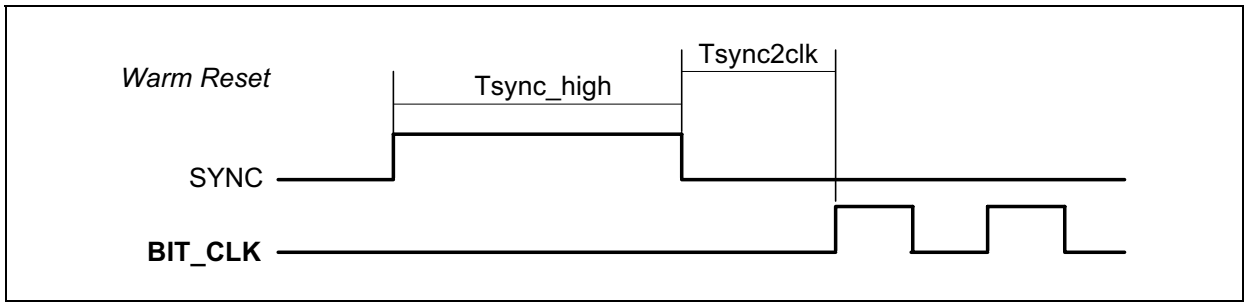
8.2 AC Timing Characteristics

Timing Diagrams: Ta = 25°C, DVdd = 5.0V or 3.3V +/- 5%; AVss = DVss = 0V; 50pF load

Cold Reset/Warm Reset



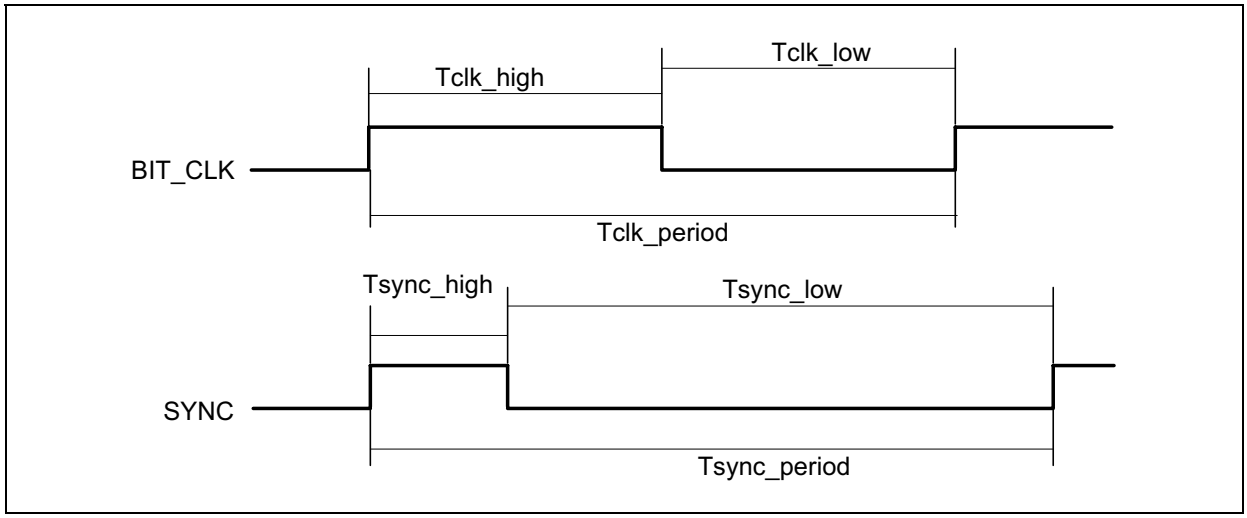
Parameters	Symbol	Min	Typ	Max	Units
RESET# active low pulse width	Trstlow	1			uS
RESET# inactive to BIT_CLK startup delay	Trst2clk	162.8			uS



Parameters	Symbol	Min	Typ	Max	Units
SYNC active high pulse width	Tsync_high		1.3		us
SYNC inactive to BIT_CLK startup delay	Tsync2clk	162.8			ns

8.3 BIT_CLK / SYNC

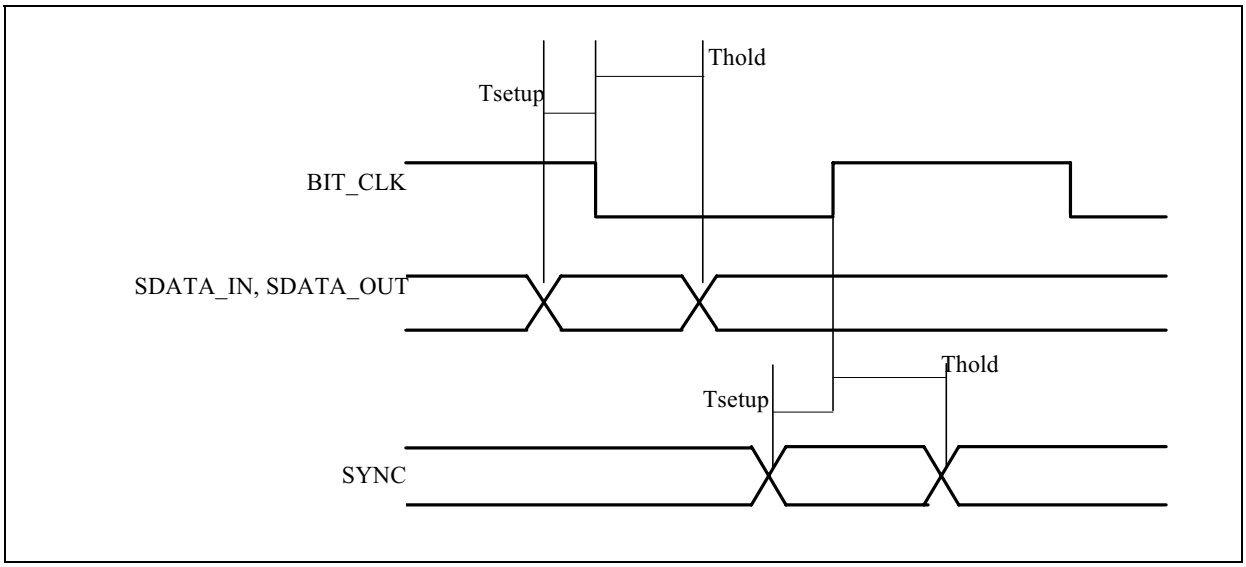
Duty Cycle: 40/60 (worst case)



Parameters	Symbol	Min	Typ	Max	Units
BIT_CLK frequency			12.288		MHz
BIT_CLK period	Tclk_period		81.4		nS
BIT_CLK output jitter				750	pS
BIT_CLK pulse width (high)	Tclk_high	32.56	40.7	48.84	nS
BIT_CLK pulse width (low)	Tclk_low	32.56	40.7	48.84	nS
SYNC frequency			48		KHz
SYNC period	Tsync_period		20.8		uS
SYNC pulse width (high)	Tsync_high		1.3		uS
SYNC pulse width (low)	Tsync_low		19.5		uS

8.4 Setup and Hold

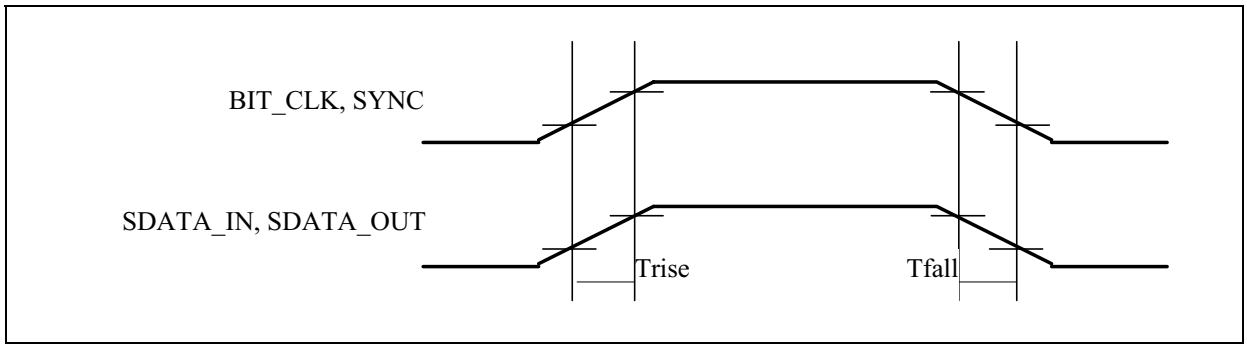
Load Capacitance: 50 pF



Parameters	Symbol	Min	Typ	Max	Units
SDATA_OUT setup to falling edge of BIT_CLK	Tsetup	15			ns
SDATA_OUT hold from falling edge of BIT_CLK	Thold	5			ns
SYNC setup to rising edge of BIT_CLK	Tsetup	15			ns
SYNC hold from rising edge of BIT_CLK	Thold	5			ns

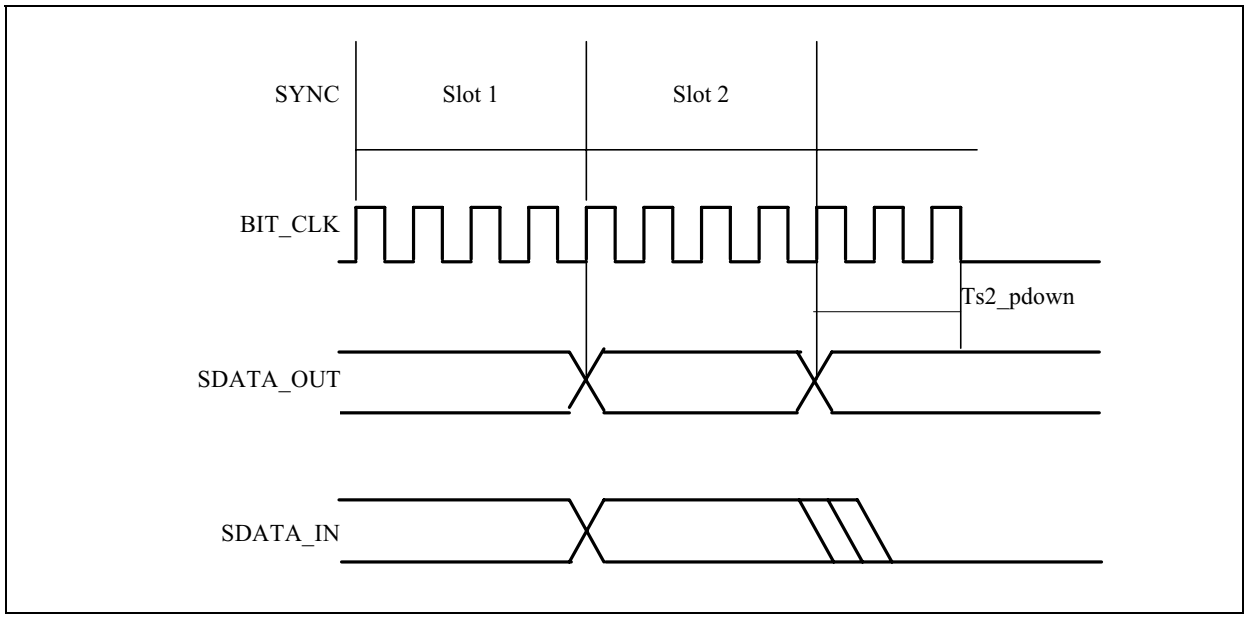
Note: SDATA_IN setup and hold calculations determined by AC'97 Controller propagation delay

8.5 Rise and Fall



Parameters	Symbol	Min	Typ	Max	Units
BIT_CLK rise time	Trise	2		6	nS
BIT_CLK fall time	Tfall	2		6	nS
SYNC rise time	Trise	2		6	nS
SYNC fall time	Tfall	2		6	nS
SDATA_IN rise time	Trise	2		6	nS
SDATA_IN fall time	Tfall	2		6	nS
SDATA_OUT rise time	Trise	2		6	nS
SDATA_OUT fall time	Tfall	2		6	nS

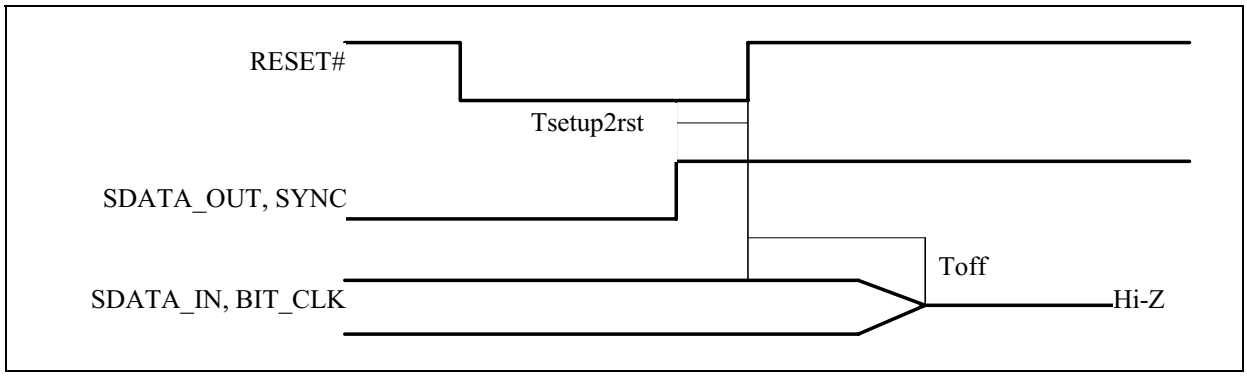
8.6 AC_Link Low Power Mode



Parameters	Symbol	Min	Typ	Max	Units
End of Slot 2 to BIT_CLK/SDATA_IN low	Ts2_pdown			1	uS

Note: BIT_CLK not to scale

8.7 ATE/ Vendor Test Mode



Parameters	Symbol	Min	Typ	Max	Units
SDATA_OUT/SYNC setup to RESET# rising edge	Tsetup2rst	15			nS
RESET# rising edge to Hi-Z state	Toff			25	nS

9. PERFORMANCE SPECIFICATIONS

9.1 Analog Characteristics:

Ta = 25°C, AVdd = 5.0V +/- 5% DVdd = 3.3V +/- 5%; AVss = DVss = 0V; 10kΩ/50pF load

Fs = 48kHz, 0dB = 1Vrms; BW: 20Hz ~ 20kHz, 0dB attenuation

Parameters	Symbol	Min	Typ	Max	Units
Full Scale Input Voltage:					
Line Inputs			1.0		Vrms
Mic Inputs (20dB = 0)			1.0		Vrms
Mic Inputs (20dB = 1)			0.1		Vrms
Full Scale Output Voltage:					
Line Outputs			1.0		Vrms
Mono Output			1.0		Vrms
Analog S/N:					
CD to LINE_OUT		90			dB
Other to LINE_OUT			85		dB
Analog Frequency Response:		20		20,000	Hz
Digital S/N:					
D/A		85	90		dB
A/D		75	80		dB
Total Harmonic Distortion:					
Line Outputs			0.007	0.02	%
D/A & A/D Frequency Response:					
D/A		20		19,200	Hz
A/D		20		19,200	Hz
Transition Band:					
D/A		19,200		28,800	Hz
A/D		19,200		28,800	Hz
Stop Band:					
D/A		28,800		infinite	Hz
A/D		28,800		infinite	Hz
Stop Band Rejection:					
D/A		-74			dB
A/D		-74			dB
Out-of-Band Rejection:			-40		dB
Group Delay:				1	mS
Power Supply Rejection Ratio:			-40		dB

Parameters	Symbol	Min	Typ	Max	Units
(1kHz)					
Input Channel Crosstalk:				-70	dB
Spurious Tone Reduction:			-100		dB
Attenuation, Gain Step Size			1.5		dB
Input Impedance:		10	50		k ohm
Input Capacitance:			15		pF
Vrefout			2.5		V

Notes: Vil = 0.8V, Vih = 2.4V

Analog Frequency Response has ± 1dB limits

SNR of rms output level with 1kHz full-scale input to rms output level with all zeros into digital input

Measured "A wtd" over a 20Hz ~ 20kHz bandwidth (AES17-1991 Idle Channel Noise or EIAJ CP-307 SNR)

THD: 0dB gain, 20kHz BW, Fs = 48kHz

A/D & D/A Frequency Response has ± 0.25dB limits

Stop Band Rejection determines filter requirements

Out-of-Band rejection determines audible noise

Integrated Out-of-Band noise generated by DAC during normal PCM audio playback over: BW = 28.8kHz ~ 100kHz, with respect to 1 Vrms DAC output

9.2 Miscellaneous Analog Performance Characteristics:

Ta = 25°C, AVdd = 5.0V +/- 5% DVdd = 3.3V +/- 5%; AVss = DVss = 0V; 10kΩ/50pF load

Fs = 48kHz, 0dB = 1Vrms; BW: 20Hz ~ 20kHz, 0dB attenuation

Parameters	Symbol	Min	Typ	Max	Units
Mixer Gain Range Span:					
LINE_IN, AUX, VIDEO, MIC1, MIC2, PHONE			46.5		dB
PC_BEEP			45		dB
LINE_OUT, MONO_OUT			94.5		dB
Mixer Step Size:					
All Volume Controls Except PC_BEEP			1.5		dB
PC_BEEP			3.0		dB
Mixer Mute Level:			110		dB
Mixer Gain:					
Interchannel Gain Mismatch		-0.5		0.5	dB
Gain Drift			100		ppm/°C
A/D and Analog Inputs: (Rs = 50 ohms)					
Resolution				16	bits
Gain Error			±2	±5	%
Offset Error			10		mV
Input Impedance			50		k ohm
D/A and Analog Outputs:					
Resolution				16	bits
Interchannel Isolation			85		dB
Interchannel Gain Mismatch			0.1	0.2	dB
Gain Error				±5	%
Gain Drift			60		ppm/°C

Note: Gain Error and Offset Error expressed in terms of ± values

9.3 Power Consumption:

Ta = 25°C, AVdd = 5.0V +/- 5% DVdd = 3.3V +/- 5%; AVss = DVss = 0V; 50pF load

Parameters	Symbol	Min	Typ	Max	Units
Digital Supply Current:					
Power Up	Ivdd		70		mA
Power Down	Ivdd		0.1		mA
Analog Supply Current:					
Power Up	Iavd		28		mA
Power Down	Iavd		0.1		mA

10. POWER MANAGEMENT

Power Management is capable of shutting down portions of the Codec with Control Bits

PR<5:0>	Power Down Mode Bits
PR0	PCM_IN ADC & Input MUX Powerdown
PR1	PCM_OUT DAC Powerdown
PR2	Analog Mixer Powerdown (Vref on)
PR3	Analog Mixer Powerdown (Vref off)
PR4	Digital Interface (AC-Link) Powerdown (BIT_CLK off)
PR5	Internal Clock Disable

Note: Registers maintain values in sleep mode (PR4 write) and wake up with a warm reset (register values) or a cold reset (default values). Power Down and Status Register (Index 26) read action verifies stability before powerdown write action occurs.

10.1 Power Down / Power Up

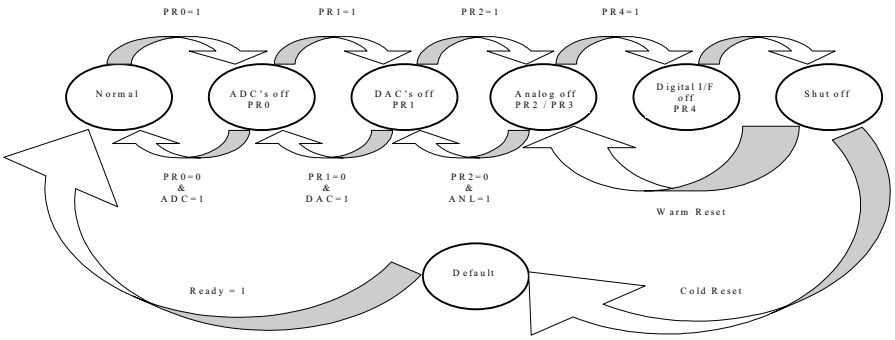


Figure 10.1: Power down/Power up Procedure

Note: In the example above, the Analog Mixer has been disabled, but the Vref is still on.

Complete Power Down of the AC'97 device is achieved by sequential writes to the Power Down and Status Control Register (Index 26h):

Normal Operation:	PR<5:0> = 0
ADC′s and Input Mux:	PR0 = 1 (write)
DAC′s:	PR1 = 1 (write)
Analog Mixer:	PR2 = 1 (write)
Vrefout:	PR3 = 1 (write)
AC-Link:	PR4 = 1 (write)
Internal Clocks:	PR5 = 1 (write)

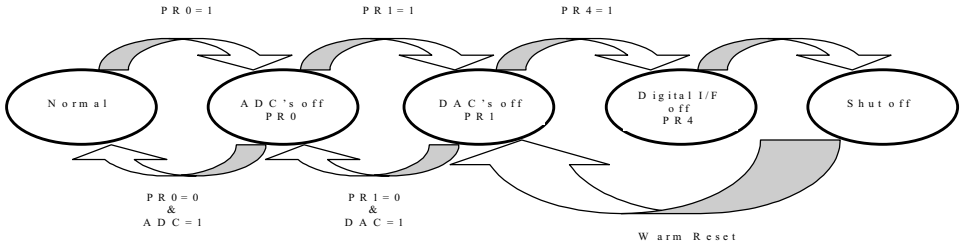


Figure 10.2: Power Down Procedure with Analog Section Still Active

Note: To Power Up the Codec, a Warm Reset or a Cold Reset is required; PR4 is reset to zero upon either reset.

11. TEST MODE OPERATION

11.1 ATE Test Mode:

PCB In-Circuit Testing of the W83972D

SDATA_OUT is sampled at the rising edge of RESET# to enter ATE test mode
SDATA_IN and BIT_CLK outputs are driven to a high impedance (Hi-Z) state

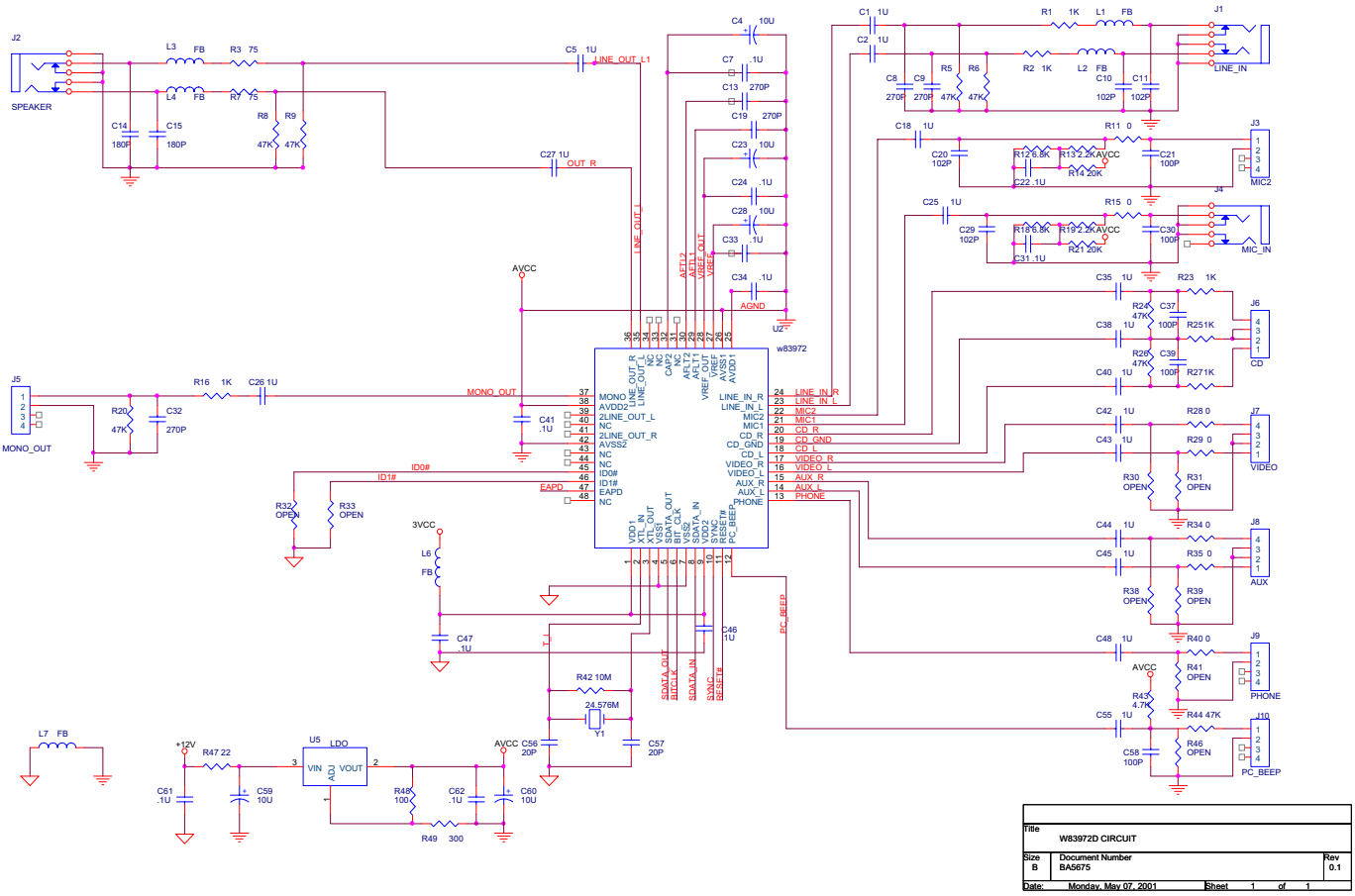
Note: this case never occurs during normal operation

11.2 Vendor Test Mode:

Vendor test mode is entered when SYNC is sampled at the rising edge of RESET# .

Note: this case never occurs during normal operation

12. APPLICATION CIRCUIT



13. HOW TO READ THE TOP MARKING

The top marking of W83972D

Left: Winbond logo

1st line: Type number W83972D, D means LQFP (Thickness = 1.4 mm).

2nd line: Tracking code 116 A D BA

116: packages made in '01, week 16

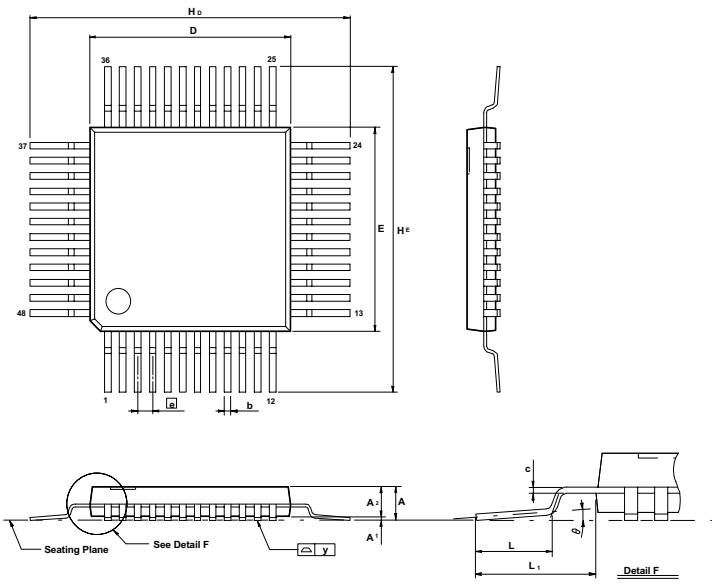
A: Assembly house ID; A means ASE, O means OSE

D: IC revision 1; A means version A, B means version B

BA: Internal use

14. PACKAGE DIMENSIONS

(48-pin QFP)



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A				---	---	1.60
A_1				0.05	---	0.15
A_2				1.35	1.40	1.45
b				0.17	0.20	0.27
c				0.09	---	0.20
D					7.00	
E					7.00	
e					0.50	
H_D					9.00	
H_E					9.00	
L				0.45	0.60	0.75
L_1					1.00	
y				---	0.08	---
θ				0	3.5°	7

Notes:

1. Dimensions D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeters
4. General appearance spec. should be based on final visual inspection spec.

Winbond Electronics Corp.

Headquarters
No. 4, Creation Rd. III
Science-Based Industrial Park
Hsinchu, Taiwan
TEL: 886-35-770066
FAX: 886-35-789467
www: http://www.winbond.com.tw/

Taipei Office
11F, No. 115, Sec. 3, Min-Sheng East Rd.
Taipei, Taiwan
TEL: 886-2-7190505
FAX: 886-2-7197502
TLX: 16485 WINTPE

Winbond Electronics (H.K.) Ltd.
Rm. 803, World Trade Square, Tower II
123 Hoi Bun Rd., Kwun Tong
Kowloon, Hong Kong
TEL: 852-27516023-7
FAX: 852-27552064

Winbond Electronics (North America) Corp.
2730 Orchard Parkway
San Jose, CA 95134 U.S.A.
TEL: 1-408-9436666
FAX: 1-408-9436668

Please note that all data and specifications are subject to change without notice. All the trade marks of products and companies mentioned in this data sheet belong to their respective owners.