

2M x 64 Stacked Flash Multi-Chip Package

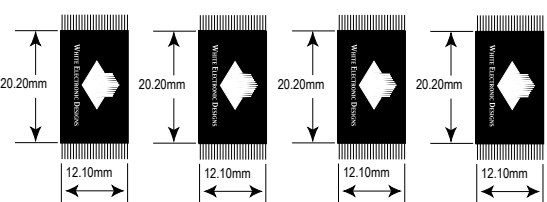

Optimum Density and Performance in One Package

WEDPF2M64-XBX3 Features

- Designed to complement PowerPC™ 750/755 and high performance memory controllers (see page 2 for typical application block diagram)

Performance Features

- Simultaneous Read/Write operations
 - Data can be continuously read from one bank while executing erase/program functions in other bank
 - Zero latency between read and write operations
- Zero Power Operation
 - Sophisticated power management circuits reduce power consumed during inactive periods to nearly zero
- 16MByte (128Mb) organized as 2Mx64
- Access Times of 100, 120, 150ns
- 1,000,000 Erase/Program Cycles per sector
- Sector Architecture
 - One 16KByte, two 8KBytes, one 32KByte, and fifteen 64KBytes in byte mode
 - Any combination of sectors can be concurrently erased. Also supports full chip erase.
- Boot Code Sector Architecture (Bottom)
- 3.3V for Read and Write Operations
- Commercial, industrial and military temperature ranges

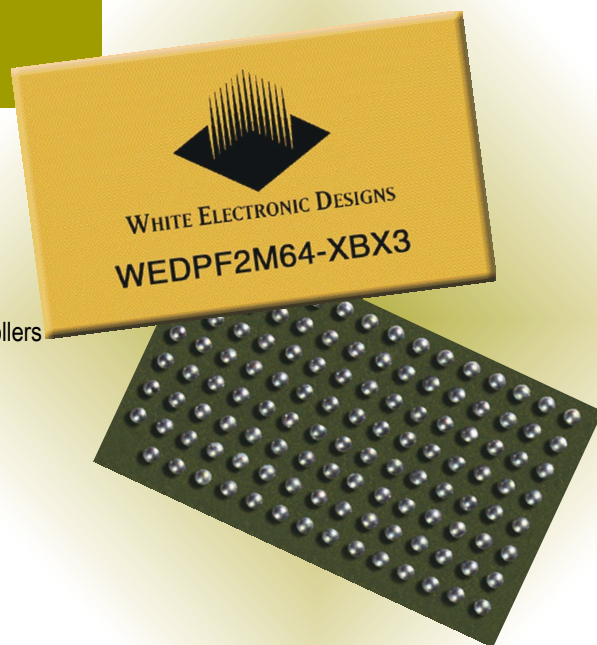
Discrete Approach		Actual Size WEDPF2M64-XBX3	S A V I N G S
			
Area	4 x 244mm ² = 978mm ²	336mm ²	
I/O Count	4 x 48 pins = 192 connections	119 PBGA	66%
			38%

Package

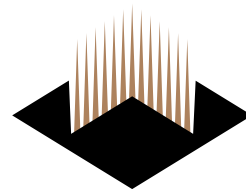
- 14x24mm, 119 Plastic Ball Grid Array (PBGA), 336mm²

For more information, visit our web site at www.whiteedc.com/mcp
or call (602) 437-1520 and ask for applications support.

* Advanced flyer. This flyer describes a product that is not fully qualified or characterized and is subject to change or cancellation without notice.
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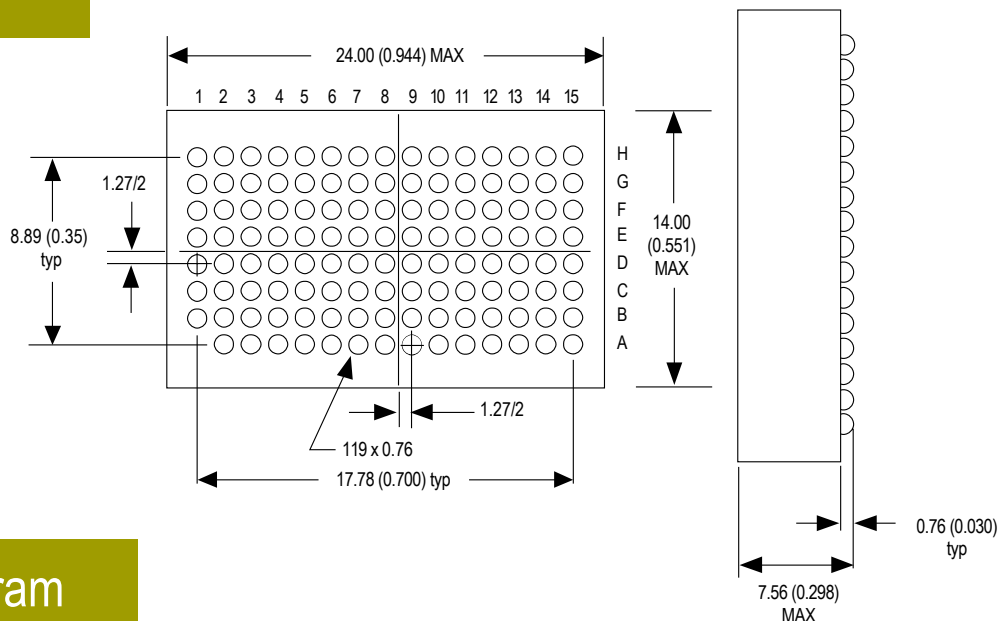


- 66% space savings
- Reduced part count
- 38% I/O reduction
- Suitable for high-reliability applications
- Upgradeable to 4Mx64 (contact factory for future availability)



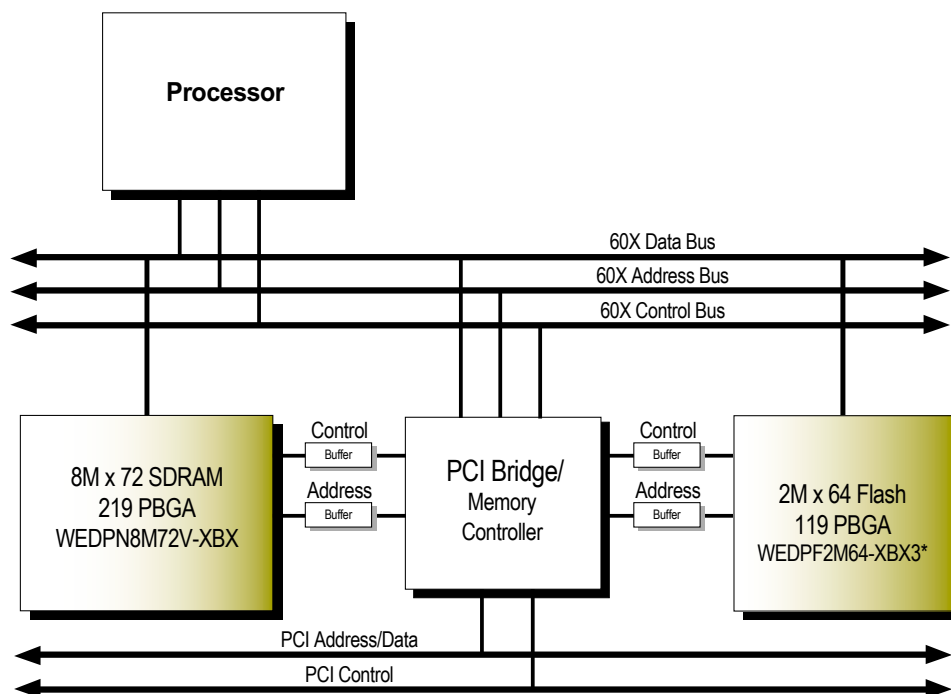
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Package Dimensions



NOTE: Dimensions in millimeters (inches)

System Block Diagram



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WHITE ELECTRONIC DESIGNS

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