



512Kx32 SRAM MODULE, SMD 5962-94611

FEATURES

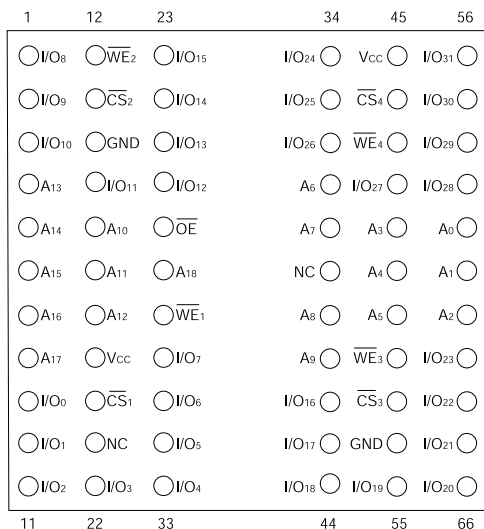
- Access Times of 15*, 17, 20, 25, 35, 45, 55ns
- Packaging
 - 66 pin, PGA Type, 1.075" square, Hermetic Ceramic HIP (Package 400).
 - 68 lead, 40mm Hermetic Low Profile CQFP, 3.5mm (0.140") (Package 502)¹, Package to be developed.
 - 68 lead, Hermetic CQFP (G2T)¹, 22.4mm (0.880") square (Package 509) 4.57mm (0.180") height. Designed to fit JEDEC 68 lead 0.990" CQFJ footprint (Fig. 3).
 - 68 lead, Hermetic CQFP (G1U), 23.9mm (0.940") square (Package 519) 3.57mm (0.140") height. Designed to fit JEDEC 68 lead 0.990" CQFJ footprint (Fig. 3).
- Organized as 512Kx32, User Configurable as 1Mx16 or 2Mx8
- Commercial, Industrial and Military Temperature Ranges
- TTL Compatible Inputs and Outputs
- 5 Volt Power Supply
- Low Power CMOS
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight
 - WS512K32-XH1X - 13 grams typical
 - WS512K32-XG2TX¹ - 8 grams typical
 - WS512K32-XG1UX - 5 grams typical
 - WS512K32-XG4TX¹ - 20 grams typical

* 15ns Access Time available only in Commercial and Industrial Temperature.
This speed is not fully characterized and is subject to change without notice.

Note 1: Package Not Recommended For New Design

FIG. 1 PIN CONFIGURATION FOR WS512K32N-XH1X

TOP VIEW



PIN DESCRIPTION

I/O ₀₋₃₁	Data Inputs/Outputs
A ₀₋₁₈	Address Inputs
\overline{WE}_{1-4}	Write Enables
\overline{CS}_{1-4}	Chip Selects
\overline{OE}	Output Enable
V _{CC}	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM

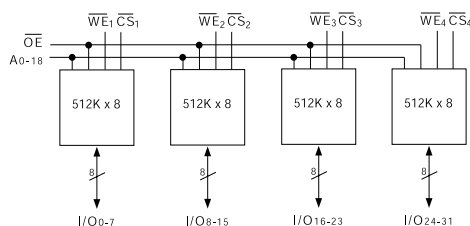
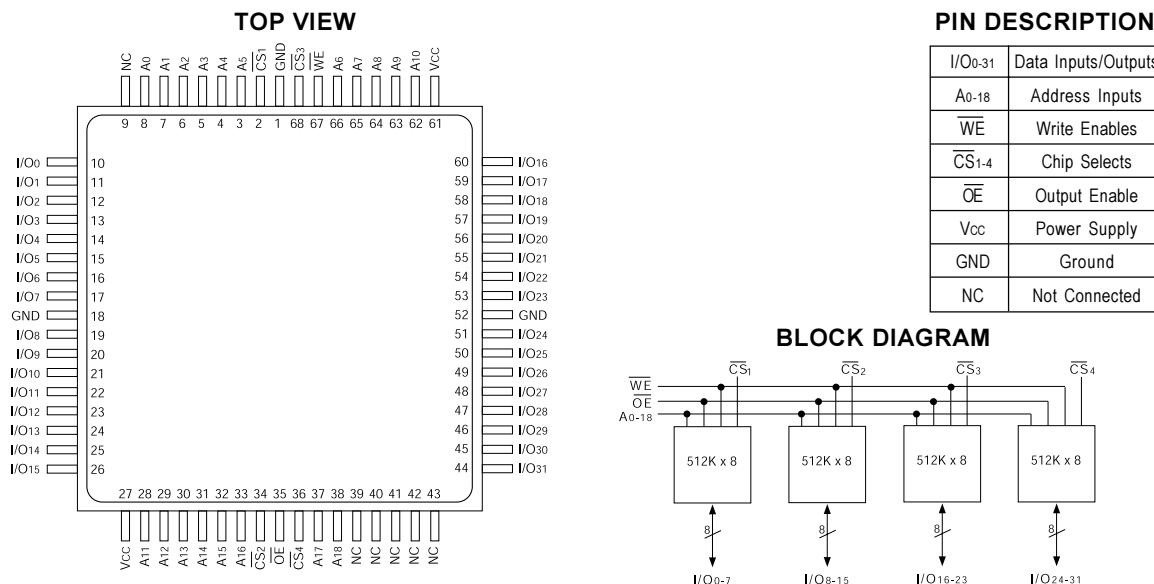


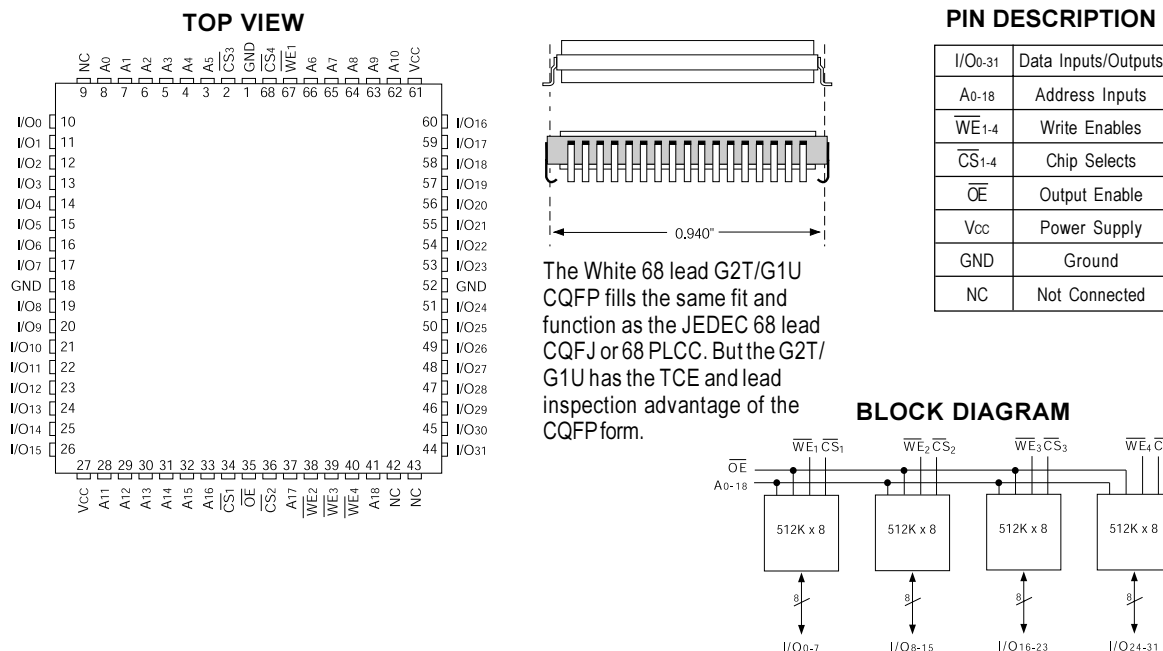


FIG.2 PIN CONFIGURATION FOR WS512K32-XG4TX¹

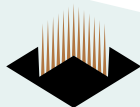


Note 1: Package Not Recommended For New Design

**FIG.3 PIN CONFIGURATION FOR WS512K32-XG2TX¹
AND WS512K32-XG1UX**



Note 1: Package Not Recommended For New Design



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T _A	-55	+125	°C
Storage Temperature	T _{STG}	-65	+150	°C
Signal Voltage Relative to GND	V _G	-0.5	V _{CC} +0.5	V
Junction Temperature	T _J		150	°C
Supply Voltage	V _{CC}	-0.5	7.0	V

TRUTH TABLE

\overline{CS}	\overline{OE}	\overline{WE}	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	H	H	Out Disable	High Z	Active
L	X	L	Write	Data In	Active

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
\overline{OE} capacitance	C _{OE}	V _{IN} = 0 V, f = 1.0 MHz	50	pF
\overline{WE}_{1-4} capacitance HIP (PGA)	C _{WE}	V _{IN} = 0 V, f = 1.0 MHz	20	pF
CQFP G4T			50	
CQFP G2T/G1U			20	
\overline{CS}_{1-4} capacitance	C _{CS}	V _{IN} = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	C _{I/O}	V _{I/O} = 0 V, f = 1.0 MHz	20	pF
Address input capacitance	C _{AD}	V _{IN} = 0 V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Units	
			Min	Max
Input Leakage Current	I _{LI}	V _{CC} = 5.5, V _{IN} = GND to V _{CC}		10
Output Leakage Current	I _{LO}	\overline{CS} = V _{IH} , \overline{OE} = V _{IH} , V _{OUT} = GND to V _{CC}		10
Operating Supply Current x 32 Mode	I _{CC x 32}	\overline{CS} = V _{IL} , \overline{OE} = V _{IH} , f = 5MHz, V _{CC} = 5.5		660
Standby Current	I _{SB}	\overline{CS} = V _{IH} , \overline{OE} = V _{IH} , f = 5MHz, V _{CC} = 5.5		80
Output Low Voltage	V _{OL}	I _{OL} = 8mA for 15 - 35ns, I _{OL} = 2.1mA for 45 - 55ns, V _{CC} = 4.5		0.4
Output High Voltage	V _{OH}	I _{OH} = -4.0mA for 15 - 35ns, I _{OH} = -1.0mA for 45 - 55ns, V _{CC} = 4.5	2.4	

NOTE: DC test conditions: V_{IH} = V_{CC} - 0.3V, V_{IL} = 0.3V

DATA RETENTION CHARACTERISTICS

(T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Units	
			Min	Max
Data Retention Supply Voltage	V _{DR}	$\overline{CS} \nless V_{CC} - 0.2V$	2.0	5.5
Data Retention Current	I _{CCDR1}	V _{CC} = 3V		28
Low Power Data Retention Current (WS512K32L-XXX)	I _{CCDR2}	V _{CC} = 3V		16



AC CHARACTERISTICS

(V_{CC}=5.0V, V_{SS}=0V, T_A= -55°C to +125°C)

Parameter	Symbol	-15*		-17		-20		-25		-35		-45		-55		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{RC}	15		17		20		25		35		45		55		ns
Address Access Time	t _{AA}		15		17		20		25		35		45		55	ns
Output Hold from Address Change	t _{OH}	0		0		0		0		0		0		0		ns
Chip Select Access Time	t _{ACS}		15		17		20		25		35		45		55	ns
Output Enable to Output Valid	t _{OE}		8		9		10		12		25		25		25	ns
Chip Select to Output in Low Z	t _{CLZ} ¹	2		2		2		2		4		4		4		ns
Output Enable to Output in Low Z	t _{OLZ} ¹	0		0		0		0		0		0		0		ns
Chip Disable to Output in High Z	t _{CHZ} ¹		12		12		12		12		15		20		20	ns
Output Disable to Output in High Z	t _{OHZ} ¹		12		12		12		12		15		20		20	ns

* 15ns Access Time available only in Commercial and Industrial Temperature. This speed is not fully characterized and is subject to change without notice.

1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS

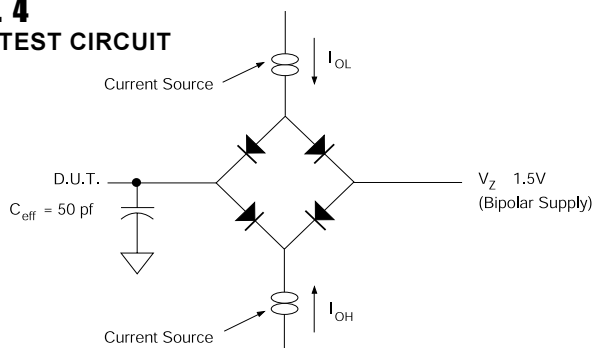
(V_{CC}=5.0V, V_{SS}=0V, T_A= -55°C to +125°C)

Parameter	Symbol	-15*		-17		-20		-25		-35		-45		-55		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{WC}	15		17		20		25		35		45		55		ns
Chip Select to End of Write	t _{CW}	13		15		15		17		25		35		50		ns
Address Valid to End of Write	t _{AW}	13		15		15		17		25		35		50		ns
Data Valid to End of Write	t _{DW}	10		11		12		13		20		25		25		ns
Write Pulse Width	t _{WP}	13		15		15		17		25		35		40		ns
Address Setup Time	t _{AS}	2		2		2		2		2		2		2		ns
Address Hold Time	t _{AH}	0		0		0		0		0		5		5		ns
Output Active from End of Write	t _{OW} ¹	2		2		3		4		4		5		5		ns
Write Enable to Output in High Z	t _{WHZ} ¹		8		9		11		13		15		20		20	ns
Data Hold Time	t _{DH}	0		0		0		0		0		0		0		ns

* 15ns Access Time available only in Commercial and Industrial Temperature. This speed is not fully characterized and is subject to change without notice.

1. This parameter is guaranteed by design but not tested.
2. The Address Setup Time of minimum 2ns is for the G2T, G1U and H1 packages. t_{AS} minimum for the G4T package is 0ns.

FIG. 4
AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V _{IL} = 0, V _{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:

V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z₀ = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.



FIG. 5
TIMING WAVEFORM - READ CYCLE

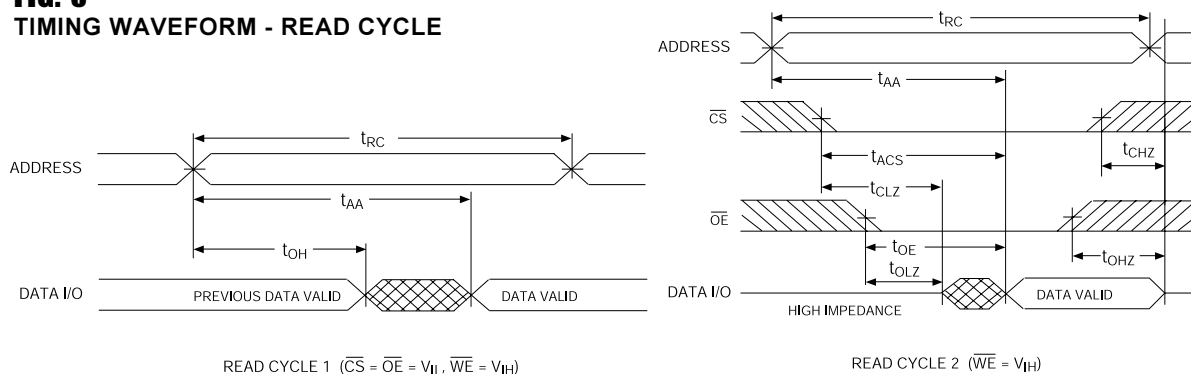


FIG. 6
WRITE CYCLE - \overline{WE} CONTROLLED

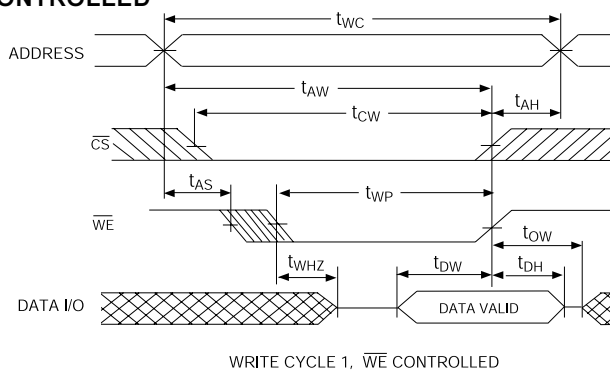
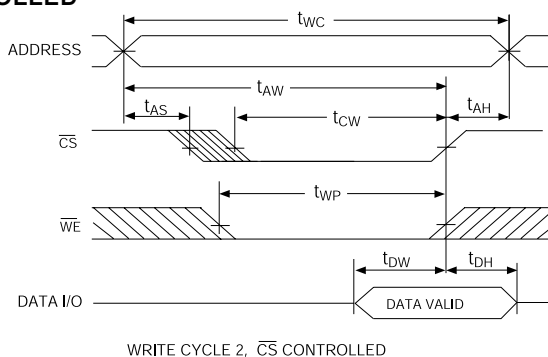
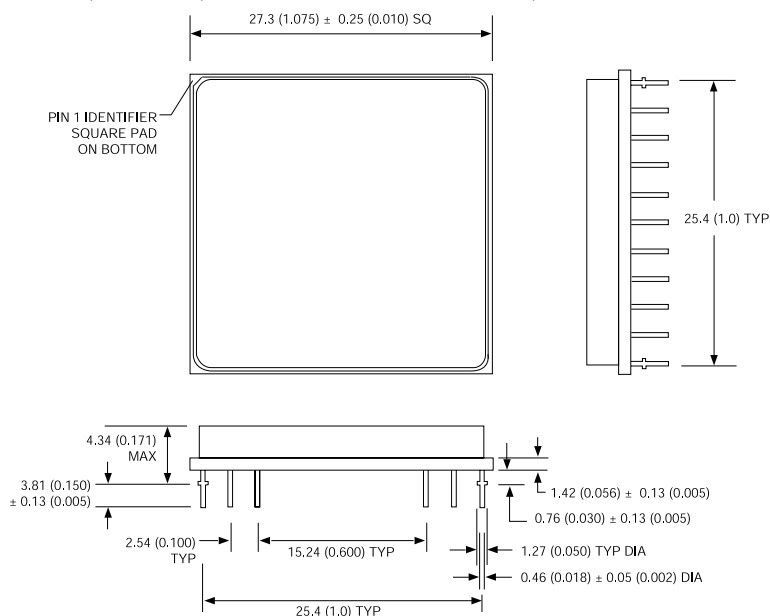


FIG. 7
WRITE CYCLE - \overline{CS} CONTROLLED



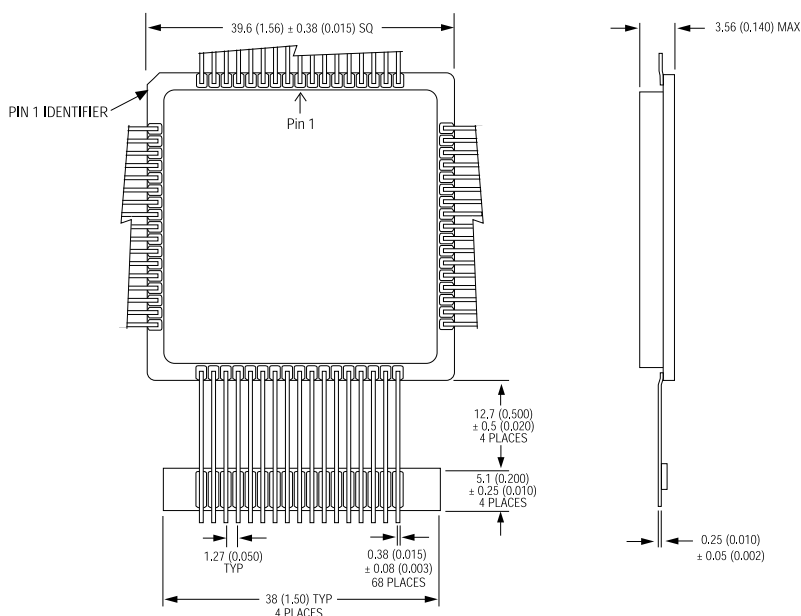


PACKAGE 400: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H1)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 502: 68 LEAD, CERAMIC QUAD FLAT PACK, LOW PROFILE CQFP (G4T)'

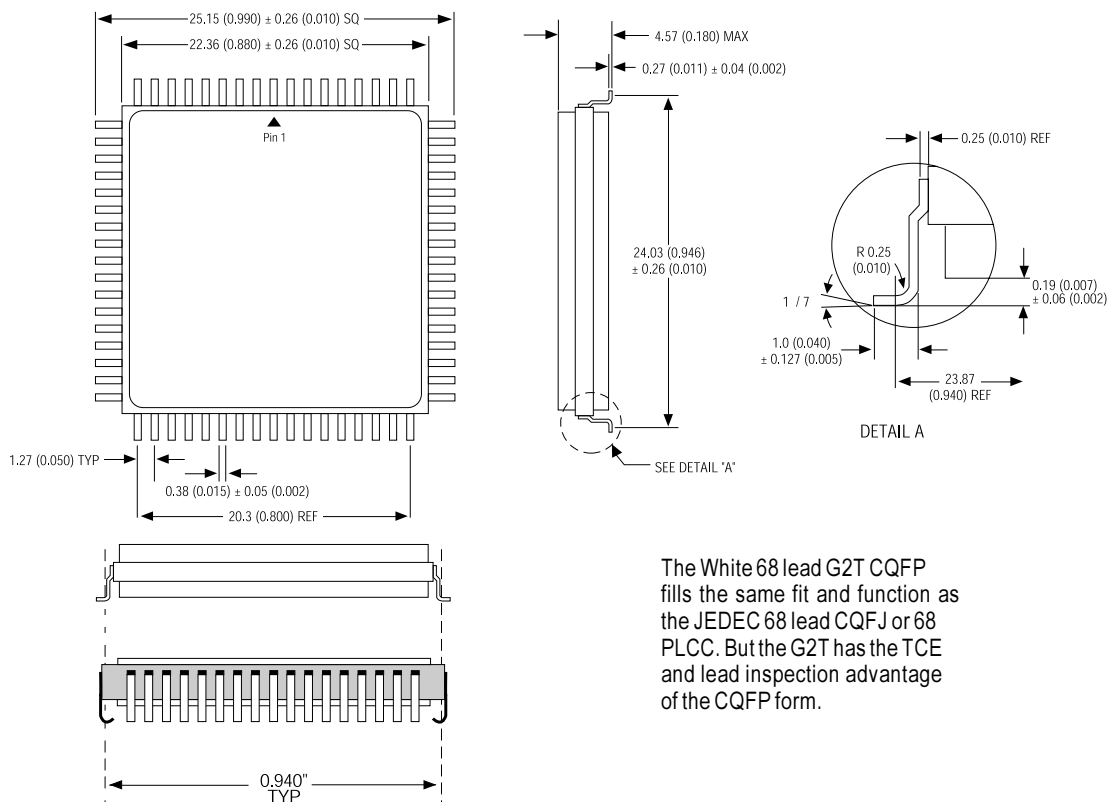


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Note 1: Package Not Recommended For New Design



PACKAGE 509: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2T)¹



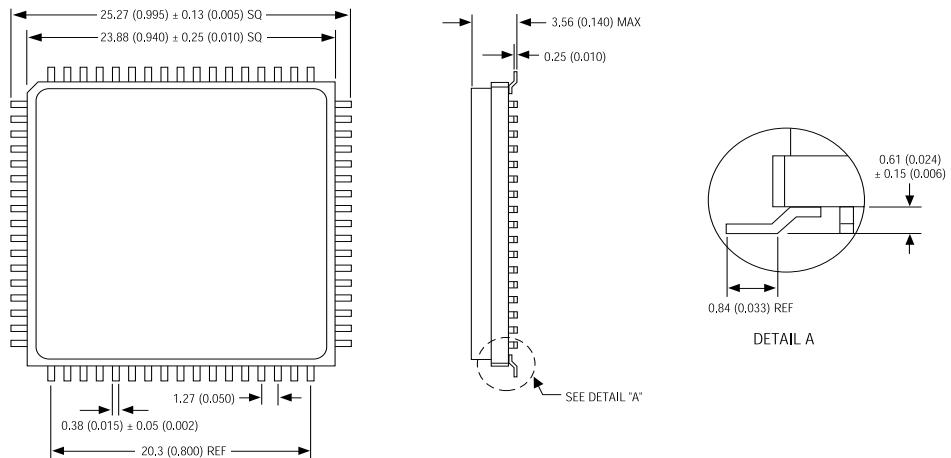
The White 68 lead G2T CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2T has the TCE and lead inspection advantage of the CQFP form.

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

Note 1: Package Not Recommended For New Design



PACKAGE 519: 68 LEAD, CERAMIC QUAD FLAT PACK, LOW PROFILE CQFP (G1U)



The White 68 lead G1U CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G1U has the TCE and lead inspection advantage of the CQFP form.

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



ORDERING INFORMATION

W S 512K 32 X - XXX X X X

LEAD FINISH:

Blank = Gold plated leads

A = Solder dip leads

DEVICE GRADE:

Q = MIL-STD-883 Compliant

M = Military Screened -55°C to +125°C

I = Industrial -40°C to 85°C

C = Commercial 0°C to +70°C

PACKAGE TYPE:

H1 = Ceramic Hex-In-line Package, HIP (Package 400)

G2T¹ = 22.4mm Ceramic Quad Flat Pack, CQFP (Package 509)

G4T¹ = 40mm Low Profile CQFP (Package 502)

G1U = 23.9mm Low Profile CQFP (Package 519)

ACCESS TIME (ns)

IMPROVEMENT MARK:

N = No Connect at pin 21 and 39 in HIP for Upgrades

Blank = Standard Power

L = Low Power Data Retention

ORGANIZATION, 512Kx32

User configurable as 1Mx16 or 2Mx8

SRAM

WHITE ELECTRONIC DESIGNS CORP.

Note 1: Package Not Recommended For New Design



DEVICE TYPE	SPEED	PACKAGE	SMD NO.
512K x 32 SRAM Module	55ns	66 pin HIP (H1)	5962-94611 05HTX
512K x 32 SRAM Module	45ns	66 pin HIP (H1)	5962-94611 06HTX
512K x 32 SRAM Module	35ns	66 pin HIP (H1)	5962-94611 07HTX
512K x 32 SRAM Module	25ns	66 pin HIP (H1)	5962-94611 08HTX
512K x 32 SRAM Module	20ns	66 pin HIP (H1)	5962-94611 09HTX
512K x 32 SRAM Module	17ns	66 pin HIP (H1)	5962-94611 10HTX
512K x 32 SRAM Module	55ns	68 lead CQFP Low Profile (G4T) ¹	5962-94611 05HYX
512K x 32 SRAM Module	45ns	68 lead CQFP Low Profile (G4T) ¹	5962-94611 06HYX
512K x 32 SRAM Module	35ns	68 lead CQFP Low Profile (G4T) ¹	5962-94611 07HYX
512K x 32 SRAM Module	25ns	68 lead CQFP Low Profile (G4T) ¹	5962-94611 08HYX
512K x 32 SRAM Module	20ns	68 lead CQFP Low Profile (G4T) ¹	5962-94611 09HYX
512K x 32 SRAM Module	17ns	68 lead CQFP Low Profile (G4T) ¹	5962-94611 10HYX
512K x 32 SRAM Module	55ns	68 lead CQFP (G2T) ¹	5962-94611 05HMX
512K x 32 SRAM Module	45ns	68 lead CQFP (G2T) ¹	5962-94611 06HMX
512K x 32 SRAM Module	35ns	68 lead CQFP (G2T) ¹	5962-94611 07HMX
512K x 32 SRAM Module	25ns	68 lead CQFP (G2T) ¹	5962-94611 08HMX
512K x 32 SRAM Module	20ns	68 lead CQFP (G2T) ¹	5962-94611 09HMX
512K x 32 SRAM Module	17ns	68 lead CQFP (G2T) ¹	5962-94611 10HMX
512K x 32 SRAM Module	55ns	68 lead CQFP (G1U)	5962-94611 05H9X
512K x 32 SRAM Module	45ns	68 lead CQFP (G1U)	5962-94611 06H9X
512K x 32 SRAM Module	35ns	68 lead CQFP (G1U)	5962-94611 07H9X
512K x 32 SRAM Module	25ns	68 lead CQFP (G1U)	5962-94611 08H9X
512K x 32 SRAM Module	20ns	68 lead CQFP (G1U)	5962-94611 09H9X
512K x 32 SRAM Module	17ns	68 lead CQFP (G1U)	5962-94611 10H9X

Note 1: Package Not Recommended For New Design