WHITE ELECTRONIC DESIGNS

1M x 36 Synchronous Pipeline Burst NBL SRAM

FEATURES

- Fast clock speed: 166, 150, 133, and 100MHz
- Fast access times: 3.5ns, 3.8ns, 4.2ns, and 5.0ns
- Fast OE access times: 3.5ns, 3.8ns, 4.2ns, and 5.0ns
- Single +2.5V ± 5% power supply (VDD)
- Snooze Mode for reduced-standby power
- Individual Byte Write control
- Clock-controlled and registered addresses, data I/Os and control signals
- Burst control (interleaved or linear burst)
- Packaging:
  - 119-bump BGA package
  - JEDEC Pin Configuration
- Low capacitive bus loading

DESCRIPTION

The WEDC SyncBurst - SRAM family employs high-speed, low-power CMOS designs that are fabricated using an advanced CMOS process. WEDC's 36Mb SyncBurst SRAMs integrate two 1M x 18 SRAMs into a single BGA package to provide 1M x 36 configuration. All synchronous inputs pass through registers controlled by a positive-edge-triggered single-clock input (CLK). The NBL or No Bus Latency Memory utilizes all the bandwidth in any combination of operating cycles. Address, data inputs, and all control signals except output enable and linear burst order are synchronized to input clock. Burst order control must be tied "High or Low." Asynchronous inputs include the sleep mode enable (ZZ). Output Enable controls the outputs at any given time. Write cycles are internally self-timed and initiated by the rising edge of the clock input. This feature eliminates complex off-chip write pulse generation and provides increased timing flexibility for incoming signals.

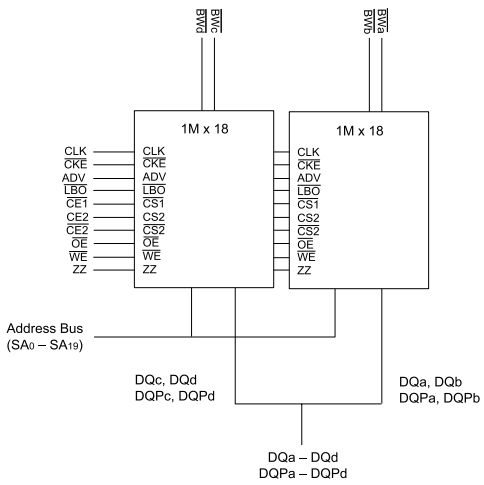
NOTE: NBL (No Bus Latency) is equivalent to ZBT™.

FIG. 1 PIN CONFIGURATION

(TOP VIEW)

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	SA	SA	SA	V_{DDQ}
B	NC	CE2	SA	ADV	SA	$\overline{CE2}$	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQc	DQPc	V_{SS}	NC	V_{SS}	DQPb	DQb
E	DQc	DQc	V_{SS}	$\overline{CE1}$	V_{SS}	DQb	DQb
F	V_{DDQ}	DQc	V_{SS}	$\overline{OE}$	V_{SS}	DQb	V_{DDQ}
G	DQc	DQc	$\overline{BWc}$	SA	$\overline{BWb}$	DQb	DQb
H	DQc	DQc	V_{SS}	$\overline{WE}$	V_{SS}	DQb	DQb
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQd	DQd	V_{SS}	CLK	V_{SS}	DQa	DQa
L	DQd	DQd	$\overline{BWd}$	NC	$\overline{BWa}$	DQa	DQa
M	V_{DDQ}	DQd	V_{SS}	$\overline{CKE}$	V_{SS}	DQa	V_{DDQ}
N	DQd	DQd	V_{SS}	SA1	V_{SS}	DQa	DQa
P	DQd	DQPd	V_{SS}	SA0	V_{SS}	DQPa	DQa
R	NC	SA	$\overline{LBO}$	V_{DD}	NC	SA	NC
T	NC	NC	SA	SA	SA	SA	ZZ
U	V_{DDQ}	NC	NC	NC	NC	NC	V_{DDQ}

BLOCK DIAGRAM



FUNCTION DESCRIPTION

The WED2ZL361MSJ is an NBL SSRAM designed to sustain 100% bus bandwidth by eliminating turnaround cycles when there is transition from Read to Write, or vice versa. All inputs (with the exception of $\overline{OE}$, $\overline{LBO}$ and ZZ) are synchronized to rising clock edges.

All read, write and deselect cycles are initiated by the ADV input. Subsequent burst addresses can be internally generated by the burst advance pin (ADV). ADV should be driven to Low once the device has been deselected in order to load a new address for next operation.

The clock Enable ($\overline{CKE}$) pin allows the operation of the chip to be suspended as long as necessary. When $\overline{CKE}$ is high, all synchronous inputs are ignored and the internal device registers will hold their previous values. NBL SSRAM latches external address and initiates a cycle when $\overline{CKE}$ and ADV are driven low at the rising edge of the clock.

Output Enable ($\overline{OE}$) can be used to disable the output at any given time. Read operation is initiated when at the rising edge of the clock, the address presented to the address inputs are latched in the address register, $\overline{CKE}$ is driven low, the write enable input signals $\overline{WE}$ are driven high, and ADV driven low. The internal array is read between the first rising edge and the second rising edge of the clock and the data is latched in the output register. At the second clock edge the data is driven out of the SRAM. During read operation $\overline{OE}$ must be driven low for the device to drive out the requested data.

Write operation occurs when $\overline{WE}$ is driven low at the rising edge of the clock. $\overline{BW}$[d:a] can be used for byte write operation. The pipe-lined NBL SSRAM uses a late-late write cycle to utilize 100% of the bandwidth. At the first rising edge of the clock, $\overline{WE}$ and address are registered, and the data associated with that address is required two cycles later.

Subsequent addresses are generated by ADV High for the burst access as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the $\overline{LBO}$ pin. When this pin is low, linear burst sequence is selected. When this pin is high, interleaved burst sequence is selected.

During normal operation, ZZ must be driven low. When ZZ is driven high, the SRAM will enter a Power Sleep Mode after 2 cycles. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM operates after 2 cycles of wake up time.

BURST SEQUENCE TABLE

(Interleaved Burst, $\overline{LBO}$ = High)

$\overline{LBO}$ Pin	High	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
		0	1	0	0	1	1	1	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	1	0	0	1	0	0

(Linear Burst, $\overline{LBO}$ = Low)

$\overline{LBO}$ Pin	High	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
		0	1	1	0	1	1	0	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	0	0	0	1	1	0

NOTES

1. $\overline{LBO}$ pin must be tied to High or Low, and Floating State must not be allowed.
2. $\overline{LBO}$ cannot change after initial power up.

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

$\overline{CEx}$	ADV	$\overline{WE}$	$\overline{BWx}$	$\overline{OE}$	$\overline{CKE}$	CLK	Address Accessed	Operation
H	L	X	X	X	L	↑	N/A	Deselect
X	H	X	X	X	L	↑	N/A	Continue Deselect
L	L	H	X	L	L	↑	External Address	Begin Burst Read Cycle
X	H	X	X	L	L	↑	Next Address	Continue Burst Read Cycle
L	L	H	X	H	L	↑	External Address	NOP/Dummy Read
X	H	X	X	H	L	↑	Next Address	Dummy Read
L	L	L	L	X	L	↑	External Address	Begin Burst Write Cycle
X	H	X	L	X	L	↑	Next Address	Continue Burst Write Cycle
L	L	L	H	X	L	↑	N/A	NOP/Write Abort
X	H	X	H	X	L	↑	Next Address	Write Abort
X	X	X	X	X	H	↑	Current Address	Ignore Clock

NOTES:

1. X means "Don't Care."
2. The rising edge of clock is symbolized by (↑)
3. A continue deselect cycle can only be entered if a deselect cycle is executed first.
4. $\overline{WRITE}$ = L means Write operation in WRITE TRUTH TABLE.
   $\overline{WRITE}$ = H means Read operation in WRITE TRUTH TABLE.
5. Operation finally depends on status of asynchronous input pins (ZZ and $\overline{OE}$).
6. $\overline{CE}$x refers to the combination of $\overline{CE1}$, CE2 and $\overline{CE2}$.

WRITE TRUTH TABLE

$\overline{WE}$	$\overline{BWa}$	$\overline{BWb}$	$\overline{BWc}$	$\overline{BWd}$	Operation
H	X	X	X	X	Read
L	L	H	H	H	Write Byte a
L	H	L	H	H	Write Byte b
L	H	H	L	H	Write Byte c
L	H	H	H	L	Write Byte d
L	L	L	L	L	Write All Bytes
L	H	H	H	H	Write Abort/NOP

NOTES:

1. X means "Don't Care."
2. All inputs in this table must meet setup and hold time around the rising edge of CLK (↑).

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{DD} Supply Relative to VSS	-0.3V to +3.6V
VIN (DQx)	-0.3V to +3.6V
VIN (Inputs)	-0.3V to +3.6V
Storage Temperature (BGA)	-55°C to +125°C
Short Circuit Output Current	100mA

* Stress greater than those listed under "Absolute Maximum Ratings: may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating condtions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS (0°C ≤ TA ≤ 70°C)

Description	Symbol	Conditions	Min	Max	Units	Notes
Input High (Logic 1) Voltage	V_{IH}		1.7	V_{DD} +0.3	V	1
Input Low (Logic 0) Voltage	V_{IL}		-0.3	0.7	V	1
Input Leakage Current	ILI	0V ≤ V_{IN} ≤ V_{DD}	-5	5	µA	2
Output Leakage Current	I_{LO}	Output(s) Disabled, 0V ≤ V_{IN} ≤ V_{DD}	-5	5	µA	
Output High Voltage	V_{OH}	I_{OH} = -1.0mA	2.0	---	V	1
Output Low Voltage	V_{OL}	I_{OL} = 1.0mA	---	0.4	V	1
Supply Voltage	V_{DD}		2.375	2.625	V	1

NOTES:

1. All voltages referenced to V_{SS} (GND)
2. ZZ pin has an internal pull-up, and input leakage = ± 10µA.

DC CHARACTERISTICS

Description	Symbol	Conditions	Typ	166 MHz	150 MHz	133 MHz	100 MHz	Units	Notes
Power Supply Current: Operating	I_{DD}	Device Selected; All Inputs ≤ V_{IL} or ≥ V_{IH}; Cycle Time = T_{CYC} MIN; V_{DD} = MAX; Output Open		650	600	560	500	mA	1, 2
Power Supply Current: Standby	I_{SB2}	Device Deselected; V_{DD} = MAX; All Inputs ≤ V_{SS} + 0.2 or VDD - 0.2; All Inputs Static; CLK Frequency = 0; ZZ ≤ VIL	30	60	60	60	60	mA	2
Power Supply Current: Current	I_{SB3}	Device Selected; All Inputs ≤ V_{IL} or ≥ V_{IH}; Cycle Time = T_{CYC} MIN; V_{DD} = MAX; Output Open; ZZ ≥ V_{DD} - 0.2V	20	40	40	40	40	mA	2
Clock Running Standby Current	I_{SB4}	Device Deselected; V_{DD} = MAX; All Inputs ≤ V_{SS} + 0.2 or V_{DD} - 0.2; Cycle Time = T_{CYC} MIN; ZZ ≤ V_{IL}		140	120	100	80	mA	2

NOTES:

1. I_{DD} is specified with no output current and increases with faster cycle times. I_{DD} increases with faster cycle times and greater output loading.
2. Typical values are measured at 2.5V, 25°C, and 10ns cycle time.

BGA CAPACITANCE

Description	Symbol	Conditions	Typ	Max	Units	Notes
Control Input Capacitance	C_I	T_A = 25°C; f = 1MHz	5	7	pF	1
Input/Output Capacitance (DQ)	C_O	T_A = 25°C; f = 1MHz	6	8	pF	1
Address Capacitance	C_A	T_A = 25°C; f = 1MHz	5	7	pF	1
Clock Capacitance	C_{CK}	T_A = 25°C; f = 1MHz	3	5	pF	1

NOTE: 1. This parameter is sampled.

AC CHARACTERISTICS

Parameter	Symbol	166MHz		150MHz		133MHz		100MHz		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Clock Time	t_{CYC}	6.0		6.7		7.5		10.0		ns
Clock Access Time	t_{CD}	--	3.5	--	3.8	--	4.2	--	5.0	ns
Output enable to Data Valid	t_{OE}	--	3.5	--	3.8	--	4.2	--	5.0	ns
Clock High to Output Low-Z	t_{LZC}	1.5	--	1.5	--	1.5	--	1.5	--	ns
Output Hold from Clock High	t_{OH}	1.5	--	1.5	--	1.5	--	1.5	--	ns
Output Enable Low to output Low-Z	t_{LZOE}	0.0	--	0.0	--	0.0	--	0.0	--	ns
Output Enable High to Output High-Z	t_{HZOE}	--	3.0	--	3.0	--	3.5	--	3.5	ns
Clock High to Output High-Z	t_{HZC}	--	3.0	--	3.0	--	3.5	--	3.5	ns
Clock High Pulse Width	t_{CH}	2.2	--	2.5	--	3.0	--	3.0	--	ns
Clock Low Pulse Width	t_{CL}	2.2	--	2.5	--	3.0	--	3.0	--	ns
Address Setup to Clock High	t_{AS}	1.5	--	1.5	--	1.5	--	1.5	--	ns
CKE Setup to Clock High	t_{CES}	1.5	--	1.5	--	1.5	--	1.5	--	ns
Data Setup to Clock High	t_{DS}	1.5	--	1.5	--	1.5	--	1.5	--	ns
Write Setup to Clock High	t_{WS}	1.5	--	1.5	--	1.5	--	1.5	--	ns
Address Advance to Clock High	t_{ADVS}	1.5		1.5		1.5		1.5		ns
Chip Select Setup to Clock High	t_{CSS}	1.5		1.5		1.5		1.5		ns
Address Hold to Clock high	t_{AH}	0.5	--	0.5	--	0.5	--	0.5	--	ns
CKE Hold to Clock High	t_{CEH}	0.5	--	0.5	--	0.5	--	0.5	--	ns
Data Hold to Clock High	t_{DH}	0.5	--	0.5	--	0.5	--	0.5	--	ns
Write Hold to Clock High	t_{WH}	0.5	--	0.5	--	0.5	--	0.5	--	ns
Address Advance to Clock High	t_{ADVH}	0.5	--	0.5	--	0.5	--	0.5	--	ns
Chip Select Hold to Clock High	t_{CSH}	0.5	--	0.5	--	0.5	--	0.5	--	ns

NOTES:

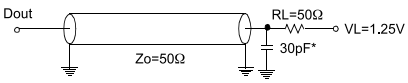
1. All Address inputs must meet the specified setup and hold times for all rising clock (CLK) edges when ADV is sampled low and $\overline{CE}$x is sampled valid. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
2. Chip enable must be valid at each rising edge of CLK (when ADV is Low) to remain enabled.
3. A write cycle is defined by $\overline{WE}$ low having been registered into the device at ADV Low.
   A Read cycle is defined by $\overline{WE}$ High with ADV Low. Both cases must meet setup and hold times.

AC TEST CONDITIONS

(TA = 0 TO 70°C, VDD = 2.5V ± 5%, UNLESS OTHERWISE SPECIFIED)

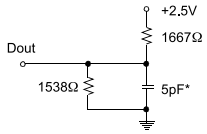
Parameter	Value
Input Pulse Level	0 to 2.5V
Input Rise and Fall Time (Measured at 20% to 80%)	1.0V/ns
Input and Output Timing Reference Levels	1.25V
Output Load	See Output Load (A)

OUTPUT LOAD (A)



OUTPUT LOAD (B)

(FOR tLZC, tLZOE, tHZOE, AND tHZC)



*Including Scope and Jig Capacitance

SNOOZE MODE

SNOOZE MODE is a low-current, "power-down" mode in which the device is deselected and current is reduced to I_{SB2Z}. The duration of SNOOZE MODE is dictated by the length of time Z is in a HIGH state. After the device enters SNOOZE MODE, all inputs except ZZ and CLK are ignored. ZZ is an asynchronous, active HIGH input that causes the device to enter SNOOZE MODE.

When ZZ becomes a logic HIGH, I_{SB2Z} is guaranteed after the setup time tZZ is met. Any READ or WRITE operation pending when the device enters SNOOZE MODE is not guaranteed to complete successfully. Therefore, SNOOZE MODE must not be initiated until valid pending operations are completed.

SNOOZE MODE

Description	Conditions	Symbol	Min	Max	Units	Notes
Current during SNOOZE MODE	ZZ ≥ VIH	I_{SB2Z}		10	mA	
ZZ active to input ignored		t_{ZZ}		2(t_{KC})	ns	1
ZZ inactive to input sampled		t_{RZZ}	2(t_{KC})		ns	1
ZZ active to snooze current		t_{ZZI}		2(t_{KC})	ns	1
ZZ inactive to exit snooze current		t_{RZZI}			ns	1

FIG. 2 SNOOZE MODE TIMING DIAGRAM

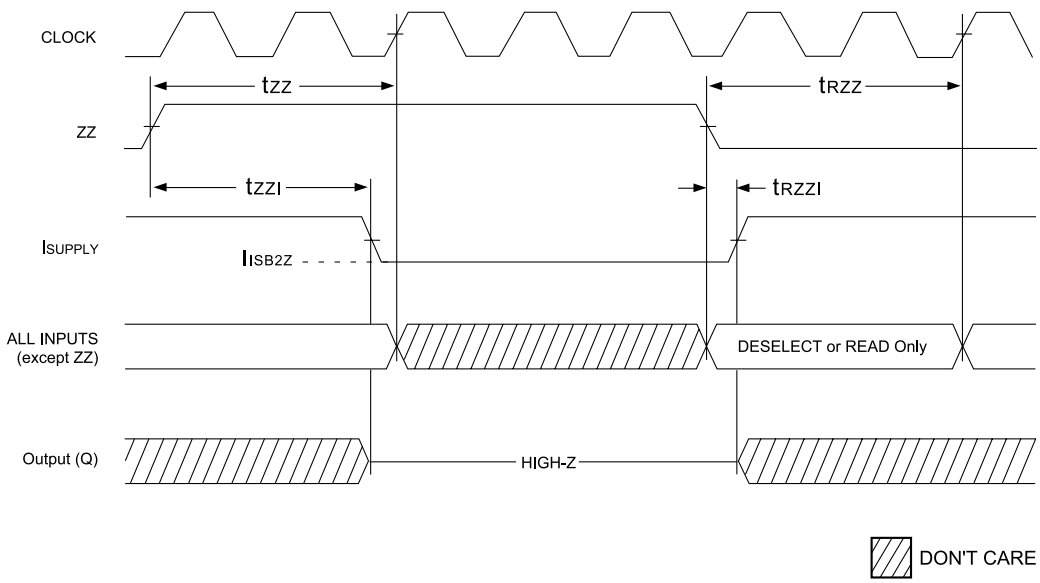
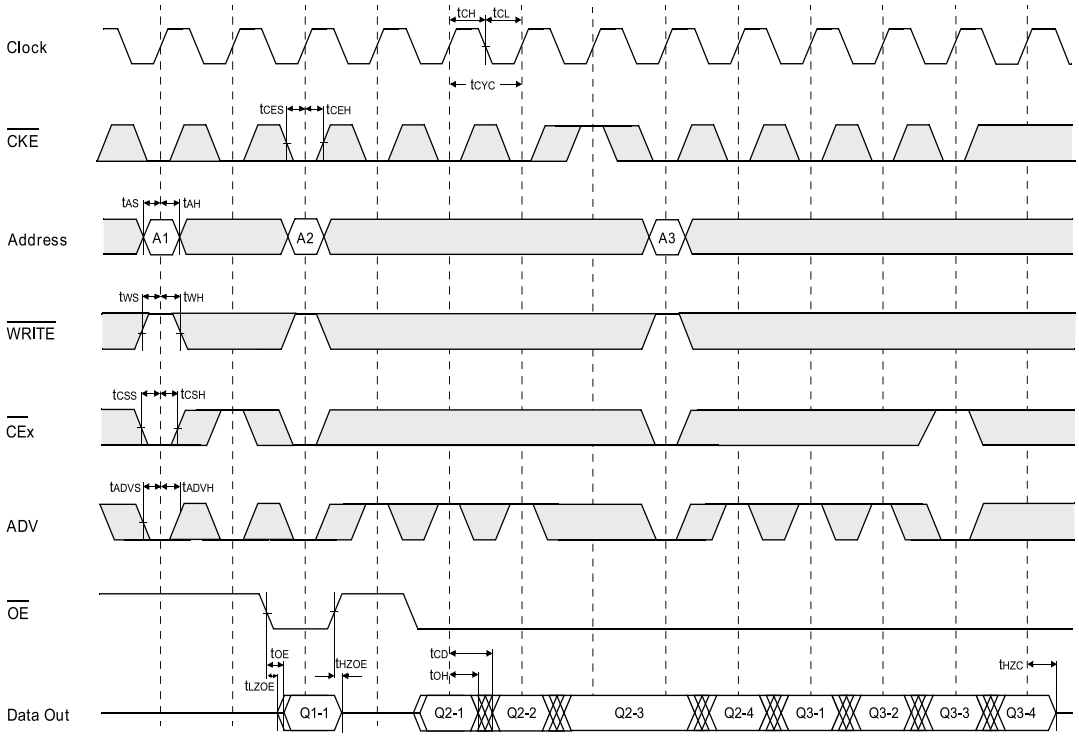
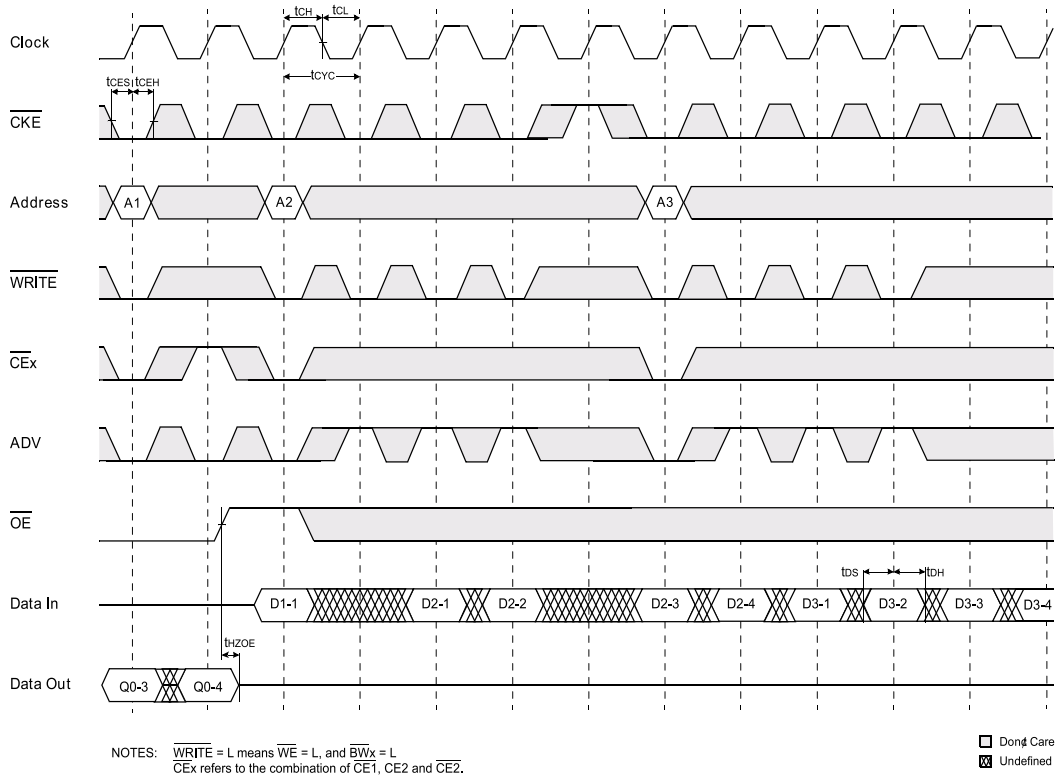


FIG. 3 TIMING WAVEFORM OF READ CYCLE



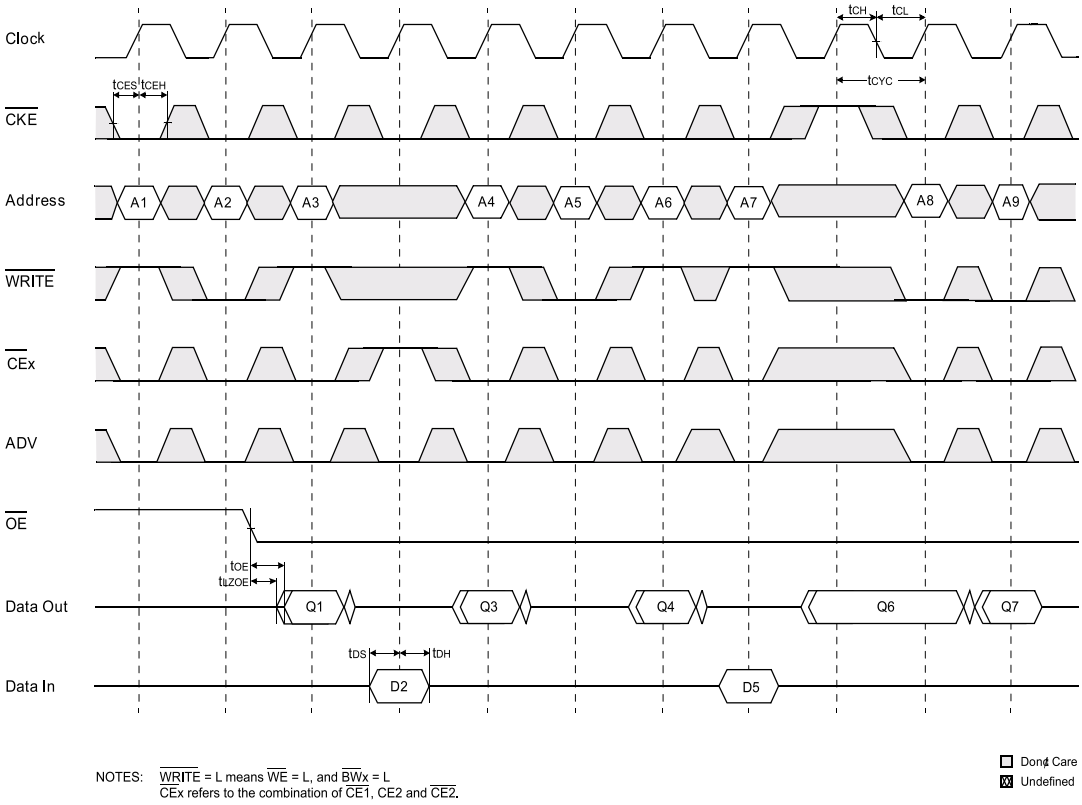
NOTES: $\overline{\text{WRITE}}$ = L means $\overline{\text{WE}}$ = L, and $\overline{\text{BW}}$x = L
CEx refers to the combination of $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ and $\overline{\text{CE2}}$.

FIG. 4 TIMING WAVEFORM OF WRITE CYCLE



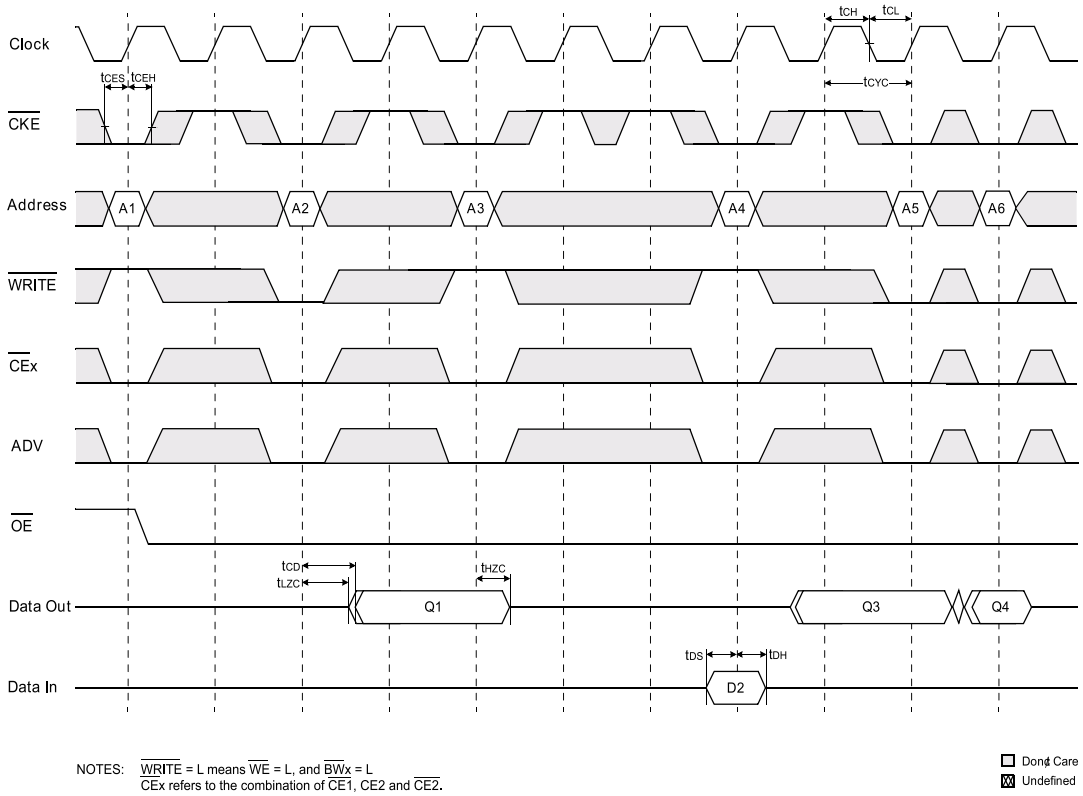
NOTES: WRITE = L means WE = L, and BWx = L
CEx refers to the combination of CE1, CE2 and CE2.

FIG. 5 TIMING WAVEFORM OF SINGLE READ/WRITE



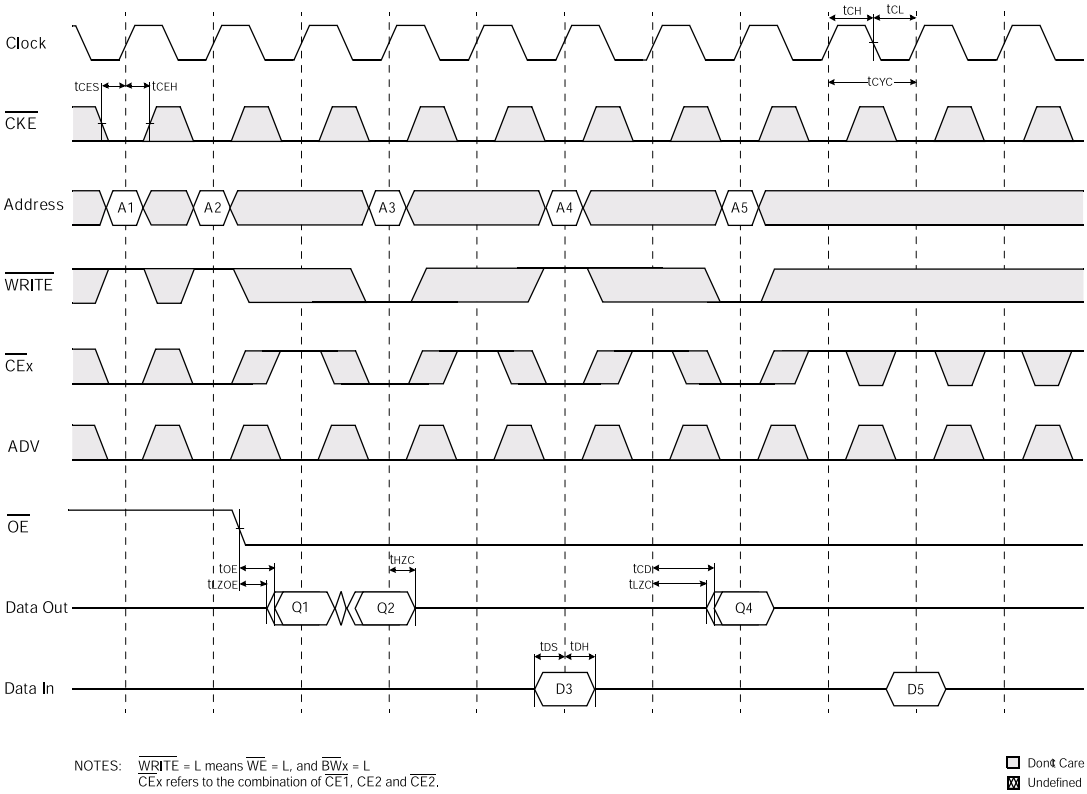
NOTES: WRITE = L means WE = L, and BWx = L
CEx refers to the combination of CE1, CE2 and CE2.

FIG. 6 TIMING WAVEFORM OF $\overline{CKE}$ OPERATION

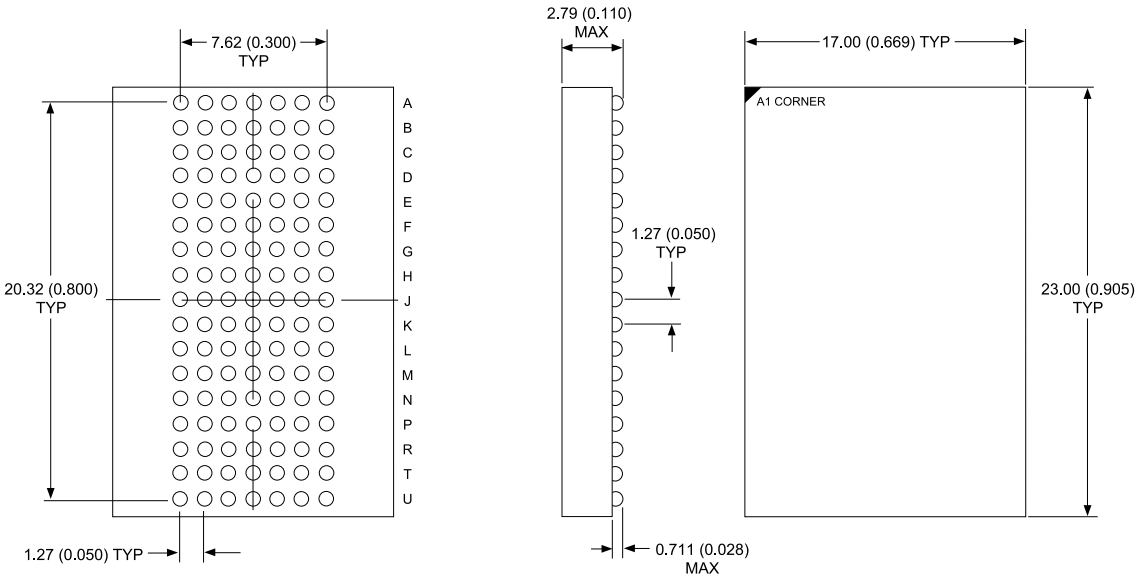


NOTES: $\overline{WRITE}$ = L means $\overline{WE}$ = L, and $\overline{BW}$x = L
CEx refers to the combination of $\overline{CE1}$, CE2 and $\overline{CE2}$.

FIG. 7 TIMING WAVEFORM OF $\overline{CE}$ OPERATION



PACKAGE DIMENSION: 119 BUMP PBGA



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE: Ball attach pad for above BGA package is 620 microns in diameter. Pad is solder mask defined.

Ordering Information

Commercial Temp Range (0°C to 70°C)

Part Number	Configuration	t_{CD} (ns)	Clock (MHz)
WED2ZL361MSJ35BC	1M x 36	3.5	166
WED2ZL361MSJ38BC	1M x 36	3.8	150
WED2ZL361MSJ42BC	1M x 36	4.2	133
WED2ZL361MSJ50BC	1M x 36	5.0	100

Industrial Temp Range (-40°C to +85°C)

Part Number	Configuration	t_{CD} (ns)	Clock (MHz)
WED2ZL361MSJ35BI*	1M x 36	3.5	166
WED2ZL361MSJ38BI	1M x 36	3.8	150
WED2ZL361MSJ42BI	1M x 36	4.2	133
WED2ZL361MSJ50BI	1M x 36	5.0	100

* consult factory for availability