512K x 64 Synchronous Pipeline Burst NBL SRAM

FEATURES

- Fast clock speed: 166, 150, 133, and 100MHz
- Fast access times: 3.5ns, 3.8ns, 4.2ns, and 5.0ns
- Fast $\overline{OE}$ access times: 3.5ns, 3.8ns, 4.2ns, and 5.0ns
- Single +2.5V ± 5% power supply (V_{DD})
- Snooze Mode for reduced-standby power
- Double Word Write Control
- Clock-controlled and registered addresses, data I/Os and control signals
- Burst control (interleaved or linear burst)
- Packaging:
  - 119-bump BGA package
- Low capacitive bus loading

DESCRIPTION

The WEDC SyncBurst - SRAM family employs high-speed, low-power CMOS designs that are fabricated using an advanced CMOS process. WEDC's 32Mb SyncBurst SRAM integrate two 512K x 32 SRAMs into a single BGA package to provide 512K x 64 configuration. All synchronous inputs pass through registers controlled by a positive-edge-triggered single-clock input (CLK). The NBL or No Bus Latency Memory utilizes all the bandwidth in any combination of operating cycles. Address, data inputs, and all control signals except output enable and linear burst order are synchronized to input clock. Burst order control must be tied "High or Low." Output Enable controls the outputs at any given time and to Asynchronous Input. Write cycles are internally self-timed and initiated by the rising edge of the clock input. This feature eliminates complex off-chip write pulse generation and provides increased timing flexibility for incoming signals.

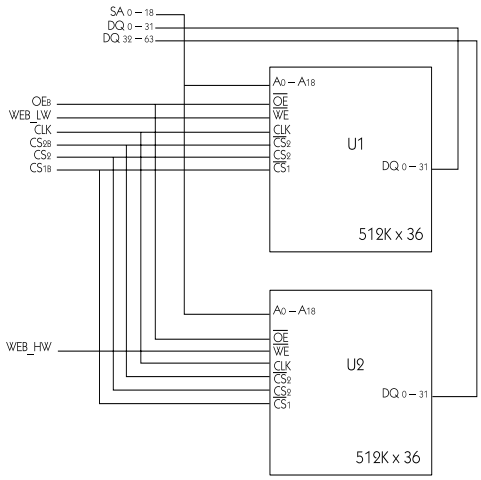
NOTE: NBL = No Bus Latency is equivalent to the industry ZBT™ devices.

FIG. 1 PIN CONFIGURATION

(TOP VIEW)

	1	2	3	4	5	6	7	8	9
A	DQ_F	DQ_F	DQ_F	DQ_F	NC	DQ_G	DQ_G	DQ_G	DQ_G
B	DQ_F	DQ_F	DQ_F	DQ_F	NC	DQ_G	DQ_G	DQ_G	DQ_G
C	DQ_E	DQ_E	DQ_E	DQ_E	NC	DQ_H	DQ_H	DQ_H	DQ_H
D	DQ_E	DQ_E	DQ_E	DQ_E	NC	DQ_H	DQ_H	DQ_H	DQ_H
E	NC	NC	NC	V_{CC}	V_{CC}	V_{CC}	NC	NC	NC
F	SA	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	SA
G	SA	$\overline{CE}$	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	SA	SA
H	SA	NC	V_{SS}	$\overline{WE_1}$	V_{SS}	V_{SS}	V_{SS}	SA	SA
J	SA_{18}	$\overline{CE_2}$	SS_{CLK}	$\overline{OE}$	NC	NC	NC	SA_1	SA_0
K	SA	CE_2	V_{SS}	$\overline{WE_0}$	V_{SS}	V_{SS}	V_{SS}	SA	SA
L	SA	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	SA	SA
M	SA	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	SA
N	NC	NC	NC	V_{CC}	V_{CC}	V_{CC}	NC	NC	NC
P	DQ_D	DQ_D	DQ_D	DQ_D	NC	DQ_A	DQ_A	DQ_A	DQ_A
R	DQ_D	DQ_D	DQ_D	DQ_D	NC	DQ_A	DQ_A	DQ_A	DQ_A
T	DQ_C	DQ_C	DQ_C	DQ_C	NC	DQ_B	DQ_B	DQ_B	DQ_B
U	DQ_C	DQ_C	DQ_C	DQ_C	NC	DQ_B	DQ_B	DQ_B	DQ_B

BLOCK DIAGRAM



FUNCTION DESCRIPTION

The WED2ZL64512S is an NBL SSRAM designed to sustain 100% bus bandwidth by eliminating turnaround cycle when there is transition from Read to Write, or vice versa. All inputs (with the exception of $\overline{OE}$) are synchronized to rising clock edges.

All read, write and deselect cycles are initiated by the ADV input. Subsequent burst addresses can be internally generated by the burst advance pin (ADV). ADV should be driven to Low once the device has been deselected in order to load a new address for next operation.

Output Enable ($\overline{OE}$) can be used to disable the output at any given time. Read operation is initiated when at the rising edge of the clock, the address presented to the address inputs are latched in the address register, $\overline{CKE}$ is driven low, the write enable input signals $\overline{WE}$ are driven high, and ADV driven low. The internal array is read between the first rising edge and the second rising edge of the clock and the data is latched in the output register. At the second clock edge the data is driven out of the SRAM. During read operation $\overline{OE}$ must be driven low for the device to drive out the requested data.

Write operation occurs when $\overline{WE}$ is driven low at the rising edge of the clock. The pipe-lined NBL SSRAM uses a late-late write cycle to utilize 100% of the bandwidth. At the first rising edge of the clock, $\overline{WE}$ and address are registered, and the data associated with that address is required two cycle later.

Subsequent addresses are generated by ADV High for the burst access as shown below. The starting point of the burst seguence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is linear.

BURST SEQUENCE TABLE; LINEAR

		Case 1		Case 2		Case 3		Case 4	
$\overline{LBO}$ Pin	High	A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
		0	1	1	0	1	1	0	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	0	0	0	1	1	0

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

$\overline{CEx}$	ADV	$\overline{WE}$	$\overline{OE}$	CLK	Address Accessed	Operation
H	L	X	X	↑	N/A	Deselect
X	H	X	X	↑	N/A	Continue Deselect
L	L	H	L	↑	External Address	Begin Burst Read Cycle
X	H	X	L	↑	Next Address	Continue Burst Read Cycle
L	L	H	H	↑	External Address	NOP/Dummy Read
X	H	X	H	↑	Next Address	Dummy Read
L	L	L	X	↑	External Address	Begin Burst Write Cycle
X	H	X	X	↑	Next Address	Continue Burst Write Cycle
L	L	L	X	↑	N/A	NOP/Write Abort
X	H	X	X	↑	Next Address	Write Abort
X	X	X	X	↑	Current Address	Ignore Clock

NOTES:

1. *X means "Don't Care."*
2. *The rising edge of clock is symbolized by (↑)*
3. *A continue deselect cycle can only be entered if a deselect cycle is executed first.*
4. *$\overline{WRITE}$ = L means Write operation in WRITE TRUTH TABLE.*
   $\overline{WRITE}$ = H means Read operation in WRITE TRUTH TABLE.

ABSOLUTE MAXIMUM RATINGS*

VOLTAGE ON VDD SUPPLY RELATIVE TO VSS	-0.3V TO +3.6V
VIN (DQX)	-0.3V TO +3.6V
VIN (INPUTS)	-0.3V TO +3.6V
STORAGE TEMPERATURE (BGA)	-55°C TO +125°C
SHORT CIRCUIT OUTPUT CURRENT	100mA

*Stress greater than those listed under "Absolute Maximum Ratings: may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating condtions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 70°C$)

DESCRIPTION	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
INPUT HIGH (LOGIC 1) VOLTAGE	VIH		1.7	VDD +0.3	V	1
INPUT LOW (LOGIC 0) VOLTAGE	VIL		-0.3	0.7	V	1
INPUT LEAKAGE CURRENT	ILI	0V - VIN - VDD	-5	5	µA	2
OUTPUT LEAKAGE CURRENT	ILO	OUTPUT(S) DISABLED, 0V - VIN - VDD	-5	5	µA	
OUTPUT HIGH VOLTAGE	VOH	IOH = -1.0mA	2.0	---	V	1
OUTPUT LOW VOLTAGE	VOL	IOL = 1.0mA	---	0.4	V	1
SUPPLY VOLTAGE	VDD		2.375	2.625	V	1

NOTES:
1. *All voltages referenced to Vss (GND)*
2. *ZZ pin has an internal pull-up, and input leakage = ± 10µA.*

DC CHARACTERISTICS

DESCRIPTION	SYMBOL	CONDITIONS	TYP	166 MHZ	150 MHZ	133 MHZ	100 MHZ	UNITS	NOTES
POWER SUPPLY CURRENT: OPERATING	IDD	DEVICE SELECTED; ALL INPUTS ≤ VIL OR ≥ VIH; CYCLE TIME = TCYC MIN; VDD = MAX; OUTPUT OPEN		650	600	560	500	mA	1, 2
POWER SUPPLY CURRENT: STANDBY	ISB2	DEVICE DESELECTED; VDD = MAX; ALL INPUTS ≤ VSS + 0.2 OR VDD - 0.2; ALL INPUTS STATIC; CLK FREQUENCY = 0; ZZ ≥ VIL	30	60	60	60	60	mA	2
POWER SUPPLY CURRENT: CURRENT	ISB3	DEVICE SELECTED; ALL INPUTS ≤ VIL OR ≥ VIH; CYCLE TIME = TCYC MIN; VDD = MAX; OUTPUT OPEN; ZZ ≥ VDD - 0.2V	20	40	40	40	40	mA	2
CLOCK RUNNING STANDBY CURRENT	ISB4	DEVICE DESELECTED; VDD = MAX; ALL INPUTS ≤ VSS + 0.2 OR VDD - 0.2; CYCLE TIME = TCYC MIN; ZZ ≤ VIL		140	120	100	80	mA	2

NOTES:
1. *IDD is specified with no output current and increases with faster cycle times. IDD increases with faster cycle times and greater output loading.*
2. *Typical values are measured at 2.5V, 25°C, and 10ns cycle time.*

BGA CAPACITANCE

DESCRIPTION	SYMBOL	CONDITIONS	TYP	MAX	UNITS	NOTES
CONTROL INPUT CAPACITANCE	CL	TA = 25°C; f = 1MHz	5	7	pF	1
INPUT/OUTPUT CAPACITANCE (DQ)	CO	TA = 25°C; f = 1MHz	6	8	pF	1
ADDRESS CAPACITANCE	CA	TA = 25°C; f = 1MHz	5	7	pF	1
CLOCK CAPACITANCE	CCK	TA = 25°C; f = 1MHz	3	5	pF	1

NOTES:
1. *This parameter is sampled.*

AC CHARACTERISTICS

PARAMETER	SYMBOL	166MHz		150MHz		133MHz		100MHz		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
CLOCK TIME	t_{CYC}	6.0		6.7		7.5		10.0		ns
CLOCK ACCESS TIME	t_{CD}	--	3.5	--	3.8	--	4.2	--	5.0	ns
OUTPUT ENABLE TO DATA VALID	t_{OE}	--	3.5	--	3.8	--	4.2	--	5.0	ns
CLOCK HIGH TO OUTPUT LOW-Z	t_{LZC}	1.5	--	1.5	--	1.5	--	1.5	--	ns
OUTPUT HOLD FROM CLOCK HIGH	t_{OH}	1.5	--	1.5	--	1.5	--	1.5	--	ns
OUTPUT ENABLE LOW TO OUTPUT LOW-Z	t_{LZOE}	0.0	--	0.0	--	0.0	--	0.0	--	ns
OUTPUT ENABLE HIGH TO OUTPUT HIGH-Z	t_{HZOE}	--	3.0	--	3.0	--	3.5	--	3.5	ns
CLOCK HIGH TO OUTPUT HIGH-Z	t_{HZC}	--	3.0	--	3.0	--	3.5	--	3.5	ns
CLOCK HIGH PULSE WIDTH	t_{CH}	2.2	--	2.5	--	3.0	--	3.0	--	ns
CLOCK LOW PULSE WIDTH	t_{CL}	2.2	--	2.5	--	3.0	--	3.0	--	ns
ADDRESS SETUP TO CLOCK HIGH	t_{AS}	1.5	--	1.5	--	1.5	--	1.5	--	ns
CKE SETUP TO CLOCK HIGH	t_{CES}	1.5	--	1.5	--	1.5	--	1.5	--	ns
DATA SETUP TO CLOCK HIGH	t_{DS}	1.5	--	1.5	--	1.5	--	1.5	--	ns
WRITE SETUP TO CLOCK HIGH	t_{WS}	1.5	--	1.5	--	1.5	--	1.5	--	ns
ADDRESS ADVANCE TO CLOCK HIGH	t_{ADVS}	1.5		1.5		1.5		1.5		ns
CHIP SELECT SETUP TO CLOCK HIGH	t_{CSS}	1.5		1.5		1.5		1.5		ns
ADDRESS HOLD TO CLOCK HIGH	t_{AH}	0.5	--	0.5	--	0.5	--	0.5	--	ns
CKE HOLD TO CLOCK HIGH	t_{CEH}	0.5	--	0.5	--	0.5	--	0.5	--	ns
DATA HOLD TO CLOCK HIGH	t_{DH}	0.5	--	0.5	--	0.5	--	0.5	--	ns
WRITE HOLD TO CLOCK HIGH	t_{WH}	0.5	--	0.5	--	0.5	--	0.5	--	ns
ADDRESS ADVANCE TO CLOCK HIGH	t_{ADVH}	0.5	--	0.5	--	0.5	--	0.5	--	ns
CHIP SELECT HOLD TO CLOCK HIGH	t_{CSH}	0.5	--	0.5	--	0.5	--	0.5	--	ns

NOTES:

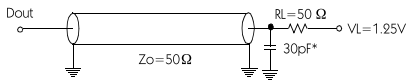
1. *All Address inputs must meet the specified setup and hold times for all rising clock (CLK) edges when ADV is sampled low and $\overline{CE}$x is sampled valid. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.*
2. *Chip enable must be valid at each rising edge of CLK (when ADV is Low) to remain enabled.*
3. *A write cycle is defined by $\overline{WE}$ low having been registered into the device at ADV Low. A Read cycle is defined by $\overline{WE}$ High with ADV Low. Both cases must meet setup and hold times.*

AC TEST CONDITIONS

(T_A = 0 TO 70°C, V_{DD} = 2.5V ± 5%, UNLESS OTHERWISE SPECIFIED)

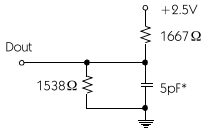
Parameter	Value
Input Pulse Level	0 to 2.5V
Input Rise and Fall Time (Measured at 20% to 80%)	1.0V/ns
Input and Output Timing Reference Levels	1.25V
Output Load	See Output Load (A)

OUTPUT LOAD (A)



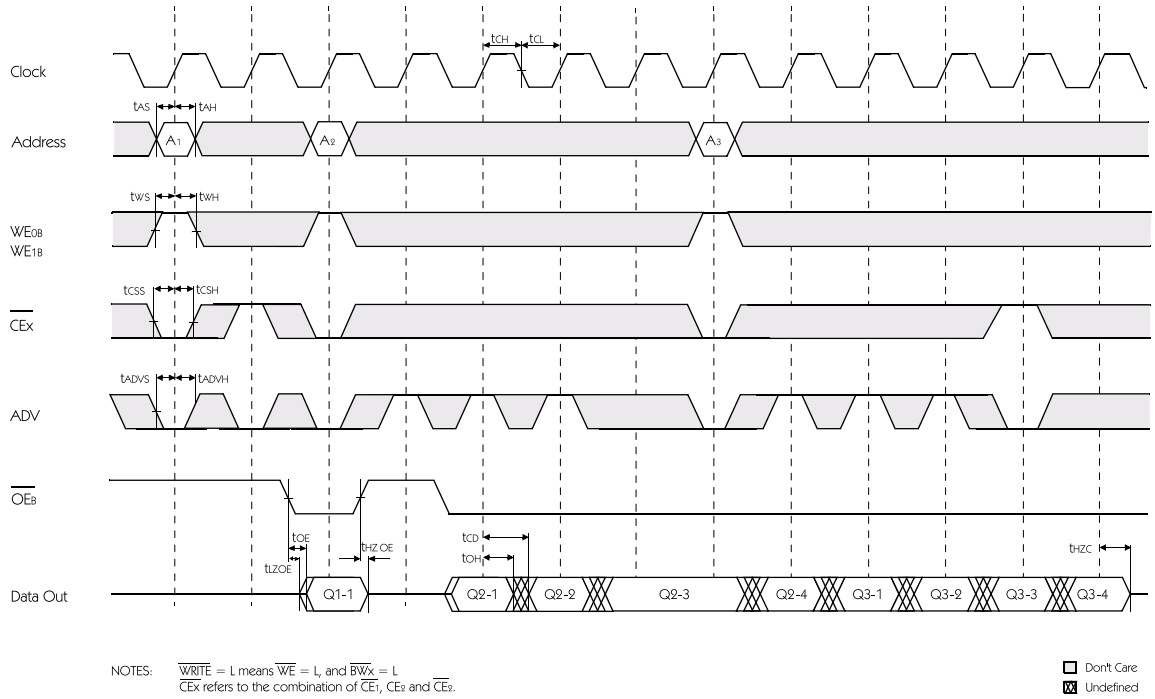
OUTPUT LOAD (B)

(FOR t_{LZC}, t_{LZOE}, t_{HZOE}, AND t_{HZC})



**Including Scope and Jig Capacitance*

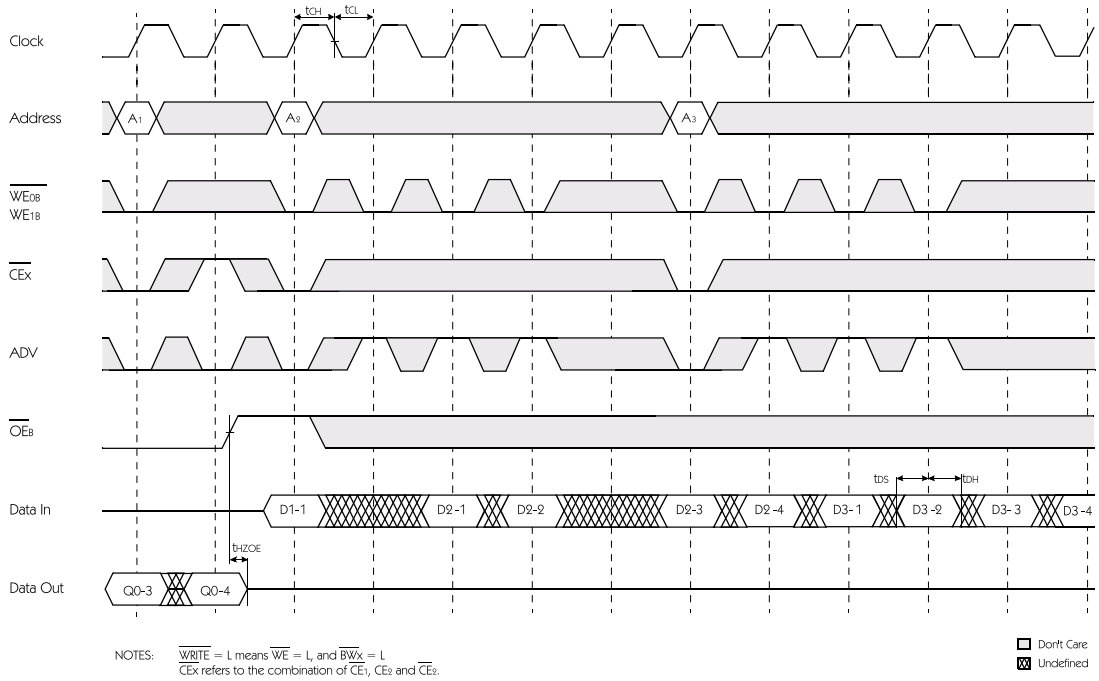
FIG. 3 TIMING WAVEFORM OF READ CYCLE



NOTES: $\overline{WRITE}$ = L means $\overline{WE}$ = L, and $\overline{BWx}$ = L
$\overline{CEx}$ refers to the combination of $\overline{CE_1}$, CE_2 and $\overline{CE_2}$.

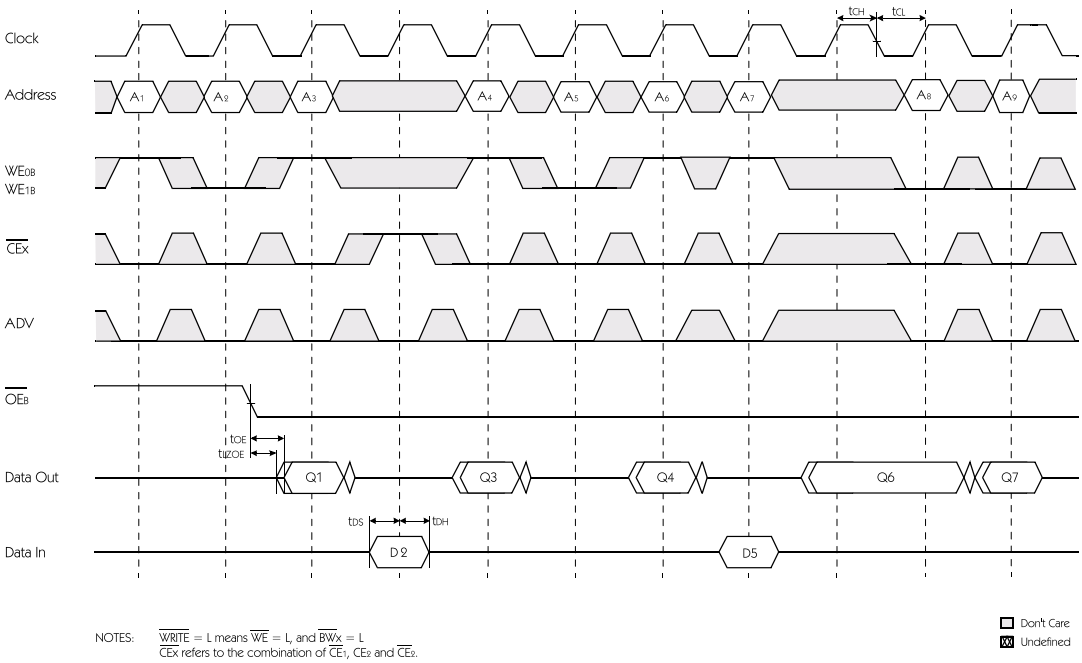
Don't Care
Undefined

FIG. 4 TIMING WAVEFORM OF WRITE CYCLE



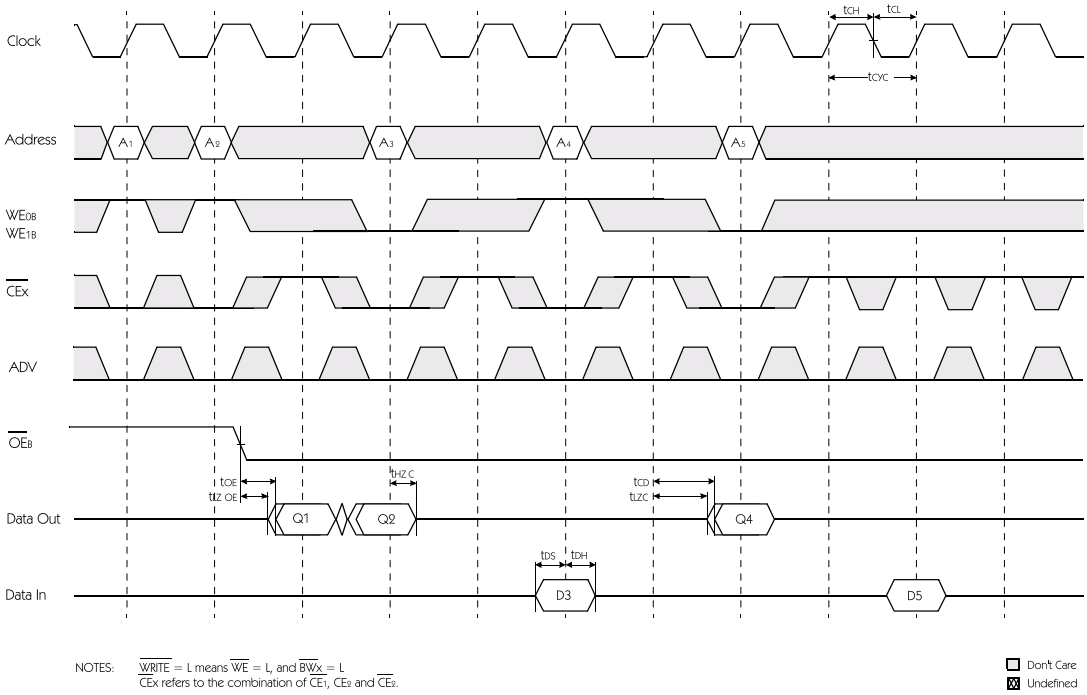
NOTES: $\overline{WRITE}$ = L means $\overline{WE}$ = L, and $\overline{BWx}$ = L
$\overline{CEx}$ refers to the combination of $\overline{CE_1}$, CE_2 and $\overline{CE_2}$.

FIG. 5 TIMING WAVEFORM OF SINGLE READ/WRITE

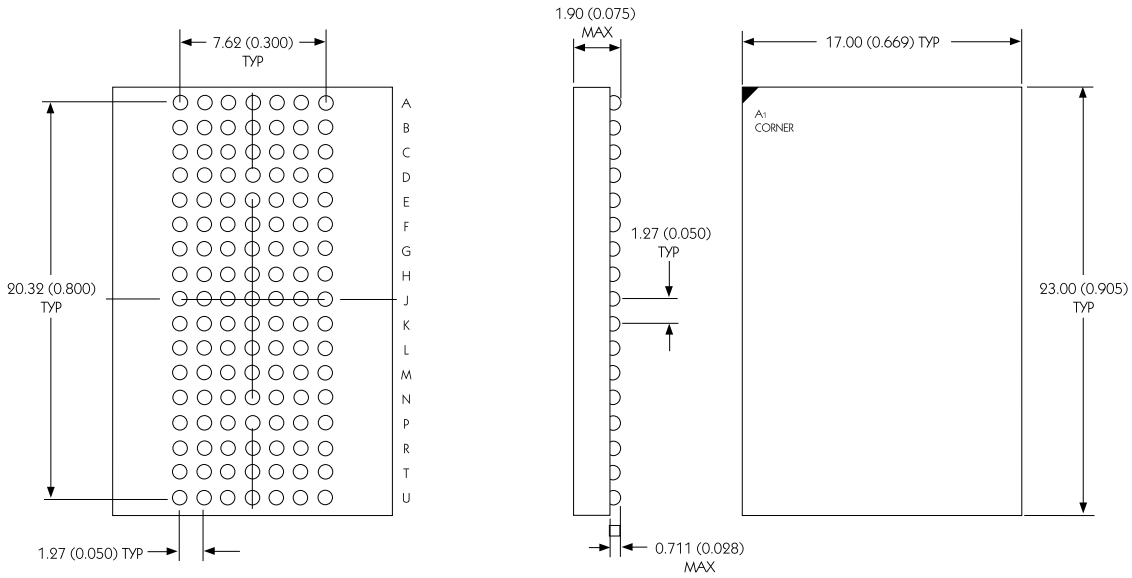


NOTES: $\overline{WRITE}$ = L means $\overline{WE}$ = L, and $\overline{BWx}$ = L
$\overline{CEx}$ refers to the combination of $\overline{CE_1}$, CE_2 and $\overline{CE_2}$.

FIG. 7 TIMING WAVEFORM OF $\overline{CE}$ OPERATION



PACKAGE DIMENSION: 119 BUMP PBGA



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE: Ball attach pad for above BGA package is 620 microns in diameter. Pad is solder mask defined.

ORDERING INFORMATION

COMMERCIAL TEMP RANGE (0°C TO 70°C)

Part Number	Configuration	t_{CD} (ns)	Clock (MHz)
WED2ZL64512S35BC	512K x 64	3.5	166
WED2ZL64512S38BC	512K x 64	3.8	150
WED2ZL64512S42BC	512K x 64	4.2	133
WED2ZL64512S50BC	512K x 64	5.0	100