512K x 72 Synchronous Pipeline Burst ZBL SRAM *Preliminary

FEATURES

- Fast clock speed: 150, 133, and 100MHz
- Fast access times: 3.8ns, 4.2ns, and 5.0ns
- Fast $\overline{OE}$ access times: 3.8ns, 4.2ns, and 5.0ns
- High performance 3-1-1-1 access rate
- 2.5V ± 5% power supply
- Common data inputs and data outputs
- Byte write enable and global write control
- Six chip enables for depth expansion and address pipeline
- Internally self-timed write cycle
- Burst control pin (interleaved or linear burst sequence)
- Automatic power-down for portable applications
- Commercial, industrial and military temperature ranges
- Packaging:
  - 152 PBGA package 17 x 23mm

BENEFITS

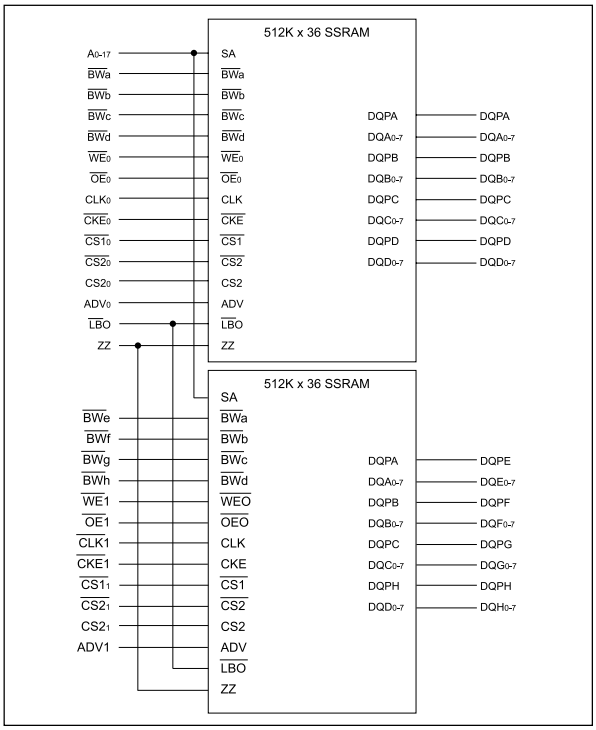
- 30% space savings compared to equivalent TQFP solution
- Reduced part count
- 24% I/O reduction
- Laminate interposer for optimum TCE match
- Low Profile
- Reduce layer count for board routing
- Suitable for hi-reliability applications
- User configurable as 1M x 36 or 2M x 18
- Upgradable to 1M x 72 (contact factory for availability)

DESCRIPTION

The WEDC SyncBurst - SRAM employs high-speed, low-power CMOS design that is fabricated using an advanced CMOS process. WEDC's 32Mb SyncBurst SRAMs integrate two 512K x 36 SSRAMs into a single BGA package to provide 512K x 72 configuration. All synchronous inputs pass through registers controlled by a positive-edge-triggered single-clock input (CLK). The ZBL or Zero Bus Latency Memory utilizes all the bandwidth in any combination of operating cycles. Address, data inputs, and all control signals except output enable and linear burst order are synchronized to input clock. Burst order control must be tied "High or Low." Asynchronous inputs include the sleep mode enable (ZZ). Output Enable controls the outputs at any given time. Write cycles are internally self-timed and initiated by the rising edge of the clock input. This feature eliminates complex off-chip write pulse generation and provides increased timing flexibility for incoming signals.

**Preliminary product that is not fully characterized, non-qualified and is subject to change without notice.*

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

(TOP VIEW)

	1	2	3	4	5	6	7	8	9
A	-	ADV_0	$\overline{OE}0$	DQB2	DQB4	DQB6	DNU	DQA6	DQA2
B	$\overline{CKE}0$	$\overline{WE}0$	DQB7	DQB5	DQB3	DQB0	DQA7	DQA3	DQA1
C	CLK0	$\overline{CS2}_0$	DQC2	DQPC	DQPB	DQB1	DQD7	DQA4	DQA0
D	$\overline{BW}a$	$\overline{BW}b$	DQC3	VSS	VSS	VSS	DQD6	DQA5	DQPA
E	$\overline{BW}c$	$\overline{BW}d$	DQC4	VDDQ	VDDQ	VDDQ	DQD5	DQPD	ZZ
F	$\overline{CS1}_0$	$CS2_0$	DQC5	VDDQ	VDDQ	VSS	DQD4	DNU	A0
G	A7	DQC0	DQC7	VSS	VDD	VDD	DQD3	A1	A3
H	A18	DQC1	DQC6	VDD	VDD	VDD`	DQD2	A2	A5
J	A9	A6	DQF2	VSS	VSS	VSS	DQD1	A4	A16
K	A8	DQF4	FQF3	VDD	VDD	VDD	DQD0	A14	A15
L	A17	DQF5	DQF6	VDD	VDD	VSS	DQE6	A12	A13
M	ADV1	$\overline{OE}1$	DQF7	VSS	VDDQ	VDDQ	DQE7	A10	A11
N	$\overline{CKE}1$	$\overline{WE}1$	DQPF	VDDQ	VDDQ	VDDQ	DQE5	DQE3	$\overline{LBO}$
P	CLK1	$\overline{CS2}_1$	DQF1	VSS	VSS	VSS	DQE4	DQE2	DQE0
R	$\overline{BW}e$	$\overline{BW}f$	DQF0	DQG1	DQG4	DQH1	DQH2	DQE1	DQPE
T	$\overline{BW}g$	$\overline{BW}h$	DQG0	DQG2	DQG5	DQH0	DQH4	DQH7	DQPH
U	$\overline{CS1}_1$	$CS2_1$	DQG3	DQPG	DQG6	DQG7	DQH3	DQH5	DQH6

NOTE: DNU means Do Not Use and are reserved for future use.

FUNCTION DESCRIPTION

The WEDPZ512K72S-XBX is an ZBL SSRAM designed to sustain 100% bus bandwidth by eliminating turnaround cycle when there is transition from Read to Write, or vice versa. All inputs (with the exception of $\overline{OE}$, LBO and ZZ) are synchronized to rising clock edges.

All read, write and deselect cycles are initiated by the ADV input. Subsequent burst addresses can be internally generated by the burst advance pin (ADV). ADV should be driven to Low once the device has been deselected in order to load a new address for next operation.

Clock Enable ($\overline{CKE}$) pin allows the operation of the chip to be suspended as long as necessary. When CKE is high, all synchronous inputs are ignored and the internal device registers will hold their previous values. NBL SSRAM latches external address and initiates a cycle when CKE and ADV are driven low at the rising edge of the clock.

Output Enable ($\overline{OE}$) can be used to disable the output at any given time. Read operation is initiated when at the rising edge of the clock, the address presented to the address inputs are latched in the address register, $\overline{CKE}$ is driven low, the write enable input signals $\overline{WE}$ are driven high, and ADV driven low. The internal array is read between the first rising edge and the second rising edge of the clock and the data is latched in the output register. At the second clock edge the data is driven out of the SRAM. During read operation $\overline{OE}$ must be driven low for the device to drive out the requested data.

Write operation occurs when $\overline{WE}$ is driven low at the rising edge of the clock. BW[h:a] can be used for byte write operation. The pipe-lined ZBL SSRAM uses a late-late write cycle to utilize 100% of the bandwidth. At the first rising edge of the clock, $\overline{WE}$ and address are registered, and the data associated with that address is required two cycles later.

Subsequent addresses are generated by ADV High for the burst access as shown below. The starting point of the burst seguence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the LBO pin. When this pin is low, linear burst sequence is selected. And when this pin is high, Interleaved burst sequence is selected.

During normal operation, ZZ must be driven low. When ZZ is driven high, the SRAM will enter a Power Sleep Mode after two cycles. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM operates after two cycles of wake up time.

BURST SEQUENCE TABLE

(Interleaved Burst, $\overline{LBO}$ = High)

$\overline{LBO}$ Pin	High	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
		0	1	0	0	1	1	1	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	1	0	0	1	0	0

(Linear Burst, $\overline{LBO}$ = Low)

$\overline{LBO}$ Pin	High	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
		0	1	1	0	1	1	0	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	0	0	0	1	1	0

NOTE 1: LBO pin must be tied to High or Low, and Floating State must not be allowed.

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

$\overline{CEx}$	ADV	$\overline{WE}$	$\overline{BWx}$	$\overline{OE}$	$\overline{CKE}$	CLK	Address Accessed	Operation
H	L	X	X	X	L	↑	N/A	Deselect
X	H	X	X	X	L	↑	N/A	Continue Deselect
L	L	H	X	L	L	↑	External Address	Begin Burst Read Cycle
X	H	X	X	L	L	↑	Next Address	Continue Burst Read Cycle
L	L	H	X	H	L	↑	External Address	NOP/Dummy Read
X	H	X	X	H	L	↑	Next Address	Dummy Read
L	L	L	L	X	L	↑	External Address	Begin Burst Write Cycle
X	H	X	L	X	L	↑	Next Address	Continue Burst Write Cycle
L	L	L	H	X	L	↑	N/A	NOP/Write Abort
X	H	X	H	X	L	↑	Next Address	Write Abort
X	X	X	X	X	H	↑	Current Address	Ignore Clock

NOTES: 1. X means "Don't Care."
2. The rising edge of clock is symbolized by (↑).
3. A continue deselect cycle can only be entered if a deselect cycle is executed first.
4. $\overline{WRITE}$ = L means Write operation in WRITE TRUTH TABLE.
$\overline{WRITE}$ = H means Read operation in WRITE TRUTH TABLE.
5. Operation finally depends on status of asynchronous input pins (ZZ and $\overline{OE}$).
6. $\overline{CEx}$ refers to the combination of $\overline{CS1}$, CS2 and $\overline{CS2}$.

WRITE TRUTH TABLE

$\overline{WE}$	$\overline{BWa}$	$\overline{BWb}$	$\overline{BWc}$	$\overline{BWd}$	Operation
H	X	X	X	X	Read
L	L	H	H	H	Write Byte a
L	H	L	H	H	Write Byte b
L	H	H	L	H	Write Byte c
L	H	H	H	L	Write Byte d
L	L	L	L	L	Write All Bytes
L	H	H	H	H	Write Abort/NOP

NOTES: 1. X means "Don't Care."
2. All inputs in this table must meet setup and hold time around the rising edge of CLK (↑).
3. Replace $\overline{BWa}$ with $\overline{BWe}$, $\overline{BWb}$, with $\overline{BWf}$, $\overline{BWc}$ with $\overline{BWg}$ and $\overline{BWd}$ with $\overline{BWh}$ for operation of IC2.

ABSOLUTE MAXIMUM RATINGS*

VIN Voltage or any other pin relative hovss	-0.3V to +3.6V
Voltage on V_{DD} Supply Relative to V_{SS}	-0.3V to +3.6V
Storage Temperature (BGA)	-55°C to +150°C

**Stress greater than those listed under "Absolute Maximum Ratings: may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating condtions for extended periods may affect reliability.*

ELECTRICAL CHARACTERISTICS

(-55°C - TA - +125°C)

Description	Symbol	Conditions	Min	Max	Units	Notes
Input High (Logic 1) Voltage	V_{IH}		1.7	V_{DD} +0.3	V	1
Input Low (Logic 0) Voltage	V_{IL}		-0.3	0.7	V	1
Input Leakage Current	I_{IL}	V_{DD} = Max, 0V - V_{IN} - V_{DD}	-4	+4	µA	2
Output Leakage Current	I_{LO}	Output(s) Disabled, Vout = Vss to V_{DDQ}	-2	+2	µA	
Output High Voltage	V_{OH}	I_{OH} = -1.0mA	2.0	---	V	1
Output Low Voltage	V_{OL}	I_{OL} = 1.0mA	---	0.4	V	1
Supply Voltage	V_{DD}		2.375	2.625	V	1
I/O Power Suply	V_{DDQ}		2.375	2.625	V	1

NOTES: 1. All voltages referenced to VSS (GND)
2. ZZ pin has an internal pull-up, and input leakage = ± 20 µA.

DC CHARACTERISTICS

(-55°C - TA - + 125°C)

Description	Symbol	Conditions	150 MHz (Max)	133 MHz (Max)	100 MHz (Max)	Units	Notes
Power Supply Current: Operating	I_{DD}	Device Selected; All Inputs ≤ V_{IL} or ≥ V_{IH}; Cycle Time ≥ T_{CYC} MIN; V_{DD} = MAX; Output Open	640	600	560	mA	1
Power Supply Current: Standby	I_{SB2}	Device Deselected; V_{DD} = MAX; All Inputs ≤ V_{IL} or ≥ V_{IH} All Inputs Static; CLK Frequency = MAX Output Open, zz ≥ V_{DD} - 0.2V	60	60	60	mA	
Clock Running Standby Current	I_{SB}	Device Deselected; V_{DD} = MAX; All Inputs ≤ V_{SS} + 0.2 or V_{DD} - 0.2; f = max ; ZZ ≤ V_{IL}	140	120	100	mA	

NOTES: 1. I_{DD} is specified with no output current and increases with faster cycle times.
I_{DD} increases with faster cycle times and greater output loading.

BGA CAPACITANCE

(T_A = + 25C)

Description	Symbol	Conditions	Max	Units	Notes
Control Input Capacitance	C_I	T_A = 25°C; f = 1MHz	10	pF	1
Input/Output Capacitance (DQ)	C_O	T_A = 25°C; f = 1MHz	10	pF	1
Address Capacitance	C_A	T_A = 25°C; f = 1MHz	20	pF	1
Clock Capacitance	C_{CK}	T_A = 25°C; f = 1MHz	7	pF	1

NOTES: 1. This parameter is not tested but guaranteed by design.

AC CHARACTERISTICS

(-55°C - TA - +125°C)

Parameter	Symbol	150MHz		133MHz		100MHz		Units
		Min	Max	Min	Max	Min	Max	
Clock Time	t_{CYC}	6.7		7.5		10.0		ns
Clock Access Time	t_{CD}	--	3.8	--	4.2	--	5.0	ns
Output enable to Data Valid	t_{OE}	--	3.8	--	4.2	--	5.0	ns
Clock High to Output Low-Z	t_{LZC}	1.5	--	1.5	--	1.5	--	ns
Output Hold from Clock High	t_{OH}	1.5	--	1.5	--	1.5	--	ns
Output Enable Low to output Low-Z	t_{LZOE}	0.0	--	0.0	--	0.0	--	ns
Output Enable High to Output High-Z	t_{HZOE}	--	3.0	--	3.5	--	3.5	ns
Clock High to Output High-Z	t_{HZC}	--	3.0	--	3.5	--	3.5	ns
Clock High Pulse Width	t_{CH}	2.5	--	2.5	--	3.0	--	ns
Clock Low Pulse Width	t_{CL}	2.5	--	2.5	--	3.0	--	ns
Address Setup to Clock High	t_{AS}	1.5	--	1.5	--	1.5	--	ns
CKE Setup to Clock High	t_{CES}	1.5	--	1.5	--	1.5	--	ns
Data Setup to Clock High	t_{DS}	1.5	--	1.5	--	1.5	--	ns
Write Setup to Clock High	t_{WS}	1.5	--	1.5	--	1.5	--	ns
Address Advance to Clock High	t_{ADVS}	1.5		1.5		1.5		ns
Chip Select Setup to Clock High	t_{CSS}	1.5		1.5		1.5		ns
Address Hold to Clock high	t_{AH}	0.5	--	0.5	--	0.5	--	ns
CKE Hold to Clock High	t_{CEH}	0.5	--	0.5	--	0.5	--	ns
Data Hold to Clock High	t_{DH}	0.5	--	0.5	--	0.5	--	ns
Write Hold to Clock High	t_{WH}	0.5	--	0.5	--	0.5	--	ns
Address Advance to Clock High	t_{ADVH}	0.5	--	0.5	--	0.5	--	ns
Chip Select Hold to Clock High	t_{CSH}	0.5	--	0.5	---	0.5	--	ns

NOTES: *1. All Address inputs must meet the specified setup and hold times for all rising clock (CLK) edges when ADV is sampled low and $\overline{CS}$x is sampled valid. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.*

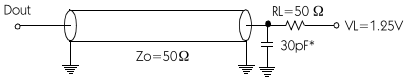
2. Chip enable must be valid at each rising edge of CLK (when ADV is Low) to remain enabled.

3. A write cycle is defined by $\overline{WE}$ low having been registered into the device at ADV Low. A Read cycle is defined by $\overline{WE}$ High with ADV Low. Both cases must meet setup and hold times.

AC TEST CONDITIONS

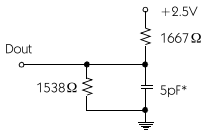
Parameter	Value
Input Pulse Level	0 to 2.5V
Input Rise and Fall Time	1.0V/ns
Input and Output Timing Reference Levels	1.25V
Output Load	See Output Load (A & B)

OUTPUT LOAD (A)



OUTPUT LOAD (B)

(FOR t_{LZC}, t_{LZOE}, t_{HZOE}, AND t_{HZC})



**Including Scope and Jig Capacitance*

SNOOZE MODE

SNOOZE MODE is a low-current, "power-down" mode in which the device is deselected and current is reduced to ISB2Z. The duration of SNOOZE MODE is dictated by the length of time Z is in a HIGH state. After the device enters SNOOZE MODE, all inputs except ZZ become gated inputs and are ignored. ZZ is an asynchronous, active HIGH input that causes the device to enter SNOOZE MODE.

When ZZ becomes a logic HIGH, ISB2Z is guaranteed after the setup time tZZ is met. Any READ or WRITE operation pending when the device enters SNOOZE MODE is not guaranteed to complete successfully. Therefore, SNOOZE MODE must not be initiated until valid pending operations are completed.

SNOOZE MODE

Description	Conditions	Symbol	Min	Max	Units
Current during SNOOZE MODE	ZZ ≥ VIH	I_{SB2Z}		20	mA
ZZ active to input ignored		t_{ZZ}		2	cycle
ZZ inactive to input sampled		t_{RZZ}	2		cycle
ZZ active to snooze current		t_{ZZI}		2	cycle
ZZ inactive to exit snooze current		t_{RZZI}	O		ns

FIG. 2 SNOOZE MODE TIMING DIAGRAM

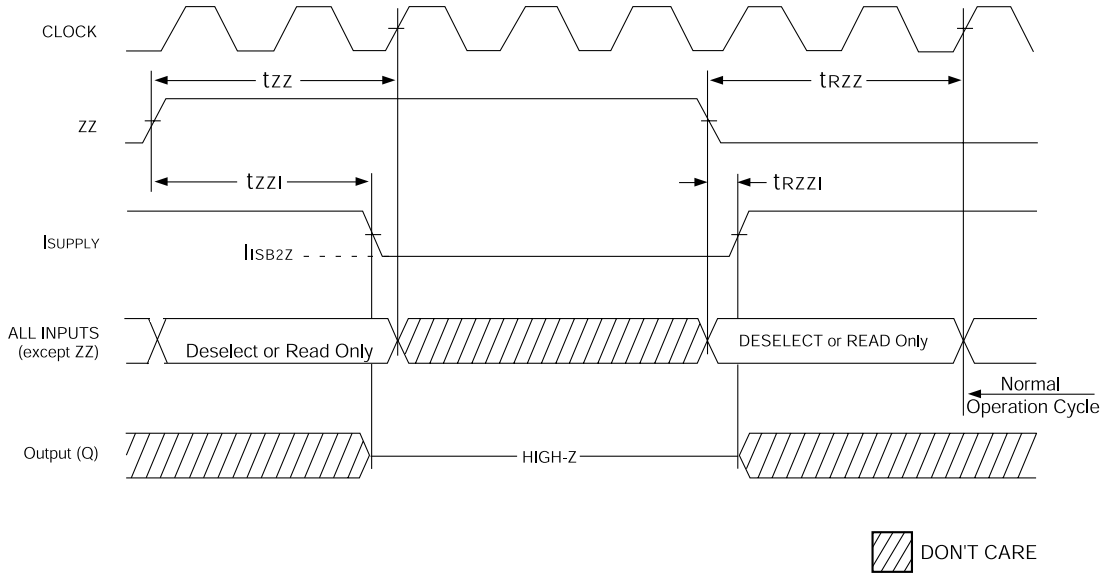
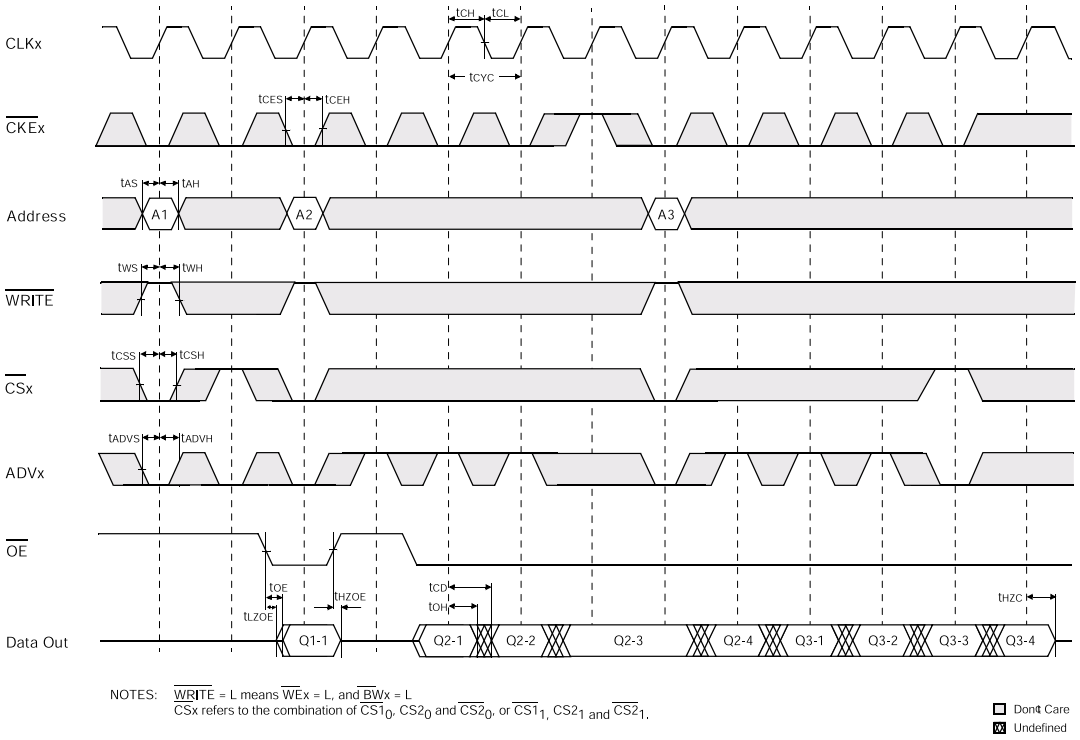
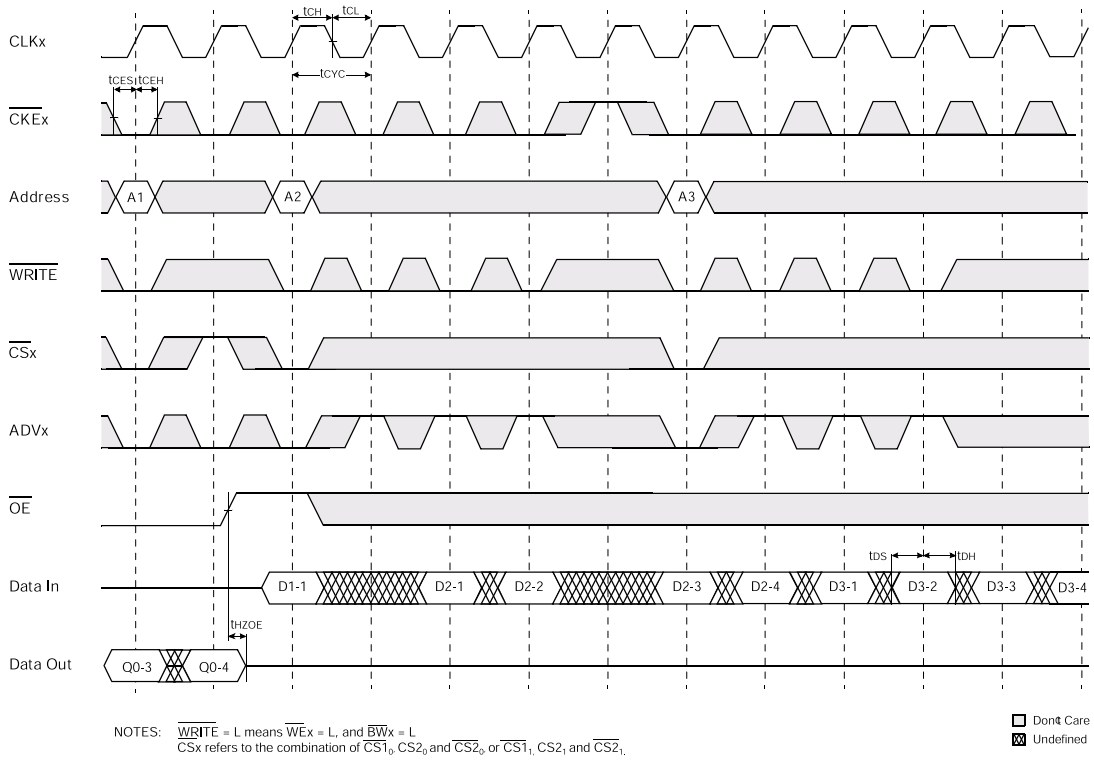


FIG. 3 TIMING WAVEFORM OF READ CYCLE



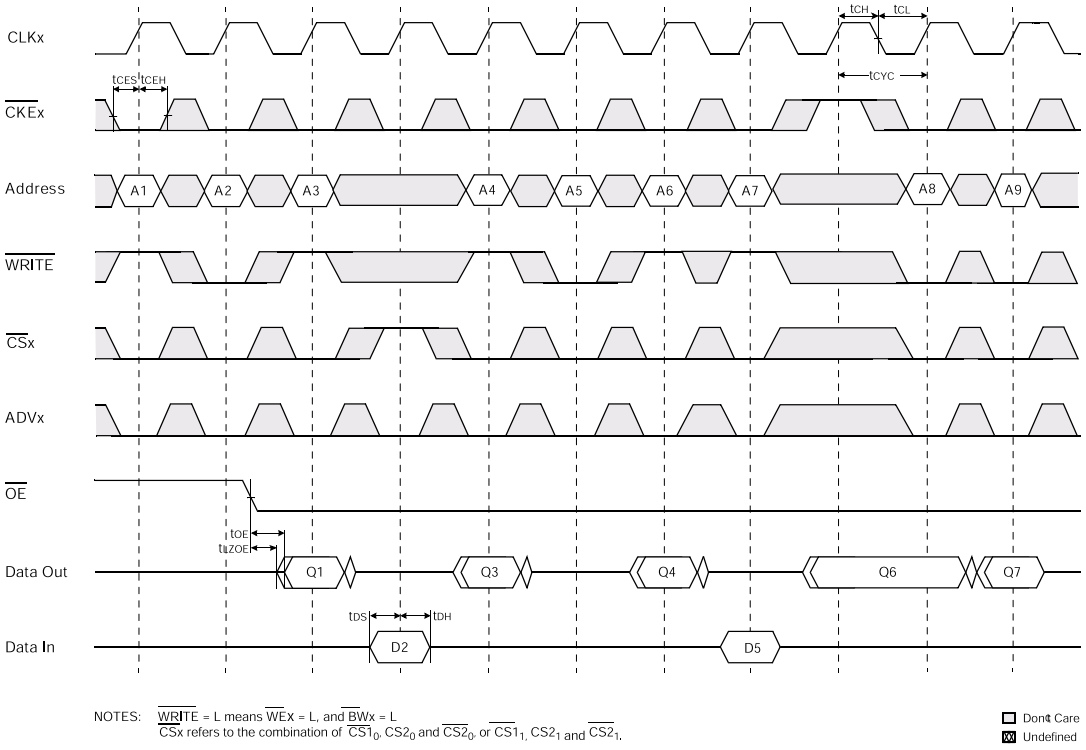
NOTES: $\overline{WRITE}$ = L means $\overline{WE}x$ = L, and $\overline{BW}x$ = L
CSx refers to the combination of $\overline{CS1}_0$, $CS2_0$ and $\overline{CS2}_0$, or $\overline{CS1}_1$, $CS2_1$ and $\overline{CS2}_1$.

FIG. 4 TIMING WAVEFORM OF WRITE CYCLE



NOTES: $\overline{WRITE}$ = L means $\overline{WE}x$ = L, and $\overline{BW}x$ = L
$\overline{CS}x$ refers to the combination of $\overline{CS1}_0$, $CS2_0$ and $\overline{CS2}_0$, or $\overline{CS1}_1$, $CS2_1$ and $\overline{CS2}_1$.

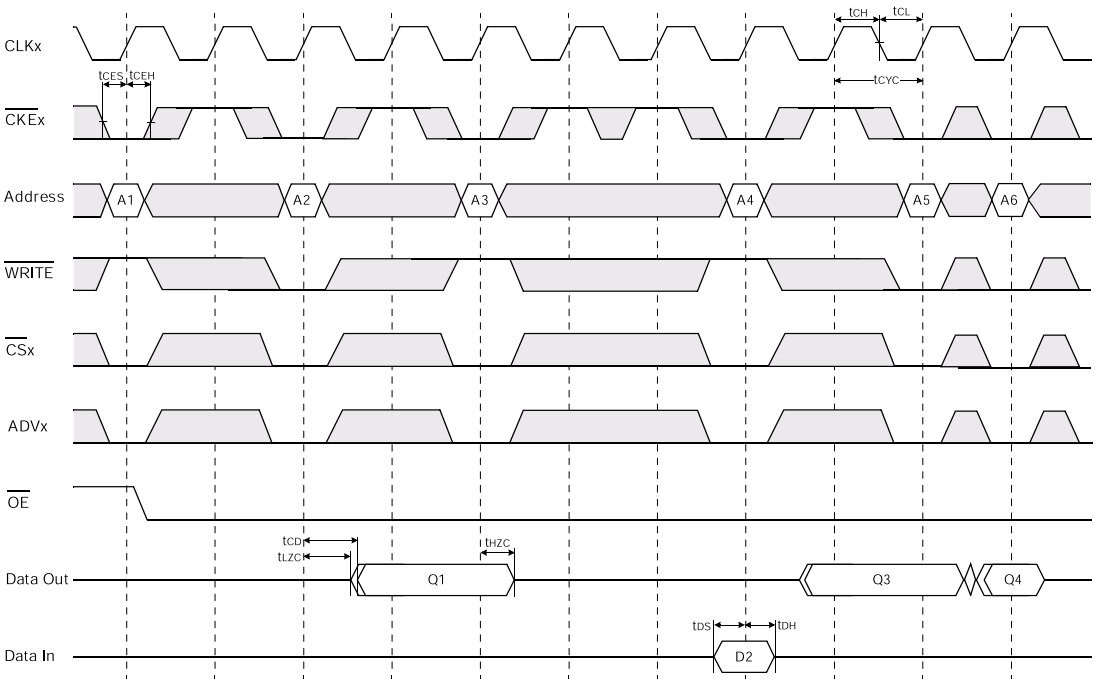
FIG. 5 TIMING WAVEFORM OF SINGLE READ/WRITE



NOTES: WRITE = L means WEx = L, and BWx = L
CSx refers to the combination of $\overline{CS1}_0$, $CS2_0$ and $\overline{CS2}_0$, or $\overline{CS1}_1$, $CS2_1$ and $\overline{CS2}_1$.

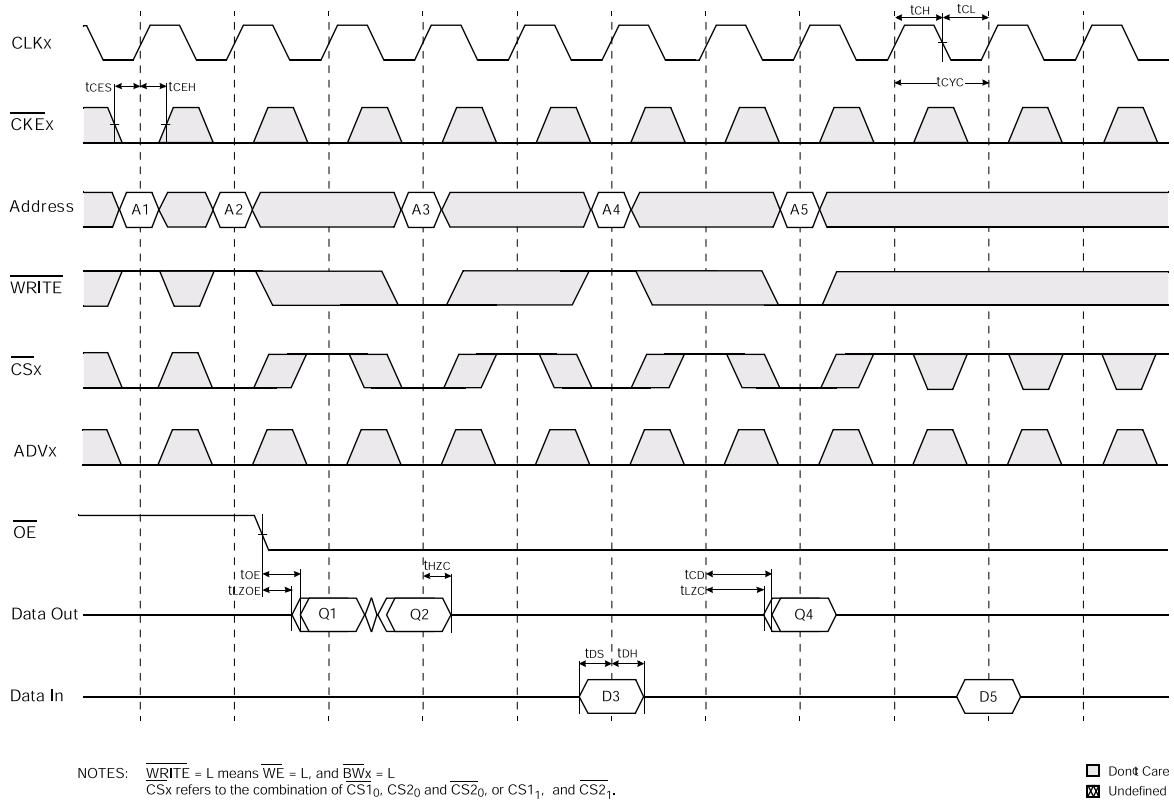
Don't Care
Undefined

FIG. 6 TIMING WAVEFORM OF CKE OPERATION

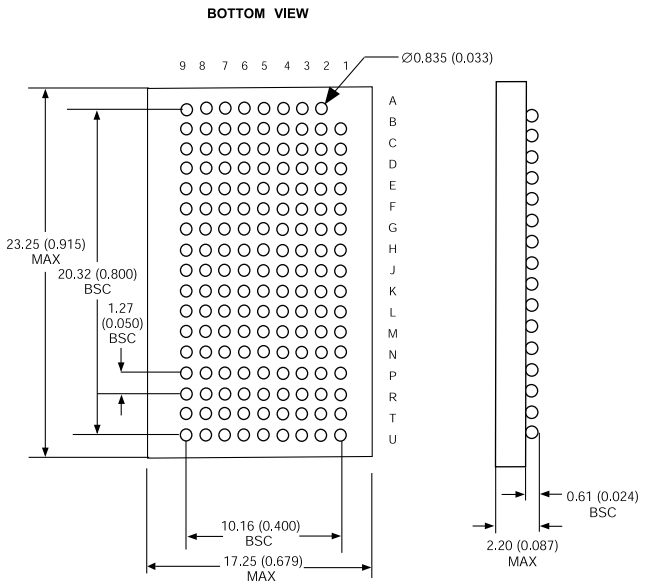


NOTES: WRITE = L means WE = L, and BWx = L
CSx refers to the combination of $CS1_0$, $CS2_0$ and $CS2_0$, or $CS1_1$, $CS2_1$ and $CS2_1$.

FIG. 7 TIMING WAVEFORM OF CE OPERATION



PACKAGE DIMENSION: 152 BUMP PBGA



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

WED P Z 512K 72 S - XXX B X

DEVICE GRADE:
- M = Military -55°C to +125°C
- I = Industrial -40°C to +85°C
- C = Commercial 0°C to +70°C

PACKAGE:
- B = 152 Plastic Ball Grid Array (PBGA)

FREQUENCY (MHz)
- 100 = 100MHz
- 133 = 133MHz
- 166 = 166MHz

2.5 V Voltage

CONFIGURATION, 512K x 72

SSRAM ZBL

PLASTIC

WHITE ELECTRONIC DESIGNS CORP.