# 1M x 36 Synchronous Pipeline Burst NBL SRAM

## FEATURES

- Fast clock speed: 166, 150, 133, and 100MHz
- Fast access times: 3.5ns, 3.8ns, 4.2ns, and 5.0ns
- Fast $\overline{OE}$ access times: 3.5ns, 3.8ns, 4.2ns, and 5.0ns
- Single +3.3V ± 5% power supply (VDD)
- Snooze Mode for reduced-standby power
- Individual Byte Write control
- Clock-controlled and registered addresses, data I/Os and control signals
- Burst control (interleaved or linear burst)
- Packaging:
  - 119-bump BGA package
- Low capacitive bus loading

## DESCRIPTION

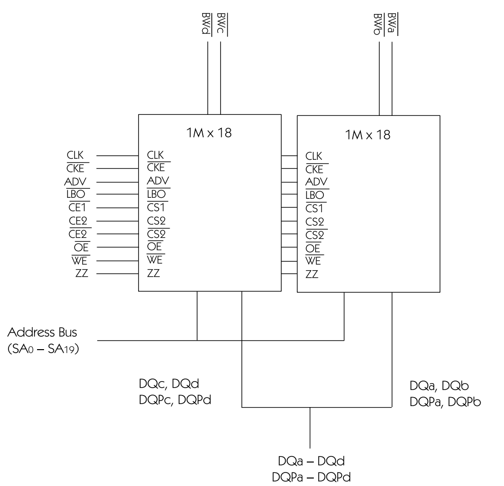
The WEDC SyncBurst - SRAM family employs high-speed, low-power CMOS designs that are fabricated using an advanced CMOS process. WEDC's 32Mb SyncBurst SRAMs integrate two 1M x 18 SRAMs into a single BGA package to provide 1M x 36 configuration. All synchronous inputs pass through registers controlled by a positive-edge-triggered single-clock input (CLK). The NBL or No Bus Latency Memory utilizes all the bandwidth in any combination of operating cycles. Address, data inputs, and all control signals except output enable and linear burst order are synchronized to input clock. Burst order control must be tied "High or Low." Asynchronous inputs include the sleep mode enable (ZZ). Output Enable controls the outputs at any given time. Write cycles are internally self-timed and initiated by the rising edge of the clock input. This feature eliminates complex off-chip write pulse generation and provides increased timing flexibility for incoming signals.

**FIG. 1** PIN CONFIGURATION

(TOP VIEW)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| A | $V_{DD}$ | SA | SA | SA | SA | SA | $V_{DD}$ |
| B | SA | $CE_2$ | SA | $\overline{ADV}$ | SA | $\overline{CE_2}$ | NC |
| C | NC | SA | SA | $V_{DD}$ | SA | SA | NC |
| D | $DQ_C$ | $DQP_C$ | $V_{SS}$ | NC | $V_{SS}$ | $DQP_B$ | $DQ_B$ |
| E | $DQ_C$ | $DQ_C$ | $V_{SS}$ | $\overline{CE_1}$ | $V_{SS}$ | $DQ_B$ | $DQ_B$ |
| F | $V_{DD}$ | $DQ_C$ | $V_{SS}$ | $\overline{OE}$ | $V_{SS}$ | $DQ_B$ | $V_{DD}$ |
| G | $DQ_C$ | $DQ_C$ | $\overline{BW_C}$ | SA | $\overline{BW_B}$ | $DQ_B$ | $DQ_B$ |
| H | $DQ_C$ | $DQ_C$ | $V_{SS}$ | $\overline{WE}$ | $V_{SS}$ | $DQ_B$ | $DQ_B$ |
| J | $V_{DD}$ | $V_{DD}$ | NC | $V_{DD}$ | NC | $V_{DD}$ | $V_{DD}$ |
| K | $DQ_D$ | $DQ_D$ | $V_{SS}$ | CLK | $V_{SS}$ | $DQ_A$ | $DQ_A$ |
| L | $DQ_D$ | $DQ_D$ | $\overline{BW_D}$ | NC | $\overline{BW_A}$ | $DQ_A$ | $DQ_A$ |
| M | $V_{DD}$ | $DQ_D$ | $V_{SS}$ | $\overline{CKE}$ | $V_{SS}$ | $DQ_A$ | $V_{DD}$ |
| N | $DQ_D$ | $DQ_D$ | $V_{SS}$ | $SA_1$ | $V_{SS}$ | $DQ_A$ | $DQ_A$ |
| P | $DQ_D$ | $DQP_D$ | $V_{SS}$ | $SA_0$ | $V_{SS}$ | $DQP_A$ | $DQ_A$ |
| R | NC | SA | LBO | $V_{DD}$ | NC | SA | NC |
| T | NC | NC | SA | SA | SA | NC | ZZ |
| U | $V_{DD}$ | NC | NC | NC | NC | NC | $V_{DD}$ |

BLOCK DIAGRAM



## FUNCTION DESCRIPTION

The WED2ZL361MV is an NBL SSRAM designed to sustain 100% bus bandwidth by eliminating turnaround cycle when there is transition from Read to Write, or vice versa. All inputs (with the exception of $\overline{OE}$, LBO and ZZ) are synchronized to rising clock edges.

All read, write and deselect cycles are initiated by the $\overline{ADV}$ input. Subsequent burst addresses can be internally generated by the burst advance pin ($\overline{ADV}$). $\overline{ADV}$ should be driven to Low once the device has been deselected in order to load a new address for next operation.

Clock Enable (CKE) pin allows the operation of the chip to be suspended as long as necessary. When CKE is high, all synchronous inputs are ignored and the internal device registers will hold their previous values. NBL SSRAM latches external address and initiates a cycle when CKE and ADV are driven low at the rising edge of the clock.

Output Enable (OE) can be used to disable the output at any given time. Read operation is initiated when at the rising edge of the clock, the address presented to the address inputs are latched in the address register, CKE is driven low, the write enable input signals $\overline{WE}$ are driven high, and $\overline{ADV}$ driven low. The internal array is read between the first rising edge and the second rising edge of the clock and the data is latched in the output register. At the second clock edge the data is driven out of the SRAM. During read operation $\overline{OE}$ must be driven low for the device to drive out the requested data.

Write operation occurs when $\overline{WE}$ is driven low at the rising edge of the clock. $\overline{BW}$[d:a] can be used for byte write operation. The pipe-lined NBL SSRAM uses a late-late write cycle to utilize 100% of the bandwidth. At the first rising edge of the clock, $\overline{WE}$ and address are registered, and the data associated with that address is required two cycle later.

Subsequent addresses are generated by ADV High for the burst access as shown below. The starting point of the burst seguence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the LBO pin. When this pin is low, linear burst sequence is selected. And when this pin is high, Interleaved burst sequence is selected.

During normal operation, ZZ must be driven low. When ZZ is driven high, the SRAM will enter a Power Sleep Mode after 2 cycles. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM operates after 2 cycles of wake up time.

## BURST SEQUENCE TABLE

(Interleaved Burst, LBO = High)

| | | Case 1 | | Case 2 | | Case 3 | | Case 4 | |
|---|---|---|---|---|---|---|---|---|---|
| LBO Pin | High | A1 | A0 | A1 | A0 | A1 | A0 | A1 | A0 |
| First Address | | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| ↓ | | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| Fourth Address | | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |

(Linear Burst, LBO = Low)

| | | Case 1 | | Case 2 | | Case 3 | | Case 4 | |
|---|---|---|---|---|---|---|---|---|---|
| LBO Pin | High | A1 | A0 | A1 | A0 | A1 | A0 | A1 | A0 |
| First Address | | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| ↓ | | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| Fourth Address | | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |

*NOTE 1: LBO pin must be tied to High or Low, and Floating State must not be allowed.*

# TRUTH TABLES

## SYNCHRONOUS TRUTH TABLE

| $\overline{CEx}$ | ADV | $\overline{WE}$ | $\overline{BWx}$ | $\overline{OE}$ | $\overline{CKE}$ | CLK | Address Accessed | Operation |
|---|---|---|---|---|---|---|---|---|
| H | L | X | X | X | L | ↑ | N/A | Deselect |
| X | H | X | X | X | L | ↑ | N/A | Continue Deselect |
| L | L | H | X | L | L | ↑ | External Address | Begin Burst Read Cycle |
| X | H | X | X | L | L | ↑ | Next Address | Continue Burst Read Cycle |
| L | L | H | X | H | L | ↑ | External Address | NOP/Dummy Read |
| X | H | X | X | H | L | ↑ | Next Address | Dummy Read |
| L | L | L | L | X | L | ↑ | External Address | Begin Burst Write Cycle |
| X | H | X | L | X | L | ↑ | Next Address | Continue Burst Write Cycle |
| L | L | L | H | X | L | ↑ | N/A | NOP/Write Abort |
| X | H | X | H | X | L | ↑ | Next Address | Write Abort |
| X | X | X | X | X | H | ↑ | Current Address | Ignore Clock |

*NOTES:*
*1. X means "Don't Care."*
*2. The rising edge of clock is symbolized by (↑)*
*3. A continue deselect cycle can only be entered if a deselect cycle is executed first.*
*4. $\overline{WRITE}$ = L means Write operation in WRITE TRUTH TABLE. $\overline{WRITE}$ = H means Read operation in WRITE TRUTH TABLE.*
*5. Operation finally depends on status of asynchronous input pins (ZZ and $\overline{OE}$).*
*6. $\overline{CEx}$ refers to the combination of $\overline{CE_1}$, $CE_2$ and $\overline{CE_2}$.*

## WRITE TRUTH TABLE

| $\overline{WE}$ | $\overline{BWA}$ | $\overline{BWB}$ | $\overline{BWC}$ | $\overline{BWD}$ | Operation |
|---|---|---|---|---|---|
| H | X | X | X | X | Read |
| L | L | H | H | H | Write Byte A |
| L | H | L | H | H | Write Byte B |
| L | H | H | L | H | Write Byte C |
| L | H | H | H | L | Write Byte D |
| L | L | L | L | L | Write All Bytes |
| L | H | H | H | H | Write Abort/NOP |

*NOTES:*
*1. X means "Don't Care."*
*2. All inputs in this table must meet setup and hold time around the rising edge of CLK (↑).*

## ABSOLUTE MAXIMUM RATINGS*

| | |
|---|---|
| Voltage on $V_{DD}$ Supply Relative to $V_{SS}$ | -0.3V to +4.6V |
| $V_{IN}$ ($DQ_X$) | -0.3V to +4.6V |
| $V_{IN}$ (Inputs) | -0.3V to +4.6V |
| Storage Temperature (BGA) | -65°C to +150°C |
| Short Circuit Output Current | 100mA |

*Stress greater than those listed under "Absolute Maximum Ratings: may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating condtions for extended periods may affect reliability.*

## ELECTRICAL CHARACTERISTICS (0°C - TA - 70°C)

| Description | Symbol | Conditions | Min | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Input High (Logic 1) Voltage | $V_{IH}$ | | 2.0 | $V_{DD}$ +0.5 | V | 1 |
| Input Low (Logic 0) Voltage | $V_{IL}$ | | -0.3 | 0.8 | V | 1 |
| Input Leakage Current | $IL_I$ | 0V ≤ $V_{IN}$ ≤ $V_{DD}$ | -5 | 5 | µA | 2 |
| Output Leakage Current | $IL_O$ | Output(s) Disabled, 0V ≤ $V_{IN}$ ≤ $V_{DD}$ | -5 | 5 | µA | |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -4.0mA | 2.4 | --- | V | 1 |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 8.0mA | --- | 0.4 | V | 1 |
| Supply Voltage | $V_{DD}$ | | 3.135 | 3.465 | V | 1 |

*NOTES:*
1. *All voltages referenced to $V_{SS}$ (GND)*
2. *ZZ pin has an internal pull-up, and input leakage = ± 10µA.*

## DC CHARACTERISTICS

| Description | Symbol | Conditions | Typ | 166 MHz | 150 MHz | 133 MHz | 100 MHz | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| Power Supply Current: Operating | $I_{DD}$ | Device Selected; All Inputs ≤ VIL or ≥ VIH; Cycle Time = $t_{CYC}$ MIN; $V_{DD}$ = MAX; Output Open | | 840 | 800 | 760 | 640 | mA | 1, 2 |
| Power Supply Current: Standby | $I_{SB2}$ | Device Deselected; $V_{DD}$ = MAX; All Inputs ≤ VSS + 0.2 or $V_{DD}$ - 0.2; All Inputs Static; CLK Frequency = 0; ZZ ≤ VIL | 30 | 60 | 60 | 60 | 60 | mA | 2 |
| Power Supply Current: Current | $I_{SB3}$ | Device Selected; All Inputs ≤ VIL or ≥ VIH; Cycle Time = $t_{CYC}$ MIN; $V_{DD}$ = MAX; Output Open; ZZ ≥ $V_{DD}$ - 0.2V | 30 | 60 | 60 | 60 | 60 | mA | 2 |
| Clock Running Standby Current | $I_{SB4}$ | Device Deselected; $V_{DD}$ = MAX; All Inputs ≤ $V_{SS}$ + 0.2 or $V_{DD}$ - 0.2; Cycle Time = $t_{CYC}$ MIN; ZZ ≤ VIL | | 240 | 220 | 180 | 160 | mA | 2 |

*NOTES:*
1. *$I_{DD}$ is specified with no output current and increases with faster cycle times. $I_{DD}$ increases with faster cycle times and greater output loading.*
2. *Typical values are measured at 3.3V, 25°C, and 10ns cycle time.*

## BGA CAPACITANCE

| Description | Symbol | Conditions | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Control Input Capacitance | $C_I$ | $T_A$ = 25°C; f = 1MHz | 5 | 7 | pF | 1 |
| Input/Output Capacitance (DQ) | $C_O$ | $T_A$ = 25°C; f = 1MHz | 6 | 8 | pF | 1 |
| Address Capacitance | $C_A$ | $T_A$ = 25°C; f = 1MHz | 5 | 7 | pF | 1 |
| Clock Capacitance | $C_{CK}$ | $T_A$= 25°C; f = 1MHz | 3 | 5 | pF | 1 |

*NOTES: 1. This parameter is sampled.*

## AC CHARACTERISTICS

| Parameter | Symbol | 166MHz Min | 166MHz Max | 150MHz Min | 150MHz Max | 133MHz Min | 133MHz Max | 100MHz Min | 100MHz Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| Clock Time | $t_{CYC}$ | 6.0 | | 6.7 | | 7.5 | | 10.0 | | ns |
| Clock Access Time | $t_{CD}$ | -- | 3.5 | -- | 3.8 | -- | 4.2 | -- | 5.0 | ns |
| Output enable to Data Valid | $t_{OE}$ | -- | 3.5 | -- | 3.8 | -- | 4.2 | -- | 5.0 | ns |
| Clock High to Output Low-Z | $t_{LZC}$ | 1.5 | -- | 1.5 | -- | 1.5 | -- | 1.5 | -- | ns |
| Output Hold from Clock High | $t_{OH}$ | 1.5 | -- | 1.5 | -- | 1.5 | -- | 1.5 | -- | ns |
| Output Enable Low to output Low-Z | $t_{LZOE}$ | 0.0 | -- | 0.0 | -- | 0.0 | -- | 0.0 | -- | ns |
| Output Enable High to Output High-Z | $t_{HZOE}$ | -- | 3.0 | -- | 3.0 | -- | 3.5 | -- | 3.5 | ns |
| Clock High to Output High-Z | $t_{HZC}$ | -- | 3.0 | -- | 3.0 | -- | 3.5 | -- | 3.5 | ns |
| Clock High Pulse Width | $t_{CH}$ | 2.2 | -- | 2.5 | -- | 3.0 | -- | 3.0 | -- | ns |
| Clock Low Pulse Width | $t_{CL}$ | 2.2 | -- | 2.5 | -- | 3.0 | -- | 3.0 | -- | ns |
| Address Setup to Clock High | $t_{AS}$ | 1.5 | -- | 1.5 | -- | 1.5 | -- | 1.5 | -- | ns |
| CKE Setup to Clock High | $t_{CES}$ | 1.5 | -- | 1.5 | -- | 1.5 | -- | 1.5 | -- | ns |
| Data Setup to Clock High | $t_{DS}$ | 1.5 | -- | 1.5 | -- | 1.5 | -- | 1.5 | -- | ns |
| Write Setup to Clock High | $t_{WS}$ | 1.5 | -- | 1.5 | -- | 1.5 | -- | 1.5 | -- | ns |
| Address Advance to Clock High | $t_{ADVS}$ | 1.5 | | 1.5 | | 1.5 | | 1.5 | | ns |
| Chip Select Setup to Clock High | $t_{CSS}$ | 1.5 | | 1.5 | | 1.5 | | 1.5 | | ns |
| Address Hold to Clock high | $t_{AH}$ | 0.5 | -- | 0.5 | -- | 0.5 | -- | 0.5 | -- | ns |
| CKE Hold to Clock High | $t_{CEH}$ | 0.5 | -- | 0.5 | -- | 0.5 | -- | 0.5 | -- | ns |
| Data Hold to Clock High | $t_{DH}$ | 0.5 | -- | 0.5 | -- | 0.5 | -- | 0.5 | -- | ns |
| Write Hold to Clock High | $t_{WH}$ | 0.5 | -- | 0.5 | -- | 0.5 | -- | 0.5 | -- | ns |
| Address Advance to Clock High | $t_{ADVH}$ | 0.5 | -- | 0.5 | -- | 0.5 | -- | 0.5 | -- | ns |
| Chip Select Hold to Clock High | $t_{CSH}$ | 0.5 | -- | 0.5 | -- | 0.5 | -- | 0.5 | -- | ns |

*NOTES:*

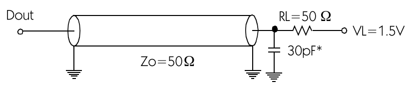
1. *All Address inputs must meet the specified setup and hold times for all rising clock (CLK) edges when $\overline{ADV}$ is sampled low and $\overline{CEx}$ is sampled valid. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.*
2. *Chip enable must be valid at each rising edge of CLK (when $\overline{ADV}$ is Low) to remain enabled.*
3. *A write cycle is defined by $\overline{WE}$ low having been registered into the device at ADV Low. A Read cycle is defined by $\overline{WE}$ High with $\overline{ADV}$ Low. Both cases must meet setup and hold times.*

## AC TEST CONDITIONS

### ($T_A$ = 0 TO 70°C, $V_{DD}$ = 3.3V ± 5%, UNLESS OTHERWISE SPECIFIED)

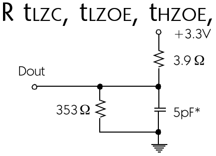
| Parameter | Value |
|---|---|
| Input Pulse Level | 0 to 3.0V |
| Input Rise and Fall Time (Measured at 20% to 80%) | 1.0V/ns |
| Input and Output Timing Reference Levels | 1.5V |
| Output Load | See Output Load (A) |

### OUTPUT LOAD (A)




### OUTPUT LOAD (B)

### (FOR $t_{LZC}$, $t_{LZOE}$, $t_{HZOE}$, AND $t_{HZC}$)




**Including Scope and Jig Capacitance*

## SNOOZE MODE

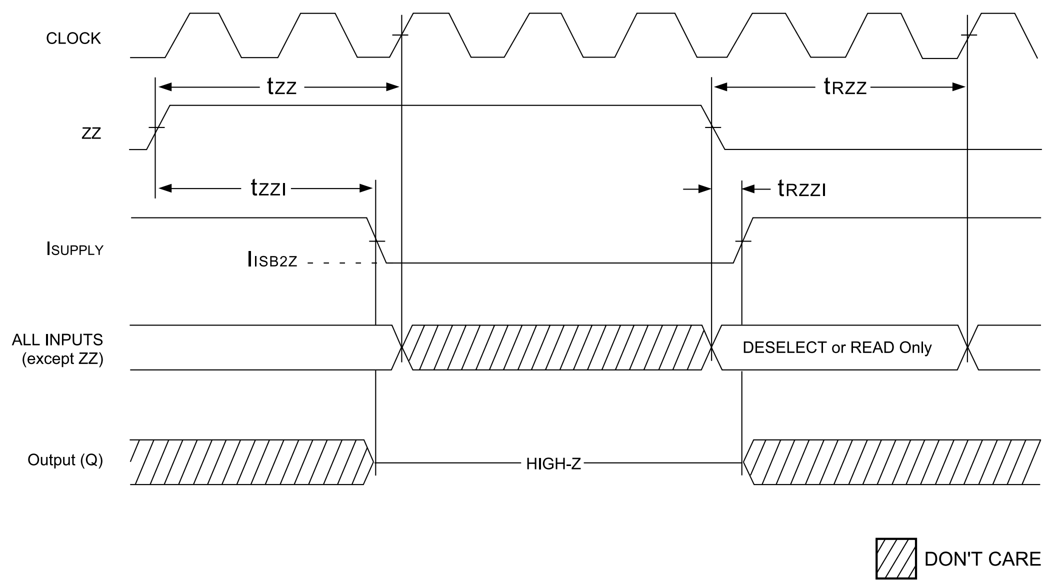
SNOOZE MODE is a low-current, "power-down" mode in which the device is deselected and current is reduced to $I_{SB2Z}$. The duration of SNOOZE MODE is dictated by the length of time Z is in a HIGH state. After the device enters SNOOZE MODE, all inputs except ZZ become gated inputs and are ignored. ZZ is an asynchronous, active HIGH input that causes the device to enter SNOOZE MODE.

When ZZ becomes a logic HIGH, $I_{SB2Z}$ is guaranteed after the setup time $t_{ZZ}$ is met. Any READ or WRITE operation pending when the device enters SNOOZE MODE is not guaranteed to complete successfully. Therefore, SNOOZE MODE must not be initiated until valid pending operations are completed.

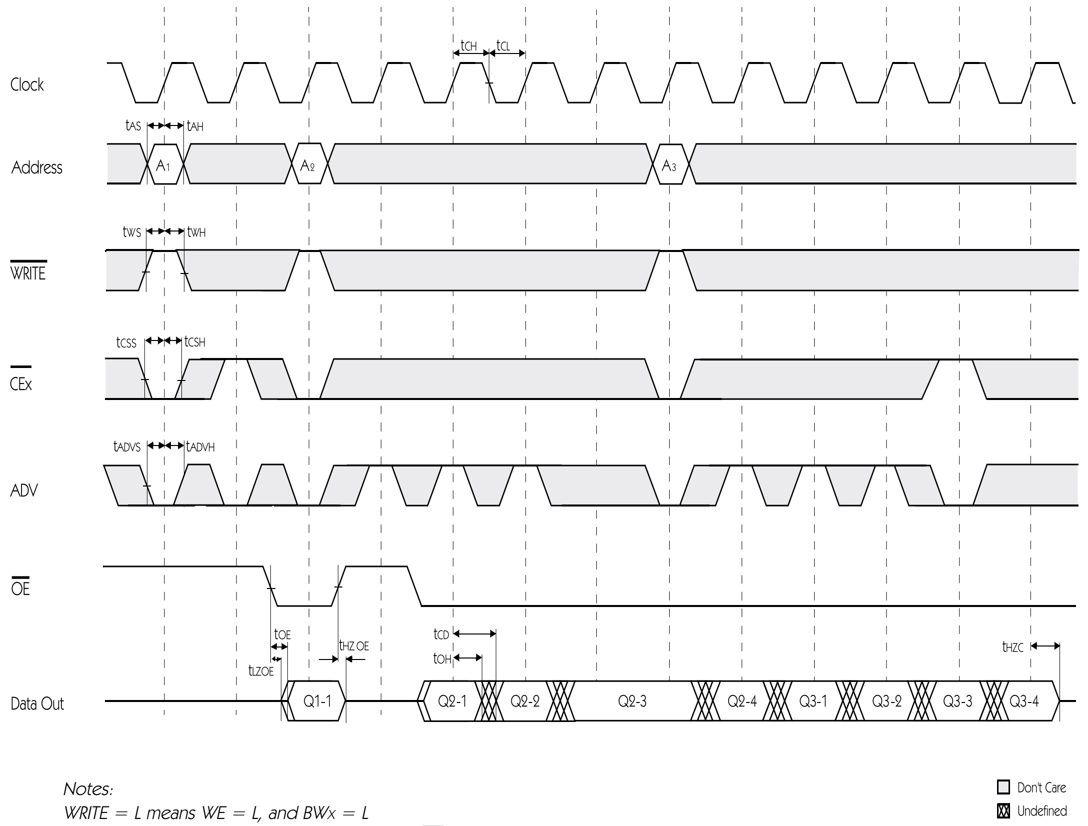
### SNOOZE MODE

| Description | Conditions | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Current during SNOOZE MODE | ZZ ≥ $V_{IH}$ | $I_{SB2Z}$ | | 10 | mA | |
| ZZ active to input ignored | | $t_{ZZ}$ | | 2($t_{KC}$) | ns | 1 |
| ZZ inactive to input sampled | | $t_{RZZ}$ | 2($t_{KC}$) | | ns | 1 |
| ZZ active to snooze current | | $t_{ZZI}$ | | 2($t_{KC}$) | ns | 1 |
| ZZ inactive to exit snooze current | | $t_{RZZI}$ | | | ns | 1 |

## FIG. 2 SNOOZE MODE TIMING DIAGRAM

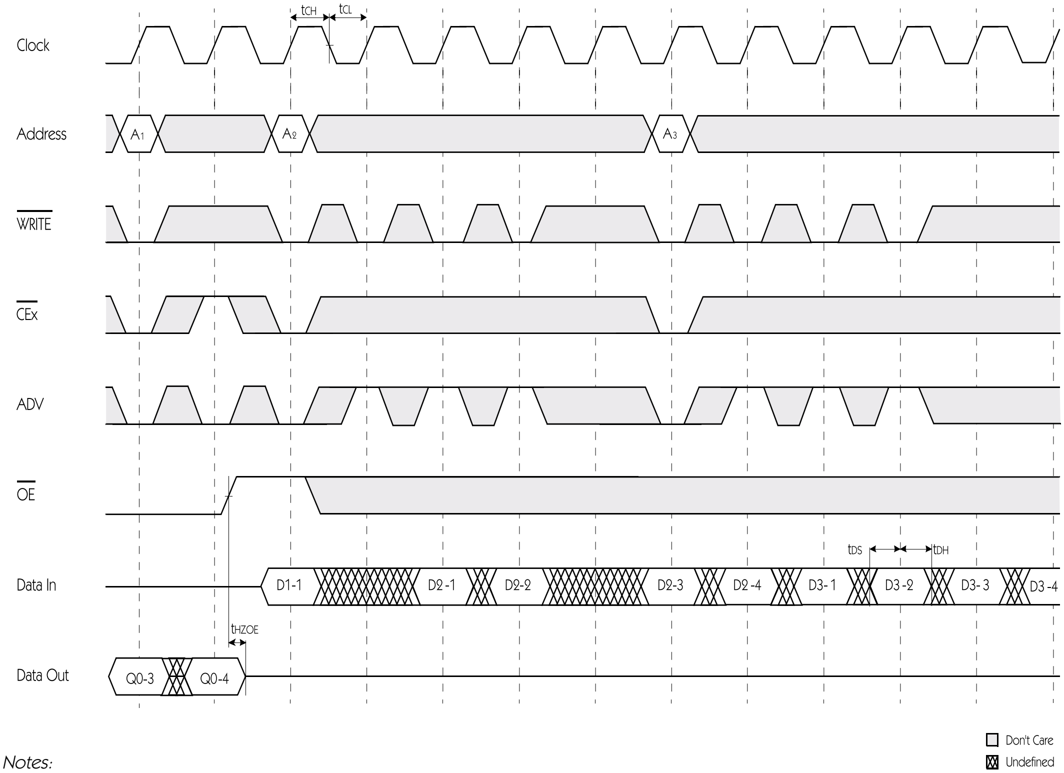


## FIG. 3 TIMING WAVEFORM OF READ CYCLE



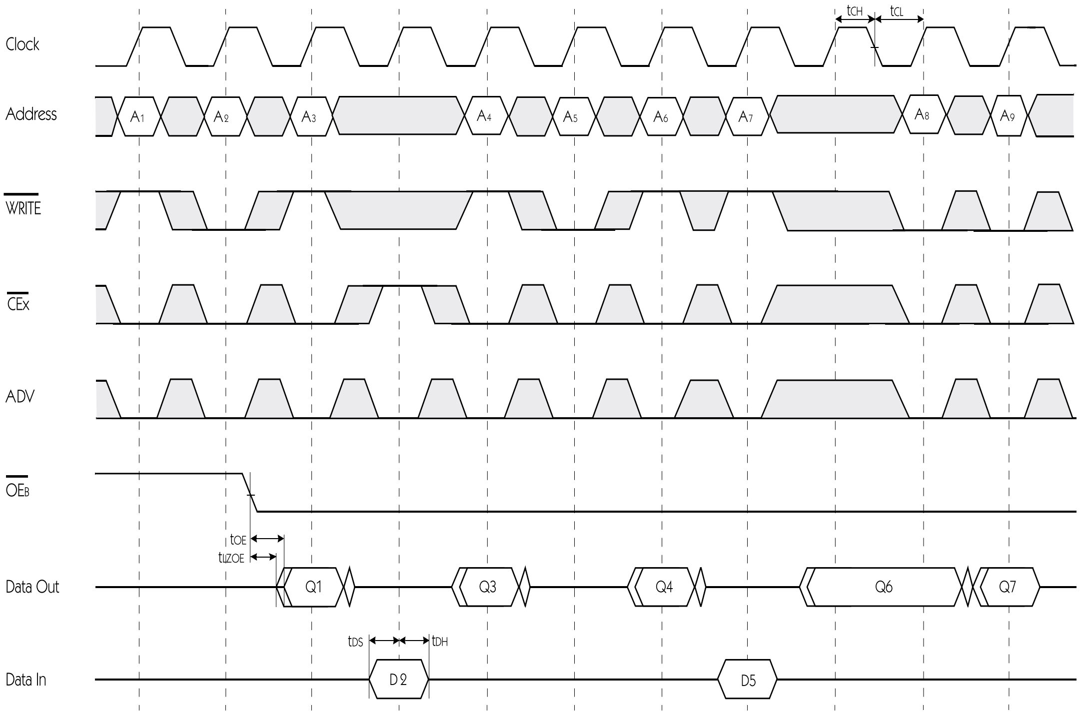

*Notes:*
*WRITE = L means WE = L, and BWx = L*
*CEx refers to the combination of $\overline{CE}_1$, $CE_2$ and $\overline{CE}_2$*

## FIG. 4 TIMING WAVEFORM OF WRITE CYCLE



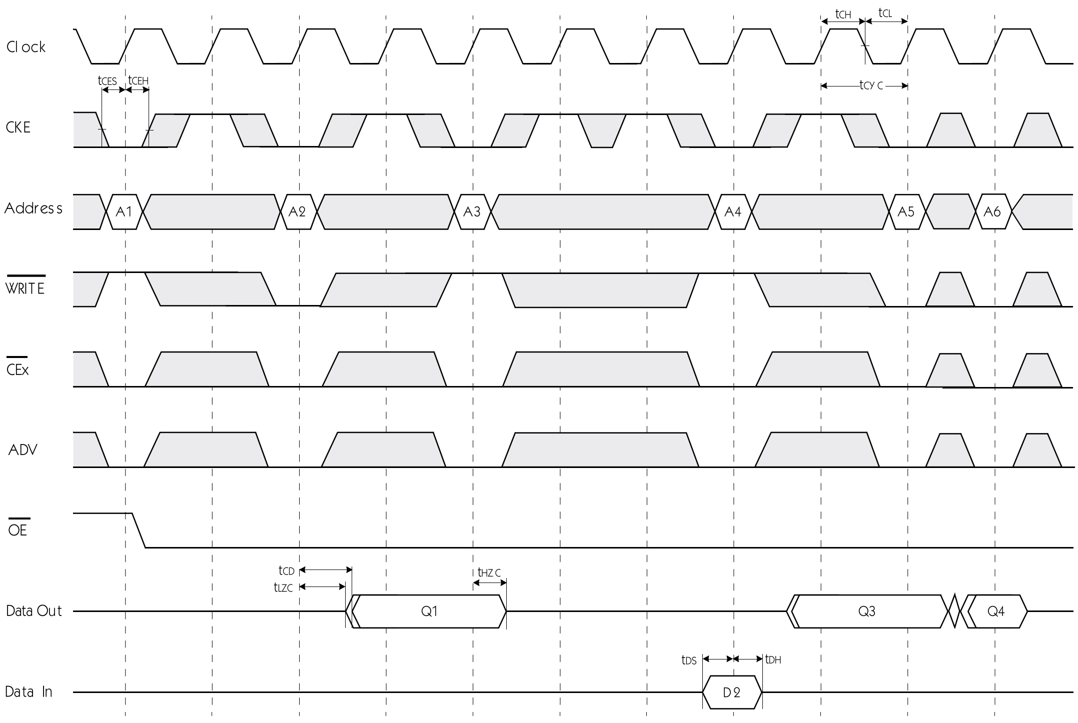

*Notes:*
*WRITE = L means WE = L, and BWx = L*
*CEx refers to the combination of $\overline{CE_1}$, $CE_2$ and $\overline{CE_2}$*

## FIG. 5 TIMING WAVEFORM OF SINGLE READ/WRITE



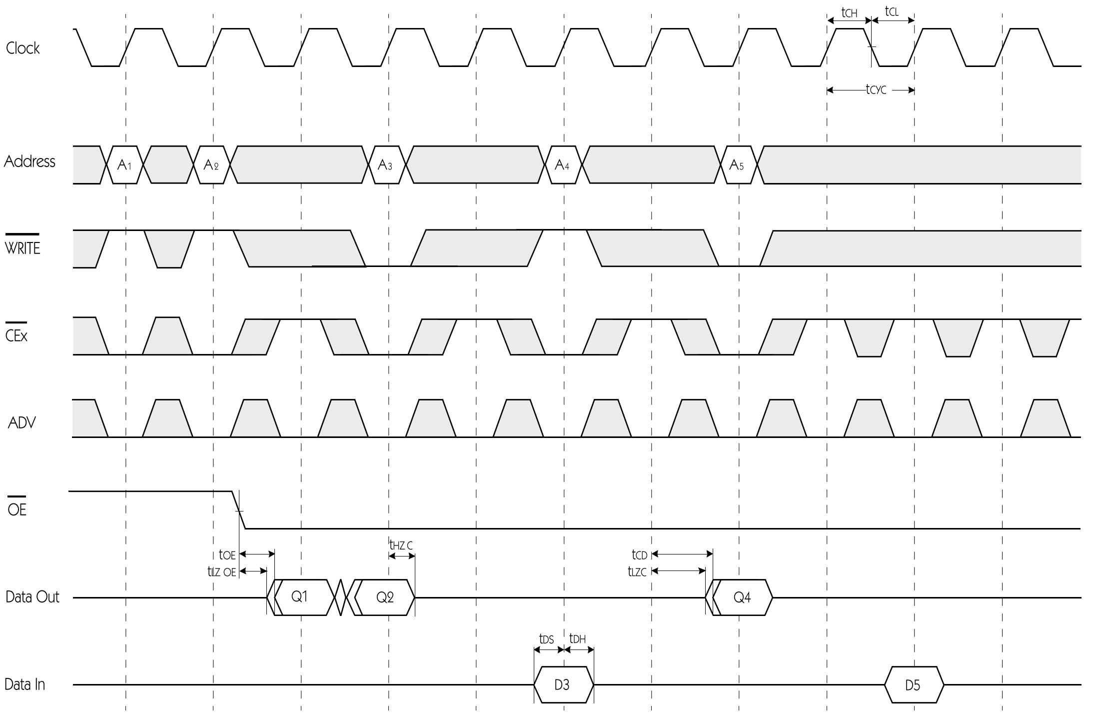

*Notes:*
*WRITE = L means WE = L, and BWx = L*
*CEx refers to the combination of CE1, CE2 and CE2*

## FIG. 6 TIMING WAVEFORM OF CKE OPERATION



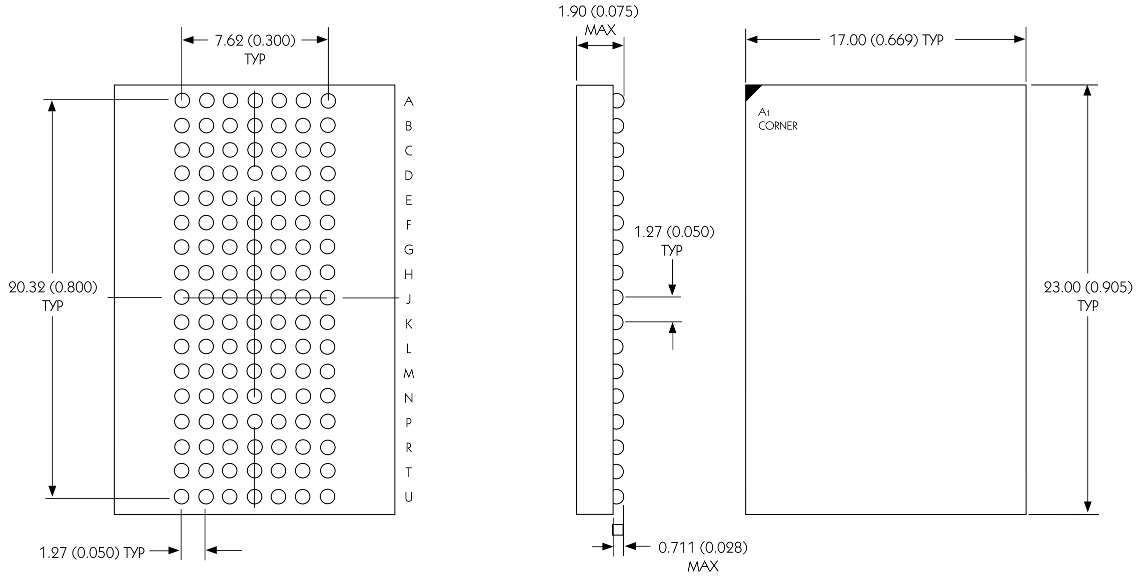

*Notes:*
*WRITE = L means WE = L, and BWx = L*
*CEx refers to the combination of $\overline{CE_1}$, $CE_2$ and $\overline{CE_2}$*

## FIG. 7 TIMING WAVEFORM OF CE OPERATION




*Notes:*
*$\overline{WRITE}$ = L means WE = L, and BWx = L*
*$\overline{CEx}$ refers to the combination of $\overline{CE_1}$, $CE_2$ and $\overline{CE_2}$*

## PACKAGE DIMENSION: 119 BUMP PBGA




*ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES*

*Note:*
*Ball attach pad for above BGA package is 620 microns in diameter. Pad is solder mask defined.*

## ORDERING INFORMATION

Commercial Temp Range (0°C to 70°C)

| Part Number | Configuration | tCD (ns) | Clock (MHz) |
|---|---|---|---|
| WED2ZL361MV35BC | 1M x 36 | 3.5 | 166 |
| WED2ZL361MV38BC | 1M x 36 | 3.8 | 150 |
| WED2ZL361MV42BC | 1M x 36 | 4.2 | 133 |
| WED2ZL361MV50BC | 1M x 36 | 5.0 | 100 |