Preliminary Data Sheet
December 1998

microelectronics group

Lucent Technologies
Bell Labs Innovations

W3041
IF Receiver with Integrated IF2 Bandpass Filters

Features

- Root Nyquist approximation 400 kHz or 450 kHz bandpass filters specified for PDC 25 kHz channel and baseband
- Small, 20-pin TSSOP package
- Low supply current for long battery life
- Wide-range RSSI
- High-gain limiter
- Low-noise, image-reject IF mixer
- Minimum external components

Applications

- PDC 800 MHz and PDC 1500 MHz (Japan RCR STD-27) portable receivers

Description

The W3041 is intended for application in cellular telephone receivers made for the Japan Personal Digital Cellular (TDMA PDC) phones. It provides the following functionality:

- IF1 mixer for translating a first IF (IF1) of 120 MHz to 200 MHz to a second IF (IF2) of 400 kHz or 450 kHz
- Integrated active IF2 bandpass filters providing selectivity, phase linearity, and dynamic range sufficient to replace conventional ceramic filters, with center frequency of 400 kHz or 450 kHz (switchable)
- Limiting RSSI amplifier strip for the IF2 filter output
- A local oscillator input buffer with on-chip coupling capacitors

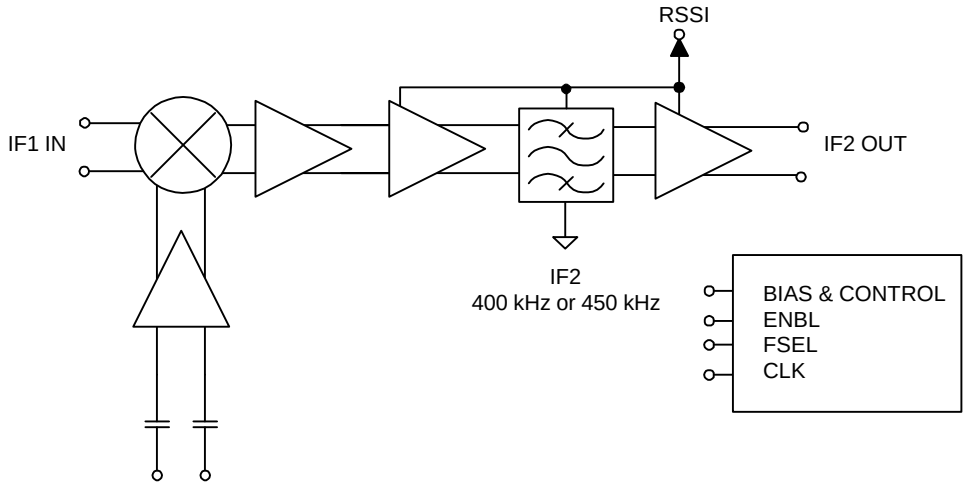


Figure 1. Circuit Block Diagram

Pin Information

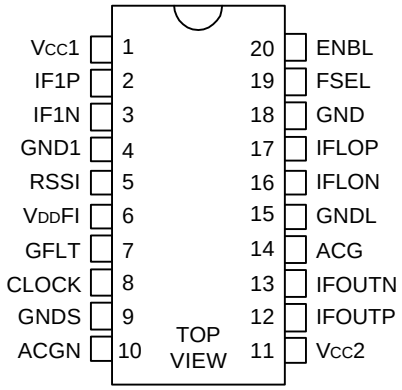


Figure 2. Pin Configuration

Table 1. Pin Descriptions

Pin	Name	Function
1	$V_{CC}1$	IF mixer positive power supply
2	IF1P	IF1 input (differential input)
3	IF1N	IF1 input (differential input)
4	GND1	Power supply ground for IF mixer
5	RSSI	RSSI output
6	$V_{DD}FI$	Active filter positive power supply
7	GFLT	Ground for integrated filter
8	CLOCK	Input for integrated IF2 filter timing clock
9	GNDS	Substrate ground for second IF section
10	ACGN	ac ground for limiting amplifier (through external capacitor to pin 14)
11	$V_{CC}2$	Positive power supply for second IF section
12	IFOUTP	IF2 limiting amplifier output (differential)
13	IFOUTN	IF2 limiting amplifier output (differential)
14	ACG	ac ground for limiting amplifier (through external capacitor to pin 10)
15	GNDL	Power supply ground for LO input buffer
16	IFLON	IF mixer local oscillator input (differential)
17	IFLOP	IF mixer local oscillator input (differential)
18	GND	Ground (no internal connection)
19	FSEL	Filter frequency select logic input
20	ENBL	Logic enable for all circuits and initiator for calibration of integrated IF2 filter (See Table 5 for requirements.)

Pin Information (continued)

Figure 3 illustrates the pinout interconnections.

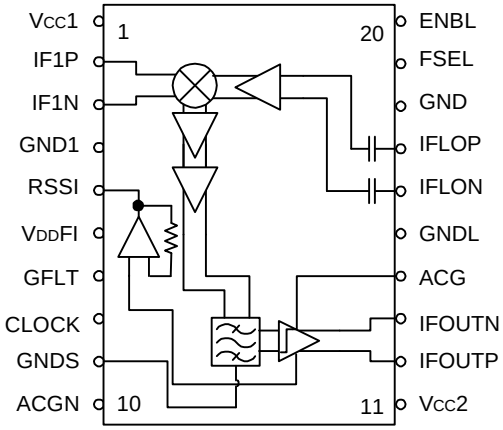


Figure 3. Package Footprint

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Ambient Operating Temperature	T_A	–30	100	°C
Storage Temperature	T_{stg}	–65	150	°C
Lead Temperature (soldering, 10 s)	—	—	300	°C
Positive Supply Voltage	V_{CC}	–0.3	4.5	V
Power Dissipation	P_D	—	100	mW
ac Peak Input Voltages	—	–0.3	≤V_{CC}	Vdc
Digital Voltages	—	–0.3	≤V_{CC}	Vdc

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. Lucent Technologies Microelectronics Group employs a human-body model (HBM) and a charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the model. No industry-wide standard has been adopted for CDM. However, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and, therefore, can be used for comparison purposes. The HBM ESD threshold presented here was obtained by using these circuit parameters:

Model	Rating	Unit
HBM	TBD	V
CDM (corner pins)	TBD	V
CDM (no corner pins)	TBD	V

Operating Ranges

The W3041 operating ranges are shown in Table 2. Performance is not guaranteed over the full range of all conditions possible within this table. However, the table lists the ranges of external conditions in which the W3041 provides general functionality, which may be useful in specific applications, without risk of permanent damage. The conditions for guaranteed performance are described in Tables 3 and 4.

Table 2. Operating Ranges

Parameter	Symbol	Min	Typ	Max	Unit
Operating Temperature (ambient air; does not include PCB heating)	T_A	–30	25	85	°C
Nominal Operating Voltage	V_{CC}	2.7	—	3.3	V
IF1 Input Frequency	—	120	—	200	MHz
IFLO Frequency (must be <f(IF1))	—	120	—	200	MHz
IFLO Input Level	V_{LO}	100	200	—	mVp-p
IF2 Frequency	IF2	—	400 or 450	—	kHz
Clock Input Level	—	0.5	—	V_{CC}	Vp-p
Clock Input Frequency	—	—	14.4	—	MHz

Control Logic

Table 3. Binary Logic Truth Table

1 = logic high voltage; 0 = logic low voltage.

ENBL	FSEL	Function
1	X	Active Mode
0	X	Sleep Mode
1	1	IF2 = 450 kHz
1	0	IF2 = 400 kHz

Table 4. Clock Frequencies

Clock (MHz)	IF2 (kHz)	
	FSEL = 1	FSEL = 0
14.4	450	400

Note: Other clock frequencies are available. Consult your Lucent Technologies Microelectronics Group Account Manager.

Electrical Characteristics

Table 5. dc and Digital Electrical Specifications

Conditions unless otherwise noted: 2.7 ≤ V_{CC} ≤ 3.3 Vdc; T_A = 25 °C ± 3 °C; RL(IF_{OUT}) = 10 kΩ; RL(RSSI) ≥ 40 kΩ; F_{IF1} = 130.45 MHz; F_{IFLO} = 130 MHz; V_{LO} = 200 mVp-p; F_{IF2} = 450 kHz; F_{CLK} = 14.4 MHz; V_{CLK} = 0.5 Vp-p.

Parameter	Symbol	Min	Typ	Max	Unit
Enable Input*					
Logic High Voltage	V_{IL}	0.7 * V_{CC}	—	V_{CC}	V
Logic Low Voltage	V_{IL}	0	—	0.3 * V_{CC}	V
Logic High Current (V_{IH} = 3.3 V)	I_{IH}	—	—	10	µA
Logic Low Current (V_{IL} = 0.4 V)	I_{IL}	—	—	10	µA
Powerup Time (enable low to high): Filter Calibration† Other Circuits (RSSI)	 — —	 — —	 — —	 12 180	 µs µs
Power Supply Current					
Active Mode, V_{CC} = 3.0, ENBL ≥ 2.1 Vdc	I_{CC}	—	7.0	—	mA
Sleep Mode, V_{CC} = 3.3, ENBL = 0.1 Vdc	I_{PDN}	—	0.5	—	µA

* To ensure normal operation of the integrated filter, enable voltage (pin 20) must be <1.4 Vdc until $V_{CC}1$ = $V_{CC}2$ = $V_{DD}FI$ > 2.5 Vdc (pins 1, 6, 11).
† Begins when 1.4 < V_{ENBL} < (0.7 * V_{CC}) and $V_{CC}1$ = $V_{CC}2$ = $V_{DD}FI$ > 2.5 Vdc. CLK signal must be present at > 0.5 Vp-p.

Table 6. ac Specifications

Conditions unless otherwise noted: 2.7 ≤ V_{CC} ≤ 3.3 Vdc; T_A = 25 °C ± 3 °C; RL(IF_{OUT}) = 10 kΩ; RL(RSSI) ≥ 40 kΩ; F_{IF1} = 130.45 MHz; F_{IFLO} = 130 MHz; V_{LO} = 200 mVp-p; F_{IF2} = 450 kHz; F_{CLK} = 14.4 MHz; V_{CLK} = 0.5 Vp-p.

Parameter	Symbol	Min	Typical	Max	Unit
Overall Cascaded Specifications (IF1 in to IF2 out)					
Overall Noise Figure	NF	—	15	—	dB
Overall Input-referred IP3 (true power)	IIP3	—	–19	—	dBm
Gain Variation within ±9 kHz Deviation (amplitude ripple)	—	—	<0.1	—	dB
Overall Group Delay Variation, at |F – Fc| < 10 kHz	—	—	18	—	µs
IF1 Mixer Specifications					
Noise Figure	NF	—	11	—	dB
IF1 Input –1 dB Compression Point (true power)	P(–1 dB)	—	—	—	dBm
Isolation, IFLO to IF1 IN (bidirectional)	—	—	—	–35	dB
Image Rejection (reduction of gain for IF1 = IFLO – IF2)	—	—	–30	–25	dB

Electrical Characteristics (continued)

Table 6. ac Specifications (continued)

Conditions unless otherwise noted: 2.7 ≤ V_{CC} ≤ 3.3 Vdc; T_A = 25 °C ± 3 °C; R_L(IF$_{OUT}$) = 10 kΩ; R_L(RSSI) > 40 kΩ; F_{IF1} = 130.45 MHz; F_{IFLO} = 130 MHz; V_{LO} = 200 mVp-p; F_{IF2} = 450 kHz; F_{CLK} = 14.4 MHz; V_{CLK} = 0.5 Vp-p.

Parameter	Symbol	Min	Typ	Max	Unit
IF2 Filters (performance of all sections combined in cascade; measurement bandwidth 25 kHz, with minimum clock input level = 0.5 Vp-p clipped sine wave)					
Clock Input Impedance (complex magnitude)	—	—	7500	—	Ω
Rejection at F_C ± 25 kHz	—	16	19	—	dB
Rejection at F_C ± 50 kHz	—	50	57	—	dB
Rejection at F_C ± 100 kHz	—	52	65	—	dB
Rejection at F_C ± 200 kHz	—	50	65	—	dB
IF2 Limiting Amplifiers, RSSI					
IF2 Output Voltage (ac load R_L ≥ 10 kΩ, dc load R_L ≥ 100 kΩ), Differential (divide by 2 for single-ended voltage)	—	1.4	—	2.2	Vp-p
IF2 Output Duty Cycle (sine input)	—	45	50	55	%
IF2 Output Rise or Fall Time (10% to 90%; ac load R_L ≥ 10 kΩ, dc load R_L ≥ 100 kΩ)	—	—	40	100	ns
RSSI Range (input power)	—	—	90	—	dB
RSSI dc Output Range (V_{MAX} – V_{MIN})	—	—	1.6	—	Vdc
RSSI Variation: –20 °C to +60 °C, –100 dBm to –40 dBm IF1 Input	—	—	—	6	dB
RSSI Output for No IF1 Input Signal	—	—	0.5	TBD	Vdc
RSSI Output for –110 dBm IF1 (true power)	—	TBD	0.7	TBD	Vdc
RSSI Voltage for –70 dBm IF1 (true power)	—	TBD	1.3	TBD	Vdc
RSSI Voltage for –30 dBm IF1 (true power)	—	TBD	2.0	TBD	Vdc
RSSI Response Time (10% to 90%): Rise Time Fall Time	 — —	 — —	 20 20	 — —	 µs µs
RSSI Enable Time (IF1 @ –60 dBm in, after V_{ENBL} exceeds 0.7 * V_{CC})	—	TBD	25	TBD	µs
RSSI Linearity: –105 dBm to –60 dBm IF1 Input –60 dBm to –30 dBm IF1 Input	 — —	 –2 TBD	 — —	 2 TBD	 dB dB

Enabling the Power Supply (No Direct Logic to Pin 20)

If the W3041 application provides logic control of the voltage regulator instead of the W3041 directly, certain precautions must be taken. This is accomplished by connecting a resistor from the positive power supply (pin 1 = $V_{CC}1$, pin 6 = $V_{DD}FI$, and pin 11 = $V_{CC}2$) to ENBL (pin 20). It is necessary to make sure that the voltage on ENBL
(pin 20) does not exceed 0.46 V_{CC} until the voltage on the positive supply pins (pin 1 = $V_{CC}1$, pin 6 = $V_{DD}FI$, and pin 11 = $V_{CC}2$) is >2.5 Vdc. This requirement can be satisfied with an RC delay circuit requiring one resistor and one capacitor.

To design the RC delay circuit, it is necessary to know:

- Minimum stable voltage regulator output voltage V_R
- Time constant of the voltage regulator output τ_R, usually established by the internal source resistance Rs and external (or internal) regulator filter capacitance (Cs)

The W3041 integrated filter uses an automatic calibration routine that takes about 8 µs typically (12 µs max). The calibration happens every time ENBL (pin 20) goes high. The calibration routine is initiated at the logic-high threshold (minimum = 0.46 V_{CC}, maximum = 0.7 V_{CC}). For the calibration to proceed correctly, the power supply voltage ($V_{CC}1$ = $V_{CC}2$ = $V_{DD}FI$) must have risen to >2.5 Vdc.

Refer to the following circuit:

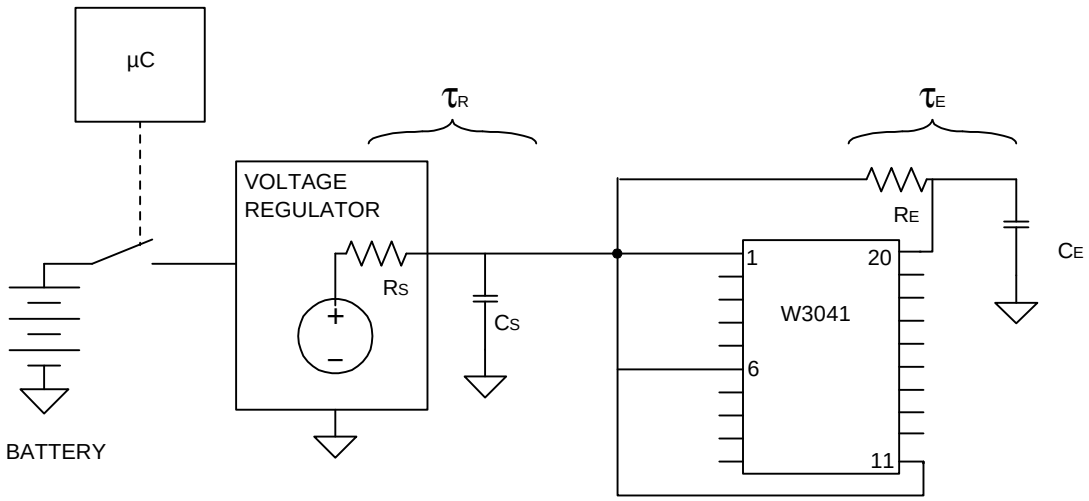


Figure 4. Power Supply Diagram

The goal is to determine the Enable Time Constant τ_E, from which convenient values of R_E and C_E can be chosen. The following equation may be used to calculate τ_E:

$$\tau_E = \frac{-\tau_R \ln\left(1 - \frac{2.5}{V_R}\right)}{0.616}$$

Enabling the Power Supply (No Direct Logic to Pin 20) (continued)

Example: Suppose the voltage regulator source resistance R_S is 2 Ω and the voltage regulator output filter capacitor Cs is 3.3 µF. The time constant τ_R is 2 * 3.3E – 6 = 6.6 µs. The voltage regulator output is specified as 3.0 ± 0.1 Vdc, so V_R = 2.9 Vdc.

$$\tau_E = \frac{-(6.6E-6)\ln\left(1-\frac{2.5}{2.9}\right)}{0.616} = (21.2E-6)\,s$$

Selecting practical values for components R_E and C_E using R_EC_E = 21.2E – 6 involves first selecting a standard capacitor value for C_E available in small physical size such as 1000 pF. The value for R_E can then be found from 21.2E-6 ÷ 1000E-12 = 21.2 kΩ for which the standard value 22 kΩ can be chosen. Using these values in an *Excel** plot, the powerup time can be seen by inspection, as shown in Figure 5.

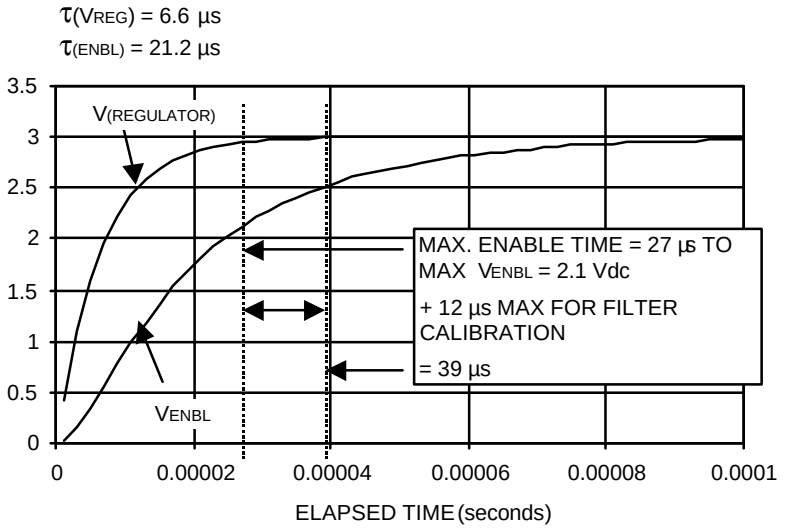


Figure 5. Required Enable Delay for Filter Calibration Circuit

**Excel* is a trademark of Microsoft Corporation.*

Characteristic Curves

Conditions unless otherwise noted: V_{CC} = 2.7; IF1 = 130.45 MHz; IF_{LO} = 130.0 MHz @ 150 mVp-p; IF2 = 400 kHz or 450 kHz; CLK = 14.40 MHz; T_A = 25 °C; mixer input terminated with 50 Ω resistor.

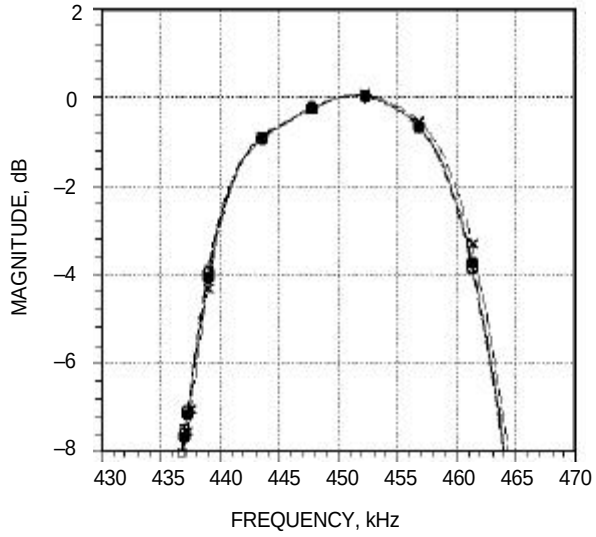


Figure 6. 450 kHz IF2 Filter Channel Passband Magnitude

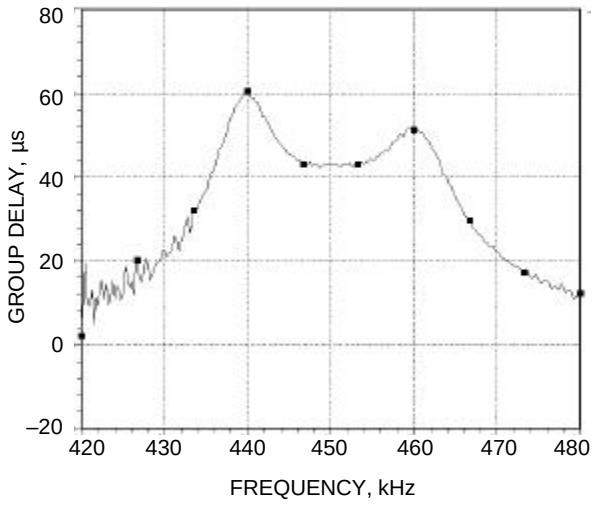


Figure 7. IF2 Bandpass Filter Group Delay Variation

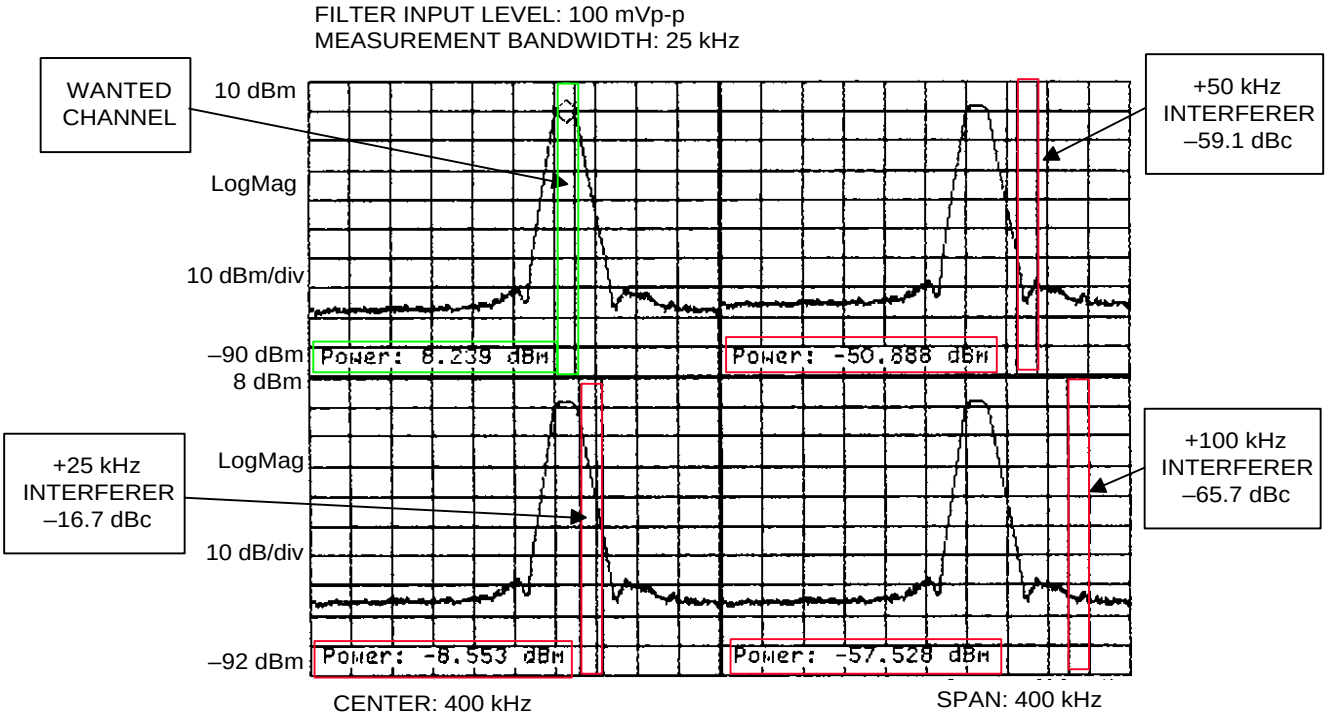


Figure 8. 450 kHz IF2 Filter Rejection

Characteristic Curves (continued)

Conditions unless otherwise noted: V_{CC} = 2.7; IF1 = 130.45 MHz; IF_{LO} = 130.0 MHz @ 150 mVp-p; IF2 = 400 kHz or 450 kHz; CLK = 14.40 MHz; T_A = 25 °C; mixer input terminated with 50 Ω resistor.

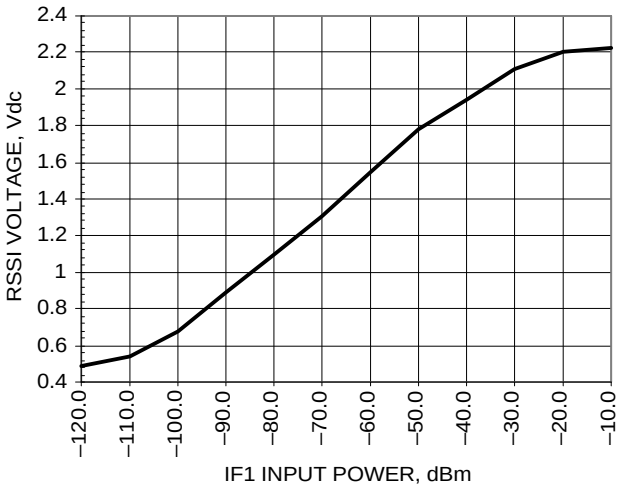


Figure 9. RSSI Response

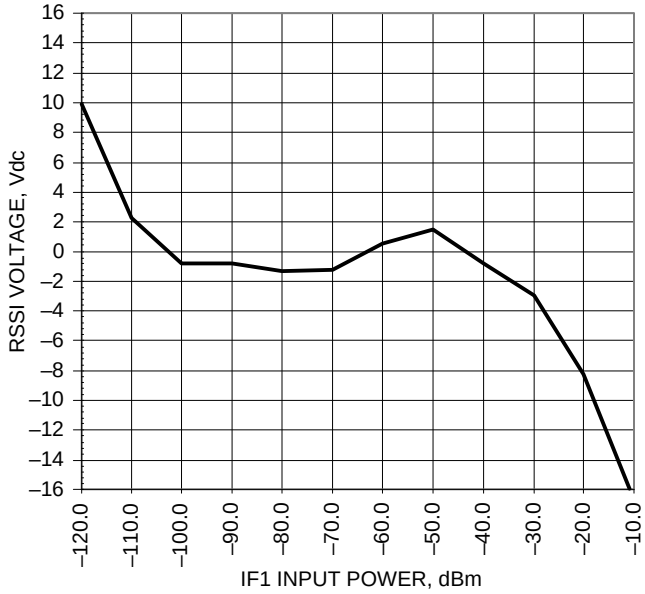
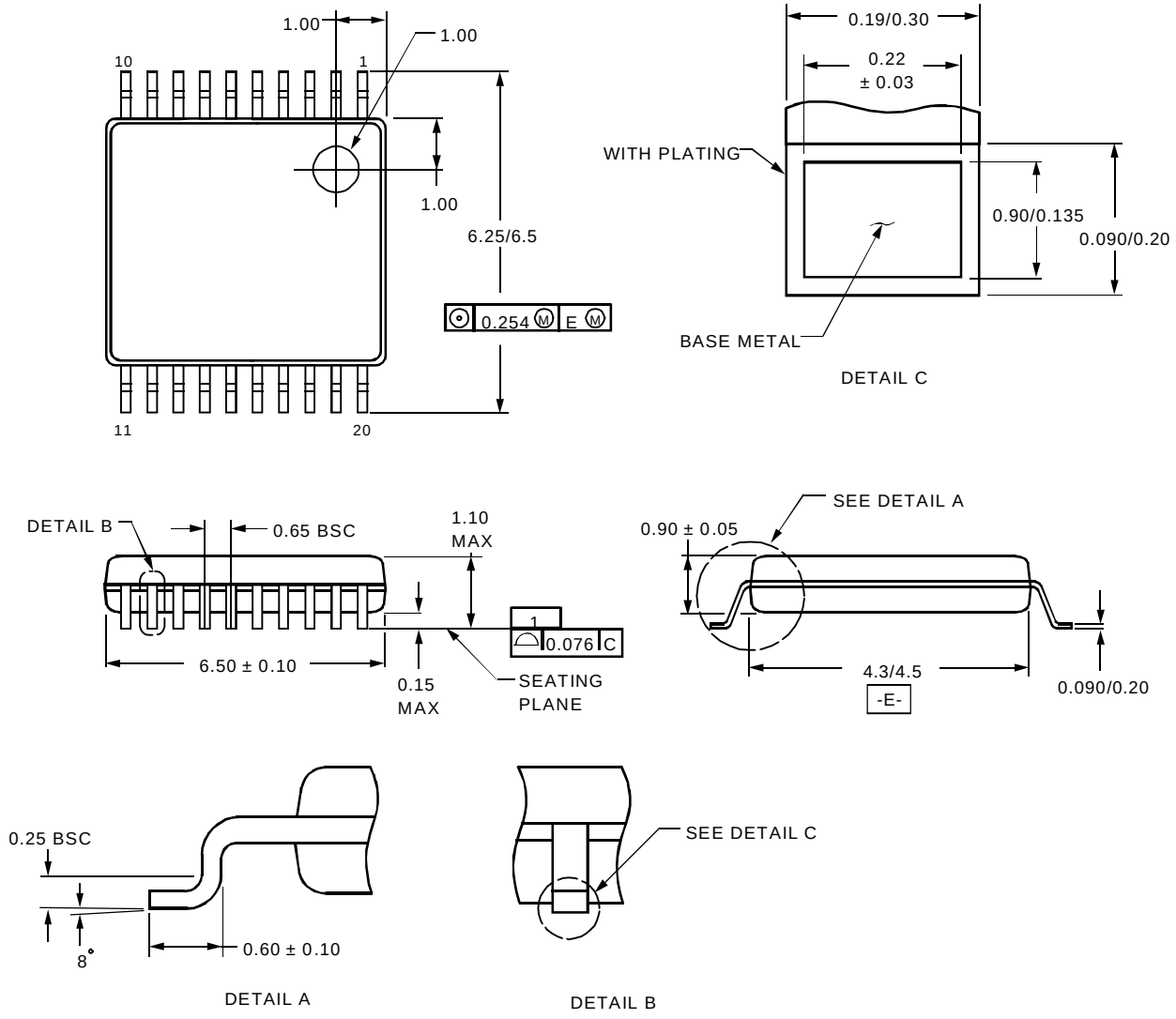


Figure 10. RSSI Linearity

Outline Diagram

20-Pin TSSOP

Dimensions are in millimeters.



Manufacturing Information

This device will be assembled in one of the following locations: assembly codes P, M, or T.

Ordering Information

Device Code	Description	Package	Comcode
W3041BCL	IF Receiver with Filters	20-pin TSSOP	108 191 388
W3041BCL-TR	IF Receiver with Filters	20-pin TSSOP, tape and reel	108 191 420
EVB3041	Evaluation Board	—	103 325 986

* Contact your Lucent Technologies Microelectronics Group Account Manager for minimum order requirements.

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