Advance Data Sheet
January 1999

microelectronics group

Lucent Technologies
Bell Labs Innovations

W3015 Modulator with Dual Synthesizers

Features

- Indirect quadrature modulator:
  - — High output power: +6 dBm typical
  - — SSB up-conversion mixer
  - — Analog attenuation control: >60 dB
  - — Modulator supply current reduces with output power
  - — Two logic-selected internal TXIF low-pass filters
- Low-power UHF integer-N PLL:
  - — Full programmable low-noise channel regulation for external VCO to 760 MHz
- Low-power dual-frequency auxiliary PLL:
  - — Two integrated VCOs for 80 MHz to 270 MHz
  - — Two preprogrammed frequencies and modes (hardware or software switching)
  - — Programmable auxiliary VCO output buffer for use with receiver
  - — Programmable ÷1 or ÷2 for use in modulator IFLO, or receiver IFLO, or both
  - — Wide-frequency plan range without trimming
- Other features:
  - — Performance specified for 2.7 Vdc power supply
  - — Reference (VC/TCXO) repeater buffer for use in baseband and other PLL devices
  - — Programmable PLL lock-detect indicator
  - — Eight enable modes for minimum operating current
  - — 48-pin TQFPT low-profile package

Applications

- PDC800 portable cellular phones

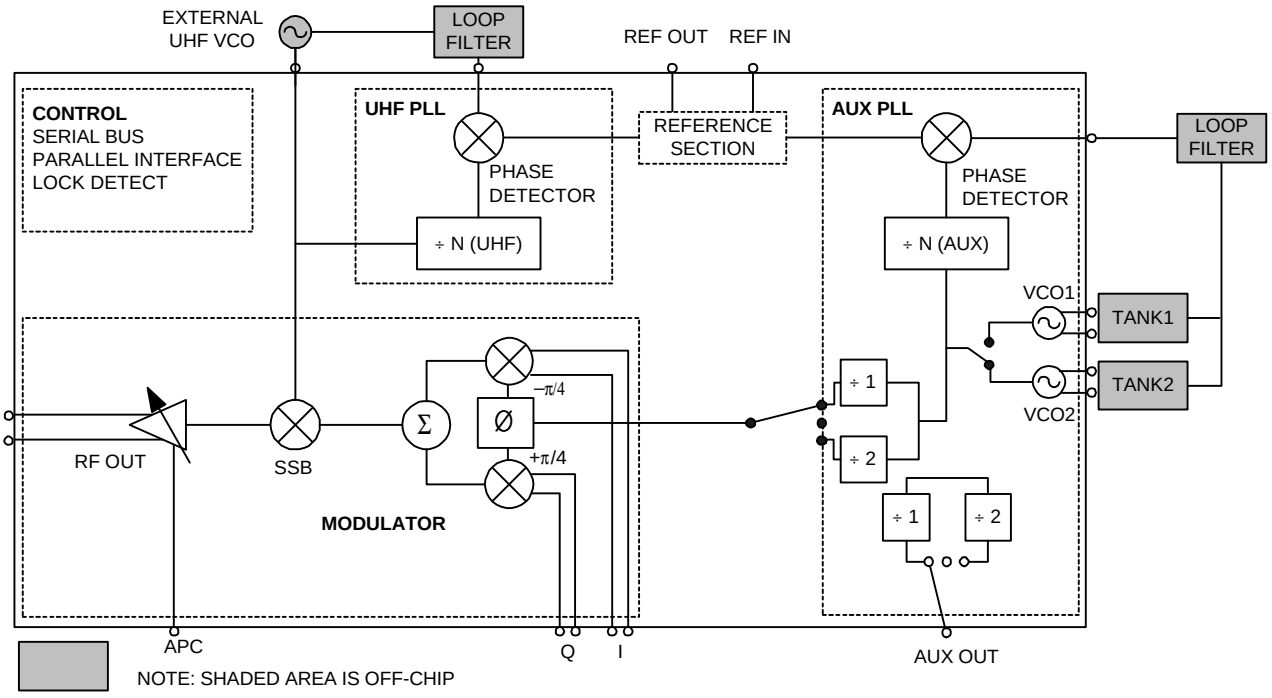

Figure 1. Circuit Block Diagram

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Description

Modulator

The modulator uses an indirect IQ modulation scheme, with a single-sideband up-conversion mixer. The on-chip auxiliary VCO output is fed to a programmable divider stage [÷1 or ÷2], which then feeds an accurate LO phase splitter. The phase splitter provides accurate TXLO signals to the I and Q mixers, generating a quadrature modulated TXIF, which is internally low-pass filtered. The internal TXIF filter has two cutoff frequencies, which are selected by the same control logic used for the auxiliary VCOs and PLL. The filtered TXIF is up-converted to the RF antenna frequency using an SSB mixer, in which the UHF LO is phase-split 90° and fed to mix with two versions of TXIF that are also phase-separated by 90°. The UHF LO phase splitter is programmable for high- or low-side LO frequencies (selectable mixer product). The summed output of the two mixers is again internally low-pass filtered and fed to a variable-gain output stage, capable of 90 dB attenuation range. The maximum usable DQPSK average power is greater than +2 dBm.

Main UHF Synthesizer

This is a programmable PLL synthesizer to be operated with an external VCO and loop filter. Programming via a serial 3-wire bus can set the reference-divider (including a reference predivider shared with the auxiliary synthesizer), main-divider, and swallow-counter values and the phase-detector polarity. The prescaler is a 64/65 countdown type, and the RF input frequency capability is over 760 MHz.

Auxiliary Synthesizer

The integrated auxiliary PLL synthesizer contains two on-chip voltage-controlled oscillators (the amplifiers with feedback), a ÷7/8 prescaler, a fully programmable main divider and swallow counter, a programmable reference divider (in addition to the 4-bit reference predivider shared with the UHF synthesizer). This PLL requires external resonant tank circuits for the VCOs and an external loop filter to connect the phase comparator charge pump output to the external varactor(s). It is programmable via the serial control bus, which can preassign two main and reference divider ratios that are quickly selectable via an external logic pin (AUXSEL) or a serial bus register bit (ASEL). The VCOs can be overdriven by an external VCO or LO source, and the VCO signal may be fed to an external receiver IF mixer through a programmable (÷1 or ÷2) divider, separate from the programmable divider that feeds the modulator. Thus any combination of {÷1, ÷1; or ÷1, ÷2; or ÷2, ÷1; or ÷2, ÷2} derived from the same VCO frequency may be fed to the modulator and auxiliary output buffer at the same time. Or only one path may be designated, with the other path disabled.

The W3015 offers considerable flexibility in frequency planning. The serial programming allows full flexibility to use a single VCO for multiple frequencies or to switch between the two VCOs for band-switching or for transmit-receive switching in TDMA systems. The availability of two VCOs and two parallel {÷1, ÷2} options ensures that two or more widely separated local oscillator frequencies can be generated without trimming of oscillator tank components.

Lock Indicator

Gross PLL out-of-lock conditions are indicated at a single output pin. The indication is programmable for either or both of the two integrated PLLs being out-of-lock.

Description (continued)

Serial Control Options

The modulator and both synthesizers are set for operating modes and frequencies by a conventional 3-wire serial control bus (data, clock, and latch lines). There are five operating registers, 24 bits each, containing bits organized for minimum reprogramming after powerup initialization. Only registers whose values change need be reloaded. There is also a sixth register for production purposes, which must be addressed and written with zeros once at power-up initialization.

Parallel Control Options

Four digital control functions are available at binary package pins. Three of these are separate enable functions for the auxiliary PLL (AUXPLLON), UHF PLL (UHFPLLON), and modulator (TXON). These are redundant to the serial bus bits MOD0, MOD1, and MOD2 respectively (UPRI register). The fourth binary control pin, AUXSEL, is redundant to the serial bus bit ASEL (UPRI register) and is mentioned in the Auxiliary Synthesizer section. These parallel control functions may be used interchangeably at any time with the associated serial bus bits.

Block Diagram: Pinout Orientation

Figure 2 shows internal functionality of the W3015 as it is accessible for connection to a printed-circuit board.

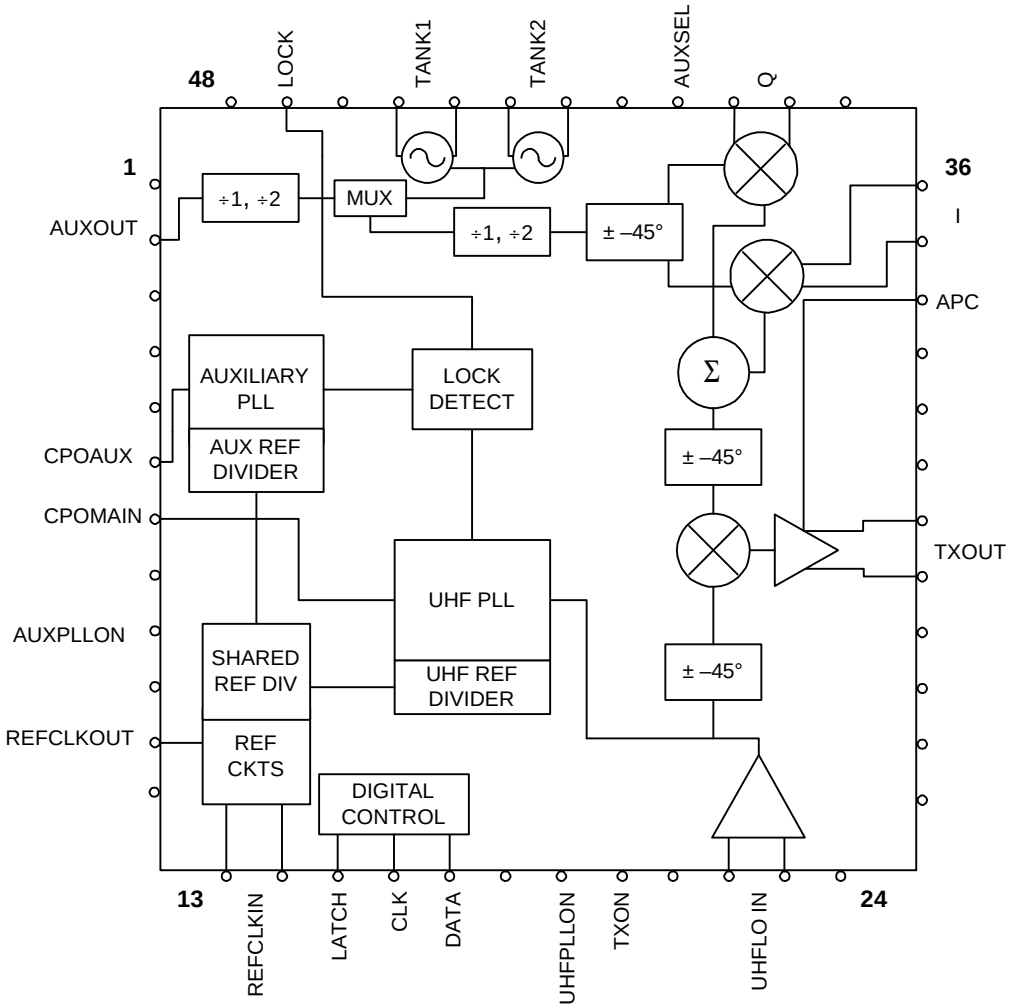


Figure 2. Block Diagram in Package Footprint

Pin Information

Figure 3 shows the footprint pinout diagram, which is explained in Table 1.

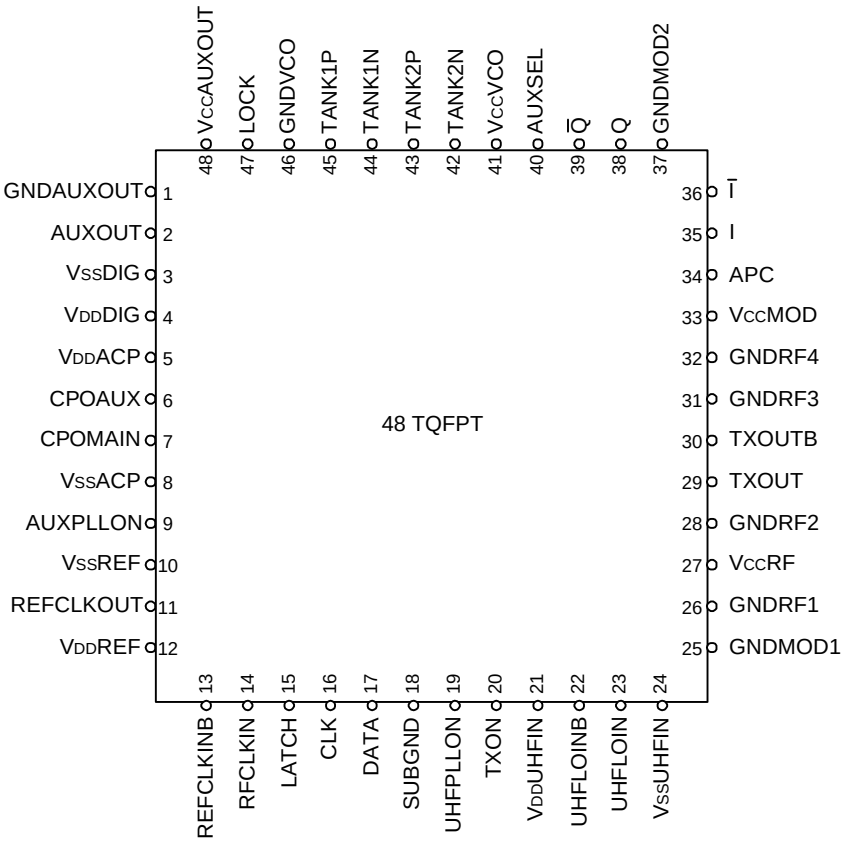


Figure 3. Pin Diagram

Pin Information (continued)

Table 1. Pin Description

Pin No.	Name	Function
1	GNDAUXOUT	Ground Return for Auxiliary Frequency Output Buffer
2	AUXOUT	Auxiliary Frequency Output Buffer
3	V_{SS}DIG	Ground Return for Synthesizers and Control Logic
4	V_{DD}DIG	Positive Power Supply for Synthesizers and Control Logic
5	V_{DD}ACP	Positive Power Supply for Both Charge Pumps
6	CPOAUX	Auxiliary Charge Pump Output
7	CPOMAIN	UHF Charge Pump Output
8	V_{SS}ACP	Ground Return for Both Charge Pumps
9	AUXPLLON	Auxiliary Synthesizer Enable Binary Logic Input
10	V_{SS}REF	Ground Return for Reference Output Buffers
11	REFCLKOUT	Reference Output Buffer
12	V_{DD}REF	Positive Power Supply for Reference Input/Output Buffers
13	REFCLKINB	VC/TCXO Input Ground
14	REFCLKIN	VC/TCXO Input
15	LATCH	Latch-enable for 3-wire Control Bus
16	CLK	Serial Bus Clock for 3-wire Control Bus
17	DATA	Serial Control Word Input for 3-wire Control Bus
18	SUBGND	Substrate Ground
19	UHFPLLON	Main Synthesizer Enable Binary Logic Input
20	TXON	Modulator Enable Binary Logic Input
21	V_{DD}UHFIN	Positive Power Supply for UHF Input Buffer and Prescaler
22	UHFLOINB	UHF Prescaler Negative Input
23	UHFLOIN	UHF Prescaler Positive Input
24	V_{SS}UHFIN	Ground Return for UHF Input Buffer and Prescaler

Pin Information (continued)

Table 1. Pin Description (continued)

Pin No.	Name	Function
25	GNDMOD1	Ground Return for Modulator Nonoutput Stages
26	GNDRF1	Ground Return for Modulator Output Stage
27	VCCRF	Positive Power Supply for Internal TX RF Gain Stage
28	GNDRF2	Ground Return for Modulator Output Stage
29	TXOUT	Differential Output from Modulator
30	TXOUTB	Differential Output from Modulator
31	GNDRF3	Ground Return for Modulator Output Stage
32	GNDRF4	Ground Return for Modulator Output Stage
33	VCCMOD	Positive Power Supply for I/Q Modulator and RF Mixers
34	APC	Power Control Input for Modulator
35	I	Differential Input for I Baseband Signal
36	$\overline{I}$	Differential Input for I Baseband Signal
37	GNDMOD2	Ground Return for Modulator Nonoutput Stages
38	Q	Differential Input for Q Baseband Signal
39	$\overline{Q}$	Differential Input for Q Baseband Signal
40	AUXSEL	Auxiliary PLL Configuration Select Logic Input
41	VCCVCO	Positive Power Supply for Auxiliary VCOs 1 and 2
42	TANK2N	Differential Auxiliary VCO 2 Resonator Connection
43	TANK2P	Differential Auxiliary VCO 2 Resonator Connection
44	TANK1N	Differential Auxiliary VCO 1 Resonator Connection
45	TANK1P	Differential Auxiliary VCO 1 Resonator Connection
46	GNDVCO	Ground Return for Auxiliary VCOs 1 and 2
47	LOCK	PLL Lock Indicator Logic Output
48	VCCAUXOUT	Positive Power Supply for Auxiliary Output Buffer

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. The ratings shown in Table 2 are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of this data sheet. Exposure to maximum ratings for extended periods can adversely affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Ambient Operating Temperature	T_A	–35	95	°C
Storage Temperature	T_{stg}	–65	150	°C
Lead Temperature (soldering, 10 s)	—	—	300	°C
Positive Supply Voltage	V_{CC}	–0.3	4.5	V
Power Dissipation	P_D	—	650	mW
ac Peak-to-Peak Input Voltage	Vp-p	—	V_{CC}	V
Digital Voltages	—	—	V_{CC}	V

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. Lucent Technologies Microelectronics Group employs a human-body model (HBM) and a charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the model. No industry-wide standard has been adopted for CDM. However, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and, therefore, can be used for comparison purposes. The HBM ESD threshold presented here was obtained by using the circuit parameters shown in Table 3.

Table 3. ESD Threshold Voltage

Model	Rating
HBM	TBD
CDM (corner pins) CDM (noncorner pins)	TBD TBD

Recommended Operating Ranges

This device is fully functional within the following operation ranges. No claims of parametric performance are stated within this range. For parametric performance, refer to the individual specifications and measurement conditions shown in the Electrical Characteristics section.

Table 4. Recommended Operating Ranges

Parameter	Symbol	Min	Max	Unit
Operating Temperature (ambient air)	T_A	–35	85	°C
Nominal Operating Voltage: V_{DD}DIG, Pin 4 V_{DD}ACP, Pin 5 V_{DD}REF, Pin 12 V_{DD}UHFIN, Pin 21 V_{CC}RF, Pin 27 TXOUT & TXOUTB, Pins 29 and 30 V_{CC}MOD, Pin 33 V_{CC}VCO, Pin 41 TANK2N, TANK2P, TANK1N, TANK1P, Pins 42 Through 45 V_{CC}AUXOUT, Pin 48	V_{CC}, V_{DD}	 2.4 2.4 2.4 2.7 2.7 2.7 2.7 2.55 2.55 2.55	 3.6 3.6 3.6 3.6 3.6 3.6 3.6 3.6 3.6 3.6	Vdc
External dc Bias Voltage for I & Q Inputs with 0.282 Vrms Differential ac Input Level	—	1.2	V_{CC} – 0.7	Vdc
Auxiliary VCO or PLL Frequency	—	80	270	MHz
Auxiliary PLL Phase Comparator Frequency	—	—	1	MHz
Auxiliary VCO to Modulator, ÷1 Frequency	—	80	265	MHz
Auxiliary VCO to Modulator, ÷2 Frequency	—	65	135	MHz
Auxiliary VCO to Output Buffer Frequency, ÷1 Mode	—	120	200	MHz
Auxiliary VCO to Output Buffer Frequency, ÷2 Mode	—	120	140	MHz
UHF PLL Frequency	—	—	760	MHz
UHF PLL Phase Comparator Frequency	—	—	1	MHz
Reference (TCXO/VCXO) Frequency	—	2	20	MHz
VC/TCXO Input Levels	—	0.5	V_{DD}REF	Vp-p
UHF Prescaler Input Level	—	100	—	mVp-p
Serial Bus Data, Clock Frequency	—	—	15	MHz

Power Supply Assignments and Options

Eleven separate power supply connections are required for the W3015, including eight V_{CC} or V_{DD} pins and three pairs of pins (six pins) which required external differential open-collector bias connections. As can be seen in the preceding Recommended Operating Ranges table (Table 4), it is possible to obtain good performance when several different power supplies at different voltages are connected. The following table shows what power supply pins are required for various functional modes of the W3015. (For more information on functional modes, please see the section on Digital Control Programming, using either external binary pins or the serial bus.)

Pin No.	Name	AUXPLL	UHFPLL	Modulator	AUXOUT Buffer	REFOUT Buffer	Control Logic
4	V_{DD}DIG	Required	Required	*	*	*	Required
5	V_{DD}ACP	Required	Required	*	*	*	*
12	V_{DD}REF	Required	Required	*	*	Required	*
41	V_{CC}VCO	Required	*	*	*	*	*
42—45	External Bias	Required	*	*	*	*	*
48	V_{CC}AUXOUT	Required	*	*	Required	*	*
21	V_{DD}UHFIN	*	Required	Required	*	*	*
27	V_{CC}RF	*	*	Required	*	*	*
29—30	External Bias	*	*	Required	*	*	*
33	V_{CC}MOD	*	*	Required	*	*	*

*Not required.

Power Supply Assignments and Options (continued)

Figure 4 further illustrates the power supply connections:

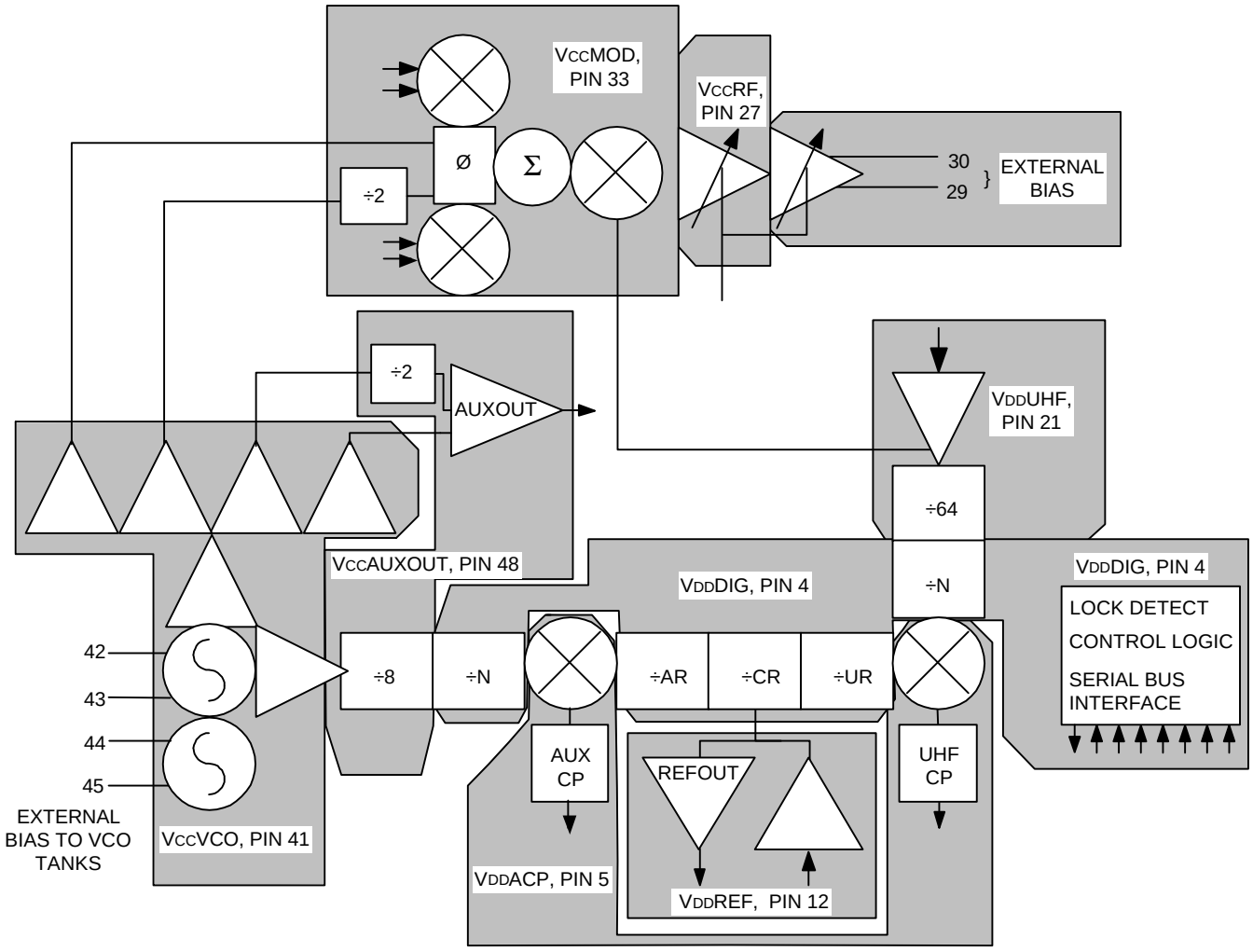


Figure 4. Power Supply Diagram

Electrical Characteristics

Conditions unless otherwise noted: RF_{OUT} frequency 889 MHz to 958 MHz; auxiliary VCO frequencies 80 MHz to 270 MHz; external UHFVCO frequency 670 MHz to 760 MHz; external VCXO/TCXO frequency 12 MHz to 17 MHz; UHFPLL phase detector comparison frequency 25 kHz; AUXPLL phase detector comparison frequency 100 kHz to 600 kHz; 2.7 Vdc ≤ V_{CC}RF, V_{CC}MOD, V_{DD}UHF ≤ 3.3 Vdc; 2.4 Vdc ≤ V_{DD}DIG ≤ 3.3 Vdc; 2.5 Vdc ≤ V_{DD}ACP ≤ 3.6 Vdc; 2.5 Vdc ≤ V_{DD}REF ≤ 3.3 Vdc; 2.55 Vdc ≤ V_{CC}VCO; V_{CC}AUXOUT ≤ 3.3 Vdc; –30 °C ≤ T_A ≤ +85 °C; $I - \overline{I} = 0.4 \cos(2\pi t \bullet 80\text{ kHz})$; $Q - \overline{Q} = 0.4 \cos(2\pi t \bullet 80\text{ kHz} - \pi/2)$; Vbias of I, $\overline{I}$, Q, and $\overline{Q}$ = 1.22 Vdc; APC = 2.7 Vdc.

Table 5. Digital Input Specifications

V_{DD} refers to the positive supply voltage applied to V_{DD}DIG, pin 4.

Parameter	Symbol	Min	Typ	Max	Unit
Logic High Voltage	V_{IH}	0.7 V_{DD}	—	V_{DD}	Vdc
Logic Low Voltage	V_{IL}	GND	—	0.3 V_{DD}	Vdc
Logic High Current (V_{IH} = 3.3 V)	I_{IH}	—	—	10	µA
Logic Low Current (V_{IL} = 0.4 V)	I_{IL}	—	—	10	µA

Table 6. Lock Detect Output Specifications

V_{DD} refers to the positive supply voltage applied to V_{DD}DIG, pin 4. (See also Table 41.)

Parameter	Symbol	Min	Typ	Max	Unit
Logic High Voltage (indicates both PLLs are locked or one is locked and the other off)	V_{OH}	V_{DD} – 0.4	—	—	Vdc
Logic Low Voltage (indicates one or both PLLs are out of lock or both PLLs are off)	V_{OL}	—	—	0.4	Vdc
Logic High Current (source) (V_{OH} > V_{DD} – 0.4 V)	$\lvert I_{OH} \rvert$	1.5	—	—	mA
Logic Low Current (sink) (V_{OL} < 0.4 V)	$\lvert I_{OL} \rvert$	1.5	—	—	mA

Table 7. Bias Enable Time

The following do not include PLL settling times, which are dependent on phase detector frequency, and design of the loop filters, which are external.

Parameter	Min	Typ	Max	Unit
Modulator				
Powerup/down (after LATCH goes high or TXON goes high)	—	—	8	µs
Auxiliary Synthesizer				
VCO Bias Enable Time (after LATCH goes high or AUXPLLON goes high)	—	—	5	µs
Main Synthesizer				
Bias Enable Time (after LATCH goes high or UHFPLLON goes high)	—	—	5	µs

Electrical Characteristics (continued)

Conditions unless otherwise noted: RF_{OUT} frequency 889 MHz to 958 MHz; auxiliary VCO frequencies 80 MHz to 270 MHz; external UHFVCO frequency 670 MHz to 760 MHz; external VCXO/TCXO frequency 12 MHz to 17 MHz; UHFPLL phase detector comparison frequency 25 Hz; AUXPLL phase detector comparison frequency 100 kHz to 600 kHz; 2.7 Vdc ≤ $V_{CC}RF$, $V_{CC}MOD$, $V_{DD}UHF$ ≤ 3.3 Vdc; 2.4 Vdc ≤ $V_{DD}DIG$ ≤ 3.3 Vdc; 2.5 Vdc ≤ $V_{DD}ACP$ ≤ 3.6 Vdc; 2.5 Vdc ≤ $V_{DD}REF$ ≤ 3.3 Vdc; 2.55 Vdc ≤ $V_{CC}VCO$, $V_{CC}AUXOUT$ ≤ 3.3 Vdc; –30 °C ≤ T_A ≤ +85 °C; $I - \overline{I} = 0.4 \cos(2\pi t \bullet 80\ kHz)$, $Q - \overline{Q} = 0.4 \cos(2\pi t \bullet 80\ kHz - \pi/2)$, Vbias of I, $\overline{I}$, Q, and $\overline{Q}$ = 1.22 Vdc; APC = 2.7 Vdc.

Table 8. Supply Currents

System Mode	Min	Typ	Max	Unit
Powerdown (sleep): $V_{UHFPLLON}$ = $V_{AUXPLLON}$ = V_{TXON} = 0.1	—	<1	10	µA
UHF PLL On; and Auxiliary PLL On, Auxiliary VCO On	—	7	—	mA
UHF PLL On; and Auxiliary VCO, PLL, and Output Buffer On	—	9	—	mA
Reference Output Buffer Only On	—	1.4	—	mA
Modulator Only On, APC = 1.8, (P_{OUT} = –1 dBm)	—	57	—	mA
Modulator Only On, APC Attenuation > 20 dB	—	48	—	mA
Transmit Mode, All Active, P_{OUT} = 0 dBm	—	64	—	mA
Transmit Mode, All Active, APC Attenuation > 20 dB	—	56	—	mA

Table 9. ac Specifications

Parameter	Symbol	Min	Typ	Max	Unit
Baseband Interface					
I & Q Signal Path –3 dB Bandwidth	—	6	8	10	MHz
I & Q Input Resistance	—	—	1	—	MΩ
I & Q Input Differential Signal for Max Envelope Output	—	—	1	—	Vp-p
Single Sideband RF Up-Conversion Mixer					
Unwanted Sideband Suppression	—	—	–30	—	dBc
RF Output					
Output Power, V_{APC} ≥ 2.4 Vdc, RF < 960 MHz, CW Sine Wave, I & Q 0.8 Vp-p Cos and Sine per Conditions	P_{USB}	3	—	—	dBm
Output Power, RF < 960 MHz, TXIF < 270 with AUX1 Register Programming, or TXIF < 190 with AUX2 Register Programming; DQPSK Modulation, α = 0.5, I & Q 1.05 Vp-p for PRBS Data; or 0.8 Vp-p for All Zeros Data:					
V_{APC} ≥ 2.4 Vdc	—	3	6	—	dBm
V_{APC} = 1.8 Vdc	—	–5	–1	—	dBm
Third-order Intermodulation Distortion [2-tone IM3 suppression: V(I) = V(Q) = 0.8 Vp-p; ϕ(I) = ϕ(Q); V_{APC} = 2.7 Vdc]	—	—	–30	—	dB

Electrical Characteristics (continued)

Conditions unless otherwise noted: RF_{OUT} frequency 889 MHz to 958 MHz; auxiliary VCO frequencies 80 MHz to 270 MHz; external UHFVCO frequency 670 MHz to 760 MHz; external VCXO/TCXO frequency 12 MHz to 17 MHz; UHFPLL phase detector comparison frequency 25 Hz; AUXPLL phase detector comparison frequency 100 kHz to 600 kHz; 2.7 Vdc ≤ $V_{CC}RF$, $V_{CC}MOD$, $V_{DD}UHF$ ≤ 3.3 Vdc; 2.4 Vdc ≤ $V_{DD}DIG$ ≤ 3.3 Vdc; 2.5 Vdc ≤ $V_{DD}ACP$ ≤ 3.6 Vdc; 2.5 Vdc ≤ $V_{DD}REF$ ≤ 3.3 Vdc; 2.55 Vdc ≤ $V_{CC}VCO$, $V_{CC}AUXOUT$ ≤ 3.3 Vdc; –30 °C ≤ T_A ≤ +85 °C; $I - \overline{I} = 0.4 \cos(2\pi t \bullet 80\ kHz)$, $Q - \overline{Q} = 0.4 \cos(2\pi t \bullet 80\ kHz - \pi/2)$, Vbias of I, $\overline{I}$, Q, and $\overline{Q}$ = 1.22 Vdc; APC = 2.7 Vdc.

Table 9. ac Specifications (continued)

Parameter	Symbol	Min	Typ	Max	Unit
Power Control (APC Function)					
Gross Power Control Range, from V_{APC} < 0.5 to V_{APC} > 2.4 Vdc	—	—	85	—	dB
Usable Power Control Range: Carrier Suppression < –25 dB USB; and Noise Floor at ±100 kHz ≤ –110 dBc/Hz with DQPSK Modulation (α = 0.5, PRBS data)	—	40	—	—	dB
APC Input Voltage for Minimum Output Power	—	—	0.1	0.5	Vdc
APC Transfer Function	—	—	25	—	mV/dB
Modulation Spectrum for PDC (DQPSK/α = 0.5, 42 kbits/s, 21 kHz Measurement BW)					
Suppression: 50 kHz, All Usable APC Levels 100 kHz, All Usable APC levels	 — —	 — —	 –64 –75	 –59 –65	 dBc dBc
In-band Spurious ± >100 kHz, Upper 20 dB of APC Range, 100 kHz Measurement BW (UHF VCO harmonic suppression < –30 dBc)	—	—	—	–63	dBc
In-band Spurious ± >100 kHz, 100 kHz Measurement BW (UHF VCO harmonic suppression < –30 dBc): $P_{OUT} = P_{MAX}$ – 20 dB $P_{OUT} = P_{MAX}$ – 35 dB	 — —	 — —	 — —	 –63 –48	 dBc dBc
UHF LO Suppression, 670 MHz to 760 MHz	—	—	–40	–30	dBc
LO1 Suppression (TXIF F_C, 60 MHz to 270 MHz, auxiliary VCO output buffer off)	—	—	–45	–35	dBc
Wideband Noise Floor, APC > 1.8 Vdc F_C ± >8 MHz	—	—	—	–136	dBc/Hz

Electrical Characteristics (continued)

Conditions unless otherwise noted: auxiliary VCO frequencies 80 MHz to 270 MHz; external UHFVCO frequency 670 MHz to 760 MHz; external VCXO/TCXO frequency 12 MHz to 17 MHz; UHFPLL phase detector comparison frequency 25 kHz; AUXPLL phase detector comparison frequency 100 kHz to 600 kHz; 2.4 Vdc ≤ V_{DD}DIG ≤ 3.3 Vdc; 2.5 Vdc ≤ V_{DD}ACP ≤ 3.6 Vdc; 2.5 Vdc ≤ V_{DD}REF ≤ 3.3 Vdc; 2.55 Vdc ≤ V_{CC}VCO; V_{CC}AUXOUT ≤ 3.3 Vdc; 2.7 Vdc ≤ V_{DD}UHF ≤ 3.3 Vdc; –20 °C ≤ T_A ≤ +85 °C.

Table 10. Auxiliary Synthesizer and Reference Output Buffer (REFCLKOUT) Specifications

Parameter	Symbol	Min	Typ	Max	Unit
Charge Pump Output Voltages	V_{CP}	<0.5	—	>V_{CC} – 0.5	Vdc
Charge Pump Output Peak Current	I_{CP}	0.56	0.7	0.84	mA
Charge Pump Output Leakage Current	—	—	0.1	—	nA
Charge Pump Static Source-to-Sink Current Ratio	I_{OUT}/I_{IN}	0.95	1.0	1.05	—
Phase Detector/Charge Pump Slope Variation, Relative to Average from –2π to +2π	—	0.85	1.0	1.15	—
AUXOUT Buffer Output Level (min load 300 Ω complex magnitude, f ≤ 200 MHz)	—	200	330	—	mVp-p
Auxiliary Reference Divider Ratio (includes shared divider of 2 to 15)	—	2	—	465	—
Auxiliary Main Divider Ratio (prescaler 7/8 is additional)	—	2	—	4095	—
Reference Buffer Output Level (min load 1000 Ω complex magnitude)	—	0.5	—	—	Vp-p
Phase Detector Max Functional Frequency (performance not specified)	—	10	—	—	MHz

Table 11. UHF Synthesizer Specifications

An external VCO must be provided.

Parameter	Symbol	Min	Typ	Max	Unit
UHF PLL Charge Pump Output Voltages	V_{CP}	<0.5	—	>V_{CC} – 0.5	Vdc
Charge Pump Output Peak Current	I_{CP}	1.6	2	2.4	mA
Charge Pump Leakage Current	—	—	0.1	—	nA
Charge Pump Static Source-to-Sink Current Ratio	I_{OUT}/I_{IN}	0.95	1.0	1.05	—
Phase Detector/Charge Pump Slope Variation, Relative to Average from –2π to +2π	—	0.85	1.0	1.15	—
UHF PLL Reference Divider Ratio (including shared divider of 2 to 15)	—	4	—	3825	—
UHF PLL Main Divider Ratio Range (64/65 prescaler additional)	—	2	—	2047	—
Phase Detector Max Functional Frequency (performance not specified)	—	10	—	—	MHz

Digital Control Programming

See the Serial Bus Programming section, Figure 5, and Table 16 for descriptions of the registers referred to in the tables below.

Binary Control Pin Truth Tables

Table 12. Subcircuit Effects

AUXSEL	UHFPLLON	AUXPLLON	TXON	State*
High (ASEL bit = 1)	X†	High (MOD0 bit = 1)	X	Auxiliary PLL on with frequency, phase detector polarity, divider, and destination as set in AUX1, USEC, and SPEC registers; TXIF low-pass filter –3 dB cutoff frequency 480 MHz (nominal).
Low (ASEL bit = X)	X	High (MOD0 bit = 1)	X	Auxiliary PLL on with frequency, phase detector polarity, postdivider, and destination as set in AUX2, USEC, and SPEC registers; TXIF low-pass filter –3 dB cutoff frequency 400 MHz (nominal).
High (ASEL bit = 0)	X	High (MOD0 bit = 1)	X	Auxiliary PLL on with frequency, phase detector polarity, divider, and destination as set in AUX2, USEC, and SPEC registers; TXIF low-pass filter –3 dB cutoff frequency 400 MHz (nominal).
X	X	Low (MOD0 bit = X)	X	Auxiliary PLL off.
X	Low (MOD1 bit = X)	X	X	UHF PLL off.
X	High (MOD1 bit = 1)	X	X	UHF PLL on as set in UPRI and USEC registers.
X	X	X	Low (MOD2 bit = X)	Modulator off.
X	X	X	High (MOD2 bit = 1)	Modulator and UHF input buffer on; auxiliary VCO and ÷1 or ÷2 path to modulator on as determined by AUXSEL pin/ASEL bit, per AMOD bits (USEC register) and TANK bits (AUX1 and AUX2 registers).

* See the Serial Bus Programming section, Figure 5, and Table 16 for descriptions of the registers referred to in this table.
† X designates “don’t care” bit.

Digital Control Programming (continued)

Binary Control Pin Truth Tables (continued)

Table 13. Application Utility

ASEL bit = 1, MOD[2:0] bits = 111.

AUXSEL	UHFPLLON	AUXPLLON	TXON	State*
Low	Low	Low	Low	Sleep mode, reference output buffer on if REFOUT bit (in SPEC register) is high.
Low	Low	Low	High	Modulator on, UHF input buffer on, with auxiliary VCO/buffers/divider/destination on per AMOD2[0:2] bits (USEC register); TANK2 bit (AUX2 register); a lab characterization mode.
Low	Low	High	Low	AUX PLL on, shared reference divider, PLL/divider/destination per AUX2 register, AMOD2[0:2] bits; a lab characterization mode.
Low	Low	High	High	Modulator, UHF input buffer, shared reference divider, AUX PLL on, with PLL/divider/destination per AUX2 register, AMOD2[0:2] bits; a lab characterization mode.
Low	High	Low	Low	UHF PLL on as programmed in UPRI and USEC registers, shared reference divider; stabilization of UHF PLL prior to TX or RX; RX mode where only UHFPLL is required.
Low	High	Low	High	UHF PLL on, modulator on, with auxiliary VCO/buffers/divider/destination on per AMOD2[0:2] bits, TANK2 bit (AUX2 register); a lab characterization mode.
Low	High	High	Low	Both auxiliary and UHF PLLs, shared reference divider on, with auxiliary PLL/divider/destination per AUX2 register, AMOD2[0:2] bits; PLL settling period just prior to TX or RX; or TDMA RX mode.
Low	High	High	High	Modulator and UHF PLL on, and auxiliary PLL in PLL/divider/destination on per TANK2 bit (AUX2 register) and AMOD2[0:2] bits (USEC register); PDC800 TX mode, with TXIF = 185 MHz.
High	Low	Low	Low	Sleep mode, reference output buffer on if REFOUT bit (in SPEC register) is high.
High	Low	Low	High	Modulator on, UHF input buffer on, with auxiliary VCO/buffers/divider/destination on per AMOD1[0:2] bits (USEC register), TANK1 bit (AUX1 register); a lab characterization mode.
High	Low	High	Low	AUX PLL on, shared reference divider, PLL/divider/destination per AUX1 register, AMOD1[0:2] bits.

* See the Serial Bus Programming section, Figure 5, and Table 16 for descriptions of the registers referred to in this table.

Digital Control Programming (continued)

Binary Control Pin Truth Tables (continued)

Table 13. Application Utility (continued)

ASEL bit = 1, MOD[2:0] bits = 111.

AUXSEL	UHFPLLON	AUXPLLON	TXON	State*
High	Low	High	High	Modulator, UHF input buffer, shared reference divider, auxiliary PLL on, with PLL/divider/destination per AUX1 register and AMOD1[0:2] bits (USEC register); a lab characterization mode.
High	High	Low	Low	UHF PLL on as programmed in UPRI and USEC registers, shared reference divider; stabilization of UHF PLL prior to TX or RX; RX mode with external PLL for IFLO, where both AUXSEL conditions are used for TX bands.
High	High	Low	High	Modulator and UHF PLL on, with auxiliary VCO/buffers/divider/destination on per AMOD1[0:2] bits; TANK1 bit (AUX1 register); a lab characterization mode.
High	High	High	Low	Both auxiliary and UHF PLLs, shared reference divider on, with auxiliary PLL/divider/destination per AUX1 register, AMOD1[0:2] bits; PLL settling period just prior to TX or RX; or TDMA RX mode.
High	High	High	High	Modulator and UHF PLL on, and auxiliary PLL on in PLL/divider/destination per AUX1 register, AMOD1[0:2] bits; PDC800 TX mode with TXIF = 260 MHz.

* See the Serial Bus Programming section, Figure 5, and Table 16 for descriptions of the registers referred to in this table.

Table 14. AUXSEL Pin and ASEL Bit Control Truth Table

The unused control should be left in a high (pin) or 1 (bit) state when the other is used as follows.

Note: This can be interpreted as AND = AUX1, NAND = AUX2.

AUXSEL Pin	ASEL Bit	State
High	1 (high)	AUX1, AMOD1[0:2] configuration invoked; TXIF filter bandwidth set 480 MHz typical.
Low	1 (high)	AUX2, AMOD2[0:2] configuration invoked; TXIF filter bandwidth set 400 MHz typical.
High	0 (low)	AUX2, AMOD2[0:2] configuration invoked; TXIF filter bandwidth set 400 MHz typical.
Low	0 (low)	AUX2, AMOD2[0:2] configuration invoked; TXIF filter bandwidth set 400 MHz typical.

* See the Serial Bus Programming section, Figure 5, and Table 16 for descriptions of the registers referred to in this table.

Serial Bus Programming

The W3015 settings are programmed using a standard 3-wire bus (CLOCK, DATA, LATCH). The LATCH line initiates download and execution of the current data word. The W3015 serial programming bus provides five 24-bit user registers and one test register for control of operating functions. These registers are selected using a 3-bit address word common to all addressed registers. The registers are the following:

- **UPRI:** UHF primary control register.
- **USEC:** UHF secondary and other control register.
- **AUX1:** Auxiliary PLL frequency 1 register. This register should be used for programming the auxiliary VCO used for transmit mode when TXIF is about 260 MHz. When TXIF is 260 MHz, the AUX2 register can be used for RX Mode (IFLO = 260 ÷ 2 = 130 MHz), controlling the same VCO used for TX mode.
- **AUX2:** Auxiliary PLL frequency 2 register. This register should be used for programming the Auxiliary VCO used for transmit mode when TXIF is about 185 MHz. When TXIF is 185 MHz, the AUX1 register can be used for RX mode (IFLO = 260 ÷ 2 = 130 MHz), controlling the VCO used for TXIF = 260 MHz.
- **SPEC:** Special/miscellaneous control register.
- **TEST:** For manufacturing use only (must be programmed with address A[0:2] = 101 and remaining 21 bits set to all zeros once at initialization after V_{DD} and V_{CC} are first applied).

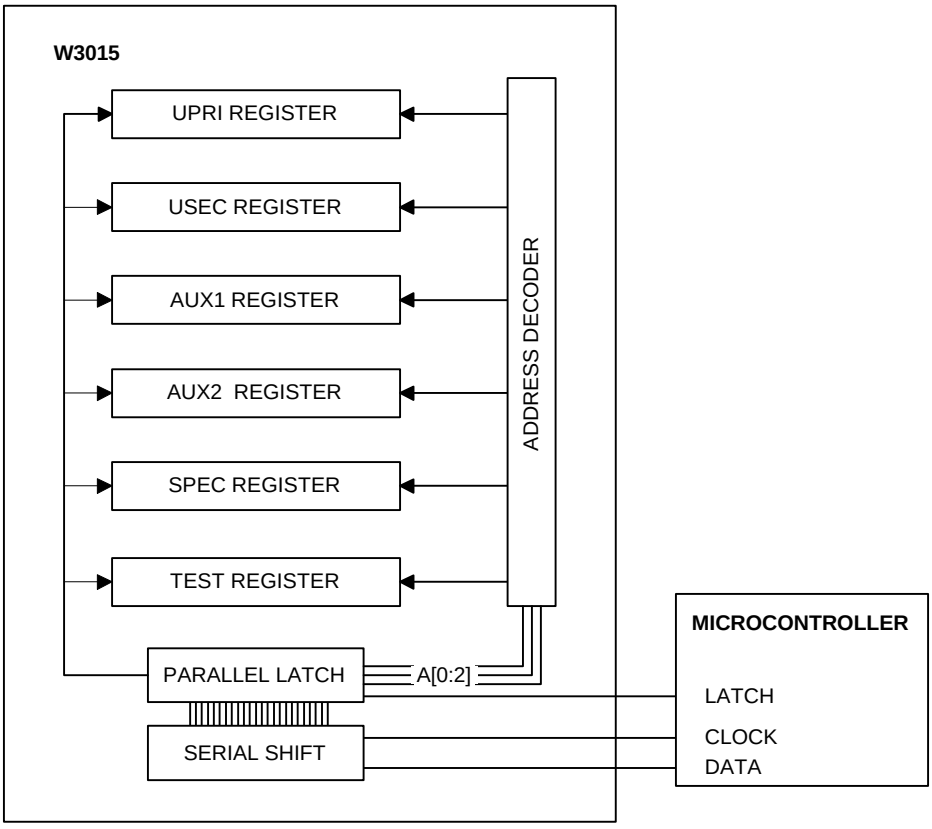


Figure 5. W3015 and Microcontroller Interconnection

Serial Bus Programming (continued)

Although there are two auxiliary registers, AUX1 and AUX2, there is only one set of auxiliary PLL counters. Two buffer registers hold two sets of counter values (AUX1 and AUX2) that are selected by either the AUXSEL device pin or the ASEL binary programming bit. Figure 6 illustrates the synthesizer programming logic, which will be explained in more detail in the Programming Examples section. Refer to Table 16 for the breakdown of registers into bit sequences.

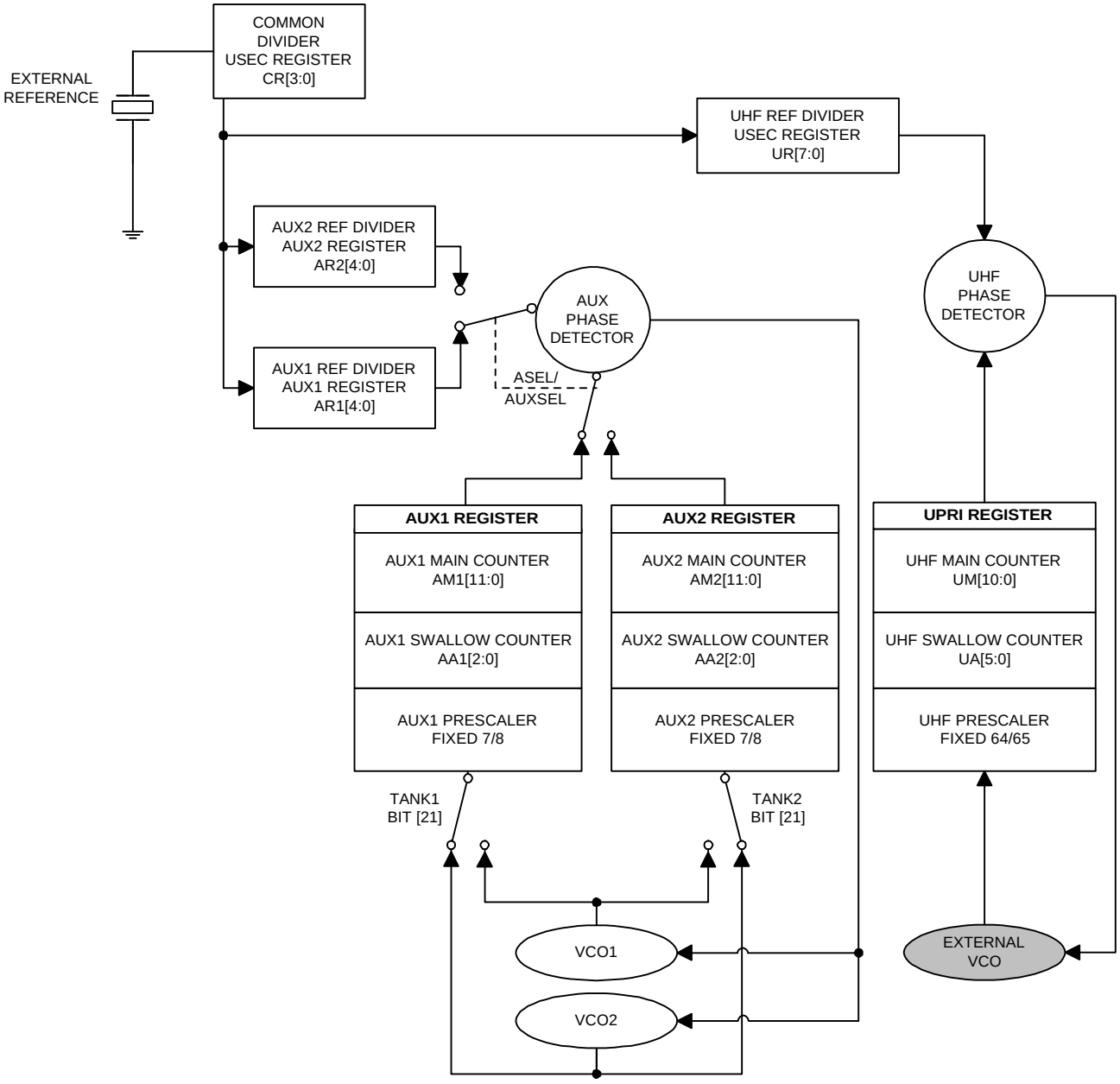


Figure 6. Synthesizer Programming Diagram

Serial Bus Programming (continued)

Serial Control Bus Timing

The control registers are loaded from a standard 3-wire serial bus, the lines of which are labeled CLOCK, DATA, and LATCH. The serial bus timing diagram can be seen below. Operation is such that when LATCH is low, as in LATCH (a) or LATCH (b), bits on the DATA line are toggled into a serial shift register at a rate established by pulses on the CLOCK line. The end of the serial input word is established when the LATCH line transitions from low to high while the CLOCK line is low. This LATCH transition also initiates download of the serial shift input register to one of six operating registers, as determined by the three ADR (address) bits. The ADR bit positions are common to all registers, and the ADR bit values are the unique identifier of each register. Table 15 provides minimum pulse duration requirements (note the timing table corresponds to the maximum specified serial CLOCK frequency, 15 MHz).

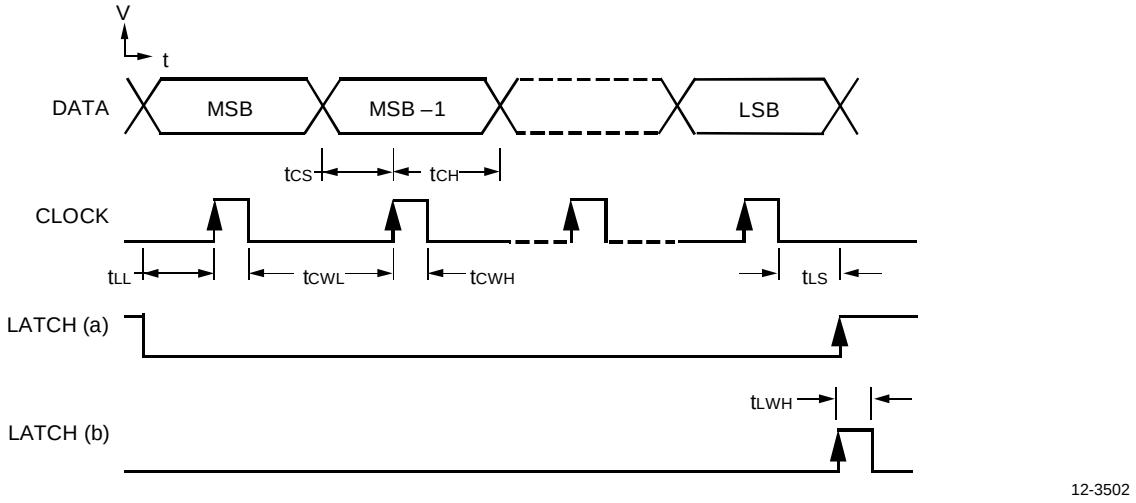


Figure 7. Serial Bus Timing Diagram

Table 15. Serial Bus Timing Information

Symbol	Parameter	Min	Typ	Max	Unit
t_{CS}	Data to Clock Setup Time	33	—	—	ns
t_{CH}	Data to Clock Hold Time	10	—	—	ns
t_{CWH}	Clock Pulse Width High	33	—	—	ns
t_{CWL}	Clock Pulse Width Low	33	—	—	ns
t_{LS}	Clock Falling Edge to Latch Setup Time	0	—	—	ns
t_{LWH}	Latch Pulse Width	50	—	—	ns
t_{LL}	Delay from Latch-low to First Clock Pulse	33	—	—	ns

Serial Bus Programming (continued)

Serial Input Registers

The user registers and their content words are described below in detail. For explanations of the pin settings referenced in the following tables, see the Digital Control Programming section.

Table 16. Serial Input Registers

Bit	Serial Input Register					
	UPRI	USEC	AUX1	AUX2	SPEC	TEST
24	ADR0 = 0	ADR0 = 1	ADR0 = 0	ADR0 = 1	ADR0 = 0	ADR0 = 1
23	ADR1 = 0	ADR1 = 0	ADR1 = 1	ADR1 = 1	ADR1 = 0	ADR1 = 0
22	ADR2 = 0	ADR2 = 0	ADR2 = 0	ADR2 = 0	ADR2 = 1	ADR2 = 1
21	MOD0	X*	TANK1	TANK2	LD0	0
20	MOD1	IMAGE	AM1[0]	AM2[0]	LD1	0
19	MOD2	PDU	AM1[1]	AM2[1]	CPU	0
18	ASEL	AMOD1[0]	AM1[2]	AM2[2]	CPA	0
17	UM0	AMOD1[1]	AM1[3]	AM2[3]	PDA1	0
16	UM1	AMOD1[2]	AM1[4]	AM2[4]	PDA2	0
15	UM2	AMOD2[0]	AM1[5]	AM2[5]	REFOUT	0
14	UM3	AMOD2[1]	AM1[6]	AM2[6]	ASYNC	0
13	UM4	AMOD2[2]	AM1[7]	AM2[7]	X	0
12	UM5	UR0	AM1[8]	AM2[8]	X	0
11	UM6	UR1	AM1[9]	AM2[9]	X	0
10	UM7	UR2	AM1[10]	AM2[10]	X	0
9	UM8	UR3	AM1[11]	AM2[11]	X	0
8	UM9	UR4	AA1[0]	AA2[0]	X	0
7	UM10	UR5	AA1[1]	AA2[1]	X	0
6	UA0	UR6	AA1[2]	AA2[2]	X	0
5	UA1	UR7	AR1[0]	AR2[0]	X	0
4	UA2	CR0	AR1[1]	AR2[1]	X	0
3	UA3	CR1	AR1[2]	AR2[2]	X	0
2	UA4	CR2	AR1[3]	AR2[3]	X	0
1	UA5	CR3	AR1[4]	AR2[4]	X	0

***** X designates “don’t care” bit.

Table 17. ADR[2:0] Register Contents: Register Address

These bits identify the destination register for a 24-bit serial-control word originating from the serial-control bus DATA line.

ADR2 Bit 22	ADR1 Bit 23	ADR0 Bit 24	Register
0	0	0	UPRI
0	0	1	UPSEC
0	1	0	AUX1
0	1	1	AUX2
1	0	0	SPEC
1	0	1	TEST
1	1	0	Not allowed
1	1	1	Not allowed

Serial Bus Programming (continued)

UPRI Register

Table 18. UPRI Register

Bit No.	Bit Name	Function
24	ADR0 = 0	Address bits
23	ADR1 = 0	
22	ADR2 = 0	
21	MOD0	Mode control
20	MOD1	
19	MOD2	
18	ASEL	Auxiliary synthesizer select
17:7	UM[0:10]	UHF PLL main divider
6:1	UA[0:5]	UHF PLL swallow counter

Table 19. MOD[2:0]: Mode Control

These bits establish the combinations of major sections operating simultaneously and offer redundant, but interdependent, functionality to the external binary control pins. See Table 12 for a description of how the MOD bits interact with binary control pins on an AND/NAND basis. For the purpose of this table, the external binary control pins TXON, UHFPLLON, and AUXPLLON are all assumed to be at logic high.

MOD2 Bit 19	MOD1 Bit 20	MOD0 Bit 21	Function
0	0	0	All sleep (powerdown), except reference output buffer on if REF bit in SPEC register is high.
X*	X	1	Auxiliary PLL, reference buffers, shared reference divider, VCO, VCO dividers and auxiliary output buffer only active; corresponds to AUXPLLON binary pin at logic high.
X	1	X	UHF PLL and reference buffers and shared reference dividers only active; corresponds to UHFPLLON binary pin at logic high.
1	X	X	Modulator, auxiliary VCO, and auxiliary path to modulator as defined by AMOD and TANK bits and selected by AUXSEL/ASEL; UHF input buffer active; corresponds to TXON binary pin at logic high.
1	1	1	Modulator and both PLLs (all circuits) active.

***** X designates “don’t care” bit.

Serial Bus Programming (continued)

UPRI Register (continued)

Table 20. ASEL: Auxiliary VCO Select

The AUXSEL pin must be fixed high for this bit to be active.

ASEL Bit 18	Function
1	AUX1 program active
0	AUX2 program active

Table 21. UM[10:0]: UHF PLL Main Divider

UM10 Bit 7	UM9 Bit 8	UM8 Bit 9	UM7 Bit 10	UM6 Bit 11	UM5 Bit 12	UM4 Bit 13	UM3 Bit 14	UM2 Bit 15	UM1 Bit 16	UM0 Bit 17	Divide Ratio
0	0	0	0	0	0	0	0	0	0	0	Not allowed
0	0	0	0	0	0	0	0	0	0	1	Not allowed
0	0	0	0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	0	0	0	1	1	3
.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	1	1	1	1	2047

Table 22. UA[5:0]: UHF PLL Swallow Counter

UA5 Bit 1	UA4 Bit 2	UA3 Bit 3	UA2 Bit 4	UA1 Bit 5	UA0 Bit 6	Count
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
0	0	0	0	1	1	3
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
1	1	1	1	1	1	63

Serial Bus Programming (continued)

USEC Register

Table 23. USEC Register

Bit No.	Bit Name	Function
24 23 22	ADR0 = 1 ADR1 = 0 ADR2 = 0	Address bits
21	X	Reserved
20	IMAGE	Single-sideband RF mixer image select
19	PDU	UHF phase detector polarity
18:16	AMOD1[0:2]	Auxiliary 1 PLL configuration
15:13	AMOD2[0:2]	Auxiliary 2 PLL configuration
12:5	UR[0:7]	UHF PLL reference divider
4:1	CR[0:3]	Common reference divider

Table 24. IMAGE: Single-Sideband RF Mixer Image Select

This bit controls whether the RF up-conversion mixer high-side (sum) product, f(AUX) + f(UHF), or low-side (difference) product f(UHF) – f(AUX) is transmitted. The other product will be suppressed as described in Table 8.

IMAGE Bit 20	Function
1	Low-frequency (difference) product transmitted
0	High-frequency (sum) product transmitted

Table 25. PDU: UHF Phase Detector Polarity

The UHF phase detector can be programmed for either negative or positive slope to accommodate the VCO and loop filter characteristics. (See Figure 8.)

PDU Bit 19	Function
0	PLL negative polarity
1	PLL positive polarity

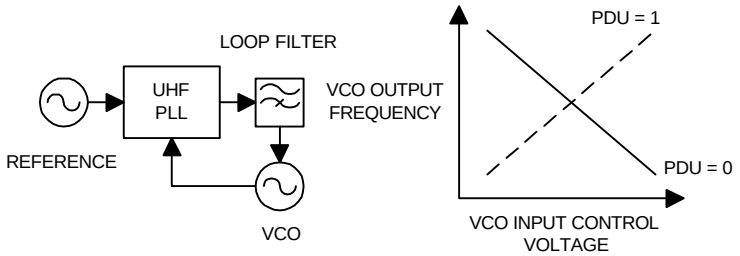


Figure 8. Programming the UHF Phase Detector Slope

Serial Bus Programming (continued)

USEC Register (continued)

Auxiliary PLL Configuration (AUXSEL Pin or ASEL Bit Setup Definition, AMOD1[2:0] and AMOD2[2:0])

There are two 3-bit AMOD codes in the UHF secondary (USEC) control register. These bits are pointers for either the ASEL bit or the AUXSEL pin to select the auxiliary PLL conditions in the AUX1 or AUX2 register, as well as definition of the programmable dividers feeding the modulator and the programmable dividers driving the AUX output buffer. Either the path to the modulator only with the output buffer off, the path to the AUX output buffer only, or both, may be enabled with any combination of ÷1 or ÷2 division of the VCO frequency to either destination.

Table 26. AMOD1[2:0]: AUX1 PLL Configuration, Bits 16 to 18

AMOD1[2] Bit 16	AMOD1[1] Bit 17	AMOD1[0] Bit 18	Function
0	0	0	AUX1 VCO frequency to divide by 1 to modulator only, output buffer off
0	0	1	AUX1 VCO frequency to divide by 1 to output buffer only, modulator off
0	1	0	AUX1 VCO frequency to divide by 1 to both modulator and output buffer
0	1	1	AUX1 VCO frequency to divide by 2 to modulator only, output buffer off
1	0	0	AUX1 VCO frequency to divide by 2 to output buffer only, modulator off
1	0	1	AUX1 VCO frequency to divide by 2 to both modulator and output buffer
1	1	0	AUX1 VCO frequency to divide by 1 to modulator and divide by 2 to output buffer
1	1	1	AUX1 VCO frequency to divide by 2 to modulator and divide by 1 to output buffer

Table 27. AMOD2[2:0]: AUX2 PLL Configuration, Bits 13 to 15

AMOD2[2] Bit 13	AMOD2[1] Bit 14	AMOD2[0] Bit 15	Function
0	0	0	AUX2 VCO frequency to divide by 1 to modulator only, output buffer off
0	0	1	AUX2 VCO frequency to divide by 1 to output buffer only, modulator off
0	1	0	AUX2 VCO frequency to divide by 1 to both modulator and output buffer
0	1	1	AUX2 VCO frequency to divide by 2 to modulator only, output buffer off
1	0	0	AUX2 VCO frequency to divide by 2 to output buffer only, modulator off
1	0	1	AUX2 VCO frequency to divide by 2 to both modulator and output buffer
1	1	0	AUX2 VCO frequency to divide by 1 to modulator and divide by 2 to output buffer
1	1	1	AUX2 VCO frequency to divide by 2 to modulator and divide by 1 to output buffer

Serial Bus Programming (continued)

USEC Register (continued)

Table 28. UR[7:0]: UHF PLL Reference Divider

The UHF reference divider is driven by the output of the CR reference divider. The UHF reference divider output frequency is the reference input to the UHF phase detector.

UR7 Bit 5	UR6 Bit 6	UR5 Bit 7	UR4 Bit 8	UR3 Bit 9	UR2 Bit 10	UR1 Bit 11	UR0 Bit 12	Divide Ratio
0	0	0	0	0	0	0	0	Not allowed
0	0	0	0	0	0	0	1	Not allowed
0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	1	1	3
. . . .	. . . .	. . . .	. . . .	. . . .	. . . .	. . . .	. . . .	. . . .
1	1	1	1	1	1	1	1	255

Table 29. CR[3:0]: Common (Shared) Reference Divider

This divider is shared between the UHF and auxiliary PLLs. The frequency plan must be designed to allow this divisor value to be the same for both PLLs, if both are to operate simultaneously. The input signal to this divider is the crystal-reference clock oscillator (VCXO or TCXO). The output signal is fed in parallel to the inputs of both the AR auxiliary reference divider and to the UR UHF reference divider.

CR3 Bit 1	CR2 Bit 2	CR1 Bit 3	CR0 Bit 4	Divide Ratio
0	0	0	0	Not allowed
0	0	0	1	Not allowed
0	0	1	0	2
0	0	1	1	3
. . . .	. . . .	. . . .	. . . .	. . . .
1	1	1	1	15

Serial Bus Programming (continued)

AUX1 Register

Table 30. AUX1 Register

Bit No.	Bit Name	Function
24 23 22	ADR0 = 0 ADR1 = 1 ADR2 = 0	Address bits
21	TANK1	Auxiliary VCO select
20:9	AM1[0:11]	Auxiliary 1 main divider
8:6	AA1[0:2]	Auxiliary 1 swallow counter
5:1	AR1[0:4]	Auxiliary 1 reference divider

Table 31. TANK1: Auxiliary VCO Select

This bit specifies which auxiliary VCO is connected to the auxiliary PLL for the Auxiliary 1 program. Note that either VCO1 (pins 44 and 45) or VCO2 (pins 42 and 43) may be selected by the AUX1 register.

TANK1 Bit 21	Function
0	VCO1 enabled
1	VCO2 enabled

Table 32. AM[11:0]: Auxiliary PLL Main Divider (AUX1 Register)

AM1[11] Bit 9	AM1[10] Bit 10	AM1[9] Bit 11	AM1[8] Bit 12	AM1[7] Bit 13	AM1[6] Bit 14	AM1[5] Bit 15	AM1[4] Bit 16	AM1[3] Bit 17	AM1[2] Bit 18	AM1[1] Bit 19	AM1[0] Bit 20	Divide Ratio
0	0	0	0	0	0	0	0	0	0	0	0	Not allowed
0	0	0	0	0	0	0	0	0	0	0	1	Not allowed
0	0	0	0	0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	0	0	0	0	1	1	3
. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
1	1	1	1	1	1	1	1	1	1	1	1	4095

Serial Bus Programming (continued)

AUX1 Register (continued)

Table 33. AA1[2:0]: Auxiliary PLL Swallow Counter

AA1[2] Bit 6	AA1[1] Bit 7	AA1[0] Bit 8	Count
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
. . .	. . .	. . .	. . .
1	1	1	7

Register Contents: Reference Dividers

Table 34. AR1[4:0]: Auxiliary PLL Reference Divider

This divider is driven by the output of the CR (shared) reference divider. The output frequency of the auxiliary PLL reference divider is the reference input to the auxiliary phase detector.

AR1[4] Bit 1	AR1[3] Bit 2	AR1[2] Bit 3	AR1[1] Bit 4	AR1[0] Bit 5	Divide Ratio
0	0	0	0	0	Not allowed
0	0	0	0	1	1
0	0	0	1	0	2
0	0	0	1	1	3
. . .	. . .	. . .	. . .	. . .	. . .
1	1	1	1	1	31

Serial Bus Programming (continued)

AUX2 Register

Table 35. AUX2 Register

Bit No.	Bit Name	Function
24 23 22	ADR0 = 1 ADR1 = 1 ADR2 = 0	Address bits
21	TANK2	Auxiliary VCO select
20:9	AM2[0:11]	Auxiliary 2 main counter
8:6	AA2[0:2]	Auxiliary 2 swallow counter
5:1	AR2[0:4]	Auxiliary 2 reference divider

Table 36. TANK2: Auxiliary VCO Select

This bit specifies which auxiliary VCO is connected to the auxiliary PLL for the Auxiliary 2 program. Note that either VCO1 (pins 44 and 45) or VCO2 (pins 42 and 43) may be selected by the AUX2 register.

TANK2 Bit 21	Function
0	VCO1 enabled
1	VCO2 enabled

Table 37. AM2[11:0]: Auxiliary PLL Main Divider (AUX2 Register)

There are two of these codes, one in each of two auxiliary control registers (auxiliary frequency 1 and auxiliary frequency 2).

AM2[11] Bit 9	AM2[10] Bit 10	AM2[9] Bit 11	AM2[8] Bit 12	AM2[7] Bit 13	AM2[6] Bit 14	AM2[5] Bit 15	AM2[4] Bit 16	AM2[3] Bit 17	AM2[2] Bit 18	AM2[1] Bit 19	AM2[0] Bit 20	Divide Ratio
0	0	0	0	0	0	0	0	0	0	0	0	Not allowed
0	0	0	0	0	0	0	0	0	0	0	1	Not allowed
0	0	0	0	0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	0	0	0	0	1	1	3
. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
1	1	1	1	1	1	1	1	1	1	1	1	4095

Serial Bus Programming (continued)

AUX2 Register (continued)

Table 38. AA2[2:0]: Auxiliary PLL Swallow Counter

AA2[2] Bit 6	AA2[1] Bit 7	AA2[0] Bit 8	Count
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
. . .	. . .	. . .	. . .
1	1	1	7

Register Contents: Reference Dividers

Table 39. AR2[4:0]: Auxiliary PLL Reference Divider

This divider is driven by the output of the CR reference divider. The output frequency of this divider is the reference input to the auxiliary phase detector.

AR2[4] Bit 1	AR2[3] Bit 2	AR2[2] Bit 3	AR2[1] Bit 4	AR2[0] Bit 5	Divide Ratio
0	0	0	0	0	Not allowed
0	0	0	0	1	1
0	0	0	1	0	2
0	0	0	1	1	3
. . .	. . .	. . .	. . .	. . .	. . .
1	1	1	1	1	31

Serial Bus Programming (continued)

SPEC Register

Table 40. SPEC Register

Bit No.	Bit Name	Function
24 23 22	ADR0 = 0 ADR1 = 0 ADR2 = 1	Address bits
21 20	LD0 LD1	Lock detect enable
19	CPU	UHF charge pump control
18	CPA	Auxiliary charge pump control
17	PDA1	Auxiliary 1 phase detector polarity
16	PDA2	Auxiliary 2 phase detector polarity
15	REFOUT	Reference output enable
14	ASYNC	Counter reload
13:1	—	Reserved

Table 41. Lock Detect (LD[1:0])

Lock detect function is ANDed with the corresponding PLLON pins and MOD bits, such that the lock detect indicates status of either or both PLLs only if either or both is active.

LD1 Bit 20	LD0 Bit 21	AUXPLL State	UHFPLL State	Lock Detect Logic Output
0	0	X	X	Low (output disabled)
0	1	Locked	X	High
0	1	Out of Lock	X	Low
1	0	X	Locked	High
1	0	X	Out of Lock	Low
1	1	Locked	Locked	High
1	1	Out of Lock	Locked	Low
1	1	Locked	Out of Lock	Low
1	1	Out of Lock	Out of Lock	Low

Table 42. CPU: UHF Charge Pump Control

CPU Bit 19	Function
0	UHF CP normal operation
1	UHF CP Off (high-Z)

Table 43. CPA: Auxiliary Charge Pump Control

CPA Bit 18	Function
0	Auxiliary CP normal operation
1	Auxiliary CP off (high-Z)

Serial Bus Programming (continued)

SPEC Register (continued)

Table 44. PDA1: Auxiliary 1 Phase Detector Polarity (See Figure 9.)

PDA1 Bit 17	Function
0	Negative polarity
1	Positive polarity

Table 45. PDA2: Auxiliary 2 Phase Detector Polarity (See Figure 9.)

PDA2 Bit 16	Function
0	Negative polarity
1	Positive polarity

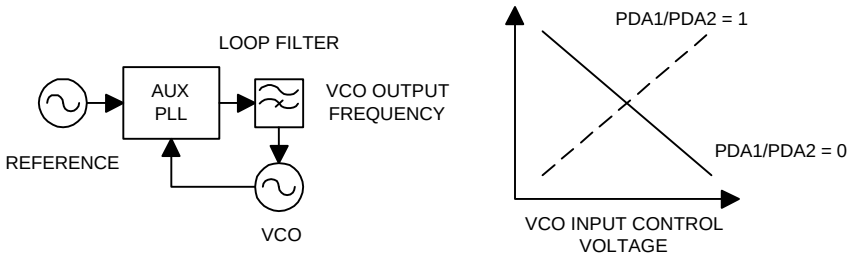


Figure 9. Programming the Auxiliary Phase Detector Slope

Table 46. REFOUT: Reference Output Buffer On/Off

This enables the reference output buffer independent of other MOD bits or enable pin controls.

REFOUT Bit 15	Function
0	Reference output buffer off
1	Reference output buffer on

Table 47. ASYNC: Synchronous or Forced Reload

ASYNC Bit 14	Function
0	Synchronous reload (preferred)
1	Forced reload

Serial Bus Programming (continued)

Test Register

The programmer must write zeros to this register at initialization.

Synthesizers

The W3015 synthesizers interface directly to an off-the-shelf reference module (VCXO/TCXO). The reference signal passes through a divider, CR, which is programmable from 2 to 15 and whose output is shared by both the UHF and auxiliary synthesizers.

Programming Examples

UHF Synthesizer

The main input, from an external UHF VCO, passes through a dual-modulus prescaler. The prescaler output signal drives a programmable main divider (UM) that divides the signal to the comparison frequency. A swallow counter (UA), in parallel with UM, also counts on the prescaler output signal and toggles the modulus control line of the prescaler. The UHF synthesizer also includes a reference divider (UR). Selection of the oscillator frequency is according to the following expression:

$$f_{VCO} = \frac{[(P * UM) + UA] * f_{REF}}{CR * UR}$$

f_{VCO}: UHF VCO frequency

fcomp: Phase detector comparison frequency

P/(P + 1): Dual modulus prescaler (64/65)

UM: Programmable divider (2 to 2047), UM > UA

UA: Swallow counter (0 to 63), UA < UM

f_{REF}: External reference oscillator frequency

UR: Reference divider (2 to 255)

CR: Common (shared) reference divider (2 to 15)

where:

$$fcomp = \frac{f_{REF}}{(CR * UR)} \qquad N = \frac{f_{VCO}}{fcomp}$$

UM = N\P (integer division) UA = N mod P (modulus division)

Example:

f_{VCO} = 960 MHz

fcomp = 30 kHz

f_{REF} = 19.44 MHz

If we choose a common reference (CR) division by 9, we calculate:

$$UR = \frac{f_{REF}}{CR * fcomp} = \frac{19.44\ MHz}{9 * 0.03\ MHz} = 72$$

$$N = \frac{960\ MHz}{0.03\ MHz} = 32000$$

$$UM = \frac{32000}{64} = 500$$

UA = 3200 mod 64 = 0

The CR count of 9 and the UR count of 72 are loaded into the USEC register as illustrated below:

Last bit in serial sequence First bit in serial sequence

Bit #	1	2	3	4	5	6	7	8	9	10	11	12	22	23	24
Bit	CR3	CR2	CR1	CR0	UR7	UR6	UR5	UR4	UR3	UR2	UR1	UR0	ADR2	ADR1	ADR0
Value	1	0	0	1	0	1	0	0	1	0	0	0	0	0	1

Programming Examples (continued)

UHF Synthesizer (continued)

The UM count of 500 and the UA count of 0 are loaded into the UPRI register as illustrated below:

Bit #	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	22	23	23
Bit	UA5	UA4	UA3	UA2	UA1	UA0	UM10	UM9	UM8	UM7	UM6	UM5	UM4	UM3	UM2	UM1	UM0	ADR2	ADR1	ADR0
Value	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0	0	0

Auxiliary Synthesizer

The auxiliary PLL has the appearance of two independent synthesizers: Auxiliary 1 and Auxiliary 2. The AUX1 group contains the main divider (AM1), the swallow counter (AA1), and a reference divider (AR1). The AUX2 group contains the main divider (AM2), the swallow counter (AA2), and a reference divider (AR2). Although there are two sets of control registers, there is only one set of counters, one phase detector, and one charge pump; therefore, only AUX1 or AUX2 will be operating at a time. AUX1 or AUX2 can be quickly selected by an external logic pin (AUXSEL) or a binary programming bit (ASEL).

The auxiliary PLL also contains two internal VCOs: VCO1 and VCO2. The VCO operating with AUX1 and AUX2 is preselected by a binary bit labeled TANK. AUX1 and AUX2 have their own TANK bits, TANK1 and TANK2, respectively. AUX1 may be programmed to operate with either VCO1 or VCO2; likewise, AUX2 may use either VCO1 or VCO2. Selection of the oscillator frequency is according to the following expression:

$$f_{VCO} = \frac{\left[(P * AM) - AA\right] * f_{REF}}{CR * AR}$$

f_{VCO}: Auxiliary VCO frequency

fcomp: Phase detector comparison frequency

P/(P – 1): Dual modulus prescaler (8/7)

AM: Programmable divider (2 to 4095), AM > AA

AA: Swallow counter (0 to 7), AA < AM

f_{REF}: External reference oscillator frequency

AR: Reference divider (2 to 255)

CR: Common (shared) reference divider (2 to 15)

where:

$$fcomp = \frac{f_{REF}}{(CR * AR)} \qquad N = \frac{f_{VCO}}{fcomp}$$

AM = N\P (integer division) AA = N mod P (modulus division)

If AA = 0, then:

AM = N\P (integer division)

AA = N mod P (modulus division)

If AA ≠ 0, then:

AM = (N\P) + 1 (integer division)

AA = P – (N mod P) (modulus division)

Programming Examples (continued)

Auxiliary Synthesizer (continued)

Example for AA = 0:

External tank 1

f_{VCO} = 134.4 MHz

fcomp = 240 kHz

f_{REF} = 19.44 MHz

If we choose a common reference (CR) division by 9, we calculate:

$$AR = \frac{f_{REF}}{CR * fcomp} = \frac{19.44\ MHz}{9 * 0.240\ MHz} = 9 \qquad N = \frac{134.4\ MHz}{0.24\ MHz} = 560$$

$$AM = \frac{560}{8} = 70 \qquad AA = 560 \bmod 8 = 0$$

The AR count of 9, the AM count of 70, and the AA count of 0 are loaded into the AUX1 register as illustrated:

Bit #	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
Bit	AR[2]	AR[1]	AR[2]	AR[1]	AR[0]	AA[2]	AA[1]	AA[0]	AM[11]	AM[10]	AM[9]	AM[8]	AM[7]	AM[6]	AM[5]	AM[4]	AM[3]	AM[2]	AM[1]	AM[0]	TANK	ADR2	ADR1	ADR0
Value	0	1	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0	0	1	0

Example for AA ≠ 0:

External tank 2

f_{VCO} = 134.64 MHz

fcomp = 240 kHz

f_{REF} = 19.44 MHz

If we choose a common reference (CR) division by 9, we calculate:

$$AR = \frac{f_{REF}}{CR * fcomp} = \frac{19.44\ MHz}{9 * 0.240\ MHz} = 9 \qquad N = \frac{134.64\ MHz}{0.24\ MHz} = 561$$

$$AM = \frac{561}{8} = 70 \qquad AA = 561 \bmod 8 = 1$$

AA ≠ 0;

Therefore:

$$AM = \left(\frac{561}{8}\right) + 1 = 71$$

AA = 8 – (561 mod 8) = 7

The AR count of 9, the AM count of 71, and the AA count of 7 are loaded into the AUX1 register as illustrated:

Bit #	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
Bit	AR[2]	AR[1]	AR[2]	AR[1]	AR[0]	AA[2]	AA[1]	AA[0]	AM[11]	AM[10]	AM[9]	AM[8]	AM[7]	AM[6]	AM[5]	AM[4]	AM[3]	AM[2]	AM[1]	AM[0]	TANK	ADR2	ADR1	ADR0
Value	0	1	0	0	1	1	1	1	0	0	0	0	0	1	0	0	0	1	1	1	1	0	1	0

Characteristic Curves

Conditions unless otherwise specified: $V_{DD} = V_{CC} = 2.7$; $T_A = 25$ °C; $I - \overline{I} = 1.4 + 0.5 \cos(2\pi t\ 80\ kHz)$; $Q - \overline{Q} = 1.4 + 0.5 \cos(2\pi t\ 80\ kHz - \pi/2)$; $V_{APC} = V_{CC}$; TXIF = 130 MHz; UHFLO = 1000 MHz; RF = 870 MHz.

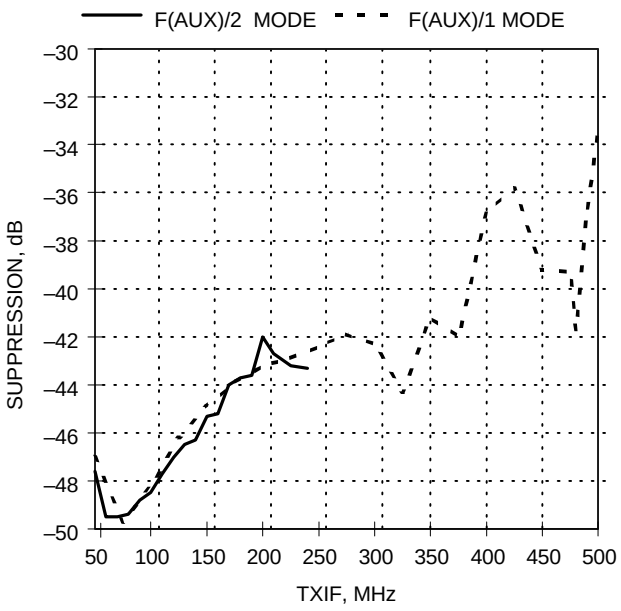


Figure 10. I/Q Modulator Unwanted Sideband Suppression vs. TXIF

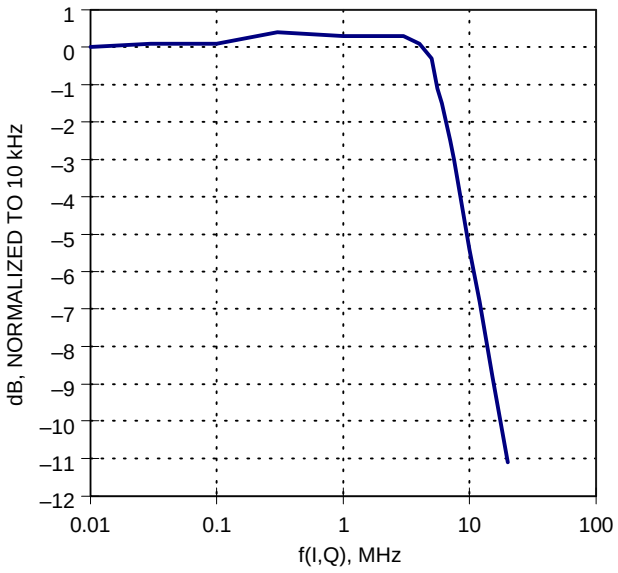


Figure 11. I/Q Input Bandwidth

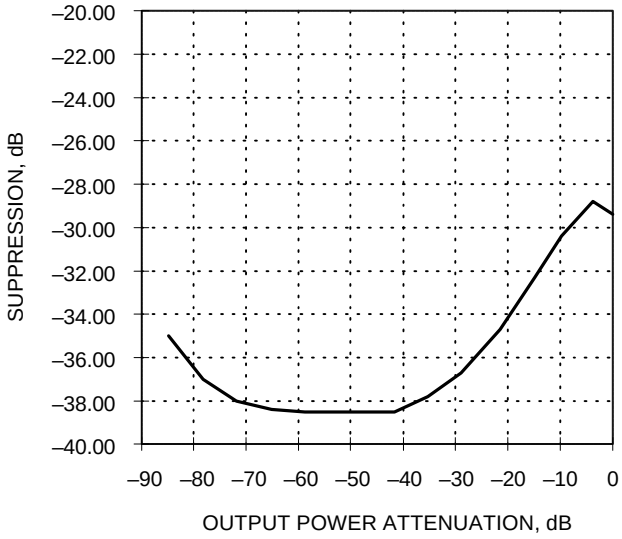


Figure 12. Carrier Suppression vs. Output Attenuation

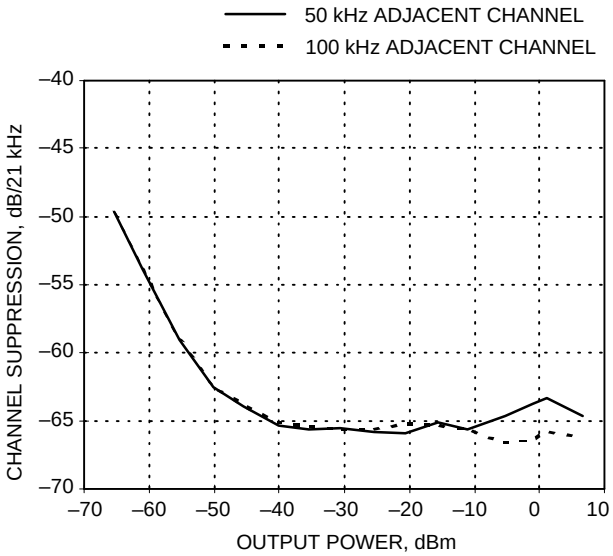
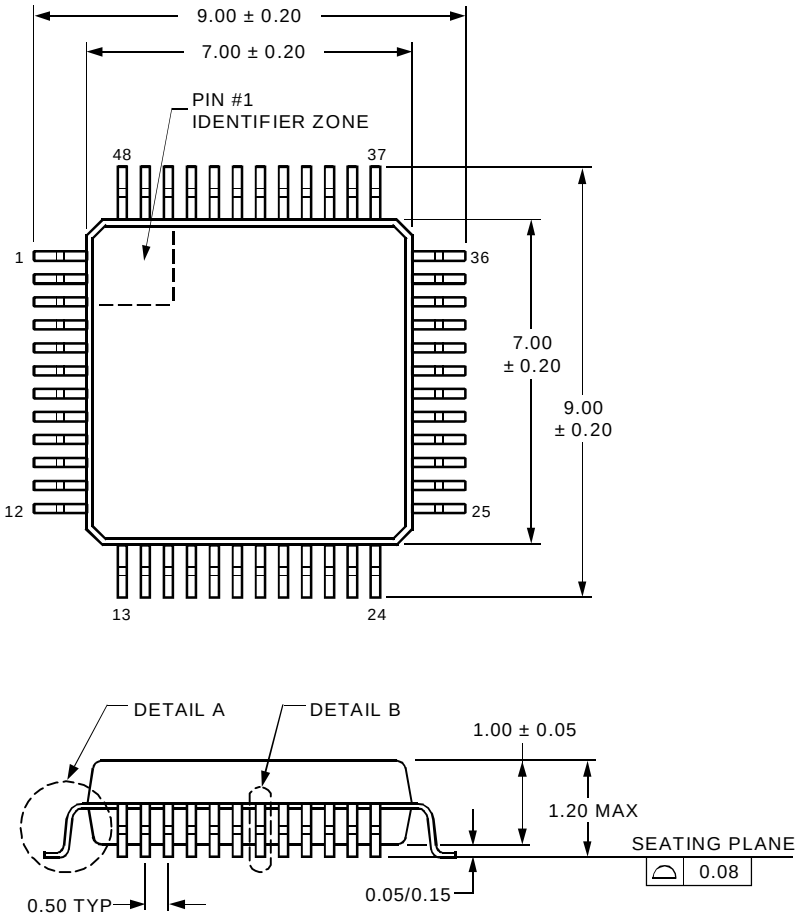


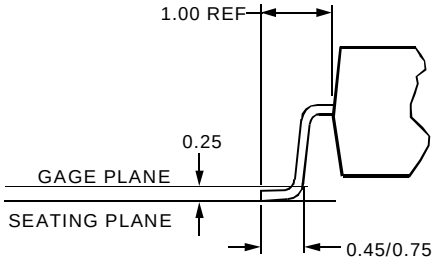
Figure 13. PDC (RCR STD-27) Adjacent Channel Suppression

Outline Diagram

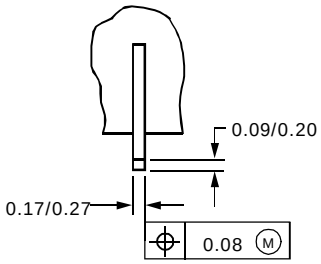
48-Pin TQFPT

All dimensions are in millimeters.





DETAIL A



DETAIL B

5-2363 a

Manufacturing Information

This device will be assembled in one of the following locations: assembly codes K or M.

Ordering Information

Device Code*	Description	Package	Comcode
LUCW3015CCR	Bulk Tray	48 TQFPT	108 132 085
LUCW3015CCR-DB	Dry Pack†	48 TQFPT	108 132 093
EVB3015A	Evaluation Board	—	108 191 255

* Contact your Lucent Technologies Microelectronics Group Account Manager for minimum order requirements.
† Tape and reel option is available upon request.

For additional information, contact your Microelectronics Group Account Manager or the following:
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January 1999
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