Data Sheet
December 1996

microelectronics group

Lucent Technologies
Bell Labs Innovations

W2020 GSM Transceiver

Features

- First commercial single-chip EGSM transceiver
- 2.7 V operation
- Low power consumption
- Single IF down conversion
- Frequency agile synthesizer
- Three synthesized local oscillators

Applications

- GSM handportables
- GSM data services

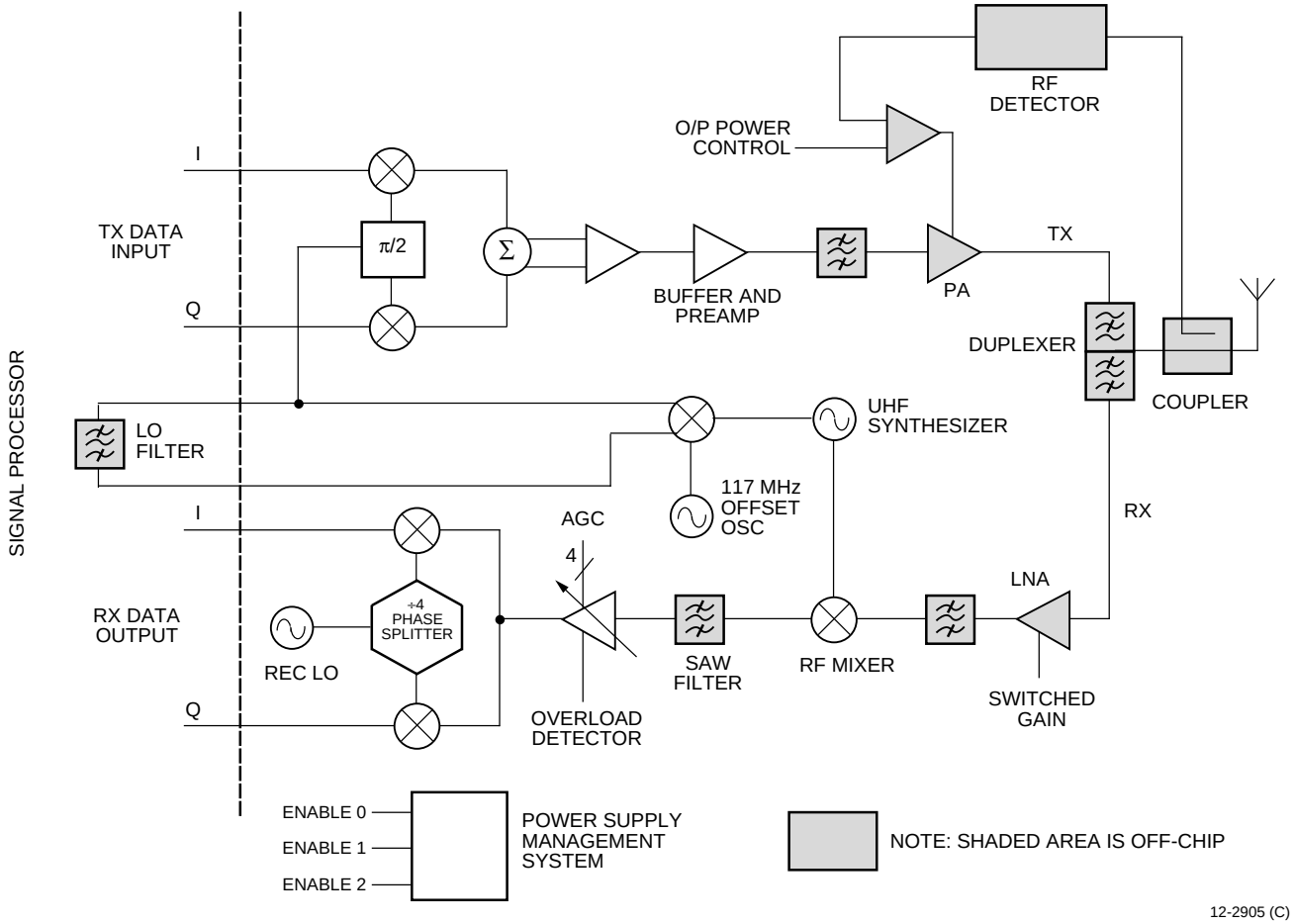


Figure 1. W2020 Block Diagram

Contents

Detailed Block Diagram

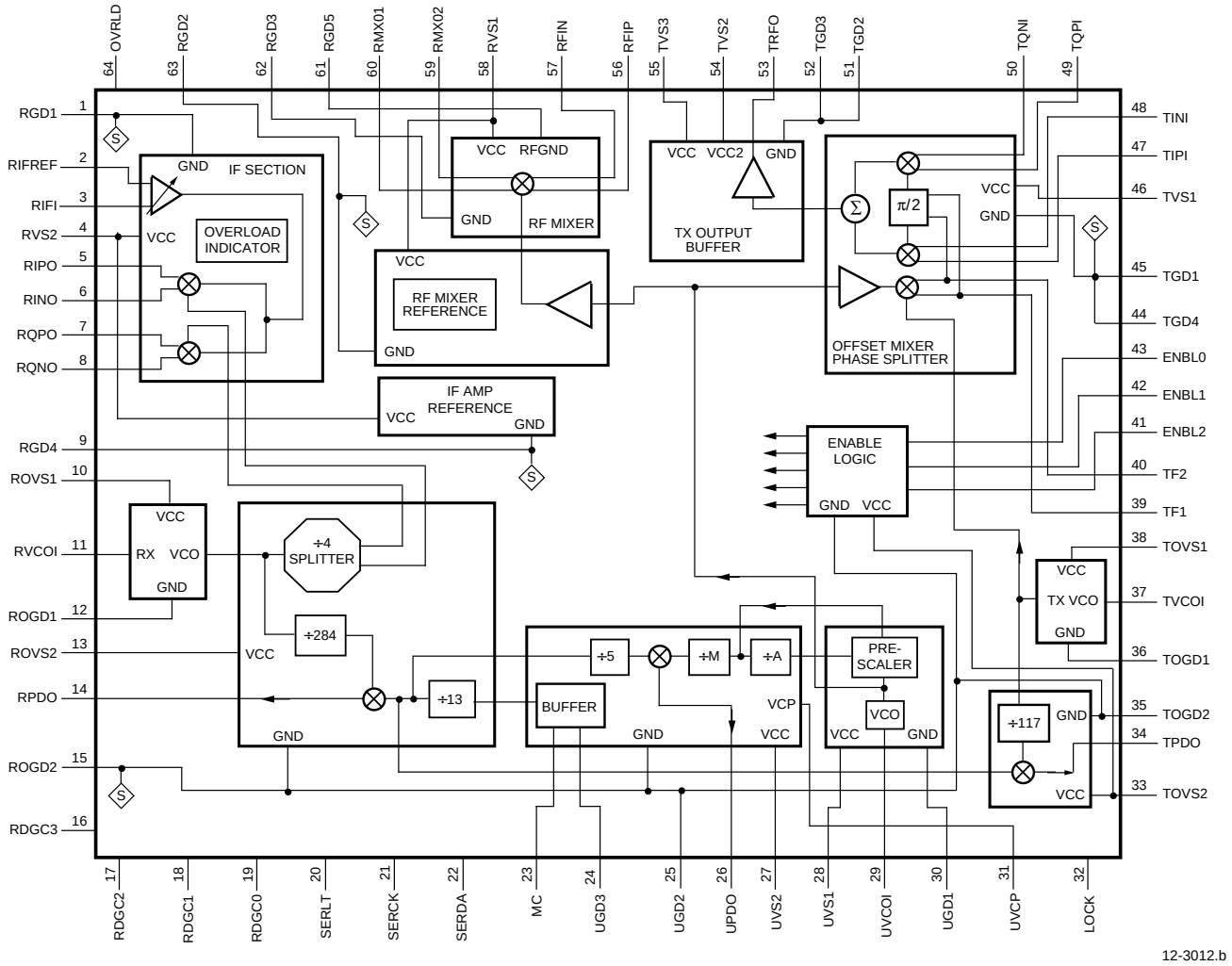


Figure 2. IC Block Diagram with Pinout

Description

The W2020 is a highly integrated RF transceiver device included in Lucent Technologies Microelectronics Group's GSM hardware platform. It has been designed to implement both the GSM and EGSM standards. By adding an external LNA, power amplifier, and filters, the complete radio channel for GSM is realized. The W2020 RF transceiver has been designed in conjunction with the CSP1088 (radio interface device) and the DSP1618 (digital signal processor) to provide a complete GSM cellular solution.

Figure 1 shows a block diagram of the W2020. It consists of the transmitter, receiver, and frequency synthesizers. The W2020 transmitter includes an offset oscillator mixer and quadrature modulator with 90° phase splitter. The receiver includes the RF mixer, digital gain controlled IF amplifier strip, and a quadrature demodulator. There are three frequency synthesizers in the transceiver: a frequency agile UHF synthesizer used for channel selection in both the transmit and receive modes, and two fixed-frequency PLLs in the receiver and transmitter. The W2020 also includes logic control for powerdown modes to minimize supply current.

Description (continued)

Transmitter

The transmitter architecture is a direct-up modulator with a frequency offset local oscillator. From two LO input signals, the offset mixer produces an internal LO signal, which prevents the external VCO or local oscillator from being pulled by the large transmitted signal. This configuration also improves the carrier feedthrough and remixing of the output signal which degrades adjacent channel leakage performance. The phase shifter splits the LO signal into two LOs with 90° phase separation and equal amplitude. The LO signals are fed to the in-phase (I) and quadrature-phase (Q) double-balanced mixers. The resulting signals are summed and fed into the output amplifier. In order to drive an external SAW bandpass filter prior to the power amplifier, a preamplifier may be required.

Receiver

The receive circuit is designed to meet the blocking requirements of GSM without going into overload. For the case where signals are greater than the GSM specification, overload indication is provided. This overload indicator is a nonlatching detector. The OVRLD output lead is high when a signal greater than the trip point is present for a specified time. When the signal is removed, the output remains high for the same specified time. This avoids AGC lockup and minimizes the amount of lost data. It can also be used in some AGC setting schemes.

The receiver uses a single IF and digital gain control along with a quadrature demodulator. Accurate quadrature demodulation is achieved using a divide-by-four technique for the 90° phase splitter. The single IF allows an inexpensive 71 MHz SAW filter to be used with the additional filtering requirements achieved in a baseband circuit (CSP1088). The digital gain control gives a high dynamic range and a resolution of 4 dB. Additional AGC may be required prior to the RF mixer for the very high input level of –15 dBm at the antenna.

The receiver design has carefully considered the GSM requirements of blocking and intermodulation. A complete system analysis has been undertaken in order to ensure the performance is met without the need of expensive external components. The connection to the filters can use either single-ended or balanced techniques.

The blocking conditions that have been considered for the receiver design have been taken from the GSM 05.05 recommendation for a class 4 handportable phone. The intermodulation condition that has been considered includes those referenced in the GSM recommendations for a handportable phone.

Receiver dc Offset Calibration

The interface between the W2020 device and the CSP1088 is dc coupled. After the signal is received by the CSP1088, the signal is amplified before processing by the A/D converter. Therefore, the offset voltage at the W2020 I & Q outputs must be canceled in order to maintain dynamic range of the receiver. The calibration between the ICs is performed on the CSP1088 device during the time immediately prior to a receive burst. The entire receive path on the W2020 device is enabled except for the UHF LO buffer. It is recommended that the LNA be switched off during dc calibration. This ensures that no RF signal is mixed into the IF band while allowing the RF mixer to be biased to maintain a constant impedance level at the IF SAW filter input. This calibration procedure is done prior to each receive or monitor burst since the IF gain may change for each burst.

Frequency Synthesizers

There are two fixed-frequency local oscillators and a programmable UHF oscillator. The local oscillators (117 MHz and 284 MHz) use inductor/varactor tuning. The UHF oscillator (996 MHz—1032 MHz) uses microstrip inductor/varactor tuning. Standard phase-locked loop techniques are employed to synchronize the oscillators to stable references derived from the 13 MHz master clock. Settling time and start-up times are set by the loop filter components in order to maintain accuracy and flexibility. The UHF frequency must be programmed when the W2020 is switched from the off state to any other state.

117 MHz and 284 MHz Local Oscillators

Both local oscillators use a fixed divide-by-13 counter to derive a reference frequency of 1 MHz (Figure 4). The VCO frequency is divided by a 117 or 284 counter to achieve the reference frequency of 1 MHz. The counters use ECL technology to achieve the division and minimize the spurious frequencies generated. The phase detector is a digital type using D-type flip-flops to compare the frequency which then feeds two current sources supplying the external loop filter. The 117 MHz oscillator is referenced to the positive supply, and the 284 MHz oscillator is referenced to ground.

Description (continued)

UHF Local Oscillator

In order to achieve the channel spacing, the reference frequency has been set to 200 kHz. This is derived from the 13 MHz master clock using a divide-by-13 counter, followed by a divide by-5-counter (Figure 4). The center frequency of the UHF oscillator changes to select the desired frequency by using an internal 64/65 dual-modulus prescaler and a programmable counter. The EGSM frequency range requires the UHF local oscillator to be programmed over the range of 996 MHz to 1032 MHz. The center frequency is set by the following equation:

UHF Frequency (MHz) = (A * 64 + M) * 0.2

A = 77, 78, 79, or 80 (See Table 1.)

M = 0 to 63 (6-bit binary counter)

Table 1. A Divide Counter

A1	A0	Count
0	0	77
0	1	78
1	0	79
1	1	80

The serial data format for the A and M dividers is:

First Bit							Last Bit
A1	A2	M5	M4	M3	M2	M1	M0

A complete programming list for channel frequencies is shown in Table 13.

Synthesizer Operation

The serial data is input by using the latch enable, clock, and data inputs. The timing diagram for the latch enable, clock, and data inputs is shown in Figure 3. The serial data controls the programmable 2-bit A divider and the 6-bit M divider. Serial data loaded into the shift register via the data input sets the frequency to be synthesized. The serial data logic level is determined at the positive-going edge of the clock. The clock shuts off after the last bit (M0) is clocked in. The latch enable goes to a logic zero during data transmission and returns to a logic one after the last bit of data. When the latch enable input goes positive, the data shifts from a serial register to a parallel register.

Synthesizer Lock Indicator

The W2020 device provides a VCO lock indicator for the UHF and TXLO. This consists of a wired-OR for lock indication of the TXLO and UHF LO. The lock indication consists of an exclusive-OR function of the up-down pulses from the phase detector.

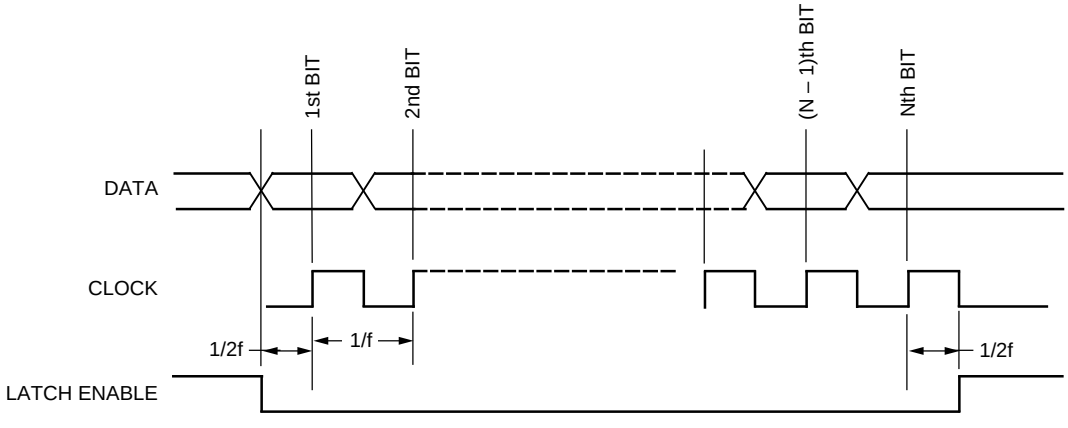
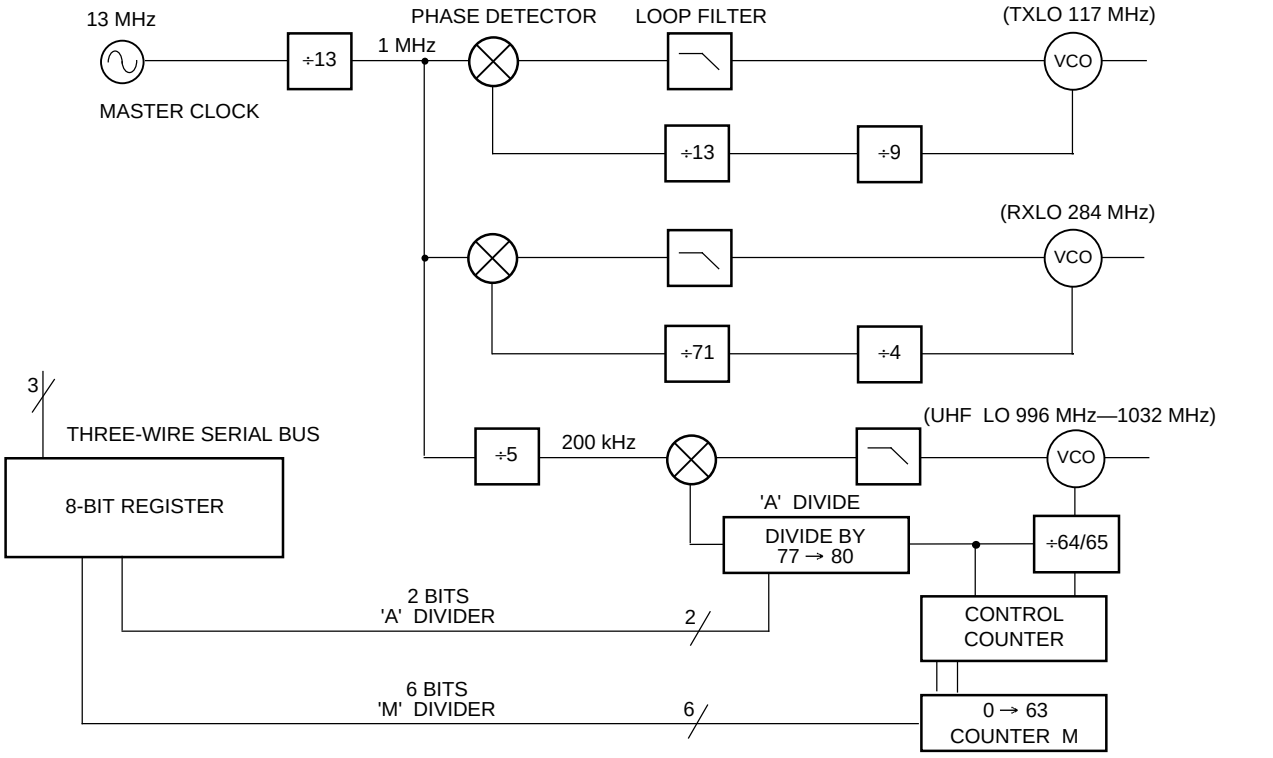


Figure 3. UHF Synthesizer Timing Diagram

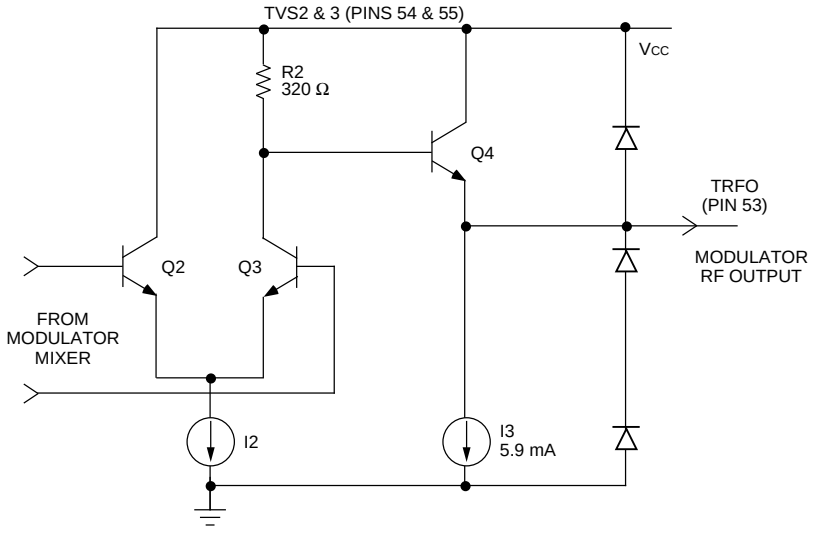
Description (continued)



12-3077 (C)

Figure 4. Synthesizer Block Diagram

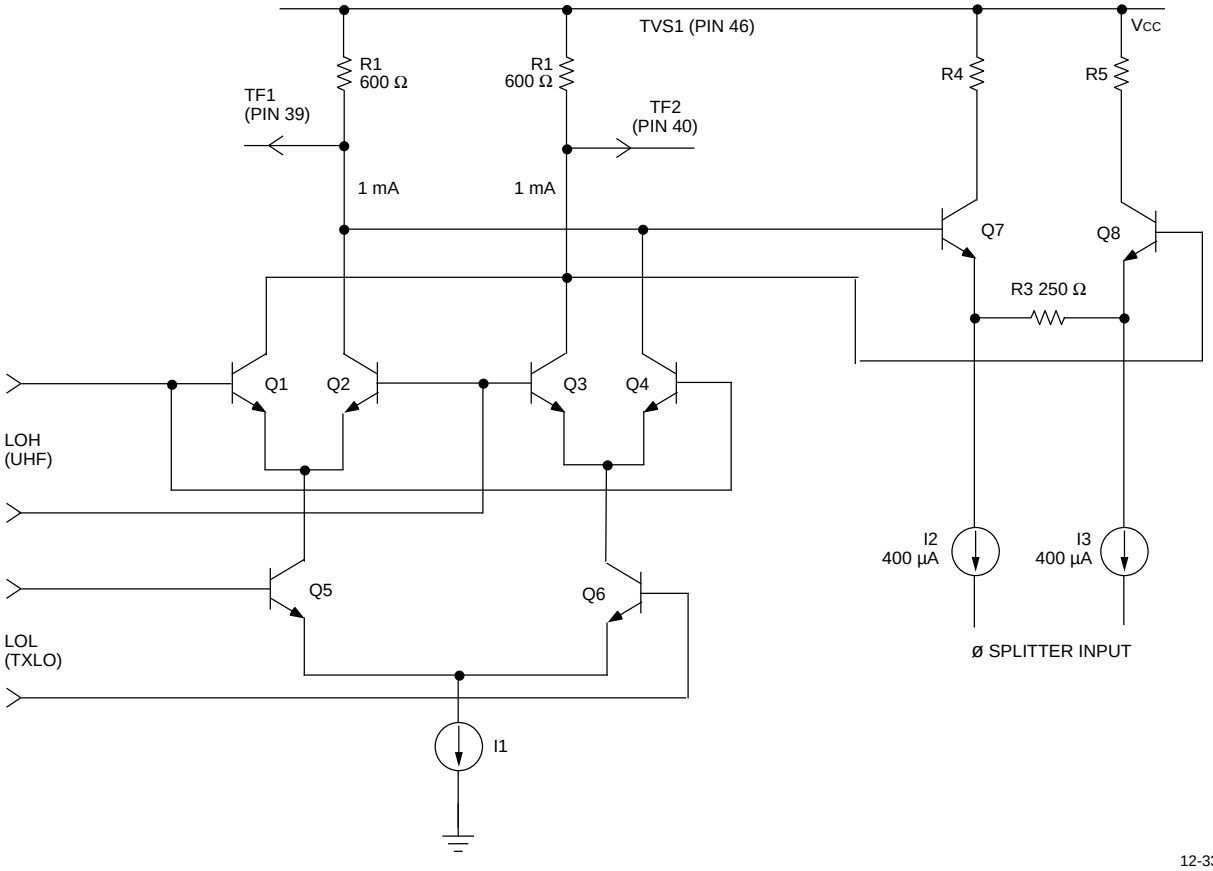
Input/Output Circuit Diagrams



12-3355 (C)

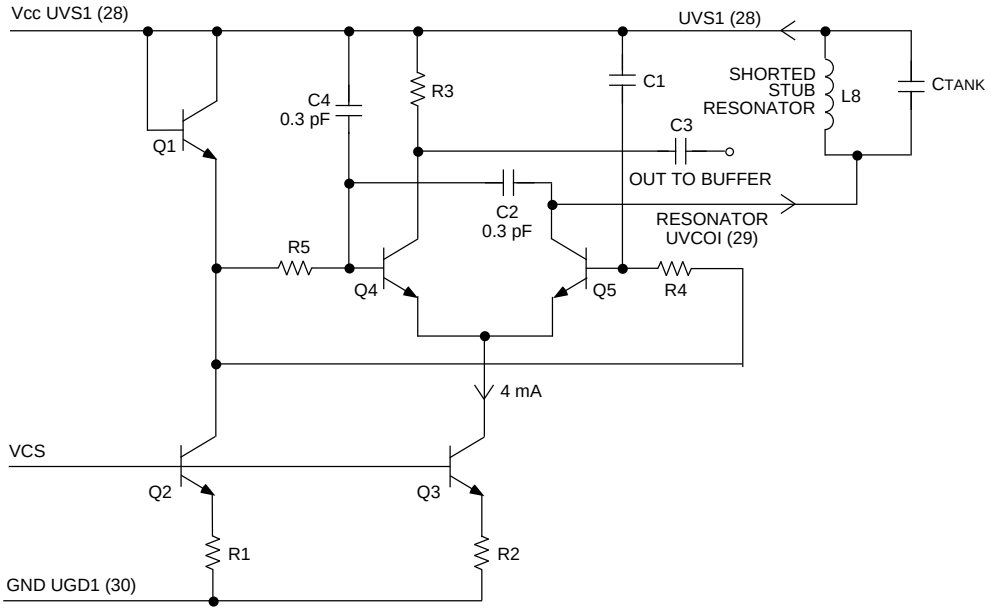
Figure 5. Modulator Output Circuit Diagram

Input/Output Circuit Diagrams (continued)



12-3356 (C)

Figure 6. Offset LO Mixer Circuit Diagram



12-3335 (C)

Figure 7. UHF VCO Circuit Diagram

Input/Output Circuit Diagrams (continued)

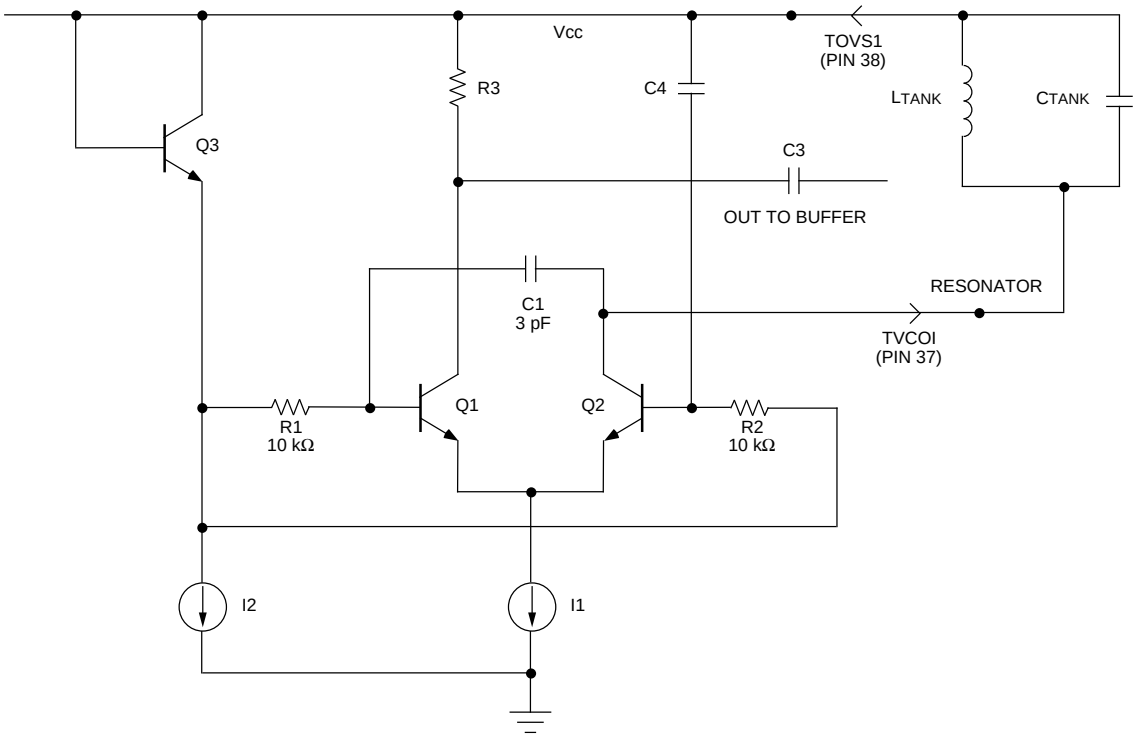


Figure 8. TX VCO Circuit Diagram

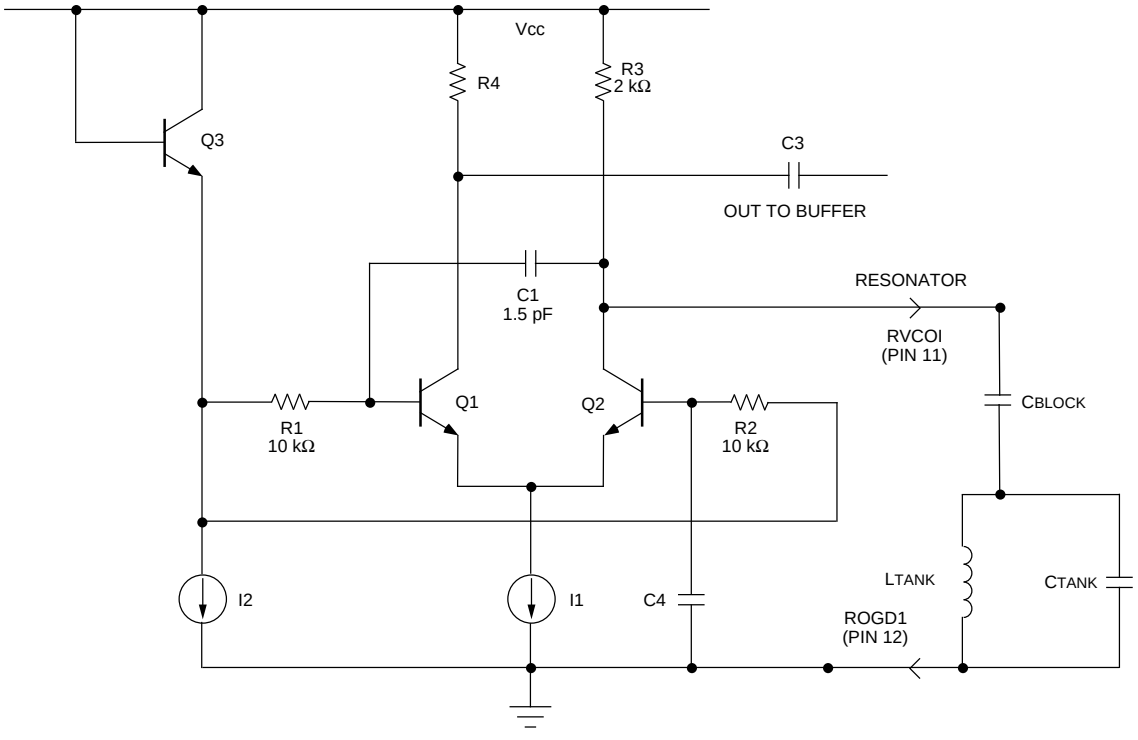


Figure 9. RX VCO Circuit Diagram

Input/Output Circuit Diagrams (continued)

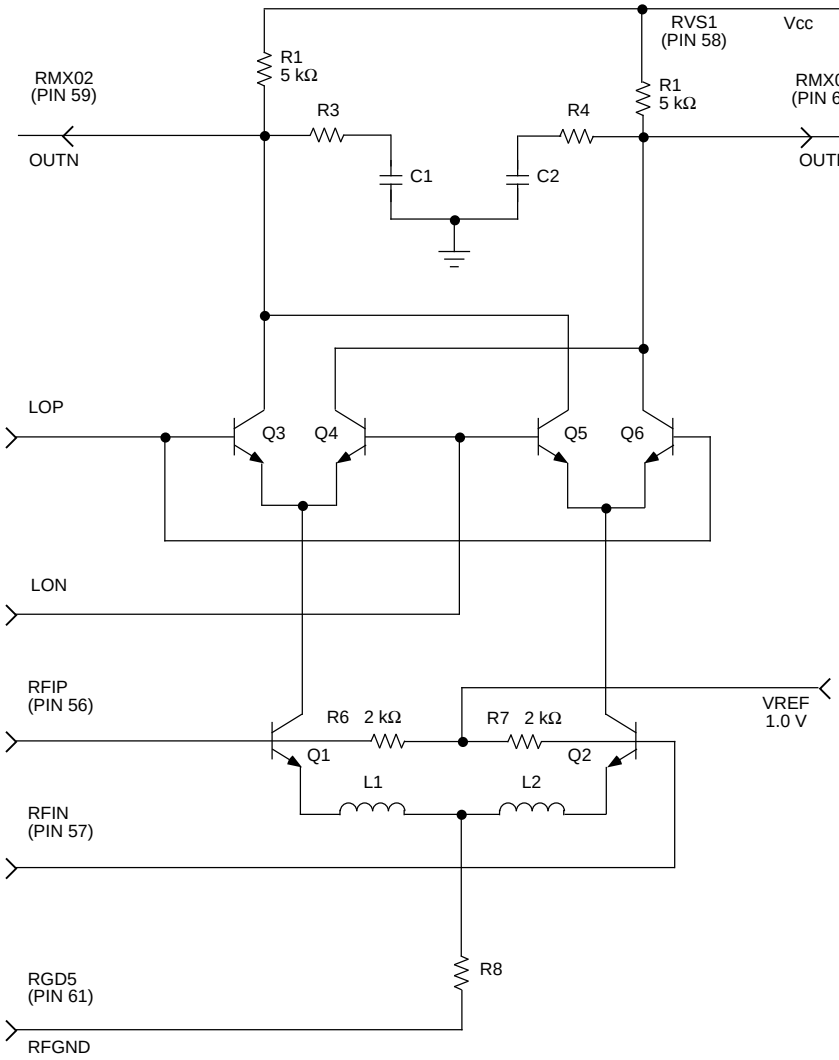


Figure 10. RF Mixer IC Diagram

Input/Output Circuit Diagrams (continued)

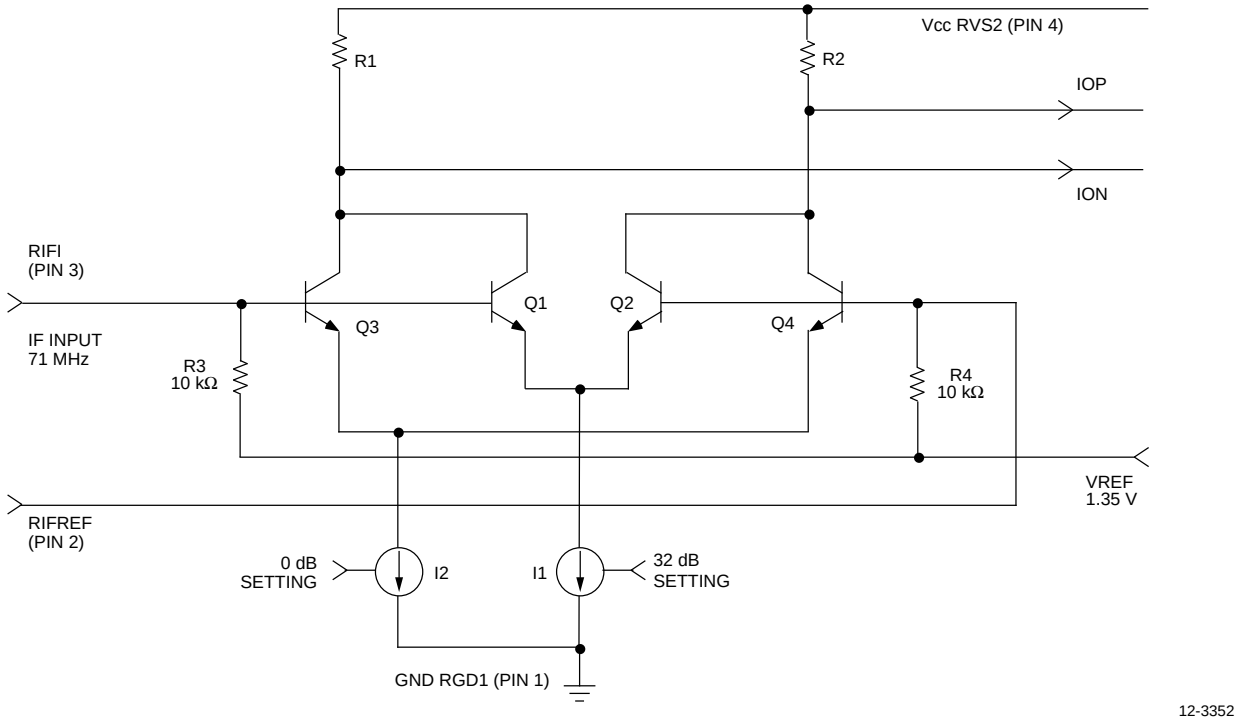


Figure 11. IF Strip Input Diagram

Pin Information

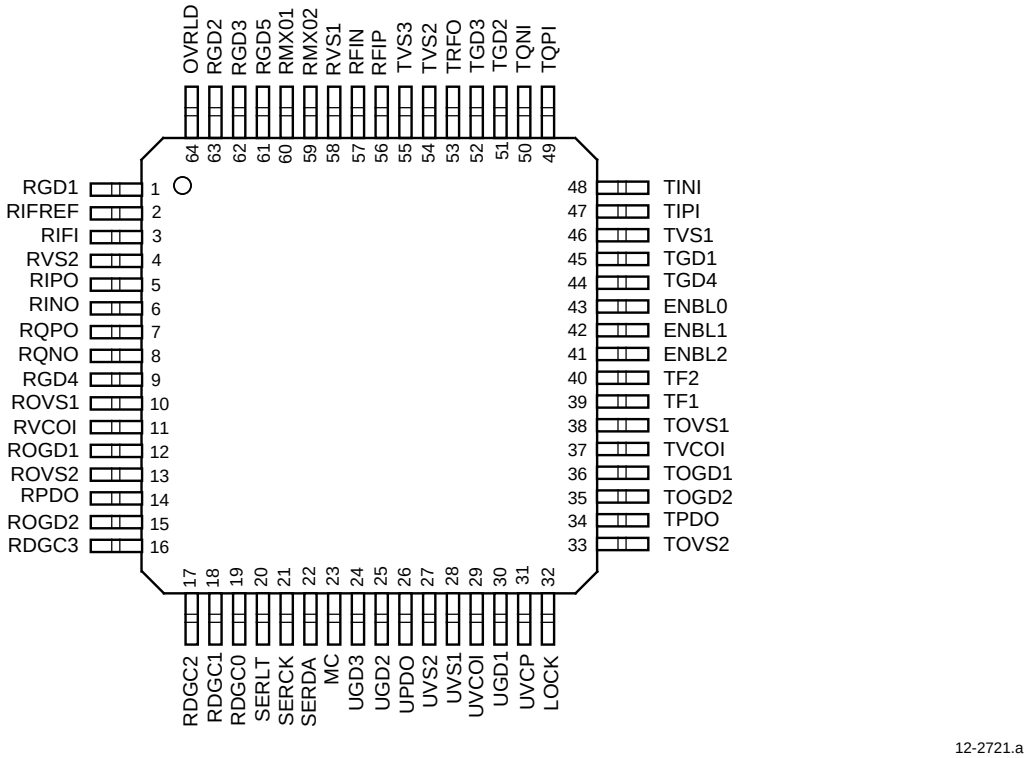


Figure 12. Pin Diagram

Pin Information (continued)

Table 2. Pin Description

Pin	Name	Function	Description
1	RGD1	Ground	Receiver Ground 1
2	RIFREF	Input	Receiver IF Amplifier Input Reference
3	RIFI	Input	Receiver IF Amplifier Input
4	RVS2	Supply	Receiver Voltage Supply 2
5	RIPO	Output	Receiver I Positive Output
6	RINO	Output	Receiver I Negative Output
7	RQPO	Output	Receiver Q Positive Output
8	RQNO	Output	Receiver Q Negative Output
9	RGD4	Ground	Receiver Ground 4
10	ROVS1	Supply	Receiver Oscillator Voltage Supply 1
11	RVCOI	Input	Receiver Oscillator Input
12	ROGD1	Ground	Receiver Oscillator Ground 1
13	ROVS2	Supply	Receiver Oscillator Voltage Supply 2
14	RPDO	Output	Receiver Oscillator Phase Detector Output
15	ROGD2	Ground	Receiver Oscillator Ground 2
16	RDGC3	Input	IF Digital Gain Control (32 dB step)
17	RDGC2	Input	IF Digital Gain Control (16 dB step)
18	RDGC1	Input	IF Digital Gain Control (8 dB step)
19	RDGC0	Input	IF Digital Gain Control (4 dB step)
20	SERLT	Input	Serial Latch Enable Input
21	SERCK	Input	Serial Clock Input
22	SERDA	Input	Serial Data Input
23	MC	Input	Master Clock Input (single-ended)
24	UGD3	Ground	UHF Synthesizer Ground 3
25	UGD2	Ground	UHF Synthesizer Ground 2
26	UPDO	Output	UHF Oscillator Phase Detector Output
27	UVS2	Supply	UHF Synthesizer Voltage Supply 2
28	UVS1	Supply	UHF Synthesizer Voltage Supply 1
29	UVCOI	Input	UHF VCO Input
30	UGD1	Ground	UHF Synthesizer Ground 1
31	UVCP	Supply	UHF Charge Pump Supply
32	LOCK	Output	UHF and TXLO Lock Indicator
33	TOVS2	Supply	Transmit Oscillator Voltage Supply 2
34	TPDO	Output	Transmit Oscillator Phase Detector Output
35	TOGD2	Ground	Transmit Oscillator Ground 2
36	TOGD1	Ground	Transmit Oscillator Ground 1
37	TVCOI	Input	Transmit Oscillator VCO Input
38	TOVS1	Supply	Transmit Oscillator Voltage Supply 1
39	TF1	In/Out	Transmit Filter Input/Output 1

Pin Information (continued)

Table 2. Pin Description (continued)

Pin	Name	Function	Description
40	TF2	In/Out	Transmit Filter Input/Output 2
41	ENBL2	Input	Control Input Enable 2
42	ENBL1	Input	Control Input Enable 1
43	ENBL0	Input	Control Input Enable 0
44	TGD4	Ground	Transmit Ground 4
45	TGD1	Ground	Transmit Ground 1
46	TVS1	Supply	Transmit Voltage Supply 1
47	TIPI	Input	Transmit I Positive Input
48	TINI	Input	Transmit I Negative Input
49	TQPI	Input	Transmit Q Positive Input
50	TQNI	Input	Transmit Q Negative Input
51	TGD2	Ground	Transmit Ground 2
52	TGD3	Ground	Transmit Ground 3
53	TRFO	Output	Transmit RF Output
54	TVS2	Supply	Transmit Voltage Supply 2
55	TVS3	Supply	Transmit Voltage Supply 3
56	RFIP	Input	Receiver RF Positive Input
57	RFIN	Input	Receiver RF Negative Input
58	RVS1	Supply	Receiver Voltage Supply 1
59	RMXO2	Output	Receiver Mixer Output 2
60	RMXO1	Output	Receiver Mixer Output 1
61	RGD5	Ground	Receiver Ground 5
62	RGD3	Ground	Receiver Ground 3
63	RGD2	Ground	Receiver Ground 2
64	OVRLD	Output	IF Amplifier Overload Indicator

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Ambient Operating Temperature	T_A	–30	85	°C
Storage Temperature	T_{stg}	–65	150	°C
Lead Soldering Temperature (soldering, 10 seconds)*	—	—	300	°C
Supply Voltage	Vcc	0	6.0	V
Power Dissipation	P_{DISS}	0	650	mW
ac Input Voltage (positive or negative peak)	V	0	Vcc	V
Digital Input Voltages	—	0	Vcc + 0.4	V

* Applies to electrical pins only.

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. Lucent employs a human-body model (HBM) and a charged-device model (CDM) for ESD susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the model. No industry-wide standard has been adopted for CDM. However, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and therefore can be used for comparison purposes. The HBM ESD threshold presented here was obtained by using these circuit parameters:

ESD Threshold Voltage		
Device	**Rating**	**Model**
W2020	≥100 V	HBM
W2020	≥200 V ≥1000 V	CDM (corner pins)

Electrical Specifications

Note: Vcc = 2.7 Vdc, T_A = 25 °C ± 3 °C.

Table 3. System Modes

System Mode	ENBL0	ENBL1	ENBL2	Min	Typ	Max	Unit
Off	0	0	0	—	6	50	µA
UHF Synthesizer On*	0	1	0	—	30	40	mA
UHF & Transmit Synthesizer On	1	1	0	—	35	46	mA
Transmit Mode	1	0	0	—	67	84	mA
UHF & Receive Synthesizer On, Receiver On Except for UHF LO Buffer (offset calibration)	0	1	1	—	56	72	mA
Receive Mode	0	0	1	—	60	76	mA
State Not Allowed	1	1	1	—	—	—	—
State Not Allowed	1	0	1	—	—	—	—

* The UHF frequency must be programmed when entering this mode.

Electrical Specifications (continued)

Note: Vcc = 2.7 Vdc, T_A = 25 °C ± 3 °C.

Table 4. General Specifications

Parameter	Min	Typ	Max	Unit
Supply Voltage	2.7	—	4.5	V
Digital Inputs:				
V_{IH}	Vcc – 0.7	—	Vcc + 0.4	V
V_{IL}	GND – 0.4	—	0.6	V
I_{IH} (V_{IH} = 3.3 V, Vcc = 4.5 V)	—	50	100	µA
I_{IL} (V_{IL} = 0.4 V, Vcc = 4.5 V)	—	—	10	µA
Noise Immunity, Digital Input	—	—	600	mV
Duration of Input Noise Pulse	2.0	—	20	ns
Digital Outputs:				
V_{OH}	2.2	—	—	V
V_{OL}	—	—	0.5	V
I_{OH} (V_{OH} = 2.2 V)	10	—	—	µA
I_{OL} (V_{OL} = 0.5 V)	20	—	—	µA
Lock Output:				
V_{OH}	Vcc – 0.5	—	—	Vpk
V_{OL}	—	—	0.5	Vpk
I_{OH} (@ Vcc – 0.4 V)	500	—	—	µA
I_{OL} (@ 0.4 Vdc)	500	—	—	µA
Powerup/down Time	—	—	4.0	µs

Table 5. UHF Synthesizer Section

Parameter	Min	Typ	Max	Unit
Frequency Range	996	—	1032	MHz
Reference Frequency	—	200		kHz
Phase Detector Gain	640	800	960	µA/cycle
Phase Detector Voltage (minimum)	—	—	0.8	V
Phase Detector Voltage (maximum)	UVCP – 0.8	—	—	V
Settling Time* (36 MHz frequency change)	—	—	0.5	ms
Start-up Time*	—	—	1.0	ms
UVCP Supply Voltage	2.7	—	4.5	V
Reference Sidebands*:				
200 kHz	—	—	–37	dBc
400 kHz	—	—	–60	dBc
>600 kHz	—	—	–64	dBc
Phase Noise†:				
200 kHz	—	—	–75	dBc/Hz
400 kHz	—	—	–105	dBc/Hz
600 kHz	—	—	–117	dBc/Hz
1.6 MHz	—	—	–129	dBc/Hz
>3 MHz	—	—	–136	dBc/Hz

* This parameter is set by external loop filter components and VCO gain.
† This parameter is set by the external VCO resonator design.

Electrical Specifications (continued)

Note: Vcc = 2.7 Vdc, T_A = 25 °C ± 3 °C.

Table 6. Transmitter Local Oscillator

Parameter	Min	Typ	Max	Unit
Center Frequency	—	117	—	MHz
Reference Frequency	—	1	—	MHz
Phase Detector Gain	80	100	120	µA/cycle
Phase Detector Voltage (minimum)	—	—	0.8	V
Phase Detector Voltage (maximum)	Vcc – 0.8	—	—	V
Start-up Time (to ±50 Hz)*	—	—	0.5	ms

* This parameter is set by external loop filter components and VCO gain.

Table 7. Master Clock

Parameter	Min	Typ	Max	Unit
Center Frequency	—	13	—	MHz
Input Level	0.4	0.8	1.0	Vp-p

Table 8. Receiver Local Oscillator

Parameter	Min	Typ	Max	Unit
Center Frequency	—	284	—	MHz
Reference Frequency	—	1	—	MHz
Phase Detector Gain	80	100	120	µA/cycle
Phase Detector Voltage (minimum)	—	—	0.8	V
Phase Detector Voltage (maximum)	Vcc – 0.8	—	—	V
Start-up Time (to ±50 Hz)*	—	—	0.5	ms

* This parameter is set by external loop filter components and VCO gain.

Electrical Specifications (continued)

Note: Vcc = 2.7 Vdc, T_A = 25 °C ± 3 °C.

Table 9. Transmitter Section

IQ common mode = 1.6 V, input differential signal = 0.7 Vp-p.

Parameter	Min	Typ	Max	Unit
I & Q Input Differential Signal	0.7	—	—	Vp-p
I & Q Signal Path Bandwidth	0.8	—	—	MHz
I & Q Input Resistance (I to I-bar or Q to Q-bar)	—	13	—	MΩ
I & Q Input Capacitance (I to I-bar or Q to Q-bar)	—	4.3	—	pF
I & Q Common-mode Input Bias Current*	—	—	5	µA
I & Q Input Common-mode Range	1.5	1.6	Vcc – 1.05	V
I & Q Input Differential Signal for Maximum Output	—	0.7	—	Vp-p
Output Impedance @ 900 MHz	—	50 + j30	—	Ω
Output Power	–3	—	—	dBm
RMS Phase Accuracy—200 kHz BW†	—	2.2	2.8	°(rms)
Output Spectrum:‡				
200 kHz (30 kHz RBW)	—	–35	–30	dBc
250 kHz (30 kHz RBW)	—	–42	–33	dBc
400 kHz (30 kHz RBW)	—	–63	–60	dBc
1.8 MHz (100 kHz RBW)	—	–75	–63	dBc
3 MHz (100 kHz RBW)	—	–75	–65	dBc
6 MHz (100 kHz RBW)	—	–76	–71	dBc
>20 MHz	—	–135	–133	dBc/Hz

* Per input pin.
† This parameter is affected by external UHF synthesizer loop filter components and by VCO gain. Verified on evaluation board only.
‡ Using random modulation.

Table 10. RF Mixer Section

Parameter	Min	Typ	Max	Unit
Gain	6.0	—	10	dB
Noise Figure (DSB)	—	—	9	dB
Input 1 dB Compression Point	–10	–8	—	dBm
RF Frequency Range	925	—	960	MHz
LO Frequency Range	996	—	1031	MHz

Electrical Specifications (continued)

Note: Vcc = 2.7 Vdc, T_A = 25 °C ± 3 °C.

Table 11. IF DGC Amplifier and Quadrature Demodulator

Parameter	Min	Typ	Max	Unit
IF Amplifier + Mixer Gain*	56	—	68	dB
DGC Resolution	—	4	—	dB
DGC Range	—	58	—	dB
Gain Flatness (±100 kHz)	—	±0.2	—	dB
Input Frequency	—	71	—	MHz
Baseband Bandwidth	—	3	—	MHz
I & Q Phase Accuracy	–3	1.1	+3	°
I & Q Amplitude Mismatch	–0.4	0.03	0.4	dB
I & Q Maximum Differential Output Swing	0.8	—	—	Vp-p
I & Q Common-mode Voltage	—	Vcc – 1.2	—	V
I & Q Differential Offset Voltage at Maximum Gain	—	—	±30	mV
I & Q Output Current	±50	—	—	µA
Output 1 dB Compression Point†	0	3	—	dBm
Overload Indication of Output Signal Level†	—	–1.2	—	dBm
Overload Indication Delay	—	4	—	µs
Noise Figure (referred to input of IF amp)‡	—	6	8.5	dB
Absolute Gain Accuracy§	–2	—	2	dB
Relative Gain Accuracy**	–1	—	1	dB

* Gain assumes 50 Ω input impedance and coupling network.
† Equivalent voltage referred to 50 Ω load.
‡ At maximum gain setting.
§ Over temperature after gain calibration.
** Over temperature, 32 dB and 16 dB gain step calibration.

Table 12. Digital Gain Control

RDGC3	RDGC2	RDGC1	RDGC0	Gain (dB)	RDGC3	RDGC2	RDGC1	RDGC0	Gain (dB)
0	0	0	0	65	1	0	0	0	33
0	0	0	1	61	1	0	0	1	29
0	0	1	0	57	1	0	1	0	25
0	0	1	1	53	1	0	1	1	21
0	1	0	0	49	1	1	0	0	17
0	1	0	1	45	1	1	0	1	13
0	1	1	0	41	1	1	1	0	9
0	1	1	1	37	1	1	1	1	5

Electrical Specifications (continued)

Table 13. UHF Frequency Programming

Freq.	A1	A0	M5	M4	M3	M2	M1	M0	Freq.	A1	A0	M5	M4	M3	M2	M1	M0
996.0	0	0	1	1	0	1	0	0	1005.2	0	1	1	0	0	0	1	0
996.2	0	0	1	1	0	1	0	1	1005.4	0	1	1	0	0	0	1	1
996.4	0	0	1	1	0	1	1	0	1005.6	0	1	1	0	0	1	0	0
996.6	0	0	1	1	0	1	1	1	1005.8	0	1	1	0	0	1	0	1
996.8	0	0	1	1	1	0	0	0	1006.0	0	1	1	0	0	1	1	0
997.0	0	0	1	1	1	0	0	1	1006.2	0	1	1	0	0	1	1	1
997.2	0	0	1	1	1	0	1	0	1006.4	0	1	1	0	1	0	0	0
997.4	0	0	1	1	1	0	1	1	1006.6	0	1	1	0	1	0	0	1
997.6	0	0	1	1	1	1	0	0	1006.8	0	1	1	0	1	0	1	0
997.8	0	0	1	1	1	1	0	1	1007.0	0	1	1	0	1	0	1	1
998.0	0	0	1	1	1	1	1	0	1007.2	0	1	1	0	1	1	0	0
998.2	0	0	1	1	1	1	1	1	1007.4	0	1	1	0	1	1	0	1
998.4	0	1	0	0	0	0	0	0	1007.6	0	1	1	0	1	1	1	0
998.6	0	1	0	0	0	0	0	1	1007.8	0	1	1	0	1	1	1	1
998.8	0	1	0	0	0	0	1	0	1008.0	0	1	1	1	0	0	0	0
999.0	0	1	0	0	0	0	1	1	1008.2	0	1	1	1	0	0	0	1
999.2	0	1	0	0	0	1	0	0	1008.4	0	1	1	1	0	0	1	0
999.4	0	1	0	0	0	1	0	1	1008.6	0	1	1	1	0	0	1	1
999.6	0	1	0	0	0	1	1	0	1008.8	0	1	1	1	0	1	0	0
999.8	0	1	0	0	0	1	1	1	1009.0	0	1	1	1	0	1	0	1
1000.0	0	1	0	0	1	0	0	0	1009.2	0	1	1	1	0	1	1	0
1000.2	0	1	0	0	1	0	0	1	1009.4	0	1	1	1	0	1	1	1
1000.4	0	1	0	0	1	0	1	0	1009.6	0	1	1	1	1	0	0	0
1000.6	0	1	0	0	1	0	1	1	1009.8	0	1	1	1	1	0	0	1
1000.8	0	1	0	0	1	1	0	0	1010.0	0	1	1	1	1	0	1	0
1001.0	0	1	0	0	1	1	0	1	1010.2	0	1	1	1	1	0	1	1
1001.2	0	1	0	0	1	1	1	0	1010.4	0	1	1	1	1	1	0	0
1001.4	0	1	0	0	1	1	1	1	1010.6	0	1	1	1	1	1	0	1
1001.6	0	1	0	1	0	0	0	0	1010.8	0	1	1	1	1	1	1	0
1001.8	0	1	0	1	0	0	0	1	1011.0	0	1	1	1	1	1	1	1
1002.0	0	1	0	1	0	0	1	0	1011.2	1	0	0	0	0	0	0	0
1002.2	0	1	0	1	0	0	1	1	1011.4	1	0	0	0	0	0	0	1
1002.4	0	1	0	1	0	1	0	0	1011.6	1	0	0	0	0	0	1	0
1002.6	0	1	0	1	0	1	0	1	1011.8	1	0	0	0	0	0	1	1
1002.8	0	1	0	1	0	1	1	0	1012.0	1	0	0	0	0	1	0	0
1003.0	0	1	0	1	0	1	1	1	1012.2	1	0	0	0	0	1	0	1
1003.2	0	1	0	1	1	0	0	0	1012.4	1	0	0	0	0	1	1	0
1003.4	0	1	0	1	1	0	0	1	1012.6	1	0	0	0	0	1	1	1
1003.6	0	1	0	1	1	0	1	0	1012.8	1	0	0	0	1	0	0	0
1003.8	0	1	0	1	1	0	1	1	1013.0	1	0	0	0	1	0	0	1
1004.0	0	1	0	1	1	1	0	0	1013.2	1	0	0	0	1	0	1	0
1004.2	0	1	0	1	1	1	0	1	1013.4	1	0	0	0	1	0	1	1
1004.4	0	1	0	1	1	1	1	0	1013.6	1	0	0	0	1	1	0	0
1004.6	0	1	0	1	1	1	1	1	1013.8	1	0	0	0	1	1	0	1
1004.8	0	1	1	0	0	0	0	0	1014.0	1	0	0	0	1	1	1	0
1005.0	0	1	1	0	0	0	0	1	1014.2	1	0	0	0	1	1	1	1

Electrical Specifications (continued)

Table 13. UHF Frequency Programming (continued)

Freq.	A1	A0	M5	M4	M3	M2	M1	M0
1014.4	1	0	0	1	0	0	0	0
1014.6	1	0	0	1	0	0	0	1
1014.8	1	0	0	1	0	0	1	0
1015.0	1	0	0	1	0	0	1	1
1015.2	1	0	0	1	0	1	0	0
1015.4	1	0	0	1	0	1	0	1
1015.6	1	0	0	1	0	1	1	0
1015.8	1	0	0	1	0	1	1	1
1016.0	1	0	0	1	1	0	0	0
1016.2	1	0	0	1	1	0	0	1
1016.4	1	0	0	1	1	0	1	0
1016.6	1	0	0	1	1	0	1	1
1016.8	1	0	0	1	1	1	0	0
1017.0	1	0	0	1	1	1	0	1
1017.2	1	0	0	1	1	1	1	0
1017.4	1	0	0	1	1	1	1	1
1017.6	1	0	1	0	0	0	0	0
1017.8	1	0	1	0	0	0	0	1
1018.0	1	0	1	0	0	0	1	0
1018.2	1	0	1	0	0	0	1	1
1018.4	1	0	1	0	0	1	0	0
1018.6	1	0	1	0	0	1	0	1
1018.8	1	0	1	0	0	1	1	0
1019.0	1	0	1	0	0	1	1	1
1019.2	1	0	1	0	1	0	0	0
1019.4	1	0	1	0	1	0	0	1
1019.6	1	0	1	0	1	0	1	0
1019.8	1	0	1	0	1	0	1	1
1020.0	1	0	1	0	1	1	0	0
1020.2	1	0	1	0	1	1	0	1
1020.4	1	0	1	0	1	1	1	0
1020.6	1	0	1	0	1	1	1	1
1020.8	1	0	1	1	0	0	0	0
1021.0	1	0	1	1	0	0	0	1
1021.2	1	0	1	1	0	0	1	0
1021.4	1	0	1	1	0	0	1	1
1021.6	1	0	1	1	0	1	0	0
1021.8	1	0	1	1	0	1	0	1
1022.0	1	0	1	1	0	1	1	0
1022.2	1	0	1	1	0	1	1	1
1022.4	1	0	1	1	1	0	0	0
1022.6	1	0	1	1	1	0	0	1
1022.8	1	0	1	1	1	0	1	0
1023.0	1	0	1	1	1	0	1	1
1023.2	1	0	1	1	1	1	0	0
1023.4	1	0	1	1	1	1	0	1
1023.6	1	0	1	1	1	1	1	0
1023.8	1	0	1	1	1	1	1	1
1024.0	1	1	0	0	0	0	0	0
1024.2	1	1	0	0	0	0	0	1
1024.4	1	1	0	0	0	0	1	0
1024.6	1	1	0	0	0	0	1	1
1024.8	1	1	0	0	0	1	0	0
1025.0	1	1	0	0	0	1	0	1
1025.2	1	1	0	0	0	1	1	0
1025.4	1	1	0	0	0	1	1	1
1025.6	1	1	0	0	1	0	0	0
1025.8	1	1	0	0	1	0	0	1
1026.0	1	1	0	0	1	0	1	0
1026.2	1	1	0	0	1	0	1	1
1026.4	1	1	0	0	1	1	0	0
1026.6	1	1	0	0	1	1	0	1
1026.8	1	1	0	0	1	1	1	0
1027.0	1	1	0	0	1	1	1	1
1027.2	1	1	0	1	0	0	0	0
1027.4	1	1	0	1	0	0	0	1
1027.6	1	1	0	1	0	0	1	0
1027.8	1	1	0	1	0	0	1	1
1028.0	1	1	0	1	0	1	0	0
1028.2	1	1	0	1	0	1	0	1
1028.4	1	1	0	1	0	1	1	0
1028.6	1	1	0	1	0	1	1	1
1028.8	1	1	0	1	1	0	0	0
1029.0	1	1	0	1	1	0	0	1
1029.2	1	1	0	1	1	0	1	0
1029.4	1	1	0	1	1	0	1	1
1029.6	1	1	0	1	1	1	0	0
1029.8	1	1	0	1	1	1	0	1
1030.0	1	1	0	1	1	1	1	0
1030.2	1	1	0	1	1	1	1	1
1030.4	1	1	1	0	0	0	0	0
1030.6	1	1	1	0	0	0	0	1
1030.8	1	1	1	0	0	0	1	0
1031.0	1	1	1	0	0	0	1	1
1031.2	1	1	1	0	0	1	0	0
1031.4	1	1	1	0	0	1	0	1
1031.6	1	1	1	0	0	1	1	0
1031.8	1	1	1	0	0	1	1	1
1032.0	1	1	1	0	1	0	0	0

W2020 Test Circuit

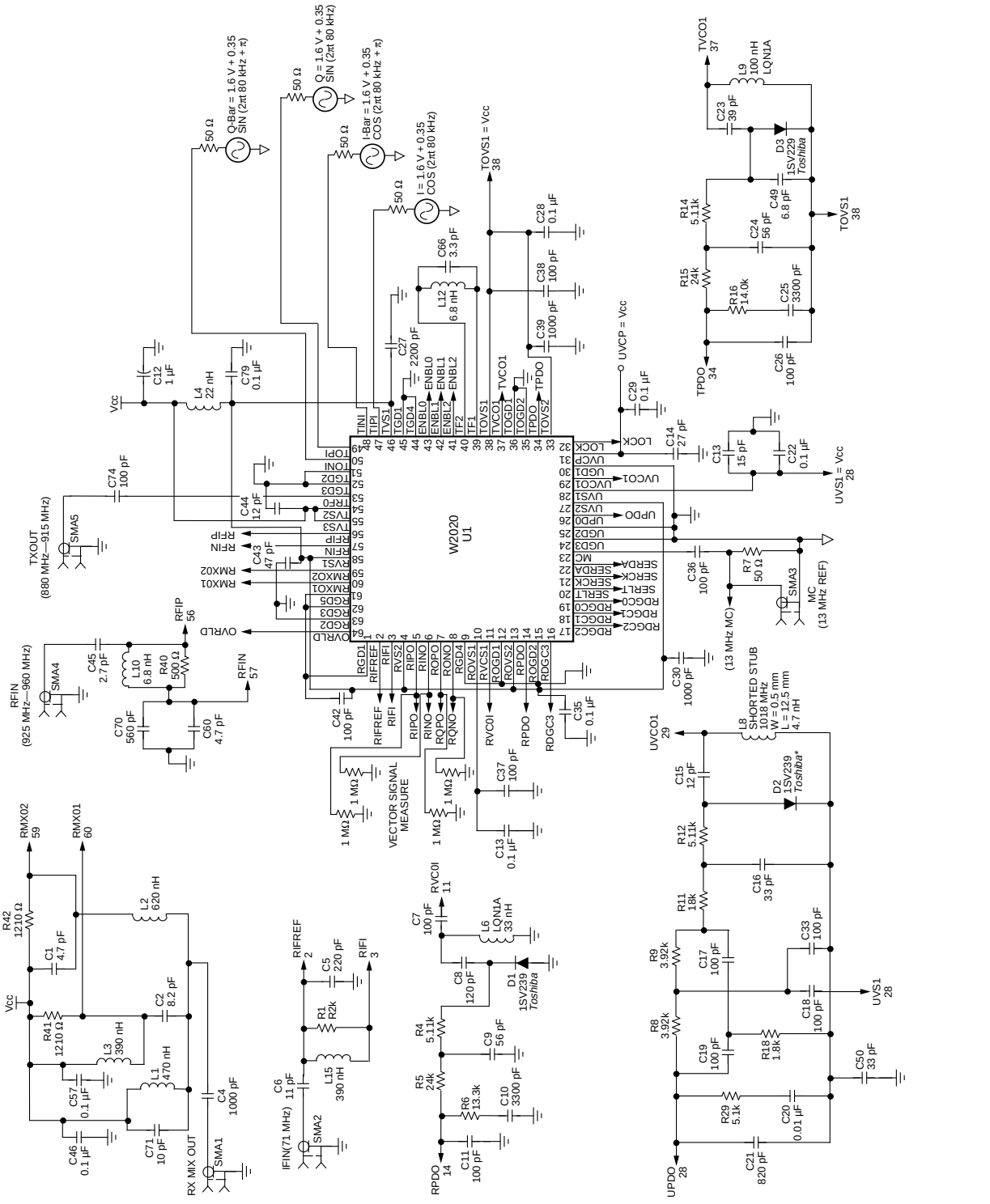


Figure 13. W2020 Test Circuit

* *Toshiba* is a registered trademark of Kabushiki Kaisha Toshiba.

S-Parameters

Note: Vcc = 3.0 Vdc, T_A = 25 °C ± 3 °C.

S-parameter data is included in table form and graphed for all RF and IF ports on the W2020. The data comes from actual measurements on the recent devices.

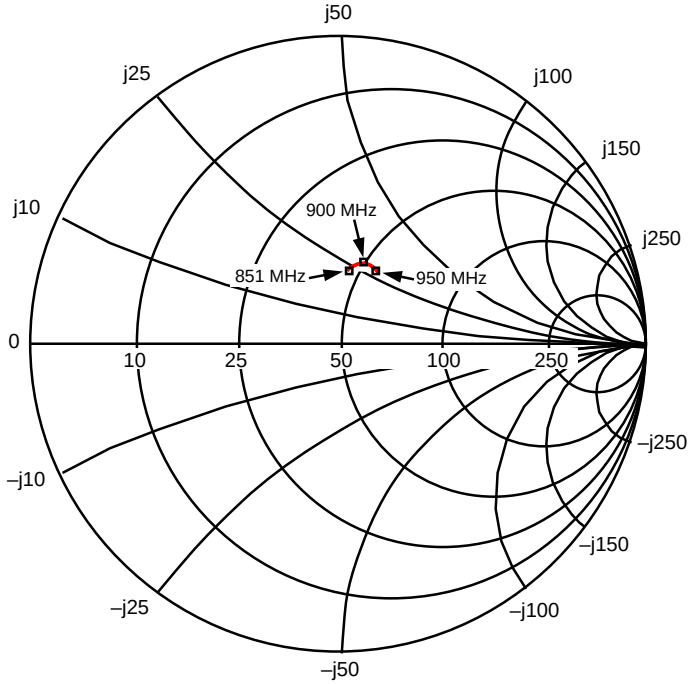


Figure 14. W2020 GSM Modulator Output Impedance

Table 14. W2020 Modulator Single-Ended Output S-Parameters

File: TXOUTPUT.S1P, Device S-Parameters		
Frequency (MHz)	Parameter	
	S11 MAG	S11 ANG
	MA R 50	
851	0.2534	83.115
860	0.2594	81.273
870	0.2598	80.902
880	0.2651	80.627
885	0.2676	80.235
890	0.2734	79.711
895	0.2835	77.006
900	0.2758	75.566
905	0.2716	74.058
910	0.2724	73.731
915	0.2679	73.426
920	0.2671	74.737
930	0.2762	73.737
940	0.28	69.935
950	0.2684	68.817

S-Parameters (continued)

Note: Vcc = 3.0 Vdc, T_A = 25 °C ± 3 °C.

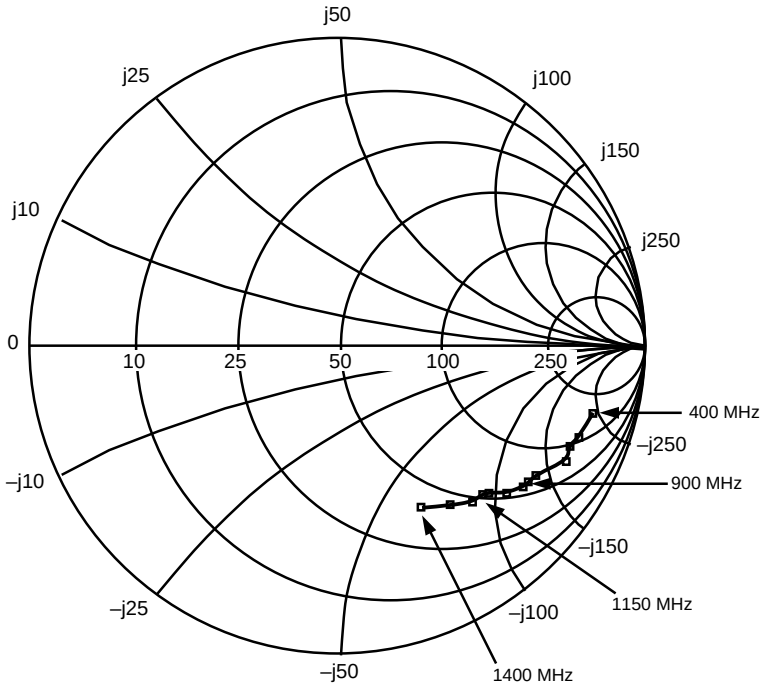


Figure 15. W2020 TX Offset LO Mixer Filter Port Input Impedance

Table 15. W2020 TX Offset LO Mixer Filter Port Differential Input S-Parameters

File: Txoffmx.s2p, W2020B TX Offset LO Mixer Port 1 = TF1, Port 2 = TF2, Vcc = 3.0 V, Source = –10 dBm								
Frequency (MHz)	Parameter							
	S11 M	S11 A	S21 M	S21 A	S12 M	S12 A	S22 M	S22 A
	S MA R	50						
400	0.8083	–16.913	0.0671	87.462	0.069	79.959	0.814	–16.571
500	0.7921	–21.134	0.0793	87.757	0.0838	82.363	0.7974	–20.968
600	0.775	–24.449	0.1008	89.84	0.0846	81.451	0.7848	–26.151
700	0.7974	–28.313	0.1102	72.828	0.0993	105.184	0.7359	–30.812
800	0.7423	–33.902	0.106	96.905	0.1134	85.302	0.757	–34.001
880	0.7364	–36.54	0.1131	92.264	0.1087	92.66	0.7331	–38.298
890	0.7353	–36.965	0.1124	92.532	0.1103	93.803	0.7314	–38.82
900	0.7343	–36.763	0.1035	94.79	0.1212	93.378	0.7302	–39.785
915	0.7328	–38.468	0.1127	93.359	0.1156	94.502	0.7258	–39.719
1000	0.7054	–42.55	0.1092	101.999	0.1095	97.071	0.7134	–43.504
1100	0.6648	–45.859	0.1231	107.479	0.1161	108.294	0.6827	–48.917
1150	0.6587	–47.349	0.1282	109.205	0.1263	112.206	0.6676	–51.389
1200	0.6509	–50.383	0.1281	111.67	0.1309	112.6	0.6487	–54.308
1300	0.6179	–56.662	0.1411	120.854	0.1458	120.192	0.6081	–61.389
1400	0.5773	–64.278	0.1656	130.436	0.1633	128.185	0.5554	–70.301

S-Parameters (continued)

Note: Vcc = 3.0 Vdc, T_A = 25 °C ± 3 °C.

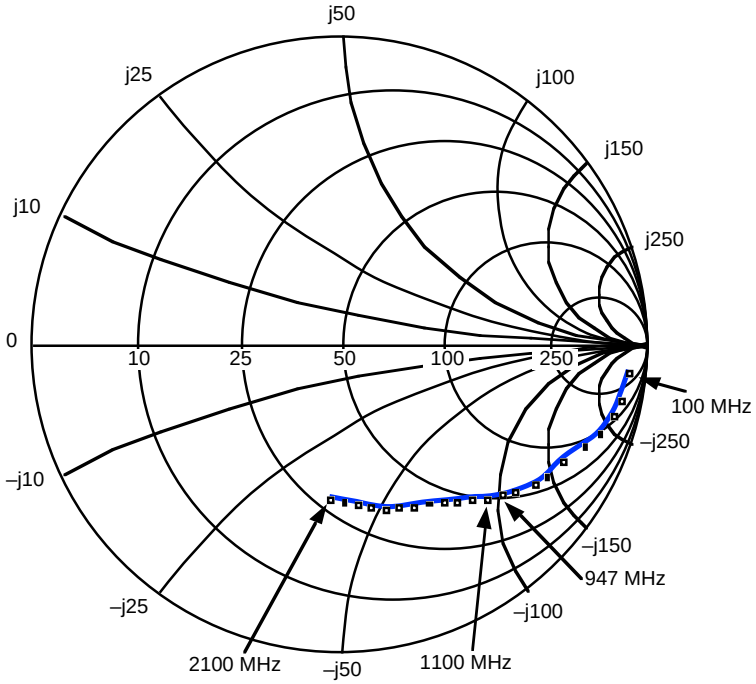


Figure 16. W2020 RF Mixer Input Impedance (S11)

S-Parameters (continued)

Note: Vcc = 3.0 Vdc, T_A = 25 °C ± 3 °C.

Table 16. W2020 RF Mixer Differential Input S-Parameters

File: Rfmxdfin.s2p, W2020B RF Mixer Differential Input Port1 = pin 56, Port2 = pin 57, 25 °C, Vcc = 3.0 V								
Frequency (MHz)	S-Parameter							
	S11 M	S11 A	S21 M	S21 A	S12 M	S12 A	S22 M	S22 A
	S MA R	50						
100	0.9193	–6.102	0.0352	50.941	0.0389	53.687	0.9144	–6.267
200	0.8947	–11.579	0.0734	46.269	0.074	45.7	0.8932	–11.776
300	0.8642	–16.21	0.0973	34.866	0.0996	35.672	0.864	–16.661
400	0.8312	–20.388	0.1243	27.108	0.119	27.687	0.8301	–20.274
500	0.8048	–24.153	0.1411	21.135	0.1357	19.643	0.812	–23.559
600	0.7881	–27.578	0.1498	9.663	0.1461	9.519	0.8018	–27.992
700	0.7744	–32.091	0.1358	–5.442	0.1515	–2.964	0.7918	–32.058
800	0.7491	–36.953	0.1296	–15.777	0.138	–13.305	0.7647	–37.788
900	0.7157	–41.328	0.1212	–20.143	0.124	–18.842	0.7357	–43.087
947.5	0.7043	–43.39	0.0973	–21.197	0.1067	–21.543	0.7284	–44.645
1000	0.6888	–45.417	0.1019	–18.632	0.1062	–20.315	0.714	–48.074
1100	0.6594	–49.051	0.0858	–17.347	0.0944	–22.024	0.6933	–52.63
1200	0.6297	–52.912	0.0754	–18.79	0.0834	–24.307	0.672	–58.187
1300	0.6058	–55.898	0.0681	–13.605	0.0736	–25.957	0.6503	–63.864
1400	0.584	–58.992	0.0618	–8.483	0.0668	–26.463	0.6318	–71.614
1500	0.5765	–63.039	0.0599	–4.518	0.0592	–25.993	0.6083	–78.229
1600	0.5644	–67.681	0.0562	4.51	0.0459	–28.621	0.5834	–85.956
1700	0.5441	–72.805	0.0535	18.901	0.0284	–29.109	0.5645	–94.368
1800	0.5231	–77.395	0.0542	28.329	0.0125	9.095	0.5403	–103.962
1900	0.5094	–82.229	0.057	29.388	0.0158	84.827	0.5198	–112.656
2000	0.4965	–88.304	0.0714	33.063	0.0454	91.377	0.496	–121.878
2100	0.4769	–94.367	0.0816	34.904	0.0608	86.941	0.4858	–132.115

S-Parameters (continued)

Note: Vcc = 3.0 Vdc, T_A = 25 °C ± 3 °C.

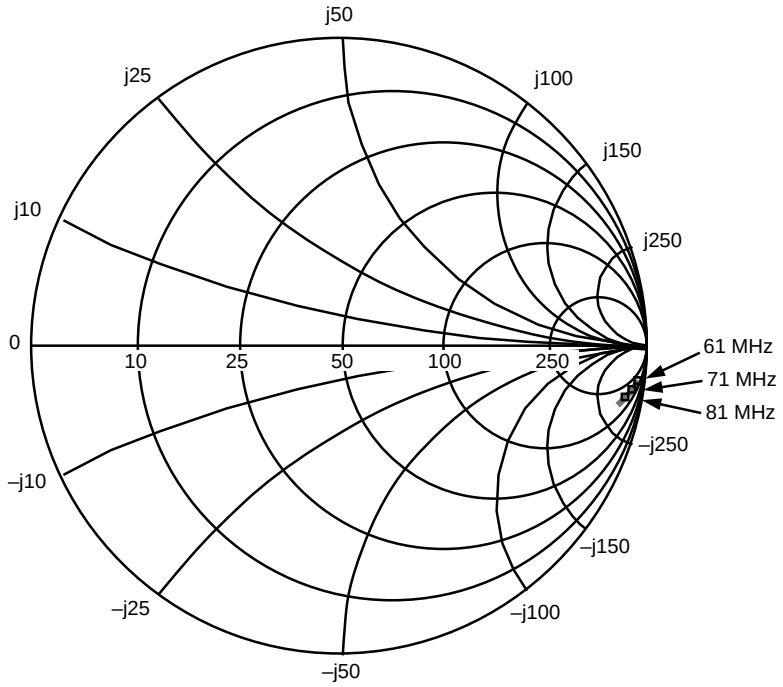


Figure 17. W2020 RF Mixer Output Impedance (S22)

Table 17. W2020 RF Mixer Differential Output S-Parameters

File: Ifmx20ot.s2p, W2020B RF Mixer Differential Output Port1 = pin59, Port2 = pin60, 25 °C, Vcc = 3.0 V, Span = 20 MHz								
	Parameter							
Frequency (MHz)	S11 M	S11 A	S21 M	S21 A	S12 M	S12 A	S22 M	S22 A
	S MA R	50						
61	0.9633	–6.951	0.0121	85.816	0.0115	81.366	0.9631	–7.066
63	0.962	–7.162	0.0124	86.163	0.0118	81.033	0.9627	–7.31
66	0.9605	–7.487	0.0133	85.929	0.0125	82.126	0.9609	–7.616
67	0.9599	–7.583	0.0135	85.209	0.0126	81.021	0.9605	–7.748
68	0.9583	–7.699	0.0136	85.729	0.0127	81.101	0.9602	–7.886
69	0.9586	–7.84	0.0134	83.353	0.0144	80.286	0.9595	–7.977
70	0.9581	–7.917	0.0142	85.374	0.0133	81.717	0.9588	–8.113
70.9	0.957	–8.031	0.0141	85.437	0.0134	82.357	0.9584	–8.176
71	0.9568	–8.042	0.0145	85.734	0.0134	81.668	0.9587	–8.199
71.1	0.9565	–8.062	0.0144	85.686	0.0136	81.249	0.9589	–8.207
72	0.9561	–8.104	0.0149	85.065	0.0136	81.423	0.9579	–8.314
73	0.9564	–8.206	0.0148	83.964	0.0137	82.047	0.9574	–8.406
74	0.9558	–8.367	0.0148	84.378	0.0139	81.626	0.957	–8.561
75	0.9544	–8.436	0.0155	84.16	0.0147	81.265	0.9561	–8.645
76	0.9545	–8.55	0.0154	84.857	0.0144	81.968	0.9553	–8.745
79	0.952	–8.861	0.0159	85.002	0.015	80.911	0.9537	–9.045
81	0.9505	–9.068	0.0163	85.103	0.0154	81.799	0.9517	–9.266

S-Parameters (continued)

Note: Vcc = 3.0 Vdc, T_A = 25 °C ± 3 °C.

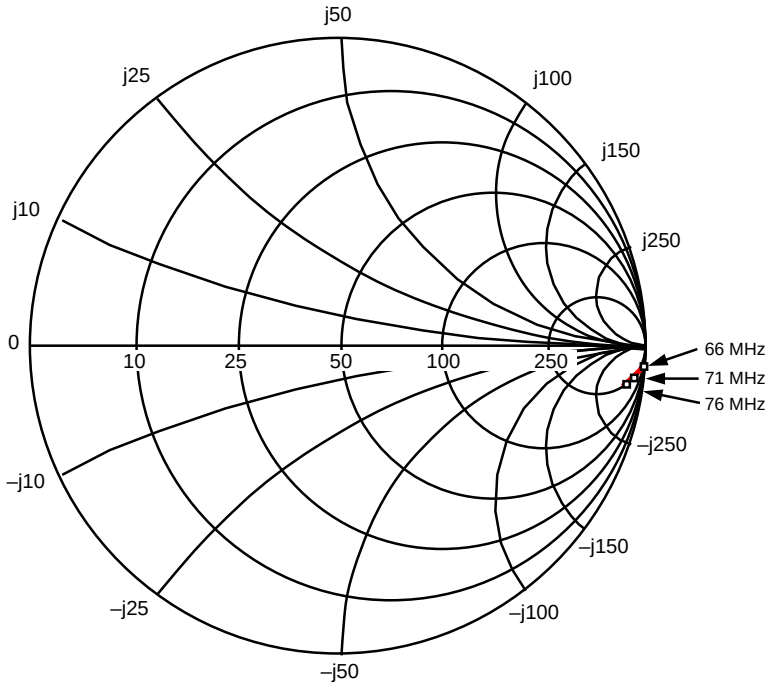


Figure 18. W2020 IF Amplifier Input Impedance (0 dB Setting)

Table 18. W2020 IF Amplifier Differential Input S-Parameters (0 dB Setting)

File: IF0dBin.s2p, W2020 Diff IF Input, 0 dB, AGC, Port1 = Pin3RIFI, Port2 = Pin2RIFREF								
Frequency (MHz)	Parameter							
	S11 M	S11 A	S21 M	S21 A	S12 M	S12 A	S22 M	S22 A
	S MA R	50						
66	0.9916	–2.967	0.0194	70.311	0.0194	68.102	0.9963	–4.031
67	0.9821	–3.931	0.0212	34.834	0.0221	56.041	0.9832	–3.937
68	0.9784	–4.428	0.0115	83.95	0.0231	41.592	0.9891	–4.158
69	0.9776	–4.67	0.0211	53.309	0.0302	66.624	0.9831	–4.922
70	0.9806	–4.881	0.0289	58.386	0.0212	50.118	0.9726	–4.847
70.9	0.9705	–5.739	0.0226	59.178	0.0281	53.409	0.9701	–5.053
71	0.9672	–6.095	0.0176	44.55	0.0216	54.996	0.9579	–5.453
71.1	0.9751	–5.476	0.0201	66.366	0.0201	70.123	0.9654	–5.353
72	0.9666	–6.111	0.0172	76.83	0.0228	66.777	0.9651	–5.699
73	0.9733	–5.672	0.0219	67.323	0.0242	49.423	0.9607	–6.047
74	0.9541	–6.675	0.0258	70.207	0.0282	61.454	0.9588	–6.45
75	0.9506	–5.985	0.0234	83.32	0.0235	51.821	0.9621	–7.26
76	0.9475	–7.067	0.0235	69.213	0.0189	50.405	0.9449	–7.154

S-Parameters (continued)

Note: Vcc = 3.0 Vdc, T_A = 25 °C ± 3 °C.

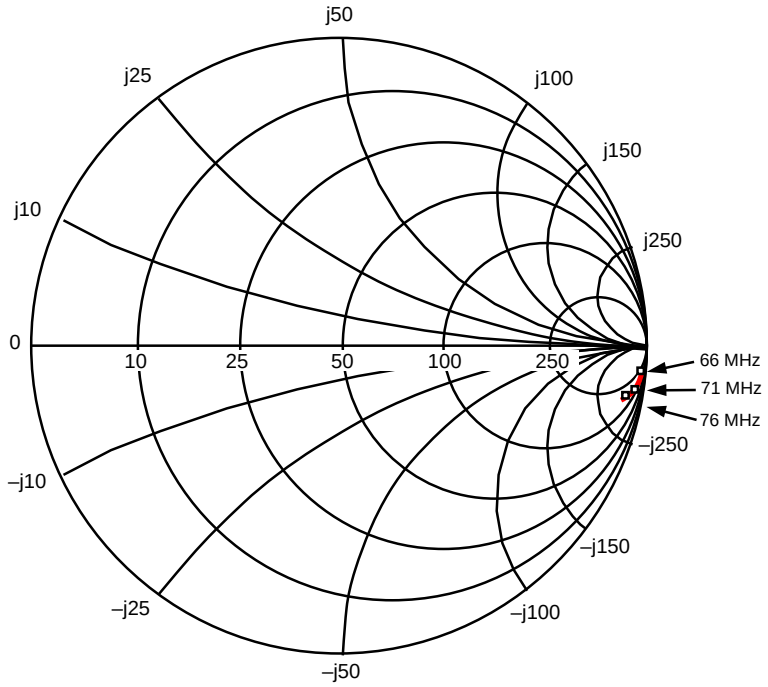


Figure 19. W2020 IF Amplifier Input Impedance (32 dB Setting)

Table 19. W2020 IF Amplifier Differential Input S-Parameters (32 dB Setting)

File: IF32dBin.s2p, W2020 Diff IF Input, 32 dB, AGC Port1 = Pin3RIFI, Port2 = Pin2RIFREF								
Frequency (MHz)	Parameter							
	S11 M	S11 A	S21 M	S21 A	S12 M	S12 A	S22 M	S22 A
	S MA R	50						
66	0.9669	–5.777	0.0706	54.748	0.0761	49.521	0.9821	–7.37
67	0.9709	–6.896	0.0762	45.216	0.075	47.308	0.9618	–7.065
68	0.9688	–7.31	0.0742	48.26	0.0848	45.612	0.9691	–7.502
69	0.958	–7.838	0.0819	47.711	0.0914	49.366	0.9582	–8.082
70	0.9641	–7.999	0.0882	47.613	0.0801	43.034	0.9513	–8.135
70.9	0.9531	–9.045	0.0816	42.382	0.0859	39.947	0.9512	–8.416
71	0.9521	–9.284	0.0753	39.879	0.0836	47.807	0.9439	–8.545
71.1	0.9571	–8.609	0.0792	43.612	0.0808	45.959	0.9417	–8.232
72	0.9522	–9.398	0.0802	48.049	0.0814	44.865	0.9494	–8.875
73	0.9544	–9.321	0.0776	46.53	0.0814	43.177	0.9409	–9.352
74	0.9396	–9.697	0.0804	42.861	0.0872	46.257	0.9411	–10.195
75	0.9402	–9.695	0.0757	45.796	0.0832	45.102	0.9341	–10.173
76	0.9289	–10.472	0.0851	52.399	0.0794	34.181	0.9286	–10.697

Characteristic Curves

Note: Unless otherwise noted, Vcc = 2.7 Vdc, T_A = 25 °C ± 3 °C.

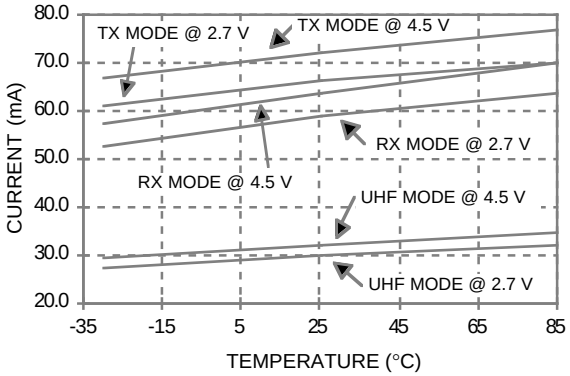


Figure 20. System Mode Supply Currents vs. Temperature and Vcc

UHF Synthesizer Performance

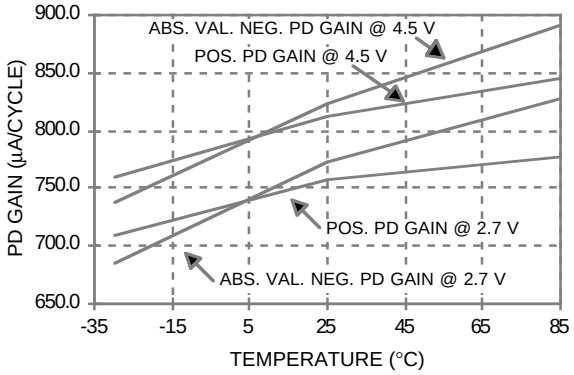


Figure 21. UHF Synthesizer Phase Detector Gain vs. Temperature and Vcc

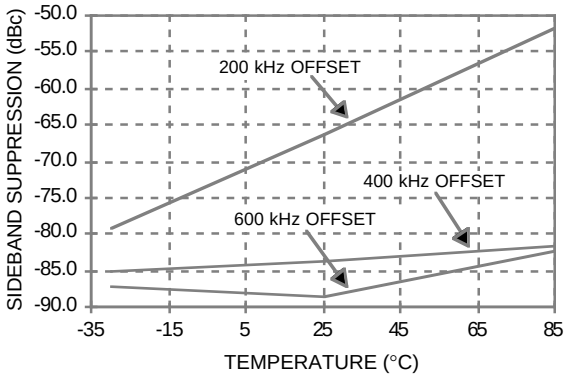


Figure 23. UHF Synthesizer Reference Sidebands vs. Temperature

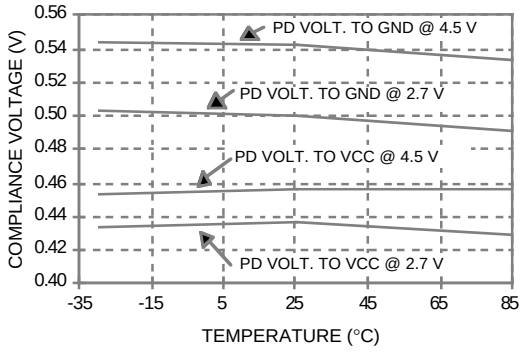


Figure 22. UHF Synthesizer Charge Pump Output Voltage Compliance vs. Temperature and Vcc

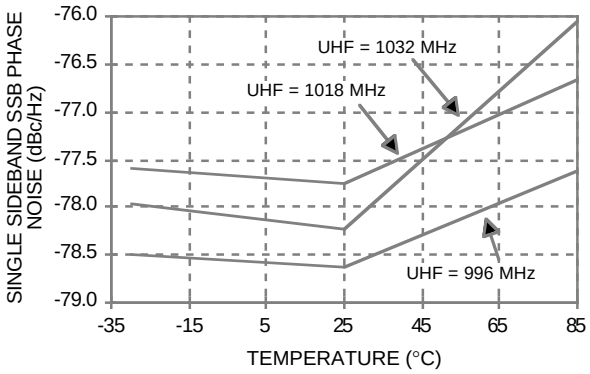


Figure 24. UHF Synthesizer Close-In Phase Noise vs. Temperature and UHF Frequency

Characteristic Curves (continued)

Note: Unless otherwise noted, Vcc = 2.7 Vdc, T_A = 25 °C ± 3 °C.

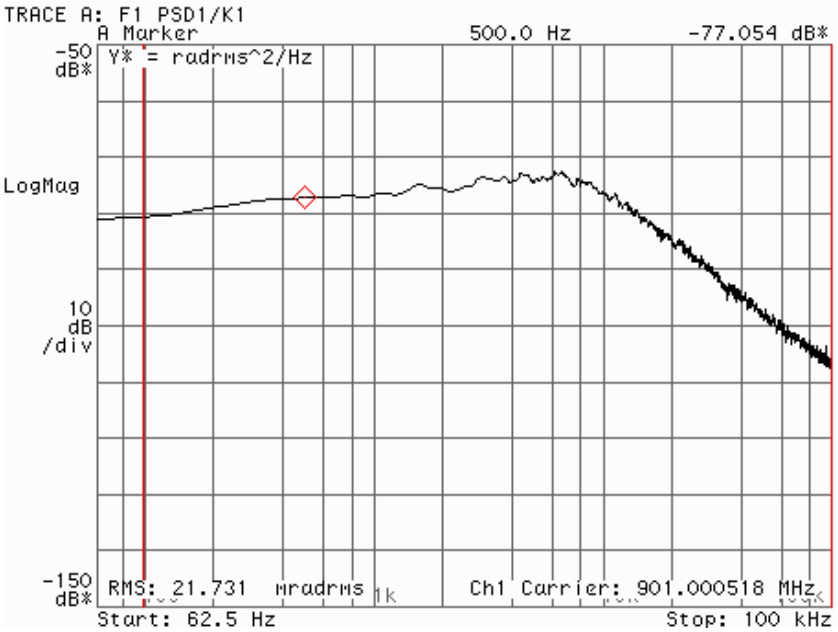


Figure 25. UHF Synthesizer Close-In SSB Phase Noise

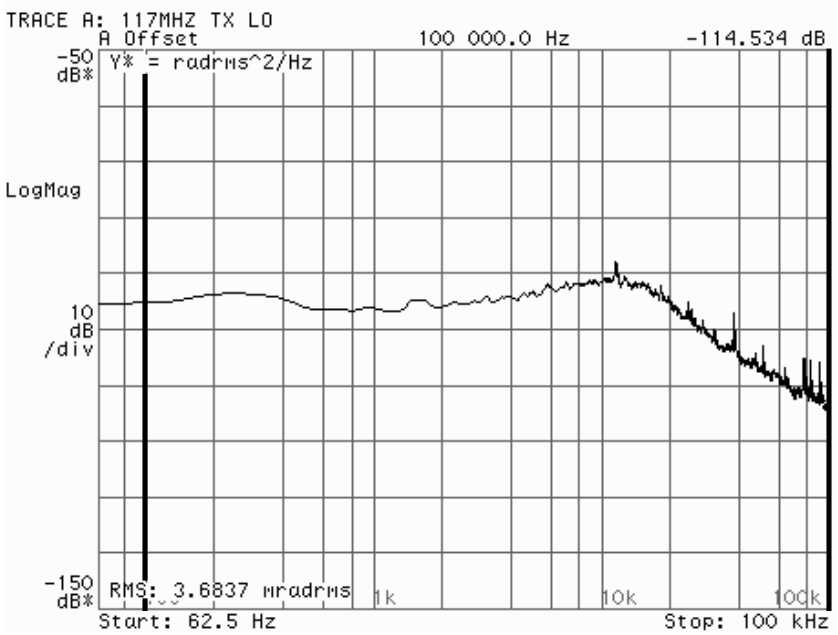


Figure 26. TX 117 MHz Fixed LO DSB Integrated Phase Noise

Characteristic Curves (continued)

Note: Unless otherwise noted, Vcc = 3.0 Vdc, T_A = 25 °C ± 3 °C.

RF Mixer Performance

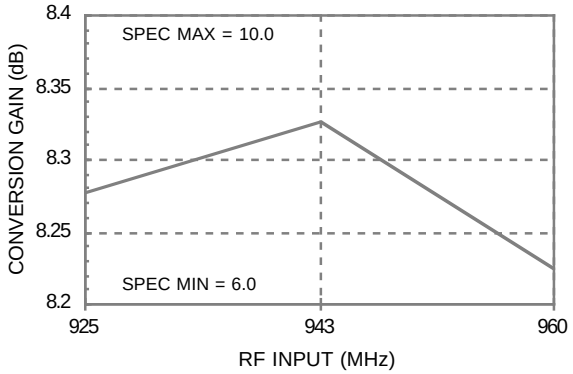


Figure 27. RF Mixer Gain vs. RF Input Frequency

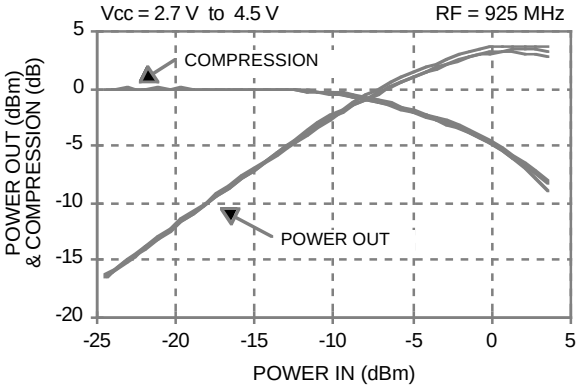


Figure 30. RF Mixer Gain Compression Characteristics

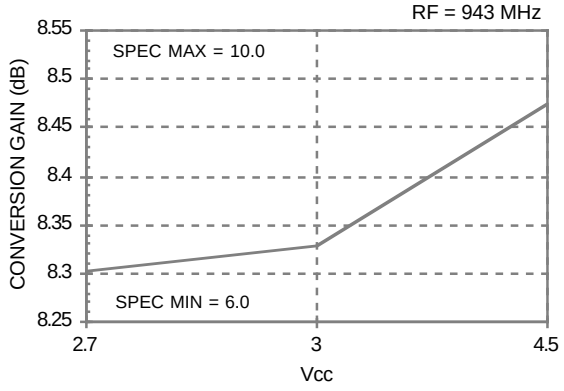


Figure 28. RF Mixer Gain vs. Vcc

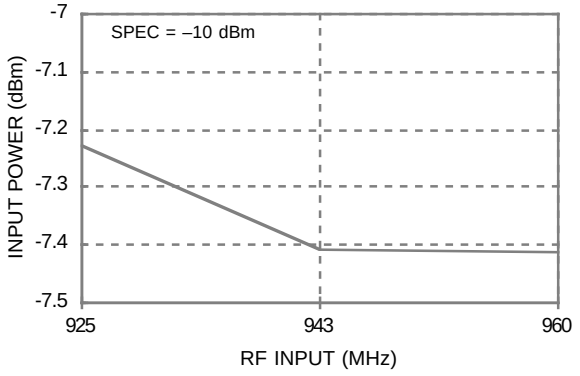


Figure 31. RF Mixer Input P-1 dB Compression Point vs. RF Input Frequency

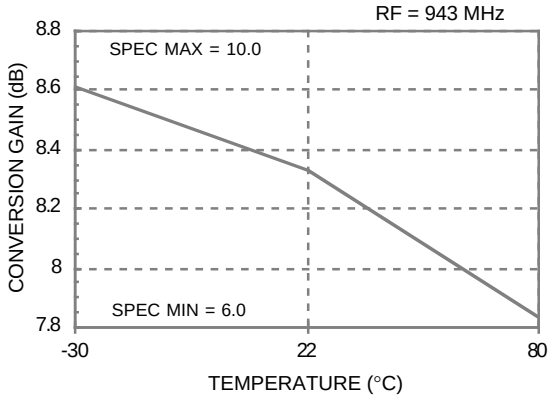


Figure 29. RF Mixer Gain vs. Temperature

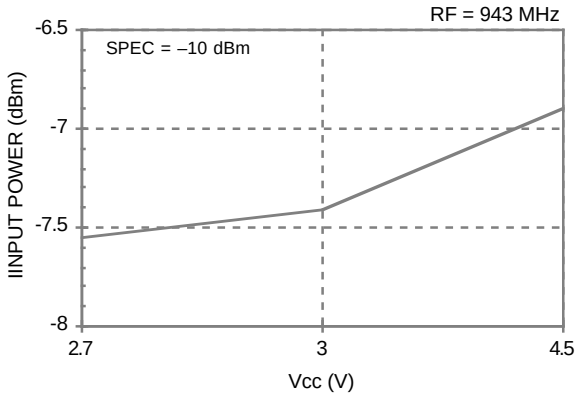


Figure 32. RF Mixer Input P-1 dB Compression Point vs. Vcc

Characteristic Curves (continued)

Note: Unless otherwise noted, Vcc = 3.0 Vdc, T_A = 25 °C ± 3 °C.

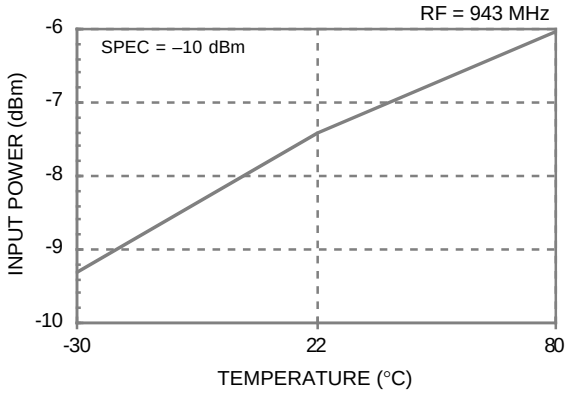


Figure 33. RF Mixer Input P-1 dB Compression Point vs. Temperature

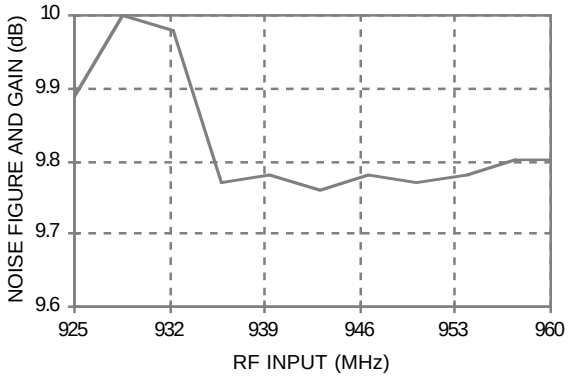


Figure 34. RF Mixer SSB Noise Figure vs. RF Input Frequency

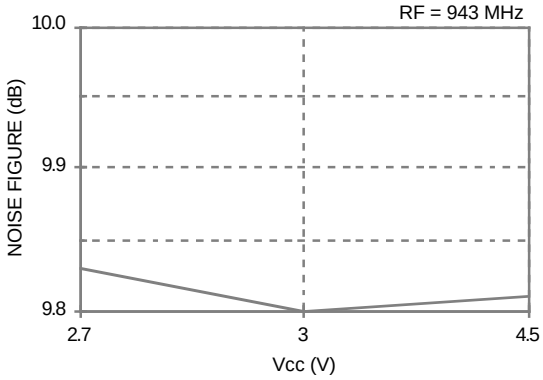


Figure 35. RF Mixer SSB Noise Figure vs. Vcc

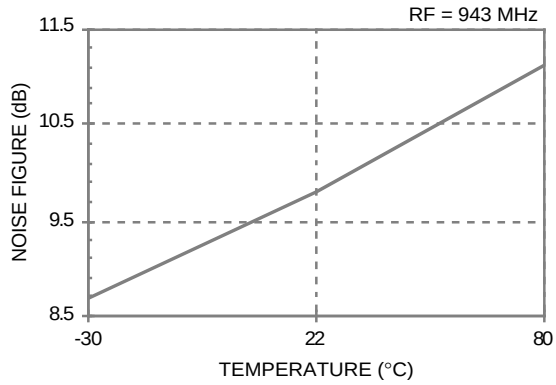


Figure 36. RF Mixer SSB Noise Figure vs. Temperature

Characteristic Curves (continued)

Note: Unless otherwise noted, Vcc = 3.0 Vdc, T_A = 25 °C ± 3 °C.

IF Strip Performance

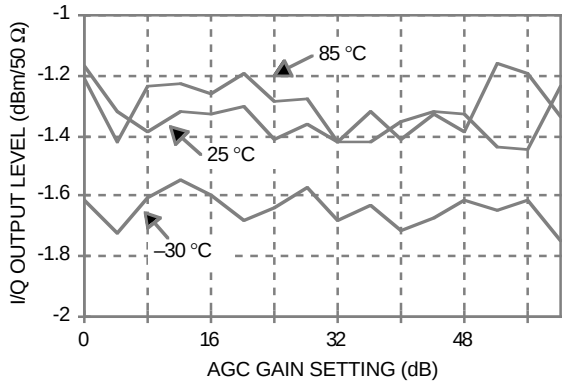


Figure 37. Overload Indicator Trip Point vs. AGC Setting and Temperature

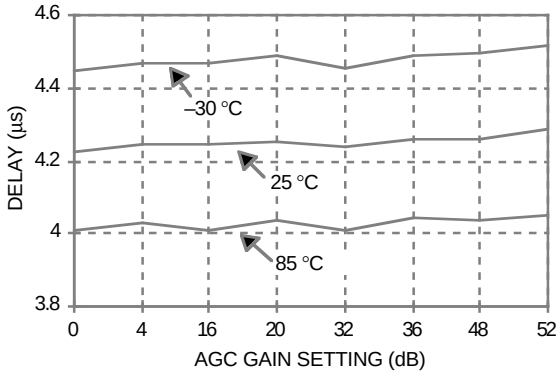


Figure 38. Overload Indicator Delay vs. AGC Setting and Temperature

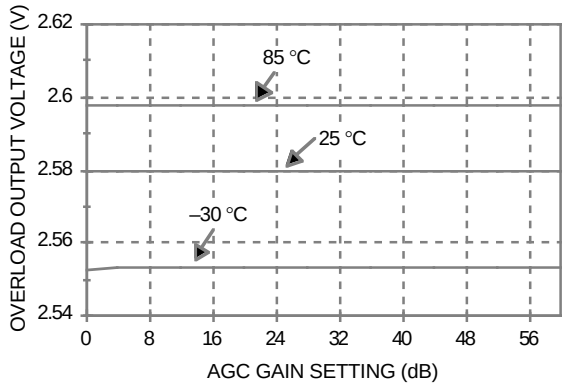


Figure 39. Overload Indicator Logic High-Level vs. AGC Setting and Temperature

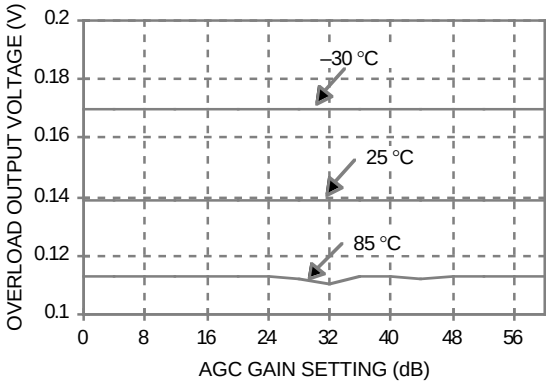


Figure 40. Overload Indicator Logic Low-Level vs. AGC Setting and Temperature

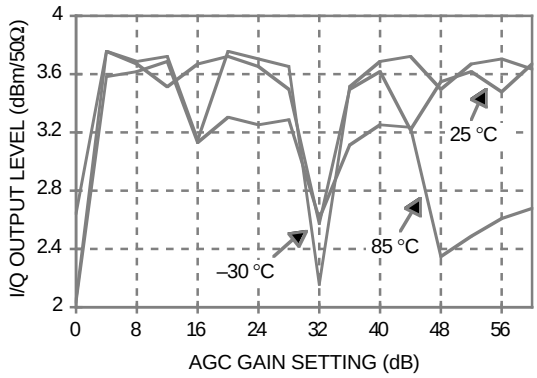


Figure 41. I/Q Output 1 dB Compression Point vs. AGC Setting and Temperature

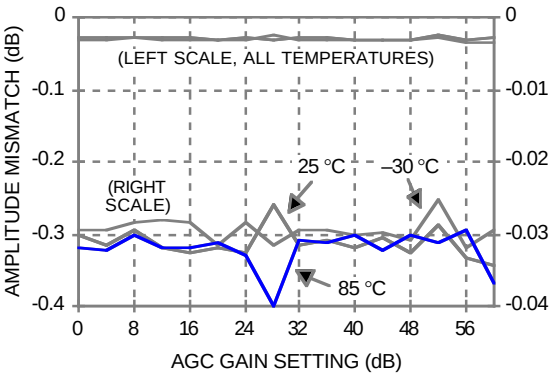


Figure 42. I/Q Amplitude Mismatch vs. AGC Setting and Temperature

Characteristic Curves (continued)

Note: Unless otherwise noted, Vcc = 2.7 Vdc, T_A = 25 °C ± 3 °C.

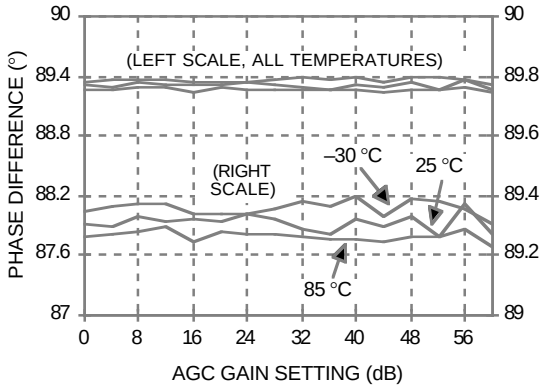


Figure 43. I/Q Phase Difference vs. AGC Setting and Temperature

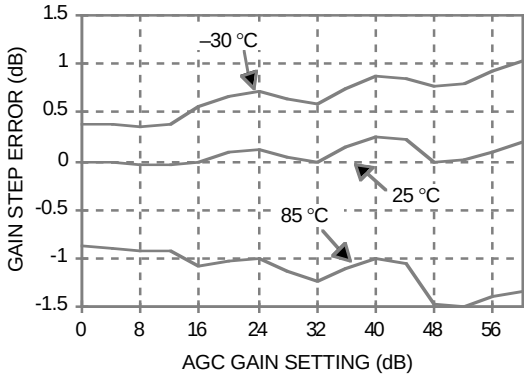


Figure 44. Gain Step Accuracy with 32 dB and 16 dB Gain Step Calibration

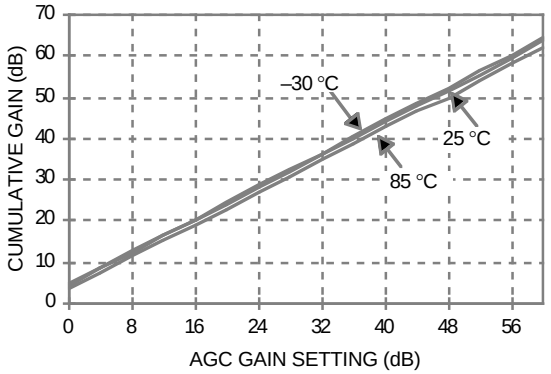


Figure 45. Cumulative Gain vs. AGC Setting and Temperature

Typical Modulator Performance

Note: Unless otherwise noted, Vcc = 3.0 Vdc, T_A = 25 °C ± 3 °C.

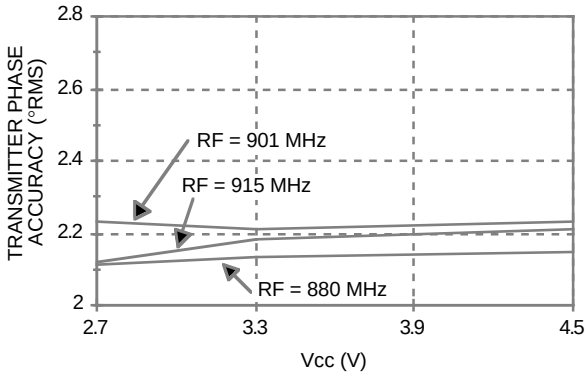


Figure 46. Transmitter RMS Phase Accuracy vs. Vcc and RF Output Frequency

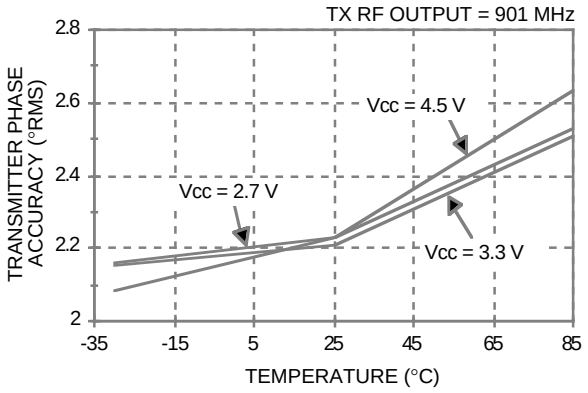


Figure 47. Transmitter RMS Phase Accuracy vs. Temperature and Vcc

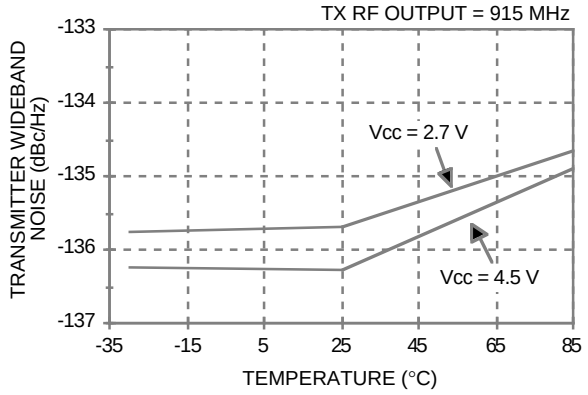


Figure 48. Transmitter Wideband Noise vs. Temperature and Vcc

Typical Modulator Performance (continued)

Note: Unless otherwise noted, Vcc = 3.0 Vdc, T_A = 25 °C ± 3 °C.

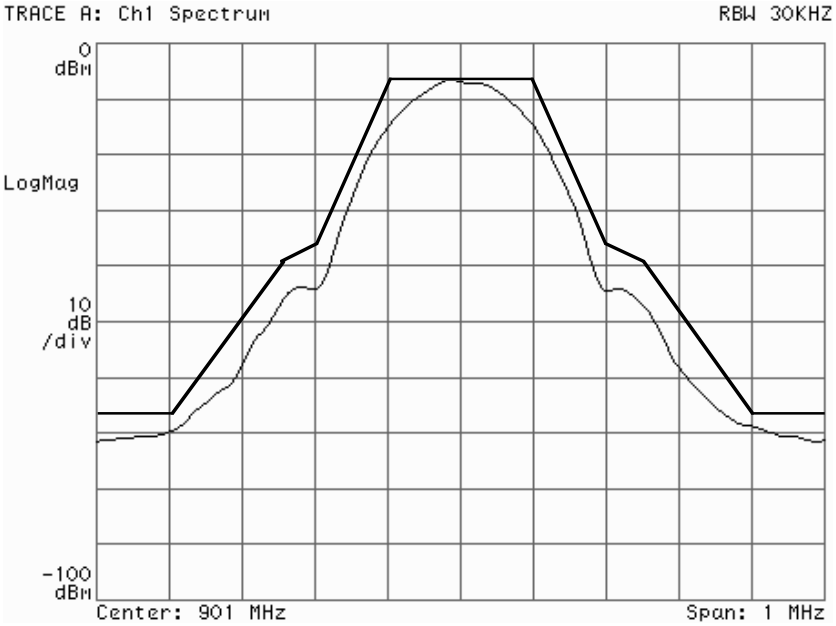


Figure 49. W2020B Output with GMSK Modulation Spectrum

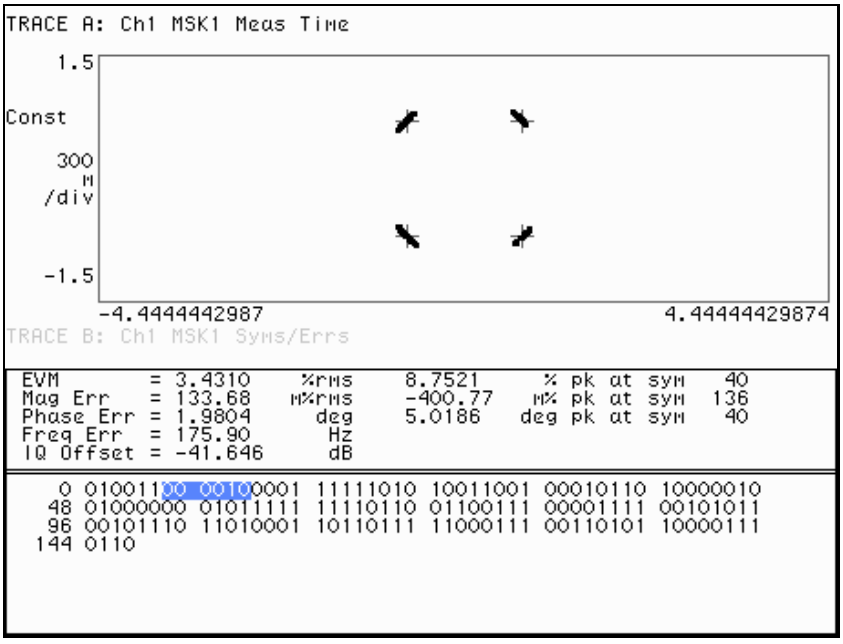


Figure 50. Demodulated GSM Transmitted Signal

Typical Modulator Performance (continued)

Note: Unless otherwise noted, Vcc = 3.0 Vdc, T_A = 25 °C ± 3 °C.

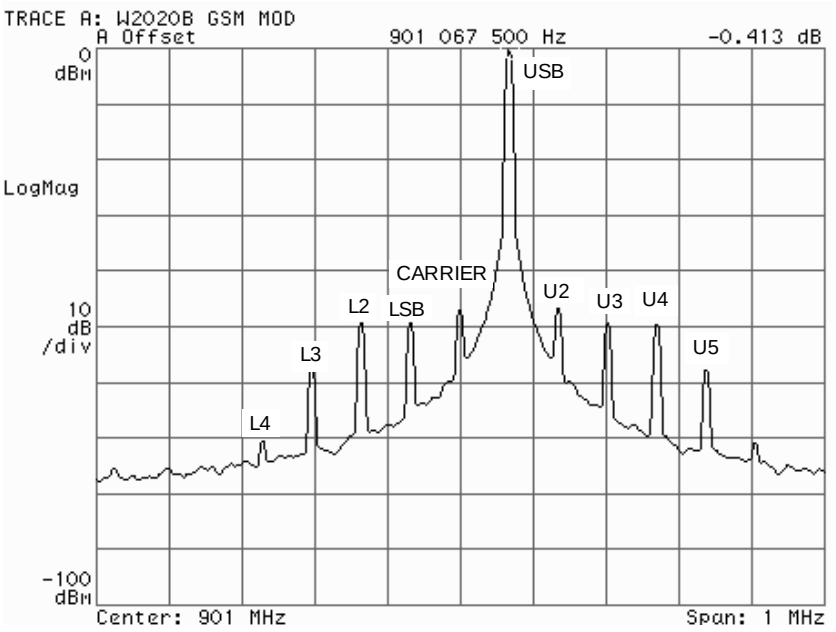


Figure 51. W2020 SSB Modulator Spectrum with 67.7 kHz IQ Inputs

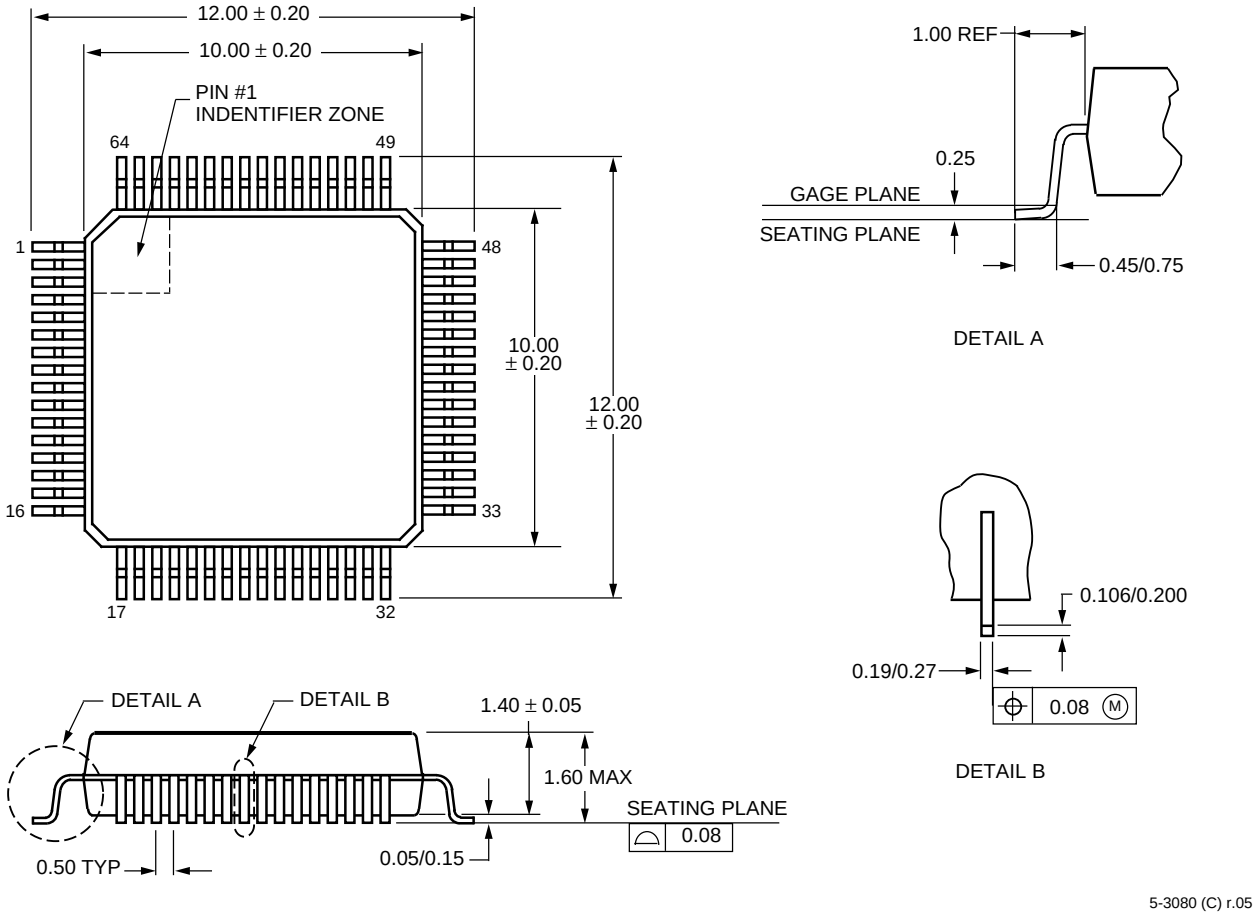
Evaluation Board Note

The ATTW2020 Evaluation Board is available for customer demonstration (see Ordering Information) of device performance characteristics. The board allows full characterization with RF laboratory bench equipment. Various applications of the device can be demonstrated on the evaluation board.

Outline Diagram

64-Pin TQFP

Dimensions are in millimeters.



5-3080 (C) r.05

Ordering Information

Device Code	Description	Package	Comcode
ATTW2020BBU	GSM Transceiver	64-pin TQFP	107645863
ATTW2020BBU-DB		Dry Pack	107645871
EVBW2020	Evaluation Board	Evaluation Board	107340218

Notes

Notes

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