

4-BIT MICROCONTROLLER***Table of Contents-***

1. GENERAL DESCRIPTION	3
2. FEATURES.....	3
3. PIN CONFIGURATION	6
4. PIN DESCRIPTION.....	7
5. BLOCK DIAGRAM	9
6. FUNCTIONAL DESCRIPTION	10
6.1 ROM Memory Map	10
6.2 RAM Memory Map.....	11
6.2.1 Special Control Reg. Area.....	11
6.2.2 Stack Reg. Area.....	12
6.2.3 Working Reg. Area	12
6.3 Internal Oscillator Circuit	13
6.4 Initial State	14
6.5 Input/Output	14
6.5.1 I/O Pull High and Open Drain Control.....	17
6.6 Serial Port.....	19
6.7 DTMF Generator.....	21
6.8 Beep Tone Generator	22
6.9 8-bit D/A Converter	23
6.10 Comparator.....	24
6.11 Timer 0-3.....	25
6.11.1 Arbitrary Waveform Generator	32
6.12 Interrupt.....	33
6.12.1 Interrupt Control Register	33
6.12.2 Interrupt Enable Flag.....	34
6.13 Operating Mode	34
6.14 Initial Condition Register of EPROM Program Method	39
6.15 Reset	39

W921E880A/W921C880



7. ADDRESSING MODE	40
7.1 ROM Addressing Mode	40
7.2 RAM Addressing Mode	40
7.3 Look-up Table Addressing Mode (1 Word/2 Cycles)	42
8. SPECIAL CONTROL REG. FORMAT	43
9. INSTRUCTION MAP	45
10. INSTRUCTION SETS	48
11. ABSOLUTE MAXIMUM RATINGS	51
12. ELECTRICAL CHARACTERISTICS	52
12.1 AC Characteristics	52
12.2 DC Characteristics	54
13. PACKAGE DIMENSIONS	56
80-pin QFP	56

W921E880A/W921C880



1. GENERAL DESCRIPTION

The W921E880A/W921C880 are 4-bit micro-processor fabricated by CMOS process. With a single channel DTMF generator, an 8-bit D/A converter circuit, a built in four by one channel comparator circuit and four multi-function timers. The excellent memory structure, 8K super EPROM in W921E880A and 8K mask ROM in W921C880 for program code and 1536 x 4 bit RAM minimize the need for external memory devices. The W921E880A/W921C880 provides good solution for consuming application, especially for telecommunication design with few external components.

Using the serial transmit/receive function, the W921E880A/W921C880 can interface with the Winbond LCD driver IC using the serial control circuit.

2. FEATURES

Memory

- ROM (Super EPROM): $8K \times 10$ bits
- RAM: 1536×4 bits
 - 64×4 bit Special registers
 - 16×4 bit Working registers
 - 128×4 bit General registers
 - 304×4 bit Multi-purpose registers
 - 4 bit serial buffer registers
 - $512 \times 4\text{-bit} \times 2$ banks

Dual-clock Operation

- Crystal or RC for the main system clock: RC up to 4 MHz
Crystal for 400 K, 800 K, 2 M, 3.58 M, 4 MHz
- Crystal for subsystem clock: 32.768 KHz

I/O Pins

- 32 bidirectional and individually controllable I/O lines:
 - P0 Port: P0.0–P0.3 large drive current Pins
 - P1 Port: P1.0–P1.3 large drive current Pins
 - P2 Port: P2.0–P2.3 large sink current pins and open drain option
 - P3 Port: P3.0–P3.3 multi-function I/O
 - P4 Port: P4.0–P4.3 open drain and pull high resistor option, multi-function I/O
 - P5 Port: P5.0–P5.3 multi-function I/O
 - P6 Port: P6.0–P6.3 open drain and pull high resistor option, multi-function I/O
 - P7 Port: P7.0–P7.3 large sink current pins and open drain option
- 32 bidirectional I/O lines:
 - P8 Port: P8.0–P8.3 large drive current pins
 - P9 Port: P9.0–P9.3 large sink current pins and open drain option

- PA Port: PA.0–PA.3 open drain and pull high resistor option
- PB Port: PB.0–PB.3 open drain and pull high resistor option
- PC Port: PC.1–PC.3 open drain and pull high resistor option
- PD Port: PD.0–PD.3 open drain and pull high resistor option
- PE Port: PE.0–PE.3
- PF Port: PF.0–PF.3

Interrupt

- Four External sources: INT0 (P4.3)
P4 Port (P4.0–P4.2)
- Six Internal sources: Timer 0
Timer 1
Timer 2
Timer 3
Comparator
Serial Port

Timer/Counter

- Timer 0: 2–19 order divider (double source)
Auto-reload timer
Watch-dog timer
- Timer 1: 2–19 order divider
Auto-reload timer
Arbitrary waveform generator
External event counter
- Timer 2: 2–19 order divider
Auto-reload timer
Arbitrary waveform generator
Period/Pulse width measurement function
- Timer 3: 2–19 order divider
Auto-reload timer

Operating Mode (System Clock)

- Normal mode: System clock operating
- HOLD mode: no operation except for oscillator (System clock stops only)
- STOP mode: no operation including oscillator



DTMF Generator and 8-bit D/A Converter

- One Channel DTMF Generator
- One Channel 8-bit D/A Converter

Voltage Comparator

- Four by one Channel Voltage Comparator

Serial I/O Interface

- Clock Synchronous multi-nibbles Serial Transmitter/Receiver Interface

Stack

- 8-bit Stack Pointer

Address Mode

- ROM: Indirect call addressing mode
Long jump/call addressing mode
- RAM: Direct addressing mode
Indirect addressing mode
Working reg. addressing mode
- Look-up table addressing mode

Instruction Sets

- 117 Instruction sets

Operating Voltage

- 2.8 to 5.5V operating voltage for W921E880A EPROM Type
- 2.4 to 5.5V operating voltage for W921C880 Mask ROM Type

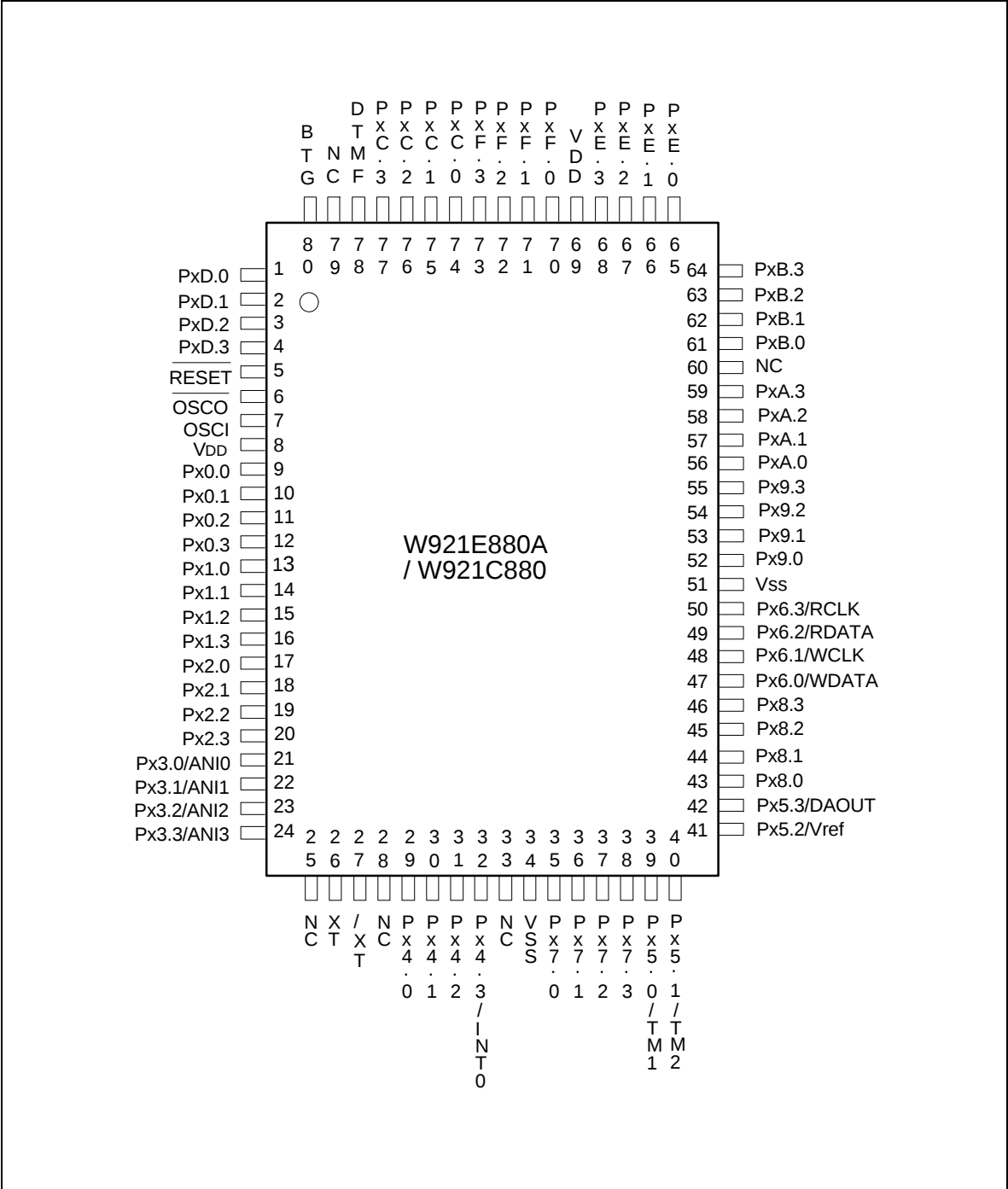
Package Type

- Packaged in 80-pin QFP

W921E880A/W921C880



3. PIN CONFIGURATION



4. PIN DESCRIPTION

SYMBOL	I/O	FUNCTION
OSCI	I	Main-oscillator input pin with internal cap.
$\overline{\text{OSCO}}$	O	Main-oscillator output pin.
PA.0–PA.3	*I/O	I/O port A.
PB.0–PB.3	*I/O	I/O port B.
PC.0–PC.3	*I/O	I/O port C. PC.3 can be as 32.768 KHz output buffer.
PD.0–PD.3	*I/O	I/O port D.
PE.0–PE.3	I/O	I/O port E.
PF.0–PF.3	I/O	I/O port F.
P0.0–P0.3	I/O	I/O with large drive current pin.
P1.0–P1.3	I/O	I/O with large drive current pin.
P2.0–P2.3	∇ I/O	I/O with large sink current pin.
P3.0/ANI0 P3.3/ANI3	I/O	I/O port 3 or Analog input pins (ANI0–ANI3).
P4.0	*I/O	I/O port 4.0 or the port P4.0 interrupt input pin.
P4.1	*I/O	I/O port 4.1 or the port P4.1 interrupt input pin.
P4.2	*I/O	I/O port 4.2 or the port P4.2 interrupt input pin.
P4.3/INT0	*I/O	I/O port 4.3 or the INT0 input pin.
P5.0/TM1	I/O	I/O port 5.0 or the control pin of the TIMER 1.
P5.1/TM2	I/O	I/O port 5.1 or the control pin of the TIMER 2.
P5.2/VREF	I/O	I/O port 5.2 or the Vref input pin of the comparator.
P5.3/DAOUT	I/O	I/O port 5.3 or the output pin of the 8bit D/A.
P6.0/WDATA	*I/O	I/O port 6.0 or the data output pin of the serial interface.
P6.1/WCLK	*I/O	I/O port 6.1 or the clock I/O pin of WDATA.
P6.2/RDATA	*I/O	I/O port 6.2 or the data input pin of the serial interface.
P6.3/RCLK	*I/O	I/O port 6.3 or the clock I/O pin of RDATA.
P7.0–P7.3	∇ I/O	I/O with large sink current pin.
P8.0–P8.3	I/O	I/O with large drive current pin.
P9.0–P9.3	∇ I/O	I/O with large sink current pin.

W921E880A/W921C880



4. Pin Description, continued

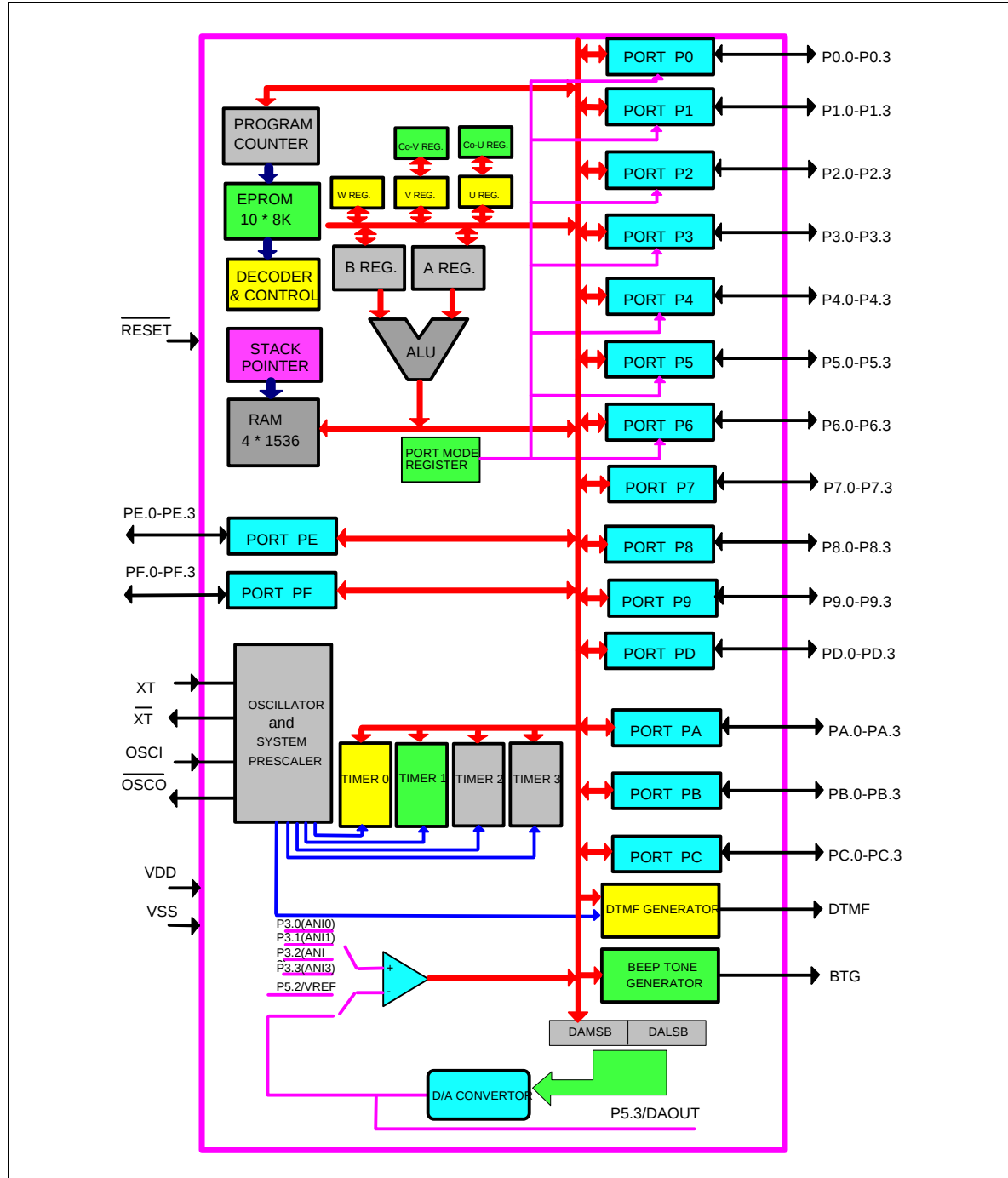
SYMBOL	I/O	FUNCTION
DTMF	O	Dual tone multi-frequency output pin.
BTG	O	Beep Tone Generator output pin.
$\overline{\text{RESET}}$	I	Reset input pin with low active.
VDD	I	Positive power supply input pin.
VSS	I	Negative power supply input pin.
XT	I	32.768 KHz subsystem clock input pin with internal cap.
$\overline{\text{XT}}$	O	32.768 KHz subsystem clock output pin.

Notes:

* open drain and pull high resistor option by software

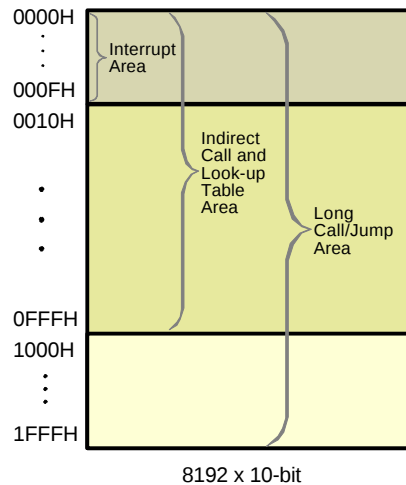
‡ open drain option by software

5. BLOCK DIAGRAM



6. FUNCTIONAL DESCRIPTION

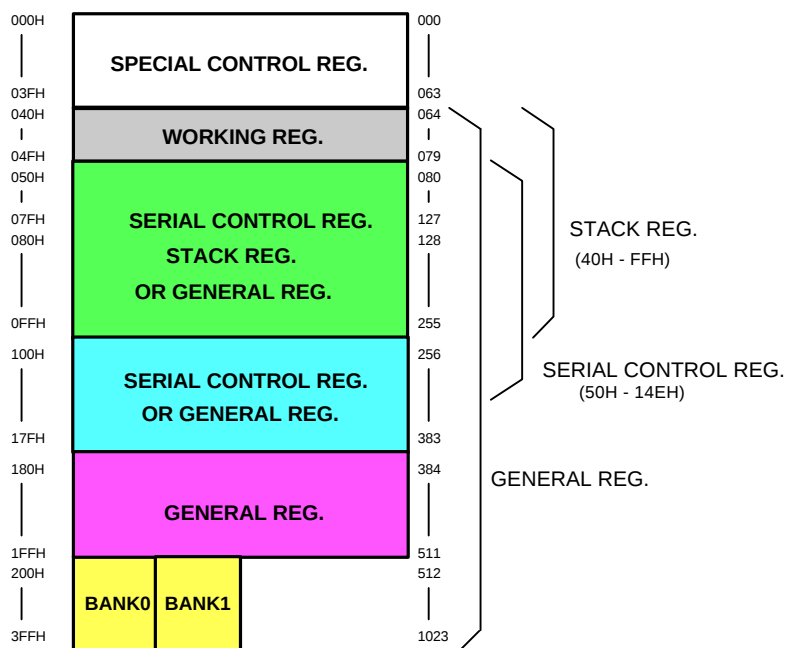
6.1 ROM Memory Map



0000H	JMPL Instruction (RESET)
0001H	XXXXXX XXXXXX
0002H	JMPL Instruction (INT0)
0003H	XXXXXX XXXXXX
0004H	JMPL Instruction (TM 0)
0005H	XXXXXX XXXXXX
0006H	JMPL Instruction (TM1)
0007H	XXXXXX XXXXXX
0008H	JMPL Instruction (TM 2)
0009H	XXXXXX XXXXXX
000AH	JMPL Instruction (Comparator / TM 3)
000BH	XXXXXX XXXXXX
000CH	JMPL Instruction (P4.0 to P4.2 - 3 PINS)
000DH	XXXXXX XXXXXX
000EH	JMPL Instruction (SERIAL PORT)
000FH	XXXXXX XXXXXX

PRIORITY: RESET > INT0 > TM0 > TM1 > TM2 > (Comparator / TM3) > P4.0 to P4.2 > SERIAL PORT

6.2 RAM Memory Map



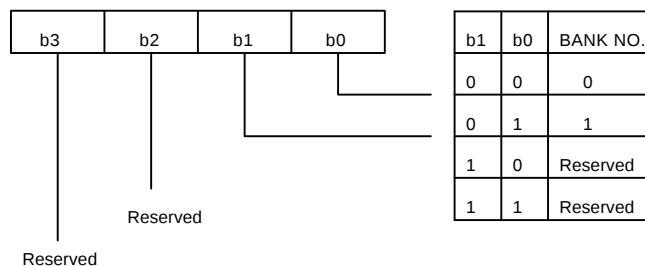
6.2.1 Special Control Reg. Area

There are 64 reg. $\times$ 4 bits in the special control register area. All control registers such as the DTMF Control Reg., System Clock Control Reg. ...etc. are in this area. Please refer to the Special Control Reg. Format.

Bank Select Reg.

BKSR REG: (ADDRESS = 001H)

(Default data = 0H)



The Bank Select Reg. can select the active bank. The memory size of each bank is 512*4 bits. Bank 0 and bank 1 are normal SRAM.



6.2.2 Stack Reg. Area

There are 8 bit stack pointers in this chip located at addresses 040H – 0FFH. After a power on reset the stack pointer will be set to 0FFH. The stack pointer will be decreased by 4 each time a CALLP or interrupt occurs, and will be increased by 4 each time the RTN or RTNI instruction is executed. The format of the stack pointer is shown in the following table.

0F8H	Z	C	—	PC12	STACK 1
0F9H	PC11	PC10	PC9	PC8	
0FAH	PC7	PC6	PC5	PC4	
0FBH	PC3	PC2	PC1	PC0	
0FCH	Z	C	—	PC12	STACK 0
0FDH	PC11	PC10	PC9	PC8	
0FEH	PC7	PC6	PC5	PC4	
0FFH	PC3	PC2	PC1	PC0	

6.2.3 Working Reg. Area

The area located from 040H to 04FH is known as the Working Reg. The instruction MOV WRn, A or MOV A, WRn can move the A reg. data to the Working reg. or move the Working reg. data to the A reg. directly within 1 word/1 machine cycle. Unlike other direct instructions such as MOV Mx, A or MOV A, Mx, these instructions use 2 words/2 machine cycles. Therefore, the Working reg. can reduce the ROM program memory size and improve the control speed of the application circuit.

For arithmetic and logic operations only WR0–WR7 are available, that is only 040H to 047H can be active.

The instructions are as follow:

```

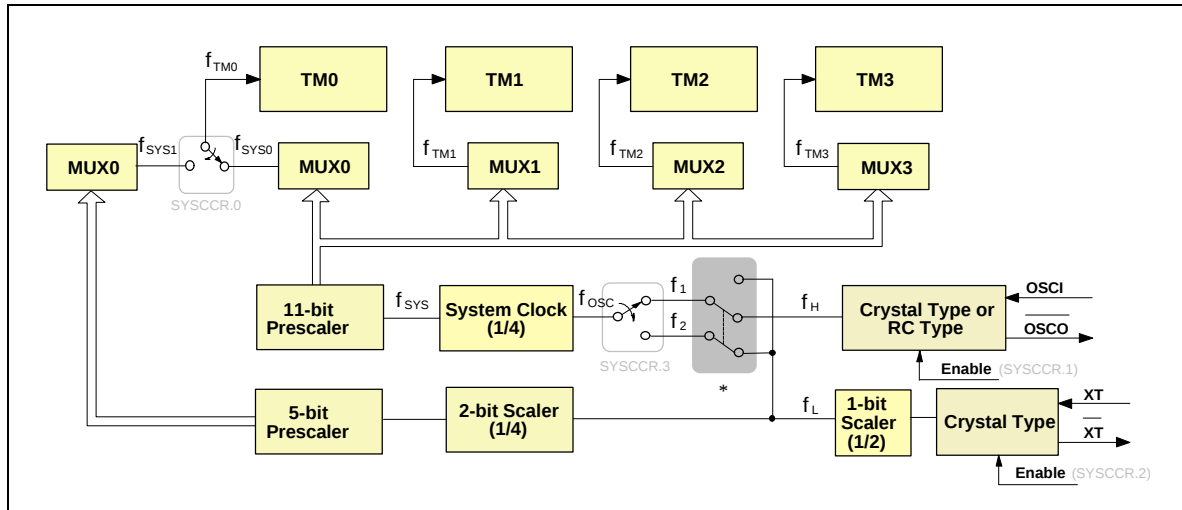
ADD  A,  WRx
ADC  A,  WRx
SUB  A,  WRx
SBC  A,  WRx
ANL  A,  WRx
ORL  A,  WRx
XRL  A,  WRx
CMP  A,  WRx

```

where x = 0 -- 7.

6.3 Internal Oscillator Circuit

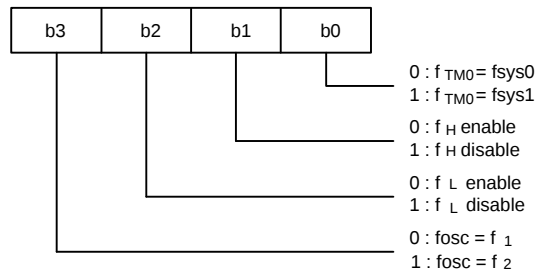
There are dual clocks in this chip, one is a high speed clock, the other a low speed clock. The block diagram is shown below:



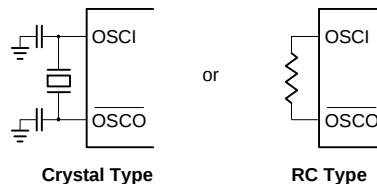
* Default: crystal type, $f_1=f_H$, $f_2=f_L$ (refer to 6.14 INI register)

The format of the system clock control reg. (SYSCCR) is shown below:

SYSCCR REG: (ADDRESS = 000H, Default data = 0H)



The W921E880A/W921C880 provides a crystal or RC oscillation circuit selected by bit0 of the INI register (refer to 6.14 INITIAL CONDITION Section) to generate the system clock through external connections. If a crystal oscillator is used, a crystal or ceramic resonator must be connected to OSCI and OSCO, and the capacitor must be connected if an accurate frequency is needed. The oscillator configuration is shown as follows.



W921E880A/W921C880



6.4 Initial State

The W921E880A/W921C880 is reset either by power-on reset or by using the external $\overline{\text{RESET}}$ pin. The initial state of the W921E880A/W921C880 after the reset function is executed is described below. The EVF interrupt request signal register value is random, so user must do CLR EVF, #1111111b instruction to clear all interrupt request signals after power-on reset.

Program counter (PC)	0000H
Stack pointer	0FFH
Special function registers	Refer to special control register table
TM0, TM1, TM2, TM3 input clock	Fosc/8
TM0, TM1, TM2, TM3 contents	0FFH
Input/Output	Input mode
PM registers	1111B
DTMF output	Disable (H-Z)
EVF interrupt request signal register	Random

6.5 Input/Output

There are 64 I/O pins (4 pins $\times$ 16 ports) including 12 large drive current pins, and 12 large sink current pins in this chip. All the I/O pins will remain in an input mode after a power on reset.

The input or output status of port 0 to port 7 can be controlled by the port mode register PMx, where x = 0 to 7. A zero indicates the corresponding pin is an output, a one indicates the relative pin is an input. For example, MOV PM0, #0101B sets P0.0 and P0.2 as inputs and P0.1 and P0.3 as outputs. The I/O instructions cannot affect the I/O status in Port 0 to Port 7.

The input or output mode of port 8 to port F only can be decided by I/O instructions. For example, MOV A, Px will change Px to input mode and MOV Px, A will change it to output mode.

The I/O instructions are described as follows:

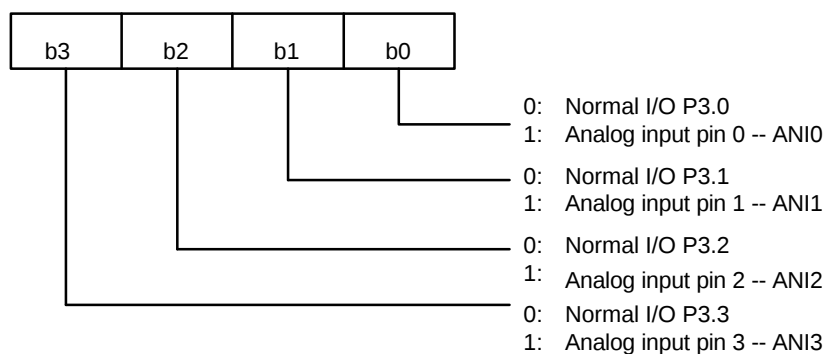
```
MOV    A, Px    input Port x to A reg.
MOV    B, Px    input Port x to B reg.
MOV    Px, A    output A reg. data to Port x.
MOV    Px, B    output B reg. data to Port x.
```

- * P0.0–P0.3: Four 10 mA drive current pins
Normal I/O pins only.
- * P1.0–P1.3: Four 10 mA drive current pins
Normal I/O pins only.
Normal function is the same as port P0
- * P2.0–P2.3: Four 15 mA sink current pins
Normal I/O pins only.
Normal function is the same as port P0

* P7.0–P7.3: Four 15 mA sink current pins
Normal I/O pins only.
Normal function is the same as port P0

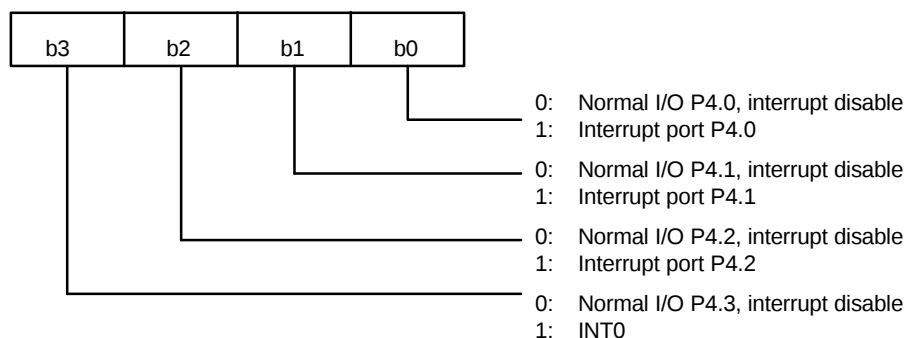
* P3.0–P3.3: Multi-function I/O pins.
Normal function is the same as port P0
Special function input pins

P3IO REG: (ADDRESS = 00FH)
(Default data = 0H)



* P4.0–P4.3: Multi-function I/O pins.
Normal function is the same as port P0
Special function input pins

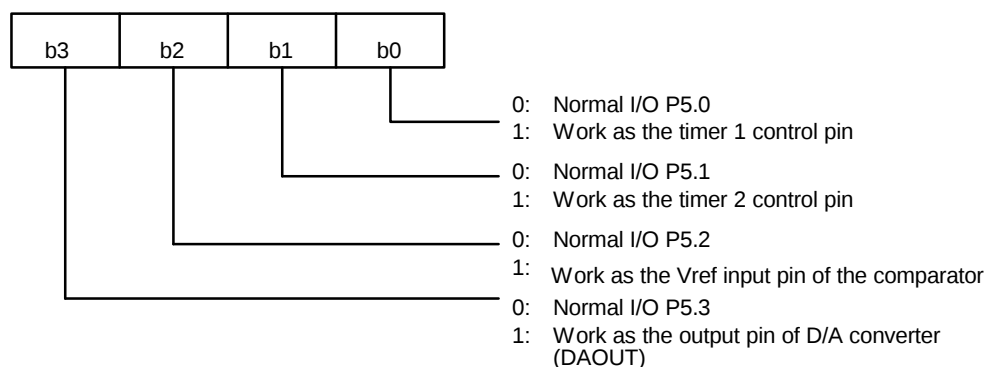
P4IO REG: (ADDRESS = 010H)
(Default data = 0H)





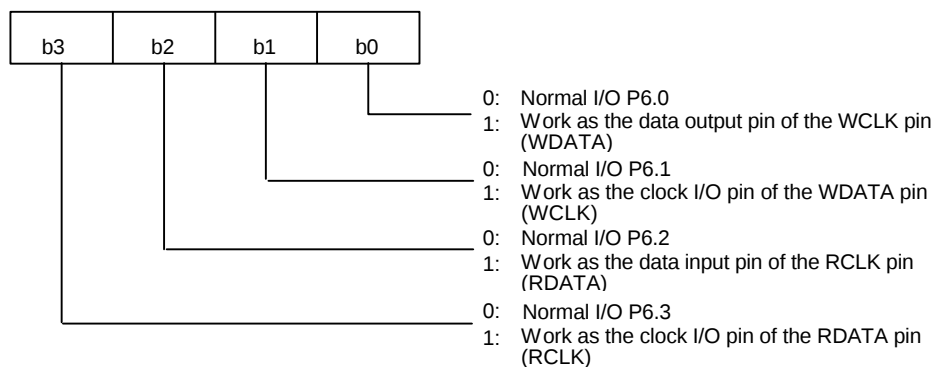
- * P5.0–P5.3: Multi-function I/O pins.
Normal function is the same as port P0
Special function
P5IO REG: (ADDRESS = 011H)

(Default data = 0H)



- * P6.0–P6.3 : Multi-function I/O pins.
Normal function is the same as port P0
Special function
P6IO REG: (ADDRESS = 012H)

(Default data = 0H)



- * P8.0–P8.3 : Four 10 mA drive current pins
Normal I/O pins only.
Normal function is the same as port P0
- * P9.0–P9.3 : Four 15 mA sink current pins
Normal I/O pins only.
Normal function is the same as port P0
- * PA.0–PA.3 : Normal I/O pins only.
Normal function is the same as port P0
- * PB.0–PB.3 : Normal I/O pins only.



- Normal function is the same as port P0
- * PC.0–PC.3: Normal I/O pins only.
Normal function is the same as port P0
 - * PD.0–PD.3: Normal I/O pins only.
Normal function is the same as port P0
 - * PE.0–PE.3: Normal I/O pins only.
Normal function is the same as port P0
 - * PF.0–PF.3: Normal I/O pins only.
Normal function is the same as port P0

6.5.1 I/O Pull High and Open Drain Control

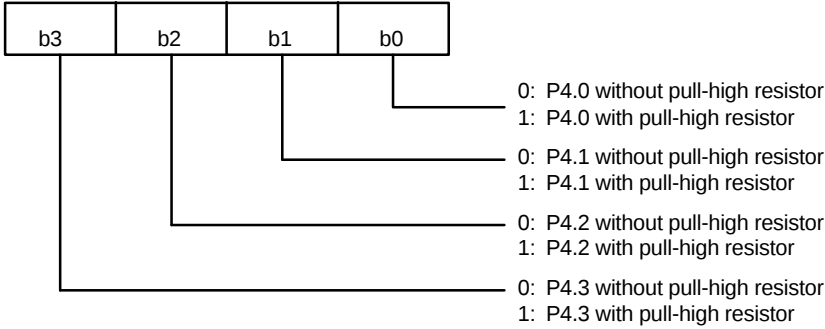
Some of the above I/O ports can be set up with a pull-high resistor or as an open drain. The user can program the I/O through the special register so that the I/O can have a pull-high resistor or open drain characteristics.

All pull-high resistors in the following table are 400 K Ω in a 3.0 voltage test condition. After a power on reset the following special reg. will all reset to "0000".

* P4.0–P4.3:

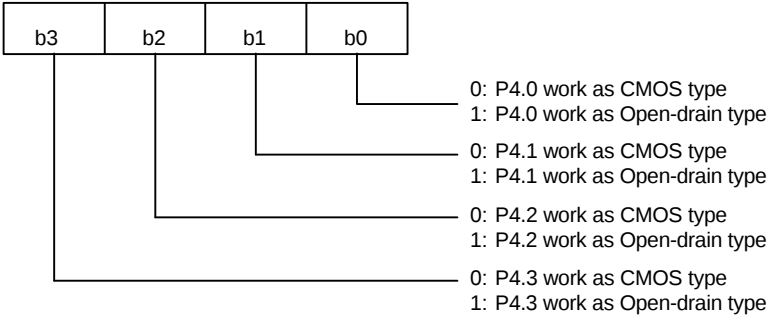
P4PH REG: (ADDRESS = 003H)

(Default data = 0H)



P4TP REG: (ADDRESS = 004H)

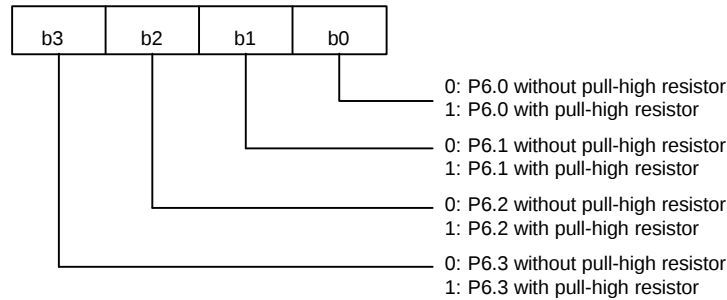
(Default data = 0H)



* P6.0–P6.3:

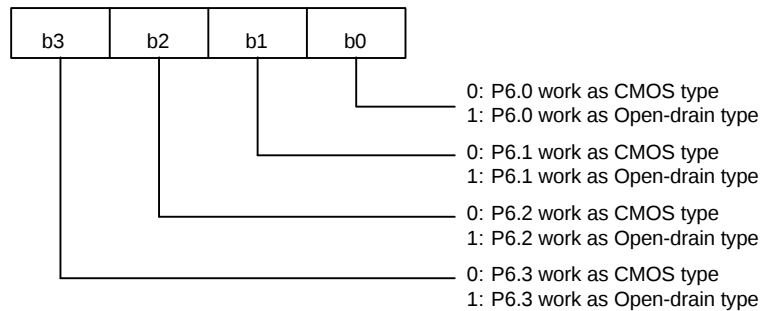
P6PH REG: (ADDRESS = 005H)

(Default data = 0H)



P6TP REG: (ADDRESS = 006H)

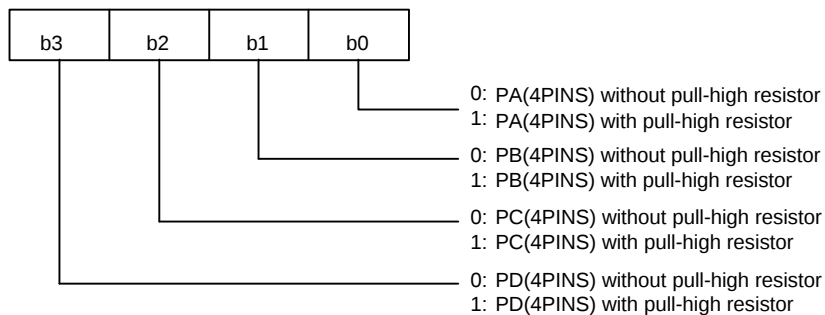
(Default data = 0H)



* PA, PB, PC, PD:

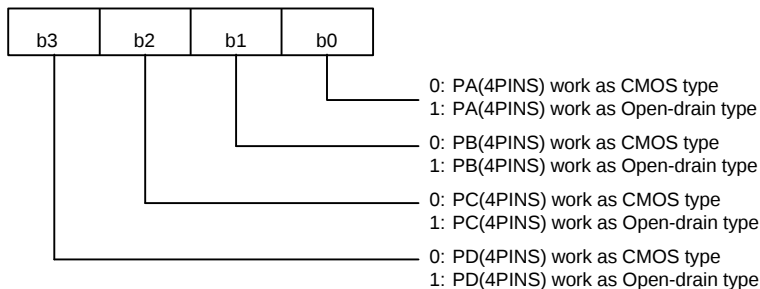
PABCDPH REG: (ADDRESS = 007H)

(Default data = 0H)



PABCDTP REG: (ADDRESS = 008H)

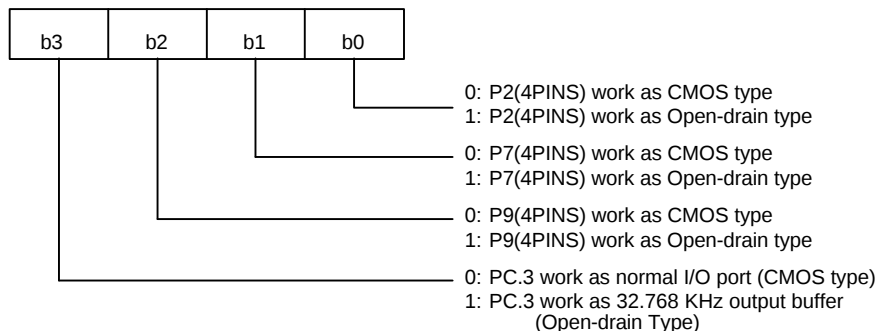
(Default data = 0H)



* P2, P7, P9:

P279TP REG: (ADDRESS = 00DH)

(Default data = 0H)



6.6 Serial Port

The W921E880A/W921C880 has a clock-synchronous serial interface which transmits or receives 8-bit data as default. The user can program the P6IO register to select port P6 as the serial port. The serial transmitter/receiver function can be operated with a multi-nibble function where the LSB of every nibble is being transmitted/received first.

The serial transmitted/received data is come from or stored in the serial buffer registers (address 050H to 14EH). The number of nibbles to be transmitted/received is decided by the serial MSB nibble register (SRMNR, address = 00AH) and the serial LSB nibble register (SRLNR, address = 009H).

SRMNR register: (address = 00AH, default data = 0H)

b3	b2	b1	b0
----	----	----	----

SRLNR register: (address = 009H, default data = 2H)

b3	b2	b1	b0
----	----	----	----

The default data in the SRMNR and SRLNR registers are 0 and 2 respectively which means the default serial interface is used to transmit/receive 8-bit data serially. As soon as these two registers are programmed and the instructions such as SOP or SIP are executed, the serial transmitter/receiver multi-nibble function will be performed. The transmitted/received number will be

Whether transceiver data will be latched on the rising or falling edge of the clock is determined by the serial clock inverter control register (SRINV, address = 00CH). Before the SOP or SIP instructions are executed the SRINV register must be set to the exact value. Once both the SRINV.3 and SRINV.2 are clear, the serial transceiver function will be forced to reset to initial status immediately.

Bit	Function
b3	0: Serial data latch at WCLK/RCLK rising edge (normal high) 1: Serial data latch at WCLK/RCLK falling edge (normal low)
b2	0: WCLK and RCLK pins work as the internal clock output pin 1: WCLK and RCLK pins work as the external clock input pin
b1	0: RCLK and RDATA disable (H-Z) 1: RCLK and RDATA enable
b0	0: WCLK and WDATA disable (H-Z) 1: WCLK and WDATA enable

[illegible]

The internal serial clock can be controlled by the serial clock speed control register (SRSPC) is described as follows:

SRSPC register: (address = 00BH, default data = 0H)

b3	b2	b1	b0	Input frequency
0	0	0	0	Reserved
0	0	0	1	fsys/4 Hz
0	0	1	0	fsys/8 Hz
0	0	1	1	fsys/16 Hz
0	1	0	0	fsys/32 Hz
0	1	0	1	fsys/64 Hz
0	1	1	0	fsys/128 Hz
0	1	1	1	fsys/256 Hz
1	0	0	0	fsys/512 Hz
1	0	0	1	fsys/1024 Hz
1	0	1	0	fsys/2048 Hz

Normally the WCLK or RCLK pin will remain in a high state and the serial data will be latched at the rising edge of the WCLK or RCLK signal, but the serial clock inverter control register (SRINV) will invert the above function. In this case the WCLK or RCLK pin will remain in a low state and the serial data will be latched at the falling edge of the the WCLK or RCLK signal.

The transmitting serial clock can come from WCLK or RCLK depending upon which one is enabled. If the serial function is disabled, it will cause the relative pins to be in a high impedance state and it will not affect the contents of the serial buffer registers (start at address 050H).

6.7 DTMF Generator

One channel of the dual tone multi-frequency (DTMF) generator is in this chip. The exact frequency must be decided by the OSCCTR REG to get the exact DTMF generator.

OSCCTR REG: (ADDRESS = 013H, Default data = 0H)

b3	b2	b1	b0	Osc. Selection
Reserved.	0	0	0	400 KHz
	0	0	1	800 KHz
	0	1	0	2 MHz
	0	1	1	4 MHz
	1	0	0	Reserved
	1	0	1	3.58MHz

There are four bits in the DTMF REG; the functions are described in the following table

DTMF REG: (ADDRESS = 014H), (Default data = 0H)

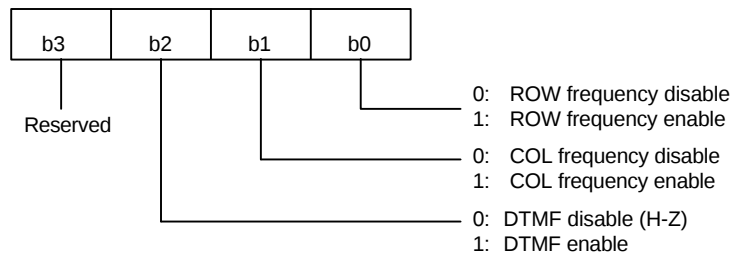
b3 b2 b1 b0	FUNCTION DESCRIPTION
X X 0 0	Col 1 (1209 Hz) output
X X 0 1	Col 2 (1336 Hz) output
X X 1 0	Col 3 (1477 Hz) output
X X 1 1	Col 4 (1633 Hz) output
0 0 X X	Row 1 (697 Hz) output
0 1 X X	Row 2 (770 Hz) output
1 0 X X	Row 3 (852 Hz) output
1 1 X X	Row 4 (941 Hz) output

Note : X --- Don't care

The output of the ROW and COL is controlled by the R/C CONTROL REG.

RCCTL REG: (ADDRESS = 015H)

(Default data = 0H)



The following table shows the DTMF keypad and its frequency.

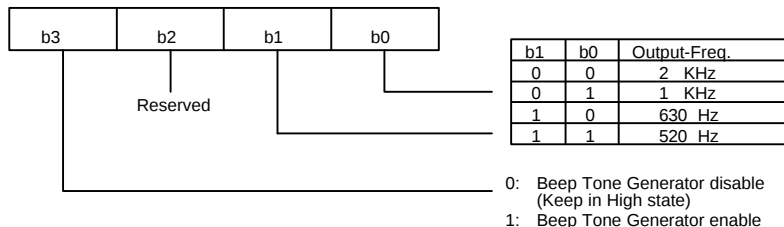
C1	C2	C3	C4		
1	2	3	A	R1	KEY FREQUENCY
4	5	6	B	R2	R1 697 Hz
7	8	9	C	R3	R2 770 Hz
*	0	#	D	R4	R3 852 Hz
					R4 941 Hz
					C1 1209 Hz
					C2 1336 Hz
					C3 1477 Hz
					C4 1633 Hz

6.8 Beep Tone Generator

There are 4 kinds of frequency outputs from the BTG pin that operate as a beep tone generator. Control of the OSCCTR REG. (ADDR = 013H) and the BTGR REG. (ADDR = 03FH) will enable the BTG pin to output the special frequencies -- 2 KHz, 1 KHz, 630 Hz or 520 Hz.

BTGR REG: ADDRESS = 03FH)

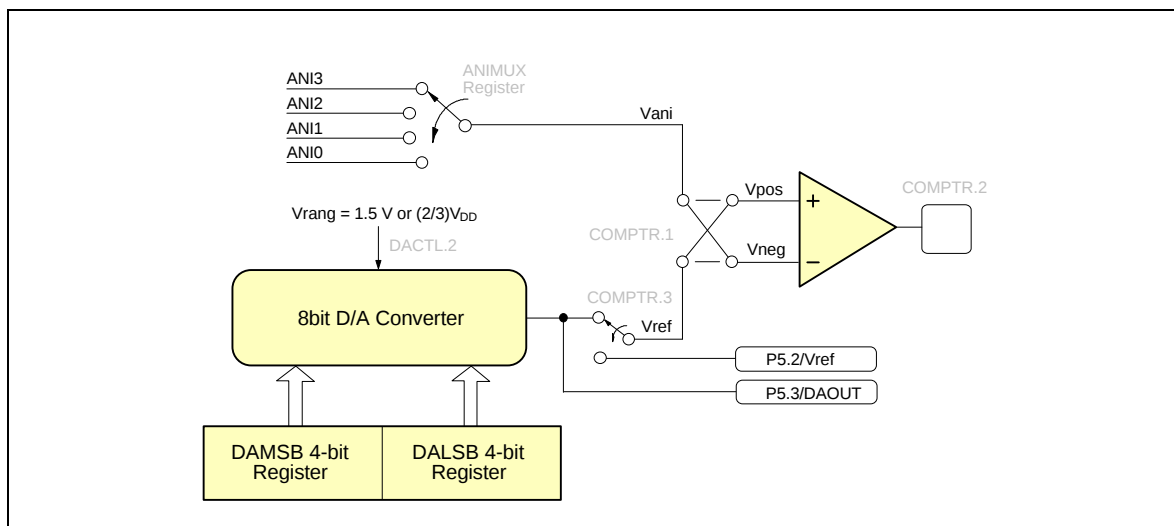
(Default data = 0H)



If the Beep Tone Generator is disabled by setting the BTGR REG. bit3 to "0" or after a power on reset, the BTG output pin will remain in a high state.

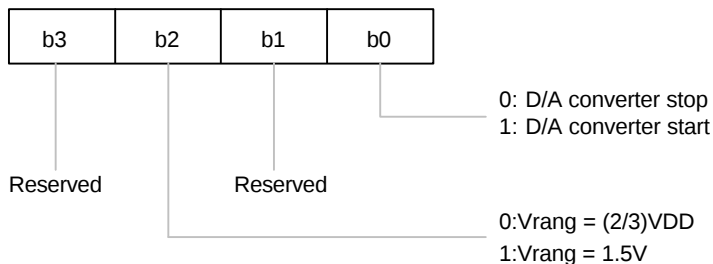
6.9 8-bit D/A Converter

The content of 8-bit D/A converter is divided into D/A MSB data register (DAMSB) and D/A LSB data register (DALSB). The block diagram is shown below.



ù D/A Converter Control Register:

DACTL register: (ADDRESS = 016H, Default data = 0H)



W921E880A/W921C880



When the DACTL register bit0 is set by software, the 8-bit D/A converter starts converting. The only way to disable the D/A converter is to reset the bit0 of the DACTL register using the software control. The analog signal will be output to the P5.3 pin in this chip if the I/O port works as the D/A output pin. The power source of the D/A converter can be selected from the $(2/3)V_{DD}$ or 1.5V by programming the DACTL register bit2.

ù D/A Converter LSB Data Register

DALSB register: (ADDRESS = 017H, Default data = 0H)

b3	b2	b1	b0
----	----	----	----

ù D/A Converter MSB Data Register

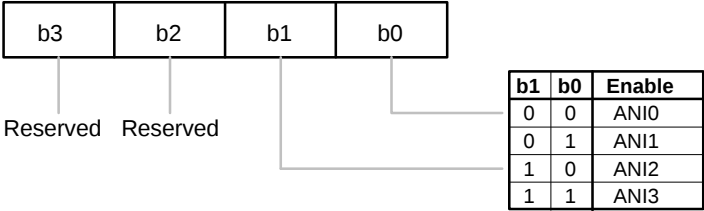
DAMSB register: (ADDRESS = 018H, Default data = 0H)

b3	b2	b1	b0
----	----	----	----

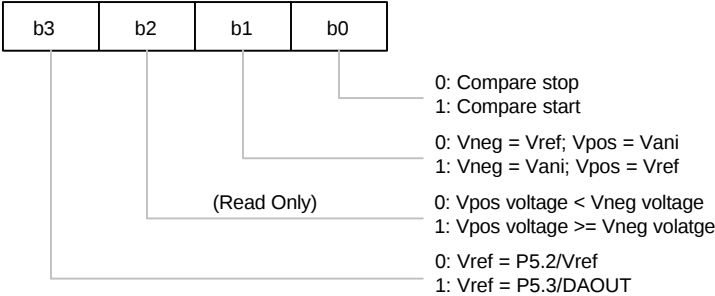
6.10 Comparator

There are 4-channel inputs to the comparator negative (can be programmed to positive) terminal, but only one channel will be active at a time. The control register is shown below.

ANIMUX register: (ADDRESS = 019H, Default data = 0H)



COMPTR register: (ADDRESS = 01AH, Default data = 4H)





When the COMPTR register bit0 is set by software, the comparator starts and the bit2 of the COMPTR register will be set to "1" initially. The comparing result will be stored in the bit2 of the COMPTR register and will keep this value until the bit0 of the COMPTR register is set again. The only way to disable the comparator is to reset the bit0 of the COMPTR register using the software control.

The initial value of the COMPTR bit2 is "1", the falling edge of COMPTR bit2 will cause the comparator interrupt to become active if the enable flag of the comparator interrupt is set.

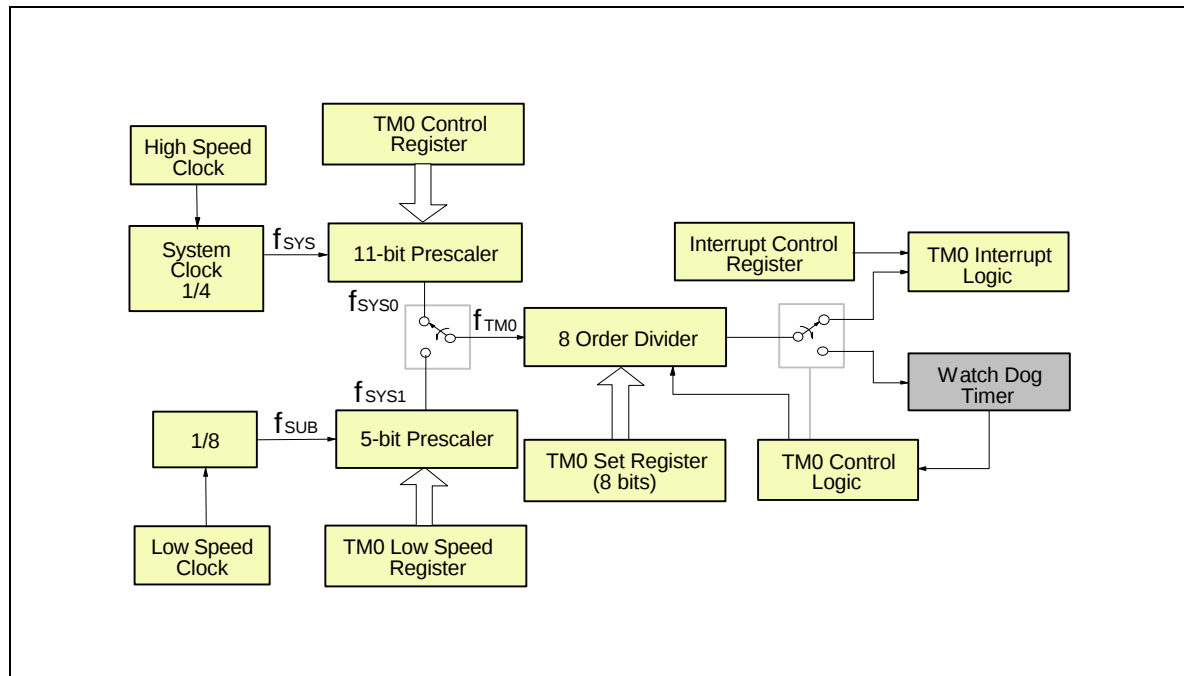
The bit3 of the COMPTR register controls the source of Input voltage reference (Vref). The input reference voltage (Vref) comes from external pin (P5.2/Vref) or D/A converter analog signal output (P5.3/DAOUT).

6.11 Timer 0-3

There are four timers (TM0, TM1, TM2 and TM3) in this chip, and all are initialized at any time by writing data into the TM0, TM1, TM2 and TM3 Set Reg.

TM0 can perform the following function:

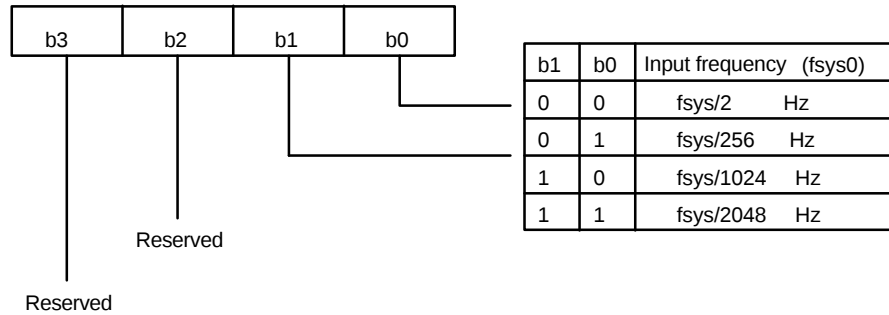
1. 2-19 order divider
2. Auto-reload Timer
3. Watch-dog timer



The format of the Timer 0 Control Register is described as follows:

TM0CR REG: (ADDRESS = 020H)

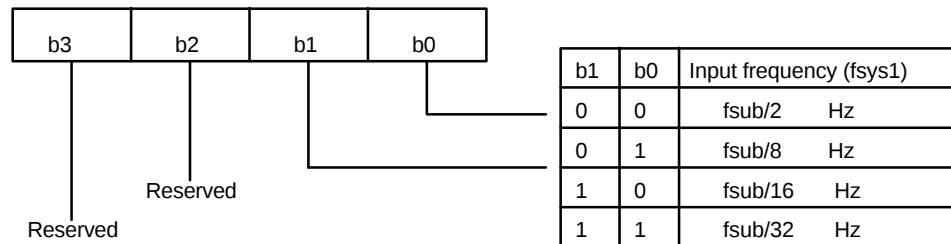
(Default data = 0H)



The format of the Timer 0 Low Speed Register is described as follows:

TM0LSR REG: (ADDRESS = 024H)

(Default data = 0H)



The Timer 0 Set REG. is divided into TIMER 0 MSB DATA REG.(TM0MSB REG, ADDRESS = 021H, Default = 0FH) and TIMER 0 LSB DATA REG.(TM0LSB REG, ADDRESS = 022H, Default = 0FH).

Timer 0 will underflow when Timer 0 Set REG. goes from 00H to 0FFH. The value in the TM0MSB and TM0LSB will be auto reloaded to the Timer 0 Set REG. when the STTM0 bit2 is set. Timer 0 will decrease by 1 continuously during each clock transition after the timer has started.

At any time, if the STTM0 bit3 goes from 0 to 1 (disable to enable) in the timer mode, the TM0MSB and TM0LSB will be auto reloaded to the Timer 0 Set Reg. again and the Timer 0 is restarted. Timer 0 will stop operating while the STTM0 bit3 is reset to 0.

The Timer 0 starts to count when the STTM0 REG. bit3 is set. When Timer 0 underflows, the STTM0 bit3 will be reset by hardware to stop Timer 0 if the auto-reload is disabled, but the STTM0 bit3 will not be reset if the auto-reload is enabled.

When the Timer 0 function is performed, the watch-dog timer function will be disabled automatically.

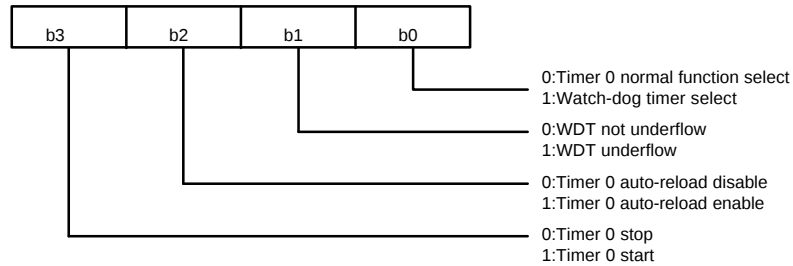
W921E880A/W921C880



The format of the Status of Timer 0 Register is shown as follows:

STTM0 REG: (ADDRESS = 023H)

(Default data = 0H)

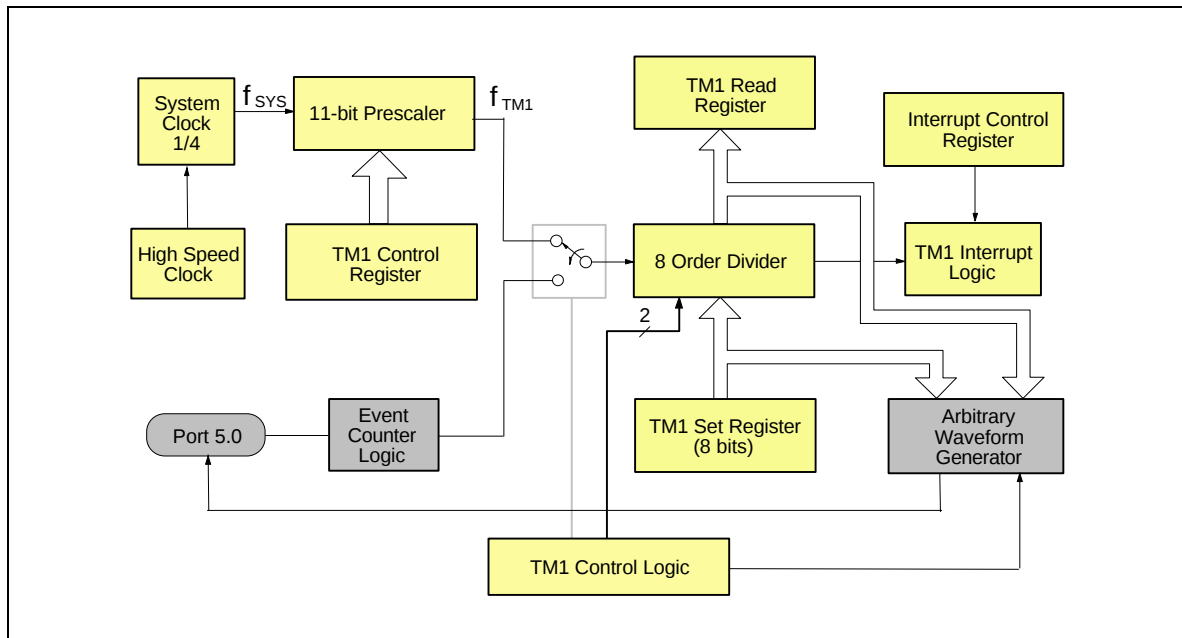


If Timer 0 works as a Watch Dog Timer, then bit1 of the STTM0 REG will be set when WDT underflows. Meanwhile, the system is reset just as in a power on reset except for the STTM0 bit1. The WDT (STTM0 bit1) will only be reset to zero during a power on reset or during the RAM write mode.

In the timer mode or event counter mode a time out will be the programming data subtract 1 ([TM0MSB,TM0LSB]-1). It is the same for timers TM1, TM2 and TM3.

TM1 can perform the following functions:

1. 2–19 order divider
2. Auto-reload timer.
3. Arbitrary waveform generator.
4. Event counter.



The format of the Timer 1 Control Register is shown as follows:

TM1CR REG: (ADDRESS = 025H)

(Default data = 0H)

b3	b2	b1	b0	Input frequency (fsys0)
0	0	0	0	fsys/2 Hz
0	0	0	1	fsys/4 Hz
0	0	1	0	fsys/8 Hz
0	0	1	1	fsys/16 Hz
0	1	0	0	fsys/32 Hz
0	1	0	1	fsys/64 Hz
0	1	1	0	fsys/128 Hz
0	1	1	1	fsys/256 Hz
1	0	0	0	fsys/512 Hz
1	0	0	1	fsys/1024 Hz
1	0	1	0	fsys/2048 Hz

The Timer 1 Set REG. is divided into TIMER 1 MSB DATA REG. (TM1MSB REG, ADDRESS = 026H, Default = 0FH) and TIMER 1 LSB DATA REG. (TM1LSB REG, ADDRESS = 027H, Default = 0FH).

The Timer 1 READ REG. is divided into TIMER 1 READ ONLY MSB DATA REG. (TM1RM REG, ADDRESS = 01CH, Default = 0FH) and TIMER 1 READ ONLY LSB DATA REG. (TM1RL REG, ADDRESS = 01DH, Default = 0FH).

The format of the Status of Timer 1 Register is shown as follows:

STTM1 REG: (ADDRESS = 028H)

(Default data = 0H)

b3	b2	b1	b0	
				0: Timer 1 normal function select 1: Special function select
				Reserved
				0:Timer 1 auto-reload disable 1:Timer 1 auto-reload enable
				0:Timer 1 stop 1:Timer 1 start

If Timer 1 is in the timer mode, the Timer 1 will underflow when it goes from 00H to 0FFH. The value in the TM1MSB and TM1LSB will be auto reloaded to the Timer 1 Set REG. when the STTM1 bit2 is set. Timer 1 will decrease by 1 continuously at each clock transition after the timer has started.

At any time the STTM1 bit3 goes from 0 to 1 (disable to enable), the TM1MSB and TM1LSB will be auto reloaded to the Timer 1 Set Reg. again and Timer 1 is restarted. Timer 1 will stop operating while the STTM1 bit3 is reset to 0.

W921E880A/W921C880



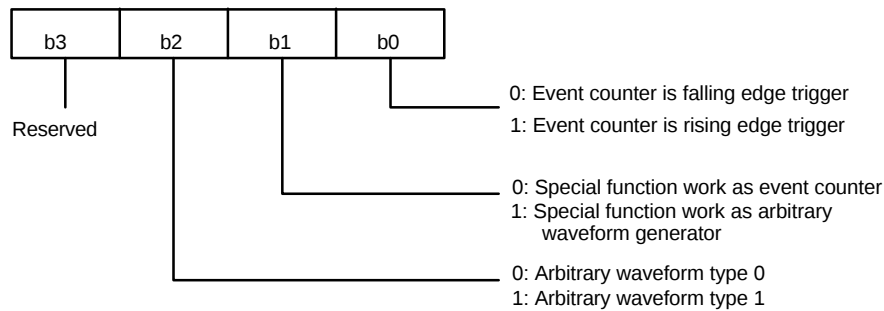
The Timer 1 starts to count when the STTM1 REG. bit3 is set. When Timer 1 underflows, the STTM1 bit3 will be reset by hardware to stop Timer 1 if the auto-reload is disabled, but the STTM1 bit3 will not be reset if the auto-reload is enabled.

When the Timer 1 function is performed, the special function will be disabled automatically. The special function input or output is from or to P5.0.

The format of the Timer 1 event counter condition is shown as follows

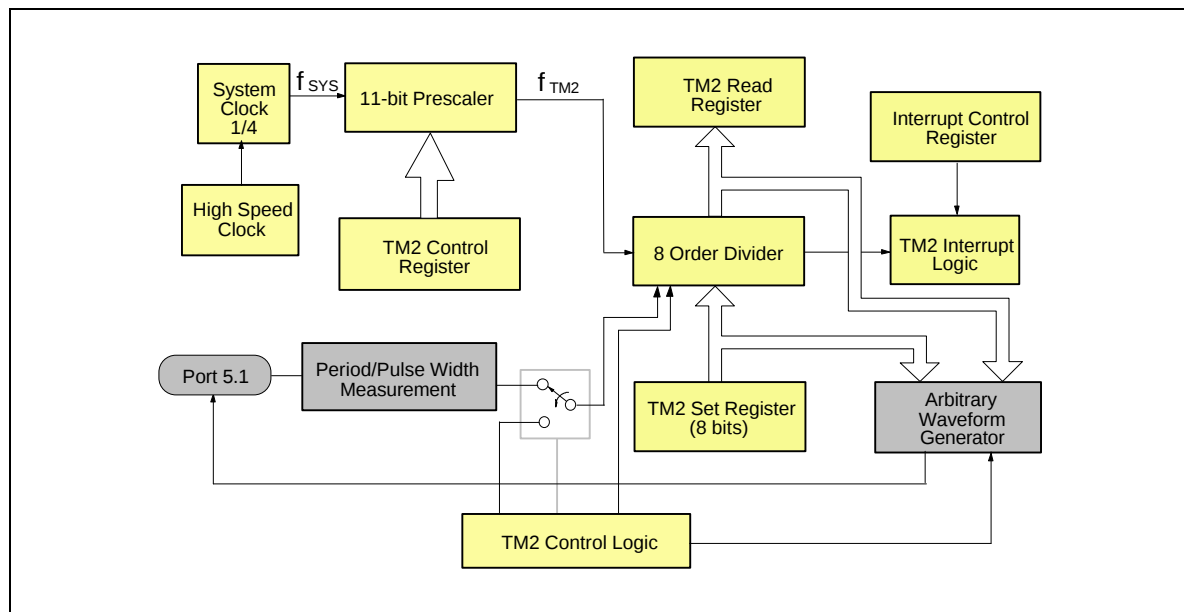
TGTM1 REG: (ADDRESS = 029H)

(Default data = 0H)



TM2 can perform the following functions:

1. 2–19 order divider
2. Auto-reload timer.
3. Arbitrary waveform generator.
4. Pulse/Period width measurement function



TM2CR REG: (ADDRESS = 02AH)

(Default data = 0H)

b3	b2	b1	b0	Input frequency (fTM2)
0	0	0	0	f _{sys} /2 Hz
0	0	0	1	f _{sys} /4 Hz
0	0	1	0	f _{sys} /8 Hz
0	0	1	1	f _{sys} /16 Hz
0	1	0	0	f _{sys} /32 Hz
0	1	0	1	f _{sys} /64 Hz
0	1	1	0	f _{sys} /128 Hz
0	1	1	1	f _{sys} /256 Hz
1	0	0	0	f _{sys} /512 Hz
1	0	0	1	f _{sys} /1024 Hz
1	0	1	0	f _{sys} /2048 Hz

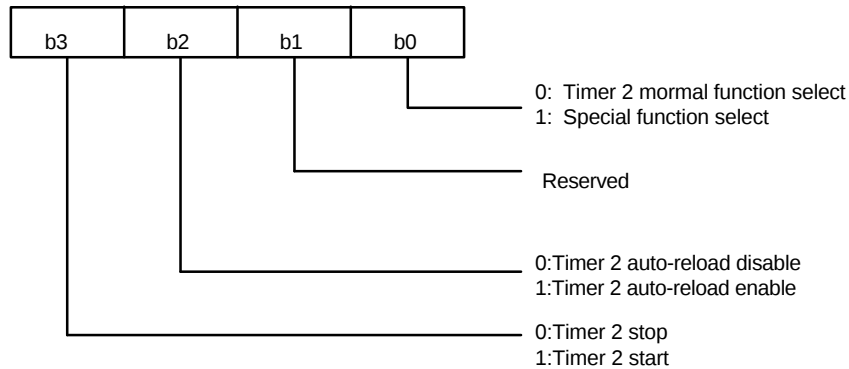
The Timer 2 Set REG. is divided into TIMER 2 MSB DATA REG. (TM2MSB REG, ADDRESS = 02BH, Default = 0FH) and TIMER 2 LSB DATA REG. (TM2LSB REG, ADDRESS = 02CH, Default = 0FH).

The Timer 2 READ REG. is divided into TIMER 2 READ ONLY MSB DATA REG. (TM2RM REG, ADDRESS = 01EH, Default = 0FH) and TIMER 2 READ ONLY LSB DATA REG. (TM2RL REG, ADDRESS = 01FH, Default = 0FH).

The format of the Status of Timer 2 Register is shown as follows:

STTM2 REG: (ADDRESS = 02DH)

(Default data = 0H)



If Timer 2 is in the timer mode, the Timer 2 will underflow when it goes from 00H to FFH. The value in TM2MSB and TM2LSB will be auto reloaded to the Timer 2 Set REG. Timer 2 will decrease by 1 continuously at each clock transition after the timer has started.

At any time the STTM2 bit3 goes from 0 to 1 (disable to enable), TM2MSB and TM2LSB will be auto reloaded to the Timer 2 Set Reg. again and the Timer 2 is restarted. Timer 2 will stop operating when the STTM2 bit3 is reset to 0.

W921E880A/W921C880



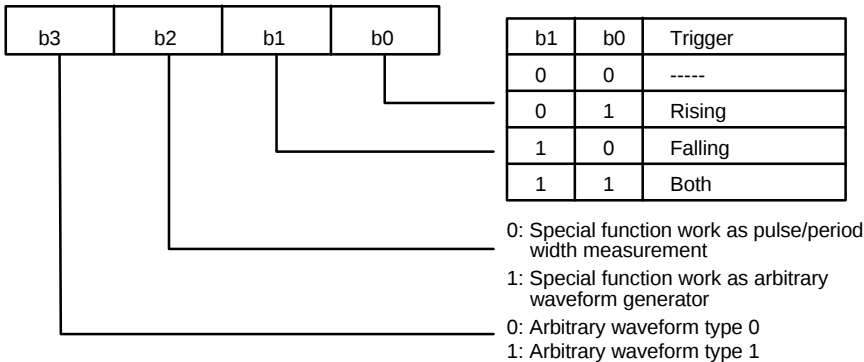
Timer 2 starts to count when the STTM2 REG. bit3 is set. When Timer 2 underflows, the STTM2 bit3 will be reset by hardware to stop Timer 2 if the auto-reload is disabled, but the STTM2 bit3 will not be reset if the auto-reload is enabled.

When the Timer 2 function is performed, the special function is automatically disabled.

The format of the trigger condition of the Timer 2 Register is shown as follows:

TGTM2 REG: (ADDRESS = 02EH)

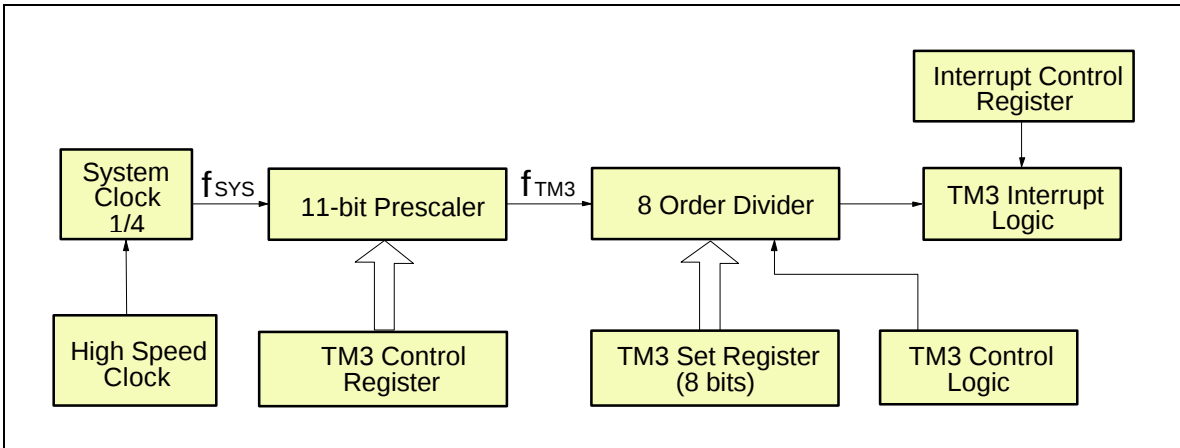
(Default data = 0H)



In pulse/period width measurement mode, the measuring-data is the 1'S complement of the exact data and the TM2 interrupt flag is set at every 255 timer clock occurrences or if the 2nd trigger condition occurs. So the measured pulse/period width is $(255(N-1) + \overline{TM2}) * T$, where N is the number of interrupt flag occurrences, $\overline{TM2}$ is the 1'S complement of timer2 register, and T is the period of the timer 2 clock. The special function input or output is from or to P5.1.

TM3 can perform the following functions:

1. 2-19 order divider
2. Auto-reload timer.





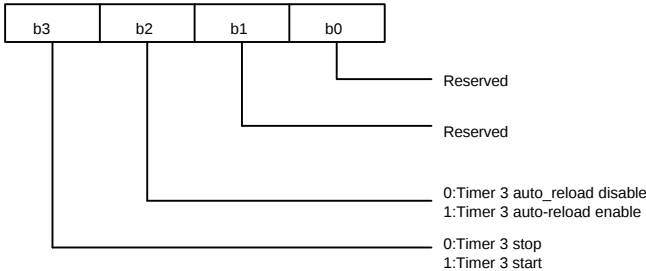
TM3CR REG: (ADDRESS = 02FH)
(Default data = 0H)

b3	b2	b1	b0	Input frequency (fTM3)
0	0	0	0	f _{sys} /2 Hz
0	0	0	1	f _{sys} /4 Hz
0	0	1	0	f _{sys} /8 Hz
0	0	1	1	f _{sys} /16 Hz
0	1	0	0	f _{sys} /32 Hz
0	1	0	1	f _{sys} /64 Hz
0	1	1	0	f _{sys} /128 Hz
0	1	1	1	f _{sys} /256 Hz
1	0	0	0	f _{sys} /512 Hz
1	0	0	1	f _{sys} /1024 Hz
1	0	1	0	f _{sys} /2048 Hz

The Timer 3 Set REG. is divided into TIMER 3 MSB DATA REG. (TM3MSB REG, ADDRESS = 030H, Default = 0FH) and TIMER 3 LSB DATA REG. (TM3LSB REG, ADDRESS = 031H, Default = 0FH).

The format of the Status of Timer 3 Register is shown as follows:

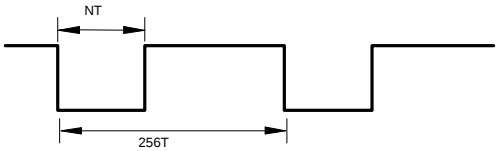
STTM3 REG: (ADDRESS = 032H)
(Default data = 0H)



6.11.1 Arbitrary Waveform Generator

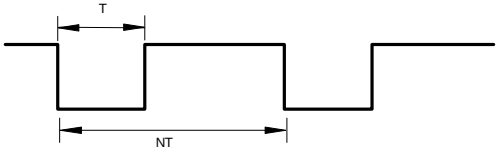
Both TM1 and TM2 have arbitrary waveform generator circuits. The following description describes their operation.

TYPE 0 :



$N = 0$ Will keep the waveform in the high state.

TYPE 1 :



$N = 1$ Will keep the waveform in the low state.

Note: N is the value stored in the TM1 Set Reg. (TM1MSB, TM1LSB) or TM2 Set Reg. (TM2MSB, TM2LSB)



6.12 Interrupt

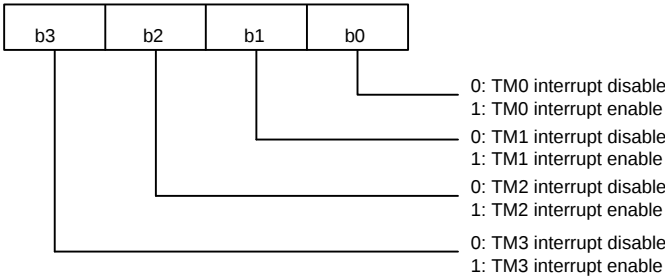
There are 10 interrupt sources. There are four external sources: INT0 (P4.3) and P4 Port (P4.0–P4.2), triggered by the falling edge signals of external sources, and six internal sources: Timer0, Timer1, Timer2, Timer3, Comparator and Serial Port. The priority of those interrupts is INT0 > TM0 > TM1 > TM2 > (Comparator / TM3) > P4.0 to P4.2 > SERIAL.

6.12.1 Interrupt Control Register

The INTERRUPT CONTROL REG.1–3 (INTCT1–INTCT3) controls which interrupt is enabled. The formats are shown below:

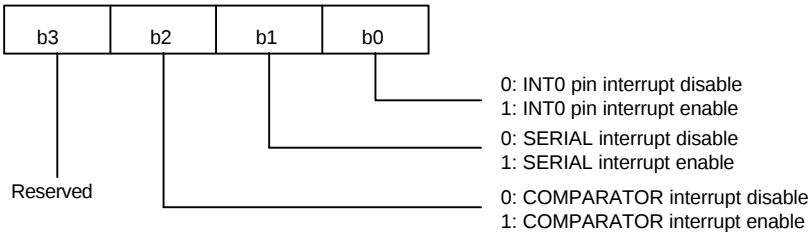
INTCT1 REG: (ADDRESS = 039H)

(Default data = 0H)



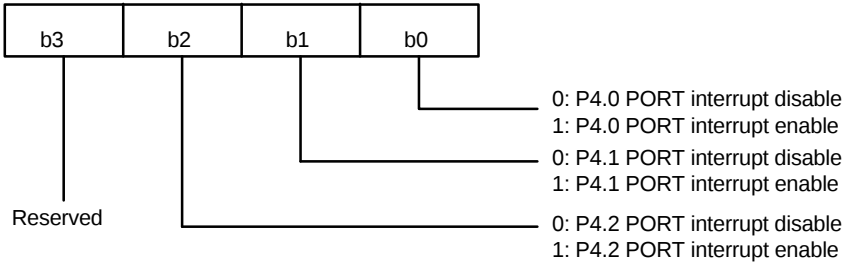
INTCT2 REG: (ADDRESS = 03AH)

(Default data = 0H)



INTCT3 REG: (ADDRESS = 03BH)

(Default data = 0H)



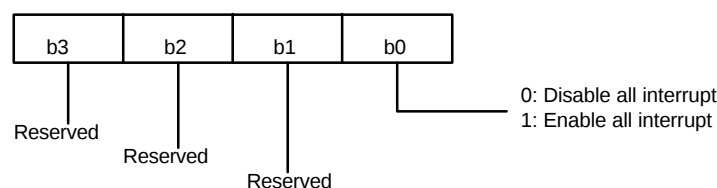


6.12.2 Interrupt Enable Flag

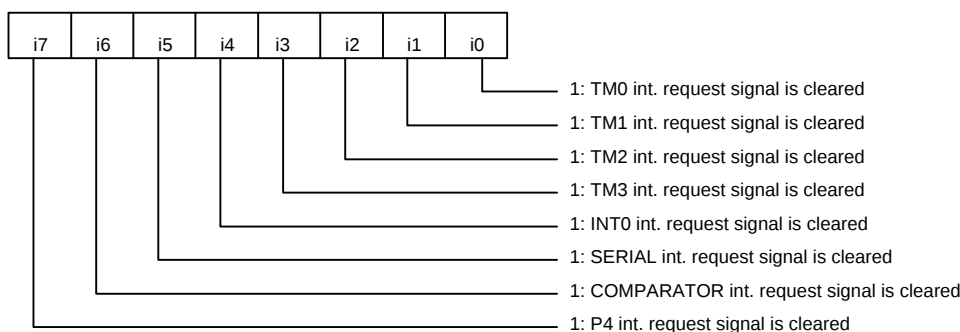
When the interrupt is enabled by an event, the program counter will jump to the interrupt address and the Enable Interrupt Flag (ENINT) bit0 is cleared. All the interrupts will also be disabled at the same time. The only method to enable the interrupt again is to set the ENINT bit0 or to execute the RTNI instruction.

ENINT REG: (ADDRESS = 034H)

(Default data = 0H)



When the interrupt is enabled by an event, the individual interrupt request signal is automatically cleared by the hardware with the other interrupt request signals kept in the same condition. The only way to reset the interrupt request signal is to execute the instruction CLR EVF, #I (I is a 8bits data, for example, CLR EVF, #00000001b instruction implies to clear TM0 interrupt request signal). This instruction is a 2 word / 2 cycle instruction; the format of the immediate data is shown as follows:



6.13 Operating Mode

There are 3 types of operating mode, Normal Mode , Hold Mode, and Stop Mode.

6.13.1 Normal Mode

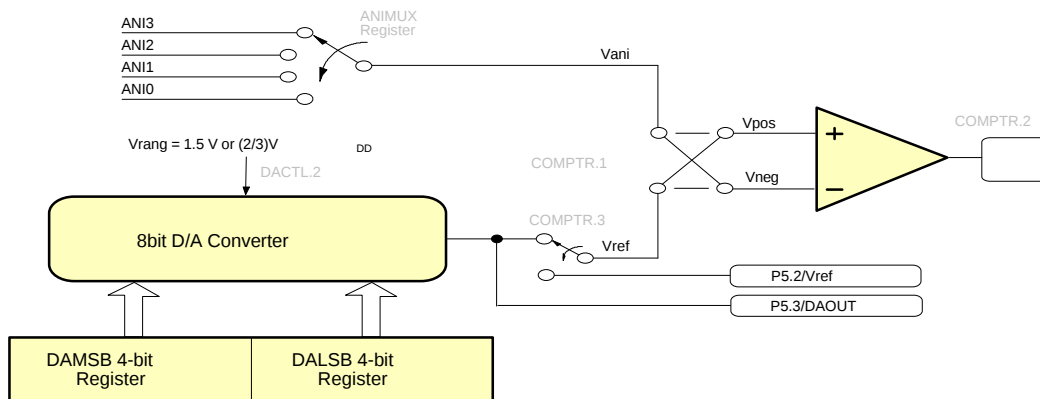
All functions operate with the μ P functioning according to the system clock.

6.13.2 Hold Mode

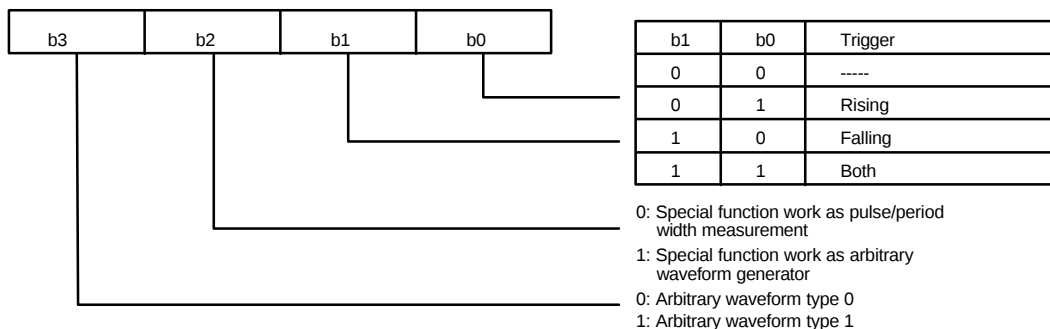
The μ P enters the HOLD MODE when the HOLD instruction is executed from NORMAL MODE. In this mode, the system clock is stopped, so the program counter (PC) will also stop. But the oscillator, timer/ counter, serial port and interrupt active pins continue to function.

The HOLD MODE can be released only by the $\overline{\text{RESET}}$ pin or by an interrupt request signal. When the hold mode is released, either the hold mode is released only, or the hold mode is released and the interrupt subroutine (interrupt vector) is serviced. The HOLD MODE RELEASES FLAG 1, 2, 3 (HMRF1, 2, 3) (ADDRESS = 036H, 037H, 038H) which can control the flow. The formats of these three flags are shown below.

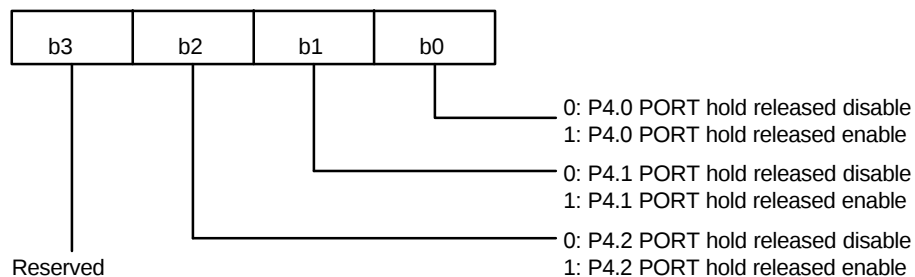
HMR1 REG: (ADDRESS = 036H)
(Default data = 0H)



HMR2 REG: (ADDRESS = 037H)
(Default data = 0H)



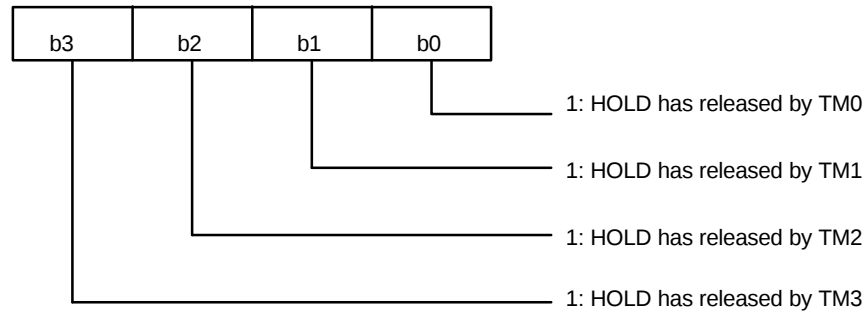
HMR3 REG: (ADDRESS = 038H)
(Default data = 0H)



The HOLD RELEASED STATUS FLAG 1, 2, 3 (HRSTS1, 2, 3) (ADDRESS = 03CH, 03DH, 03EH) stores the information that caused the HOLD MODE to be released. The format is shown below.

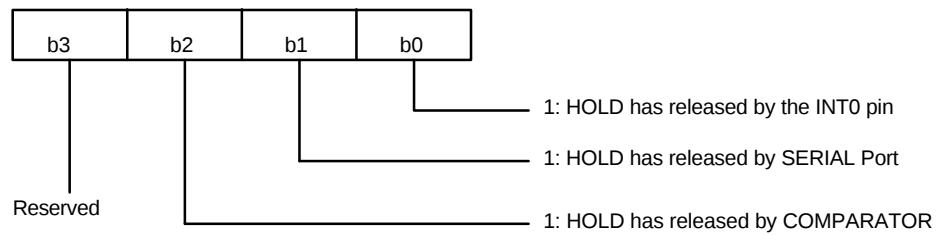
HRSTS1 REG: (ADDRESS = 03CH) (Read Only)

(Default data = 0H)



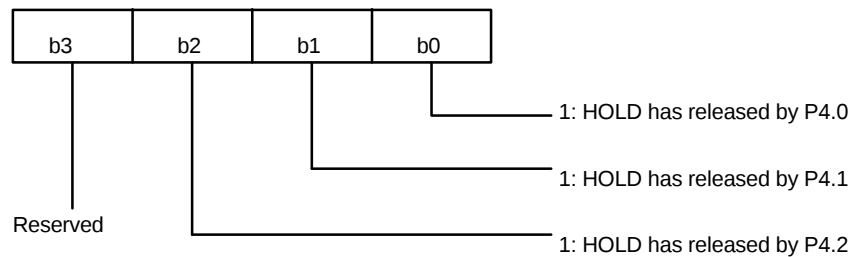
HRSTS2 REG: (ADDRESS = 03DH) (Read Only)

(Default data = 0H)



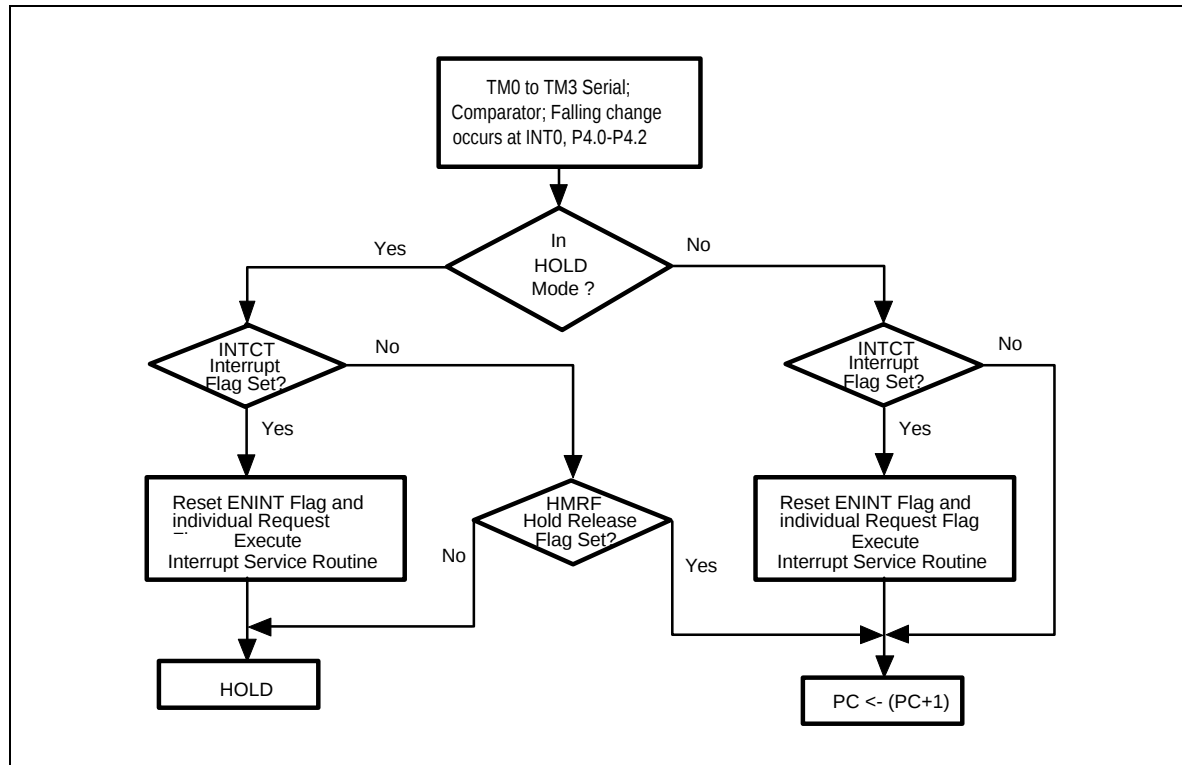
HRSTS3 REG: (ADDRESS = 03EH) (Read Only)

(Default data = 0H)



HRSTS1, 2, and 3 are read only registers and cleared by the instruction CLR EVF #I.

Hold Mode Operation Flow Chart



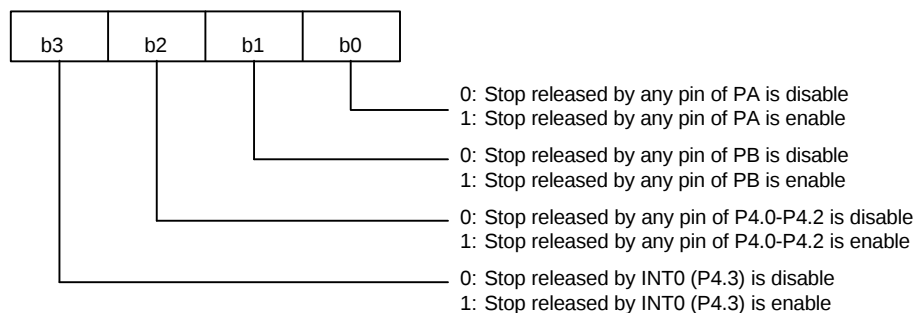
6.13.3 Stop Mode

The μ P enters the STOP MODE only if the stop instruction is executed. All chip functions are disabled because both of the oscillators are stopped.

The stop mode can be released by the low level of the RESET pin, INT0 pin, P4 port, PA port or PB port. The STOP CONDITION RELEASE FLAG (STPRF ADDRESS = 035H) is the STOP mode release control reg.

STPRF REG.: (ADDRESS = 035H)

(Default data = 8H)

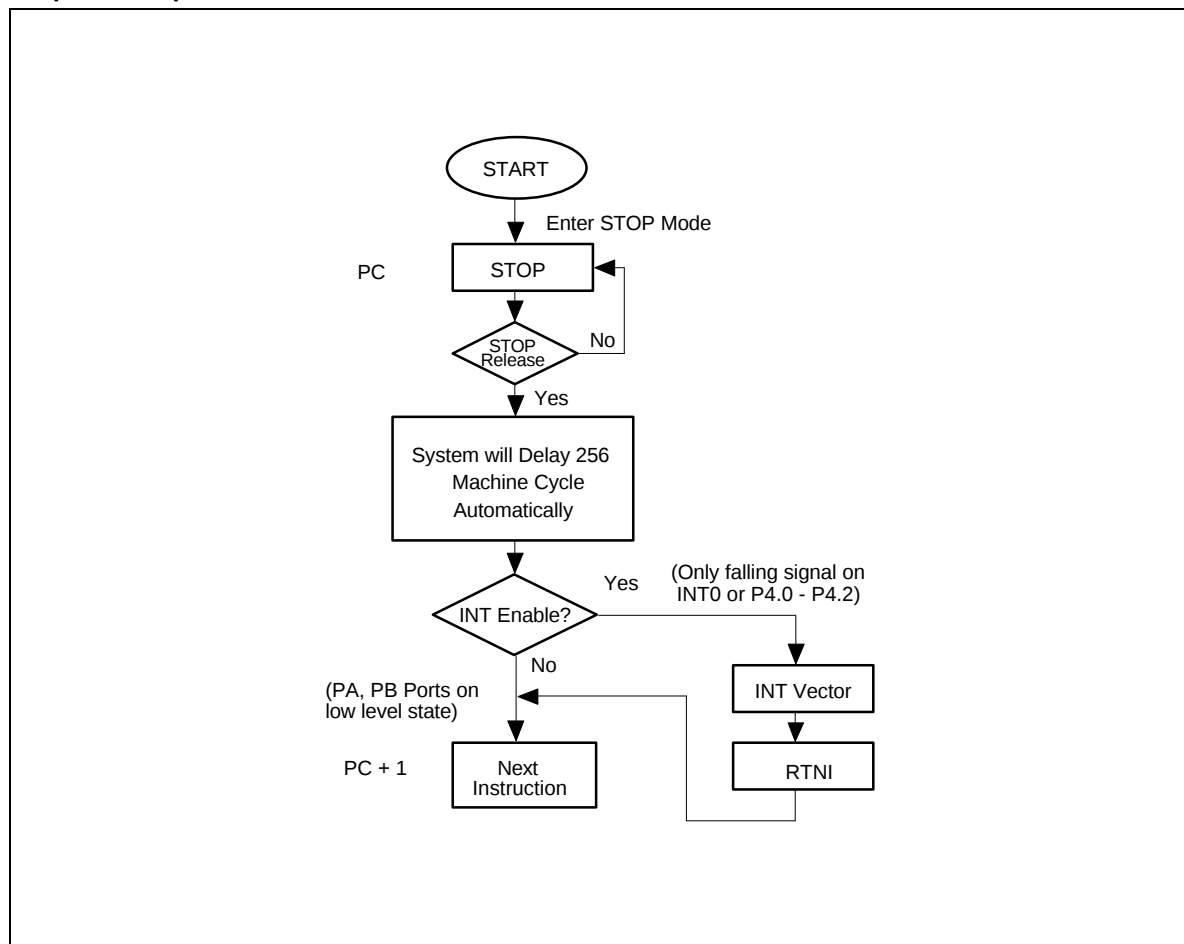


When the STOP CONDITION RELEASE FLAG (STPRF) and the INTERRUPT CONTROL REG. (INTCT1–INTCT3) are set before the STOP instruction is executed, a low level signal on the P4, PA or PB ports will cause the STOP MODE to be released. There will be a delay of about 256 machine cycles after the stop mode is released. The interrupt subroutine (interrupt vector) is then executed according to the set bit in the STPRF REG. If the interrupt enable flag is not set before the STOP instruction is executed, then the next instruction after the STOP instruction will be executed. It also has a delay of about 256 machine cycles before the next instruction is executed.

It should be noted that if STOP MODE is released by the PA or PB port, then the chip will execute the (PC+1) instruction only because there is no individual interrupt subroutine in the PA and PB ports.

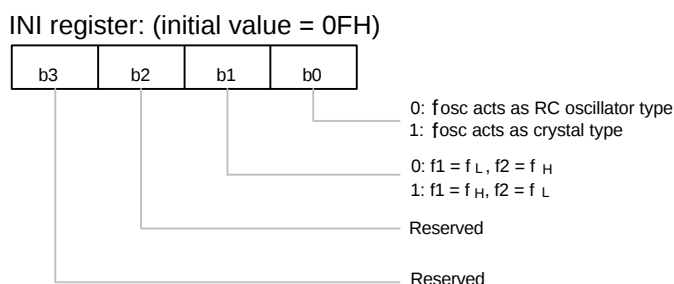
The control flow chart is shown as follows:

Stop Mode Operation Flow Chart



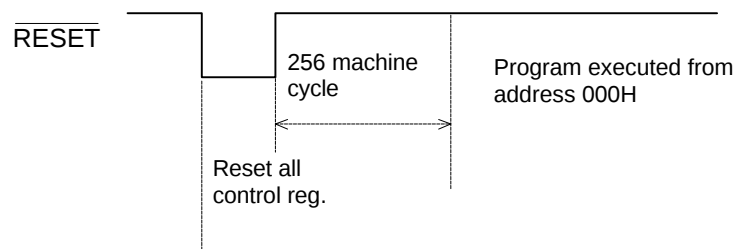
6.14 Initial Condition Register of EPROM Program Method

There is one 4-bit of the initial condition register (not part of the RAM) in W921E880A to control the micro-controller initial status after power-on. The format is described as following:



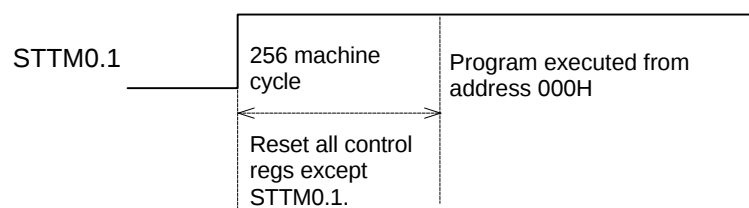
6.15 Reset

1. Reset by $\overline{\text{RESET}}$



As $\overline{\text{RESET}}$ pin is pulled low, system and all control registers are reset to initial state. After $\overline{\text{RESET}}$ pin is in high level, system will delay 256 machine cycle time then program is executed from address 000H.

2. Reset by Watch Dog Timer



As watch dog timer underflows, the STTM0.1 is set, in the mean while, system and all control registers, except data 1 in STTM0.1 bit is reserved, are reset to initial state then after a delay of 256 machine cycle time program is executed from address 000H. After system reset, user can detect STTM0.1 to recognize which method of reset was done before.



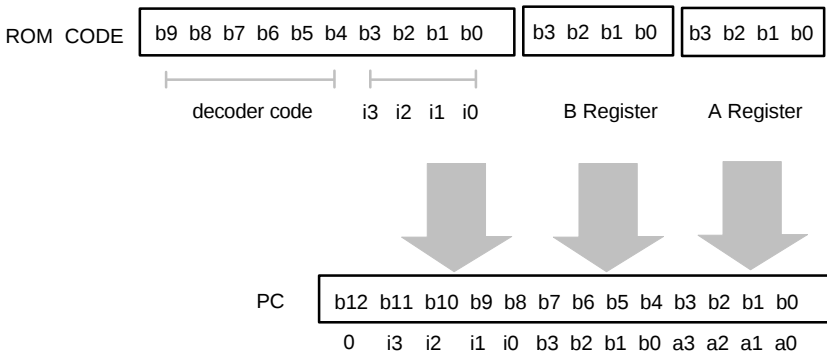
7. ADDRESSING MODE

7.1 ROM Addressing Mode

There are two ROM addressing modes in this chip

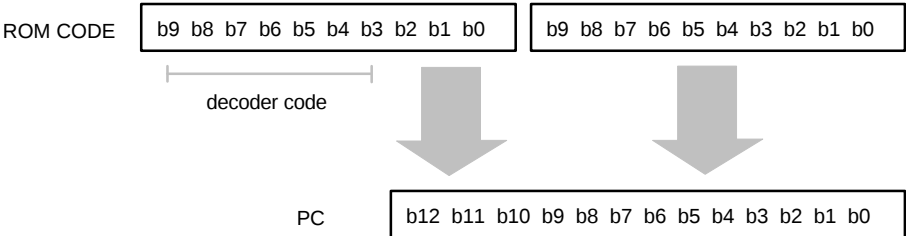
- * Indirect Call Addressing Mode (0H–0FFFH)
- * Long Call/Jump Addressing Mode (0H–1FFFH)

Indirect Call Addressing Mode (1 Word/2 Cycles)



Instruction: CALLP

Long Call/Jump Addressing Mode (2 Words/2 Cycles)



Instruction: CALL, JMPL, JB0, JB1, JB2, JB3, JC, JNC, JZ, JNZ

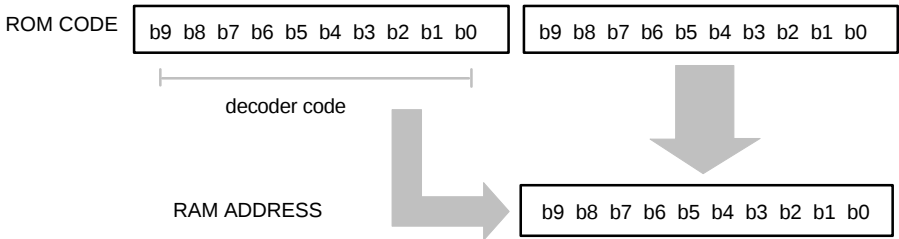
7.2 RAM Addressing Mode

There are three RAM addressing modes.

- * Direct Addressing Mode
- * Indirect Addressing Mode
- * Working Register Addressing Mode

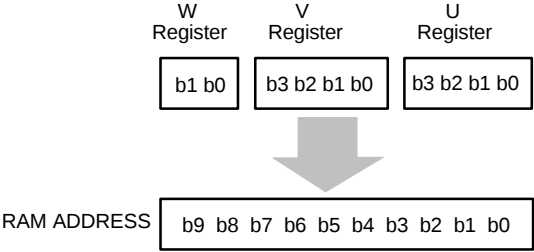


Direct Addressing Mode (2 Words/2 Cycles)



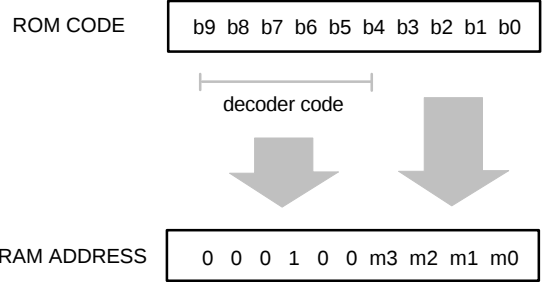
Instruction: MOV A, Mx; MOV B, Mx; MOV Mx, A; MOV Mx, B; ..., etc.

Indirect Addressing Mode (1 Word/1 Cycle)



Instruction: MOV A, @M; MOV B, @M; MOV @M, A; ..., etc.

Working REG Addressing Mode (1 Word/1 Cycle)

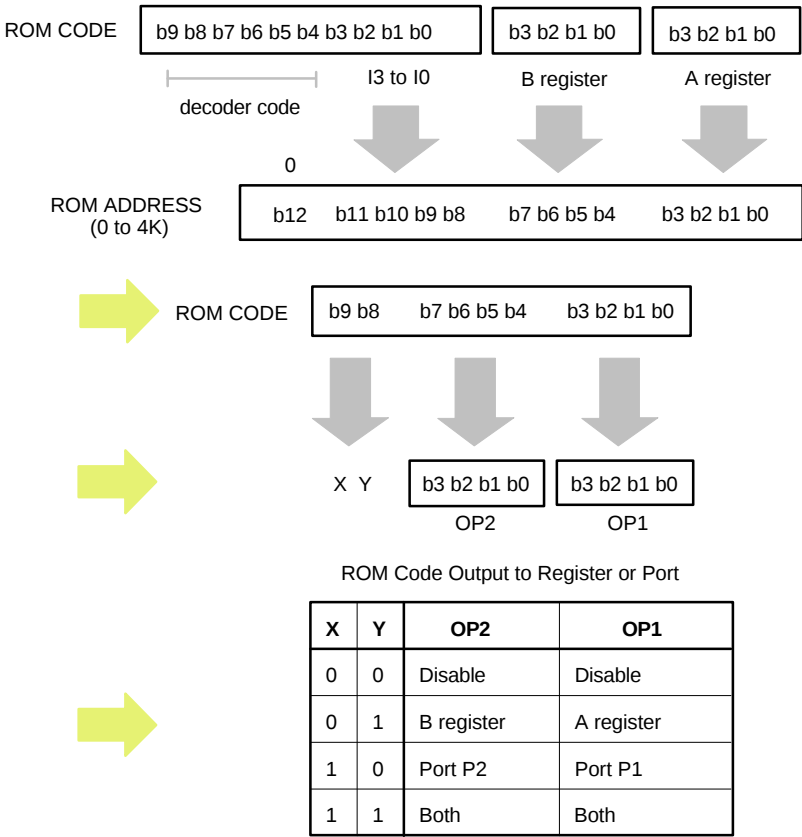


Instruction: MOV A, WRn; MOV WRn, A; ..., etc.



7.3 Look-up Table Addressing Mode (1 Word/2 Cycles)

There is one special function look-up table addressing mode in this chip; the instruction is TBL I and the function is shown in the following table.



Example:

```
.
.
.
MOV    A, #03H
MOV    B, #01H
TBL    02H                      ; A = 0CH, B = Port2 = 0DH
.
.
.
ORG    213H
DC     3DCH
.
.
.
```

W921E880A/W921C880



8. SPECIAL CONTROL REG. FORMAT

ADDR.	DESCRIPTION	ABBREVIATION	INITIAL VALUE
000H	System Clock Control Register	(SYSCCR)	00H
001H	Bank Select Register	(BKSR)	02H
002H	Reserved	-	-
003H	Port P4 Pull High Resistor Register	(P4PH)	00H
004H	Port P4 Output Type Register	(P4TP)	00H
005H	Port P6 Pull High Resistor Register	(P6PH)	00H
006H	Port P6 Output Type Register	(P6TP)	00H
007H	Port PABCD Pull High Resistor Register	(PABCDPH)	00H
008H	Port PABCD Output Type Register	(PABCDTP)	00H
009H	Serial LSB Nibble Register	(SRLNR)	02H
00AH	Serial MSB Nibble Register	(SRMNR)	00H
00BH	Serial Speed Control Register	(SRSPC)	00H
00CH	Serial Clock Inverter Control Register	(SRINV)	00H
00DH	Port P2 Output Type Register	(P2TP)	00H
00EH	Reserved		-
00FH	Port P3 I/O Status Control Register	(P3IO)	00H
010H	Port P4 I/O Status Control Register	(P4IO)	00H
011H	Port P5 I/O Status Control Register	(P5IO)	00H
012H	Port P6 I/O Status Control Register	(P6IO)	00H
013H	DTMF Oscillation Control Register	(OSCCTR)	00H
014H	DTMF Register	(DTMF)	00H
015H	Row/Column Frequency Control Register	(RCCTL)	00H
016H	D/A Control Register	(DACTL)	00H
017H	D/A Converter LSB Data Register	(DALSB)	00H
018H	D/A Converter MSB Data Register	(DAMSB)	00H
019H	Comparator Analog Input Multiplexer	(ANIMUX)	00H
01AH	Comparator Control Register	(COMPTR)	04H
01BH	Reserved		-
01CH	TM1 Read Only MSB Data Register	(TM1RM)	0FH
01DH	TM1 Read Only LSB Data Register	(TM1RL)	0FH
01EH	TM2 Read Only MSB Data Register	(TM2RM)	0FH
01FH	TM2 Read Only LSB Data Register	(TM2LM)	0FH
020H	TM0 Control Register	(TM0CR)	00H
021H	TM0 MSB Data Register	(TM0MSB)	0FH

W921E880A/W921C880



8. Special Control REG. Format, continued

ADDR.	DESCRIPTION	ABBREVIATION	INITIAL VALUE
022H	TM0 LSB Data Register	(TM0LSB)	0FH
023H	TM0 Status Register	(STTM0)	00H
024H	Reserved or Timer 0 Low Speed Register	(TM0LSR)	00H
025H	TM1 Control Register	(TM1CR)	00H
026H	TM1 MSB Data Register	(TM1MSB)	0FH
027H	TM1 LSB Data Register	(TM1LSB)	0FH
028H	TM1 Status Register	(STTM1)	00H
029H	TM1 Trigger Condition Register	(TGTM1)	00H
02AH	TM2 Control Register	(TM2CR)	00H
02BH	TM2 MSB Data Register	(TM2MSB)	0FH
02CH	TM2 LSB Data Register	(TM2LSB)	0FH
02DH	TM2 Status Register	(STTM2)	00H
02EH	TM2 Trigger Condition Register	(TGTM2)	00H
02FH	TM3 Control Register	(TM3CR)	00H
030H	TM3 MSB Data Register	(TM3MSB)	0FH
031H	TM3 LSB Data Register	(TM3LSB)	0FH
032H	TM3 Status Register	(STTM3)	00H
033H	Reserved		-
034H	Interrupt Enable Flag	(ENINT)	00H
035H	Stop Mode Released Flag	(STPRF)	08H
036H	Hold Mode Released Flag 1	(HMRF1)	00H
037H	Hold Mode Released Flag 2	(HMRF2)	00H
038H	Hold Mode Released Flag 3	(HMRF3)	00H
039H	Interrupt Control Register 1	(INTCT1)	00H
03AH	Interrupt Control Register 2	(INTCT2)	00H
03BH	Interrupt Control Register 3	(INTCT3)	00H
03CH	Hold Released Status Flag 1	(HRSTS1)	00H
03DH	Hold Released Status Flag 2	(HRSTS2)	00H
03EH	Hold Released Status Flag 3	(HRSTS3)	00H
03FH	Beep Tone Generator Register	(BTGR)	00H

W921E880A/W921C880



9. INSTRUCTION MAP

b9 = 0

b8 = 0

MSB \ LSB	0	1	2	3	4	5	6	7	8	9	0A	0B	0C	0D	0E	0F
0	NOP	MOV A, B	MOV A, Mx	MOV A, @M	MOV A, W	MOV A, V	MOV A, U		SRL A	INC B	ADD A, Mx	ADD A, @M		CLRB Mx, bit		
1	MOV B, A		MOV B, Mx	MOV B, @M					SRH A	INC DP	ADC A, Mx	ADC A, @M		CLRB @M, bit		
2	MOV Mx, A	MOV Mx, B							SLL A	DEC B	SUB A, Mx	SUB A, @M		SETB Mx, bit		
3	MOV @M, A	MOV @M, B							SLH A	DEC DP	SBC A, Mx	SBC A, @M		SETB @M, bit		
4	MOV W, A								RRC A		ANL A, Mx	ANL A, @M	CLR EVF	XCH A, B	MOV DP, #I	SOP
5	MOV V, A										ORL A, Mx	ORL A, @M				SIP
6	MOV U, A								RLC A	XRL A, B	XRL A, Mx	XRL A, @M	SET CF	XCH V, CV	HOLD	RTN
7										CMP A, B	CMP A, Mx	CMP A, @M	CLR CF	XCH U, CU	STOP	RTNI
8									ADD A, #I							
9									ADC A, #I							
0A									SUB A, #I							
0B									SBC A, #I							
0C									ANL A, #I							
0D									ORL A, #I							
0E									XRL A, #I							
0F									CMP A, #I							

☐ 1W/1C ☐ 1W/2C ☐ 1W/3C
☐ 2W/2C ☐ 2W/3C ☐ 3W/3C
☐ Undecided

W921E880A/W921C880



b9 = 1

b8 = 0

MSB \ LSB	0	1	2	3	4	5	6	7	8	9	0A	0B	0C	0D	0E	0F
0																
1																
2																
3																
4																
5																
6																
7																
8				JB0								JB1				
9				JB2								JB3				
0A				JC								JNC				
0B				JZ								JNZ				
0C				JMPL								CALL				
0D									CALLP							
0E									TBL							
0F																

- ☐ 1W/1C
 ☐ 1W/2C
 ☐ 1W/3C
- ☐ 2W/2C
 ☐ 2W/3C
 ☐ 3W/3C
- ☐ Undecided

W921E880A/W921C880



b9 = 1

b8 = 1

LSB MSB	0	1	2	3	4	5	6	7	8	9	0A	0B	0C	0D	0E	0F
0								MOV A, #I								
1								MOV B, #I								
2								MOV Mx, #I								
3								MOV @M, #I								
4			ADD A, WRn								ADC A, WRn					
5			SUB A, WRn								SBC A, WRn					
6			ANL A, WRn								ORL A, WRn					
7			XRL A, WRn								CMP A, WRn					
8								MOV A, WRn								
9								MOV A, Px								
0A								MOV B, WRn								
0B								MOV B, Px								
0C								MOV WRn, A								
0D								MOV Px, A								
0E								MOV WRn, B								
0F								MOV Px, B								

☐ 1W/1C ☐ 1W/2C ☐ 1W/3C
☐ 2W/2C ☐ 2W/3C ☐ 3W/3C
☐ Undecided



10. INSTRUCTION SETS

MACHINE CODE	MNEMONIC	FUNCTION	A	B	U	V	W	STATUS	W/C	MEMO
Arithmetic										
00 0000 1010, xxxxxxxxxx	ADD A, Mx	$A + Mx \rightarrow A$	A					Z, C	2/2	
11 0100 0 iii	ADD A, WRx	$A + WRx \rightarrow A$	A					Z, C	1/1	$x = 0 \sim 7$
00 0000 1011	ADD A, @M	$A + @M \rightarrow A$	A		U	V	W	Z, C	1/1	
00 0001 1010, xxxxxxxxxx	ADC A, Mx	$A + Mx + C \rightarrow A$	A					Z, C	2/2	
11 0100 1 iii	ADC A, WRx	$A + WRx + C \rightarrow A$	A					Z, C	1/1	$x = 0 \sim 7$
00 0001 1011	ADC A, @M	$A + @M + C \rightarrow A$	A		U	V	W	Z, C	1/1	
00 0010 1010, xxxxxxxxxx	SUB A, Mx	$A - Mx \rightarrow A$	A					Z, C	2/2	
11 0101 0 iii	SUB A, WRx	$A - WRx \rightarrow A$	A					Z, C	1/1	$x = 0 \sim 7$
00 0010 1011	SUB A, @M	$A - @M \rightarrow A$	A		U	V	W	Z, C	1/1	
00 0011 1010, xxxxxxxxxx	SBC A, Mx	$A - Mx - C \rightarrow A$	A					Z, C	2/2	
11 0101 1 iii	SBC A, WRx	$A - WRx - C \rightarrow A$	A					Z, C	1/1	$x = 0 \sim 7$
00 0011 1011	SBC A, @M	$A - @M - C \rightarrow A$	A		U	V	W	Z, C	1/1	
00 1000 iiiii	ADD A, #i	$A + i \rightarrow A$	A					Z, C	1/1	
00 1001 iiiii	ADC A, #i	$A + i + C \rightarrow A$	A					Z, C	1/1	
00 1010 iiiii	SUB A, #i	$A - i \rightarrow A$	A					Z, C	1/1	
00 1011 iiiii	SBC A, #i	$A - i - C \rightarrow A$	A					Z, C	1/1	
00 1010 0001	DEC A	$A - 1 \rightarrow A$	A					Z, C	1/1	SUB A, #1
00 0010 1001	DEC B	$B - 1 \rightarrow B$		B				Z, C	1/1	
00 0011 1001	DEC DP	$DP - 1 \rightarrow DP$			U	V	W	C	1/1	
00 1000 0001	INC A	$A + 1 \rightarrow A$	A					Z, C	1/1	ADD A, #1
00 0000 1001	INC B	$B + 1 \rightarrow B$		B				Z, C	1/1	
00 0001 1001	INC DP	$DP + 1 \rightarrow DP$			U	V	W	C	1/1	
Logic										
00 0100 1010, xxxxxxxxxx	ANL A, Mx	$A \wedge Mx \rightarrow A$	A					Z	2/2	
11 0110 0 iii	ANL A, WRx	$A \wedge WRx \rightarrow A$	A					Z	1/1	$x = 0 \sim 7$
00 0100 1011	ANL A, @M	$A \wedge @M \rightarrow A$	A		U	V	W	Z	1/1	
00 0101 1010, xxxxxxxxxx	ORL A, Mx	$A \vee Mx \rightarrow A$	A					Z	2/2	
11 0110 1 iii	ORL A, WRx	$A \vee WRx \rightarrow A$	A					Z	1/1	$x = 0 \sim 7$
00 0101 1011	ORL A, @M	$A \vee @M \rightarrow A$	A		U	V	W	Z	1/1	
00 0110 1010, xxxxxxxxxx	XRL A, Mx	$A \oplus Mx \rightarrow A$	A					Z	2/2	
11 0111 0 iii	XRL A, WRx	$A \oplus WRx \rightarrow A$	A					Z	1/1	$x = 0 \sim 7$
00 0110 1011	XRL A, @M	$A \oplus @M \rightarrow A$	A		U	V	W	Z	1/1	
00 0111 1010, xxxxxxxxxx	CMP A, Mx	$A - Mx$						Z, C	2/2	
11 0111 1 iii	CMP A, WRx	$A - WRx$						Z, C	1/1	$x = 0 \sim 7$

W921E880A/W921C880



10. Instruction set, continued

MACHINE CODE	MNEMONIC	FUNCTION	A	B	U	V	W	STATUS	W/C	MEMO
00 0111 1011	CMP A, @M	A - @M			U	V	W	Z, C	1/1	
00 0110 1001	XRL A, B	A ⊕ B → A	A		B			Z	1/1	
00 0111 1001	CMP A, B	A - B						Z, C	1/1	
00 1100 iiii	ANL A, #I	A ∧ I → A	A					Z	1/1	
00 1101 iiii	ORL A, #I	A ∨ I → A	A					Z	1/1	
00 1110 iiii	XRL A, #I	A ⊕ I → A	A					Z	1/1	
00 1111 iiii	CMP A, #I	A - I						Z, C	1/1	
00 1110 1111	NOT A	NOT A → A	A					Z	1/1	XRL A, #F
Move										
00 0000 0001	MOV A, B	B → A	A	B				Z	1/1	
00 0000 0010, xxxxxxxxxx	MOV A, Mx	Mx → A	A					Z	2/2	
00 0000 0011	MOV A, @M	@M → A	A		U	V	W	Z	1/1	
00 0000 0100	MOV A, W	W → A	A				W	Z	1/1	
00 0000 0101	MOV A, V	V → A	A			V		Z	1/1	
00 0000 0110	MOV A, U	U → A	A		U			Z	1/1	
00 0001 0000	MOV B, A	A → B	A	B				--	1/1	
00 0010 0000, xxxxxxxxxx	MOV Mx, A	A → Mx	A					--	2/2	
00 0011 0000	MOV @M, A	A → @M	A		U	V	W	--	1/1	
00 0100 0000	MOV W, A	A → W	A				W	--	1/1	
00 0101 0000	MOV V, A	A → V	A			V		--	1/1	
00 0110 0000	MOV U, A	A → U	A		U			--	1/1	
00 0001 0010, xxxxxxxxxx	MOV B, Mx	Mx → B		B				--	2/2	
00 0001 0011	MOV B, @M	@M → B		B	U	V	W	--	1/1	
00 0010 0001, xxxxxxxxxx	MOV Mx, B	B → Mx		B				--	2/2	
00 0011 0001	MOV @M, B	B → @M		B	U	V	W	--	1/1	
11 0000 iiii	MOV A, #I	I → A	A					Z	1/1	
11 0001 iiii	MOV B, #I	I → B		B				--	1/1	
11 0010 iiii, xxxxxxxxxx	MOV Mx, #I	I → Mx						--	2/2	
11 0011 iiii	MOV @M, #I	I → @M			U	V	W	--	1/1	
11 1000 nnnn	MOV A, WRn	WRn → A	A					Z	1/1	
11 1001 xxxx	MOV A, Px	Px → A	A					Z	1/1	
11 1010 nnnn	MOV B, WRn	WRn → B		B				--	1/1	
11 1011 xxxx	MOV B, Px	Px → B		B				--	1/1	
11 1100 nnnn	MOV WRn, A	A → WRn	A					--	1/1	
11 1101 nnnn	MOV Px, A	A → Px	A					--	1/1	
11 1110 xxxx	MOV WRn, B	B → WRn		B				--	1/1	

Publication Release Date: July 1999

W921E880A/W921C880



10. Instruction set, continued

MACHINE CODE	MNEMONIC	FUNCTION	A	B	U	V	W	STATUS	W/C	MEMO
11 1111 xxxx	MOV Px, B	B → Px		B				--	1/1	
10 0xxx iiii	MOV PMx, #I	I → PMx						--	1/1	Mode of Port 0–7
SERIAL I/O										
00 0100 1111	SOP	--						--	*1	
00 0101 1111	SIP	--						--	*1	
Rotate or Shift										
00 0000 1000	SRL A	An→An-1, 0→A3	A					Z	1/1	n = 3–1
00 0001 1000	SRH A	An→An-1, 1→A3	A					Z	1/1	n = 3–1
00 0010 1000	SLL A	An→An+1, 0→A0	A					Z	1/1	n = 0–2
00 0011 1000	SLH A	An→An+1, 1→A0	A					Z	1/1	n = 0–2
00 0100 1000	RRC A	An→An-1, A0→C, C→A3	A					Z, C	1/1	n = 3–1
00 0110 1000	RLC A	An→An+1, A3→C, C→A0	A					Z, C	1/1	n = 0–2
Branch										
10 1000 0aaa, aaaaaaaaaa	JB0 addr	Addr → PC						--	2/2	
10 1000 1aaa, aaaaaaaaaa	JB1 addr	Addr → PC						--	2/2	
10 1001 0aaa, aaaaaaaaaa	JB2 addr	Addr → PC						--	2/2	
10 1001 1aaa, aaaaaaaaaa	JB3 addr	Addr → PC						--	2/2	
10 1010 0aaa, aaaaaaaaaa	JC addr	Addr → PC						--	2/2	
10 1010 1aaa, aaaaaaaaaa	JNC addr	Addr → PC						--	2/2	
10 1011 0aaa, aaaaaaaaaa	JZ addr	Addr → PC						--	2/2	
10 1011 1aaa, aaaaaaaaaa	JNZ addr	Addr → PC						--	2/2	
10 1100 0aaa, aaaaaaaaaa	JMPL addr	Addr → PC						--	2/2	Long Jump
10 1100 1aaa, aaaaaaaaaa	CALL addr	Addr → PC						--	2/2	
10 1101 aaaa	CALLP addr	@Addr → PC	A	B				--	1/2	Indirect address call
10 1110 aaaa	TBL addr	--	A	B				Z	1/2	Look Up Table
Other										
00 0110 1111	RTN	Stack → PC						--	1/3	
00 0111 1111	RTNI	Stack → PC, Z, C						Z, C	1/3	ENINT active again
00 0000 0000	NOP	--						--	1/1	
00 0110 1110	HOLD	--						--	1/1	
00 0111 1110	STOP	--						--	1/1	
00 0001 11bb	CLRB @M, bit	0 → @M(b)			U	V	W	--	1/1	

W921E880A/W921C880



10. Instruction set, continued

MACHINE CODE	MNEMONIC	FUNCTION	A	B	U	V	W	STATUS	W/C	MEMO
00 0000 11bb, xxxxxxxxxxxx	CLRB Mx, bit	0 → Mx(b)						--	2/2	
00 0011 11bb	SETB @M, bit	1 → @M(b)			U	V	W	--	1/1	
00 0010 11bb, xxxxxxxxxxxx	SETB Mx, bit	1 → Mx(b)						--	2/2	
00 0111 1100	CLR CF	0 → C						C	1/1	
11 0000 0000	CLR A	0 → A	A					Z	1/1	MOV A, #0
00 0100 1100, 00i i i i i i i i	CLR EVF, #I	--						--	2/2	
00 0110 1100	SET CF	C = 1						C	1/1	
00 0100 1110, i i i i i i i i i i	MOV DP, #I	I → DP			U	V	W	--	2/2	
00 0111 1101	XCH U, CU	U ↔ CU			U			--	1/1	
00 0110 1101	XCH V, CV	V ↔ CV				V		--	1/1	
00 0100 1101	XCH A, B	A ↔ B	A	B				Z	1/1	

Notes:

*DP = {W reg, V reg, U reg}

*@M = {@W, V, U}

*@Addr = {I, Breg, Areg} to be a target address for the CALLP instruction

*1: Depends on the SRMNR, SRLNR register

11. ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply Voltage to Ground Potential	-0.3 to +7.0	V
Applied input/output Voltage	-0.3 to +7.0	V
Power Dissipation	120	mW
Ambient Operating Temperature	0 to +70	°C
Storage Temperature	-55 to 150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

W921E880A/W921C880



12. ELECTRICAL CHARACTERISTICS

12.1 AC Characteristics

W921E880A EPROM Type

(VDD-VSS = 3.0V, Fosc = 4.0 MHz, TA = 25° C, unless otherwise specified)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating Frequency 1	Fosc1	OSCI, OSCO	--	400	--	KHz
Operating Frequency 2	Fosc2	OSCI, OSCO	--	800	--	KHz
Operating Frequency 3	Fosc3	OSCI, OSCO	--	2	--	MHz
Operating Frequency 4	Fosc4	OSCI, OSCO	--	3.58	--	MHz
Operating Frequency 5	Fosc5	OSCI, OSCO	--	4	--	MHz
Operating sub. system	FSUB	XT, $\overline{XT}$	--	32.768	--	KHz
Instruction Cycle Time	Ti	One Machine Cycle	--	4/Fosc	--	S
Serial Port Data Ready Time	TDR	--	200	--	--	nS
Serial Port Data Hold Time	TDH	--	200	--	--	nS
$\overline{RESET}$ Active Width	TRAW	--	2Ti	--	--	Ti
ROW 1 Frequency (697Hz)	FROW1	FOSC = 4 MHz, 2 MHz 800 KHz, 400 KHz	-0.5	--	+0.5	%
ROW 2 Frequency (770 Hz)	FROW2	"	-0.5	--	+0.5	%
ROW 3 Frequency (852 Hz)	FROW3	"	-0.5	--	+0.5	%
ROW 4 Frequency (941 Hz)	FROW4	"	-0.5	--	+0.5	%
COL 1 Frequency (1209 Hz)	FCOL1	"	-0.5	--	+0.5	%
COL 2 Frequency (1336 Hz)	FCOL2	"	-0.5	--	+0.5	%
COL 3 Frequency (1477 Hz)	FCOL3	"	-0.5	--	+0.5	%
COL 4 Frequency (1633 Hz)	FCOL4	"	-0.5	--	+0.5	%
ROW 1 Frequency (697 Hz)	FROW1	FOSC = 3.58 MHz	-0.92	--	+0.92	%
ROW 2 Frequency (770 Hz)	FROW2	"	-0.92	--	+0.92	%
ROW 3 Frequency (852 Hz)	FROW3	"	-0.92	--	+0.92	%
ROW 4 Frequency (941 Hz)	FROW4	"	-0.92	--	+0.92	%
COL 1 Frequency (1209 Hz)	FCOL1	"	-0.92	--	+0.92	%
COL 2 Frequency (1336 Hz)	FCOL2	"	-0.92	--	+0.92	%
COL 3 Frequency (1477 Hz)	FCOL3	"	-0.92	--	+0.92	%
COL 4 Frequency (1633 Hz)	FCOL4	"	-0.92	--	+0.92	%
Oscillator Start Time	TOST	OSCO, $\overline{XT}$	--	$\frac{17}{2} / F_{osc}$	--	mS

W921C880 Mask ROM Type

(V_{DD}–V_{SS} = 3.0V, F_{osc} = 4.0 MHz, T_A = 25° C, unless otherwise specified)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating Frequency	FOSC1	OSCI, $\overline{OSCO}$	–	400	–	KHz
	FOSC2		–	800	–	KHz
	FOSC3		–	2	–	MHz
	FOSC4		–	3.58	–	MHz
	FOSC5		–	4	–	MHz
Operating Sub-frequency	FSUB	XT, $\overline{XT}$	–	32.768	–	KHz
Instruction Cycle Time	TI	One Machine Cycle	–	4/F _{osc}	–	S
Serial Port Data Ready Time	TDR	–	200	–	–	nS
Serial Port Data Hold Time	TDH	–	200	–	–	nS
RESET Active Width	TRAW	–	2	–	–	Ti
ROW 1 Frequency (697Hz)	FROW1	FOSC = 4 MHz, 2 MHz, 800 KHz, 400 KHz	-0.5	–	+0.5	%
		FOSC = 3.58 MHz	-0.92	–	+0.92	
ROW 2 Frequency (770 Hz)	FROW2	Same as ROW1	-0.5	–	+0.5	%
			-0.92	–	+0.92	
ROW 3 Frequency (852 Hz)	FROW3	Same as ROW1	-0.5	–	+0.5	%
			-0.92	–	+0.92	
ROW 4 Frequency (941 Hz)	FROW4	Same as ROW1	-0.5	–	+0.5	%
			-0.92	–	+0.92	
COL 1 Frequency (1209 Hz)	FCOL1	Same as ROW1	-0.5	–	+0.5	%
			-0.92	–	+0.92	
COL 2 Frequency (1336 Hz)	FCOL2	Same as ROW1	-0.5	–	+0.5	%
			-0.92	–	+0.92	
COL 3 Frequency (1477 Hz)	FCOL3	Same as ROW1	-0.5	–	+0.5	%
			-0.92	–	+0.92	
COL 4 Frequency (1633 Hz)	FCOL4	Same as ROW1	-0.5	–	+0.5	%
			-0.92	–	+0.92	
Oscillator Start Time	TOST	$\overline{OSCO}$	–	2 ¹⁷ /F _{osc}	–	mS

W921E880A/W921C880



12.2 DC Characteristics

W921E880A EPROM Type

(V_{DD}-V_{SS} = 3.0V, F_{osc} = 4.0 MHz, T_A = 25° C, unless otherwise specified)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V _{DD}	--	2.8	3.0	5.5	V
Operating Current 1 (4 MHz) (Active mode)	I _{OP1}	Analog active. V _{DD} = 5V	--	9	12	mA
Operating Current 2 (4 MHz) (Active mode)	I _{OP2}	Analog disable V _{DD} = 5V	--	5	8	mA
Operating Current 3 (800 KHz) (Active mode)	I _{OP3}	Analog active. V _{DD} = 3V	--	3.1	4.3	mA
Operating Current 4 (800 KHz) (Active mode)	I _{OP4}	Analog disable V _{DD} = 3V	--	0.6	1.8	mA
Operating Current 5 (400 KHz) (Active mode)	I _{OP5}	Analog active. V _{DD} = 3V	--	1.0	2.0	mA
Operating Current 6 (400 KHz) (Active mode)	I _{OP6}	Analog disable V _{DD} = 3V	--	0.4	1.0	mA
Hold Mode Current 1 (4 MHz)	I _{HM1}	V _{DD} = 5V	--	1.2	2.0	mA
Hold Mode Current 2 (800 KHz)	I _{HM2}	V _{DD} = 3V	--	0.2	0.7	mA
Hold Mode Current 3 (400 KHz)	I _{HM3}	V _{DD} = 3V	--	0.1	0.4	mA
Hold Mode Current 4 (32.768 KHz)	I _{HM4}	V _{DD} = 3V	--	50	80	μA
Stop Mode Current 1 (4 MHz)	I _{SM1}	V _{DD} = 5V	--	2.0	3.0	μA
Stop Mode Current 2 (800 KHz)	I _{SM2}	V _{DD} = 3V	--	1.0	3.0	μA
Stop Mode Current 3 (400 KHz)	I _{SM3}	V _{DD} = 3V	--	1.0	3.0	μA
Stop Mode Current 4 (32.768 KHz)	I _{SM4}	V _{DD} = 3V	--	1.0	3.0	μA
Input High Voltage	V _{IH}	--	0.7 V _{DD}	--	V _{DD}	V _{DD}
Input Low Voltage	V _{IL}	--	0	--	0.3 V _{DD}	V _{DD}
Pull-high Resistor (P2, P4, P6, P7, P9, PA, PB, PC, PD)	R _{PH}	V _{DD} = 3V	--	400	--	KΩ
Output High Voltage (P0, P1, P8) (The other ports)	V _{OH1}	V _{DD} = 4.5 to 5.5V I _{OH} = -10 mA	2.0	--	--	V
	V _{OH2}	I _{OH} = -0.5 mA	V _{DD} -1.0	--	--	V
Output Low Voltage (P2, P7, P9) (The other ports)	V _{OL1}	V _{DD} = 4.5 to 5.5V I _{OL} = 15 mA	--	--	2.0	V
	V _{OL2}	I _{OL} = 0.4 mA	--	--	0.4	V

W921E880A/W921C880



W921E880A EPROM TYPE DC Characteristics, continued

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Leakage Current (RESET , TEST)	V _{IL}	V _{IN} = 0V	--	--	1	μA
DTMF Output DC Level	V _{TDC}	V _{DD} = 2.8 to 5.5V	1.0	--	3.0	V
DTMF Distortion	V _{DD}		-	-30	-23	dB
DTMF Output Voltage	V _{TO}	ROW Group, R _L = 5 KΩ	130	150	170	mV _{rms}
Pre-emphasis		COL/ROW	1	2	3	dB
D/A DC Voltage Reference	V _{REF}	--	0	--	2/3	V _{DD}
D/A Resoulution	V _{RSL}	--	--	1/256	--	V _{DAC}

W921C880 Mask ROM Type

(V_{DD}-V_{SS} = 3.0V, F_{osc} = 4.0 MHz, T_A = 25° C, unless otherwise specified)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V _{DD}	4 MHz	2.4	-	5.5	V
		2 MHz	2.0	-	5.5	V
		400 KHz	2.0	-	5.5	V
Operating Current (Active Mode) (Analog all off)	I _{OP}	V _{DD} = 3V	4 MHz	--	1.0	mA
			2 MHz	--	0.7	mA
			400 KHz	--	0.4	mA
	V _{DD} = 5V	4 MHz	--	2.5	--	mA
		2 MHz	--	2.2	--	mA
		400 KHz	--	1.5	--	mA
Hold Mode Current (Analog all off)	I _{HM1}	V _{DD} = 3V, F _{osc} = 4 MHz	--	0.5	--	mA
		V _{DD} = 5V, F _{osc} = 4 MHz	--	2.0	--	mA
Hold Mode Current (Analog all off)	I _{HM2}	V _{DD} = 3V, F _{osc} = 32.768 KHz	--	10	--	μA
		V _{DD} = 5V, F _{osc} = 32.768 KHz	--	50	--	μA
Stop Mode Current	I _{SM}	V _{DD} = 3V	--	1.0	3.0	μA
		V _{DD} = 5V	--	1.0	3.0	μA
Input High Voltage	V _{IH}	--	0.7 V _{DD}	--	V _{DD}	V _{DD}
Input Low Voltage	V _{IL}	--	0	--	0.3 V _{DD}	V _{DD}

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W921E880A/W921C880

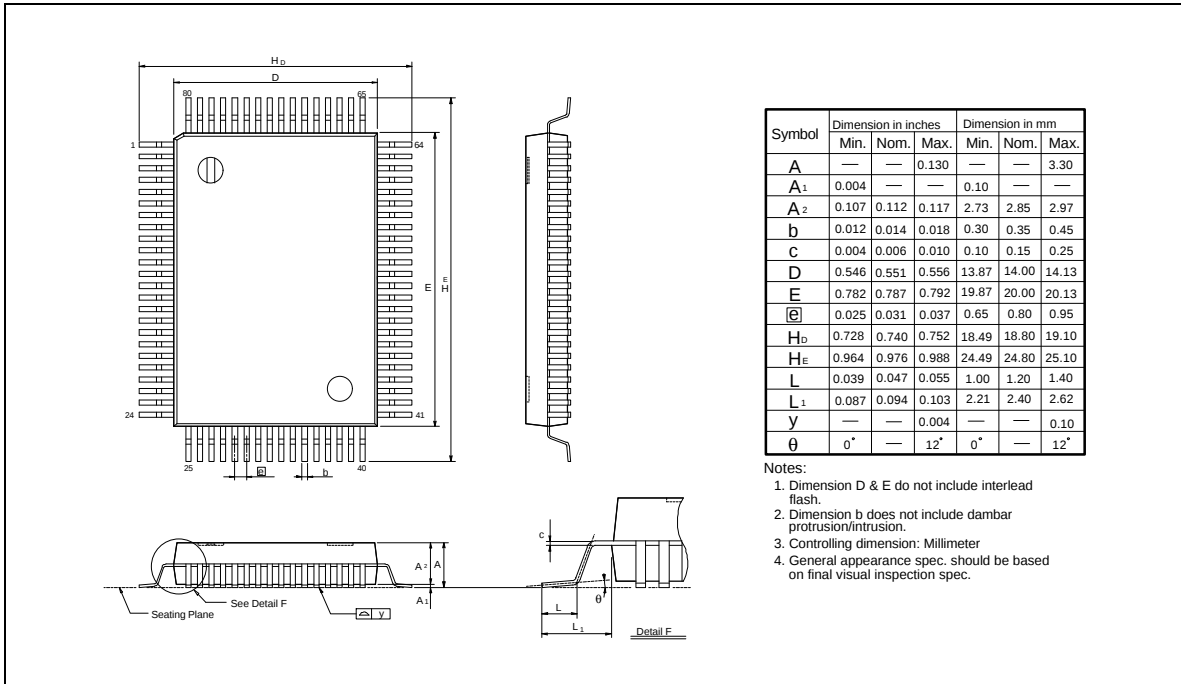


W921C880 Mask ROM Type, continued

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pull-high Resistor (P2, P4, P6, PA, PB, PC, PD)	RPH	VDD = 3V	—	400	—	K Ω
Output High Voltage	VOH	IOH = -0.5 mA	VDD -1.0		—	V
Output Low Voltage	VOL1	IOL = 15 mA, port P2	—	—	2.0	V
	VOL2	IOL = 0.4 mA, Other ports	—	—	0.4	
Input Leakage Current	VIL	VIN = 0V, RESET pin	—	—	1	μ A
DTMF Output DC Level	VTDC	VDD = 2.8 to 5.5V	1.0	—	3.0	V
DTMF Distortion	THD	VDD = 2.8 to 5.5V	-	-30	-23	dB
DTMF Output Voltage	VTO	ROW Group, RL = 5 K Ω	130	150	170	mVrms
Pre-emphasis		Col/Row VDD = 3.0 to 5.5V	1	2	3	dB
D/A DC Reference Voltage	VREF	—	0	—	2/3	VDD
D/A Resolution Voltage	VRSL	—	—	1/256	—	VDAC

13. PACKAGE DIMENSIONS

80-pin QFP



W921E880A/W921C880



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Note: All data and specifications are subject to change without notice.