DSP CONTROLLER FOR TAD

GENERAL DESCRIPTION

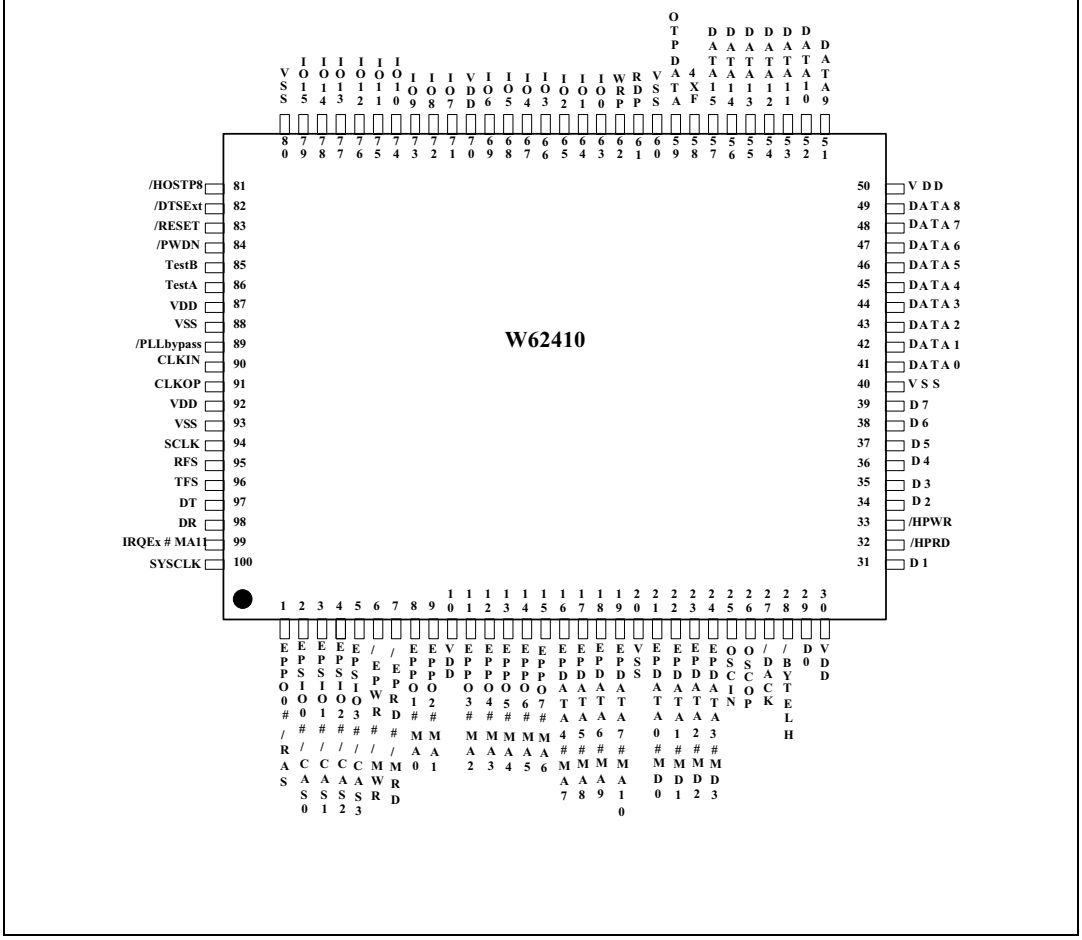
The W62410 chip is a digital speech signal processor. The W62410 implements the STREAMTALK™ speech compression, voice prompt processing, telephone line signal processing, AFlash and DRAM memory management and 16 I/O lines all in one chip for a fully digital answering machine. The W62410 acts as a slave processor to its host. The W62410 can be driven through a serial bus or an 8 bit parallel bus allowing the possibility for both 4 bit and 8 bit micro controllers to be used. Since the W62410 is a slave to the host, the host is responsible for activating and deactivating all the functions the W62410 provides.

FEATURES

- 24.576 MIPS for CHIPSET core and 24.576 MHz crystal used.
- Internal Voice Prompt ROM, 16K × 16 (256 KBits), which can be optionally swapped to an external Winbond proprietary serial OTP Message Storage Option.
- Support for up to four times 1M × 4 or one 4M × 4 types DRAM for up to 16 Mbits storage space and refresh ability.
- Support for up to four times Samsung KM29N040T, 512K × 8, NAND Flash for up to 16 Mbits of storage space.
- Support for up to four times Samsung KM29N1600T, 2M × 8, NAND Flash for up to 64 Mbits of storage space.
- Serial or 8-bits parallel μC interface supported.
- One CODEC interface (μLaw codec such as the TP3054).
- Sixteen available I/O lines. Individually programmable as an input or output line.
- No external SRAM needed.
- Real Time Clock supports Weekday/Hour/Minute.
- The RTC keeps running while in Power down mode (using a 32.768 KHz crystal).
- Low Power Consumption and Power down mode support.
- Fully static design.
- Packaged in 100-pin PQFP

PIN CONFIGURATION

The W62410 is available in a 100 pin PQFP package.



BLOCK DIAGRAM

Example TAD Application

The figure below shows the basic block diagram for building a digital answering machine using the W62410 CHIPSET. In addition to the CHIPSET the following are needed:

- A μLaw CODEC.
- DRAM of FLASH for use as external memory storage space.
- A 4 or 8-bit μController (using the serial port or 8-bit parallel port of the CHIPSET).
- A 24.576 MHz crystal as the system clock for the CHIPSET.
- A 32.768 KHz crystal for the Real Time Clock and to refresh the DRAM in Power Down mode.
- Optionally an external OTP to disable the internal voice prompts, if preferred.
- A DAA, user interface, microphone, loudspeaker, power supply, battery backup etc.

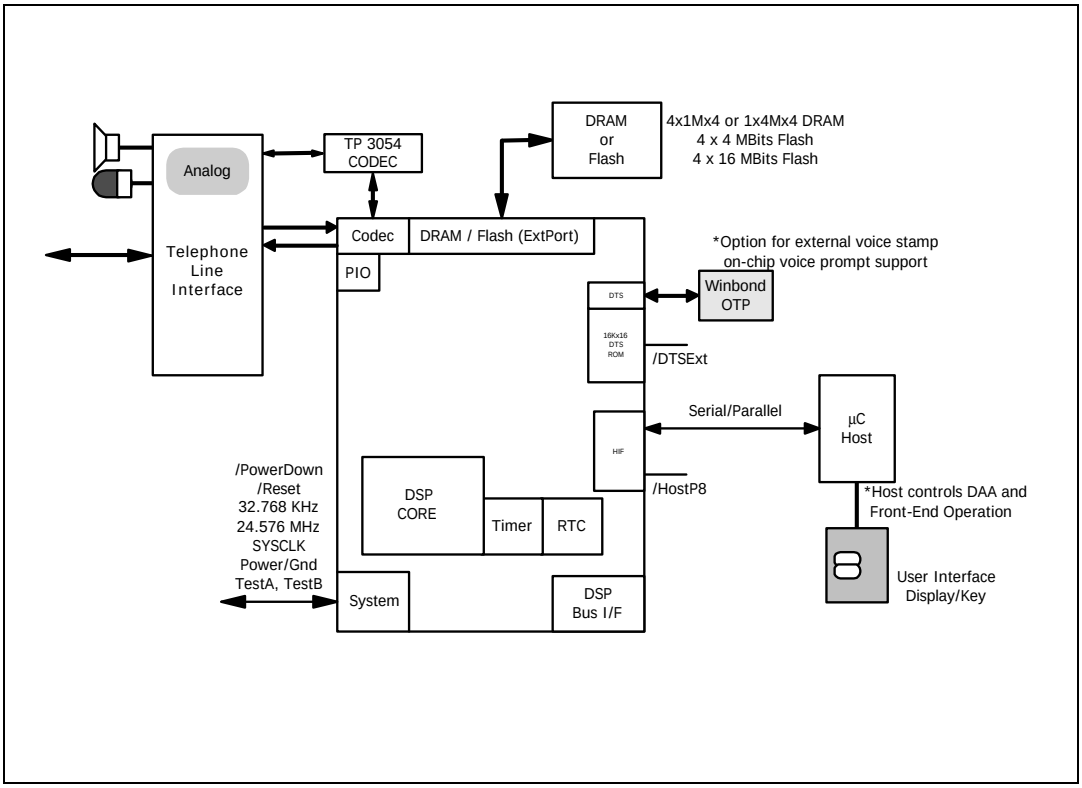


Figure 2. W62410 Block Diagram

PIN DESCRIPTION

Power and Clock

PIN NAME	PIN NUMBER	I/O	FUNCTION
VDD	10, 30, 50, 70, 87, 92		Power
GND	20, 40, 60, 80, 88, 93		Ground
OSCIN	25	I	32768 Hz Crystal Oscillator Input
OSCOP	26	O	32768 Hz Crystal Oscillator Output
ClkIN	90	I	24.576 MHz Crystal Oscillator Input
ClkOP	91	O	24.576 MHz Crystal Oscillator Output
SYSCLK	100	O	24.576 MHz System Clock Output, while bit EnSYSCLK in TEST Reg. set, otherwise tri-state
$\overline{\text{RESET}}$	83	I	System hardware reset, internal pull high, schmitt trigger input
$\overline{\text{PWDN}}$	84	I	Power low Indicator schmitt trigger input w/o pull high

Codec Interface

PIN NAME	PIN NUMBER	I/O	FUNCTION
SCLK	94	O	Serial Clock at Serial Port, 2.048 MHz
RFS	95	O	Receive frame sync. of Serial port
TFS	96	O	Transmit frame sync. of Serial port
DR	98	I	Serial DATA received at Serial port
DT	97	O	Serial DATA transmitted at Serial port

PIO Interface

PIN NAME	PIN NUMBER	I/O	FUNCTION
IO 0..15	63, 64, 65, 66, 67, 68, 69, 71, 72, 73, 74, 7, 5, 76, 77, 78, 79	I/O	Bit I/O port Internal pull-up as input

HOST Interface

PIN NAME (Parallel)	PIN NAME (Serial)	PIN NUMBER	I/O	FUNCTION
$\overline{\text{HostP8}}$	$\overline{\text{HostP8}}$	81	I	Host Selection Input Low for 8 bits parallel host mode High for serial host mode
$\overline{\text{DACK}}$	$\overline{\text{DACK}}$	27	O/P	Host acknowledge
$\overline{\text{ByteLH}}$	-------	28	I/P	Parallel : Select low or high byte
D[0]	HRdD	29	I/O	Parallel : Bi-directional data bit 0 Serial : Host Read Data Out
D[1]	HWrD	31	I/O	Parallel : Bi-directional data bit 1 Serial : Host write data In
$\overline{\text{HPRD}}$	HRdClk	32	I/P	Parallel : Read strobe in Serial : Host read clock in
$\overline{\text{HPWR}}$	HWrClk	33	I/P	Parallel : Read write in Serial : Host write clock in
D[2..7]	-------	34, 35, 36, 37, 38, 39	I/O	Parallel : Bi-directional data bit 2..7

DRAM/Flash & Extension Port Interface

PIN NAME (DRAM)	I/O	PIN NAME (Flash)	I/O	PIN NUMBER	DESCRIPTION
$\overline{\text{RAS}}$	O	EPPO0	O	1	DRAM: Row address strobe ExtPort: Extension parallel OP 0
$\overline{\text{CAS0}}$, 1, $\overline{\text{CAS2}}$, 3	O	EPSIO[0..3]	I/O	2, 3, 4, 5	DRAM: Column address strobe ExtPort: Extension serial IO [0..3] with internal pull up
$\overline{\text{MWR}}$	O	$\overline{\text{EPWR}}$	O	6	DRAM: DRAM write strobe ExtPort: Extension port write enable
$\overline{\text{MRD}}$	O	$\overline{\text{EPRD}}$	O	7	DRAM: DRAM Read strobe ExtPort: Extension port read enable
MA[0..10]	O	EPPO[1..7] EPData[4..7]	O I/O	8, 9, 11, 12, 13, 1, 4, 15, 16, 17, 18, 19	DRAM: DRAM Address bus ExtPort: Extension parallel OP[1..7], Extension bit data port[4..7]

DRAM/Flash & Extension Port Interface, continued

PIN NAME (DRAM)	I/O	PIN NAME (Flash)	I/O	PIN NUMBER	DESCRIPTION
MA[11]	O	IRQEx	I	99	DRAM : DRAM Address bit 11 ExtPort: Extension port interrupt
MD[0..3]	I/O	EPData[0..3]	I/O	21, 22, 23, 24	DRAM: Data bus for DRAM controller ExtPort: Extension bit data port[0..3] *Bi-directional I/O pin with repeater*

DTS ROM Interface

PIN NAME	PIN NUMBER	I/O	FUNCTION
$\overline{\text{DTSExt}}$	82	I	DTS ROM selection, *internal pull-up* 1: Internal DTS ROM. In this mode the following 3 pins are of no use. 0: External DTS ROM
Wrp	62	O/P	Write Clock Pulse, active high
Rdp	61	O/P	Read Clock Pulse, active high
OtpData	59	I/O	Bi-directional Data Line

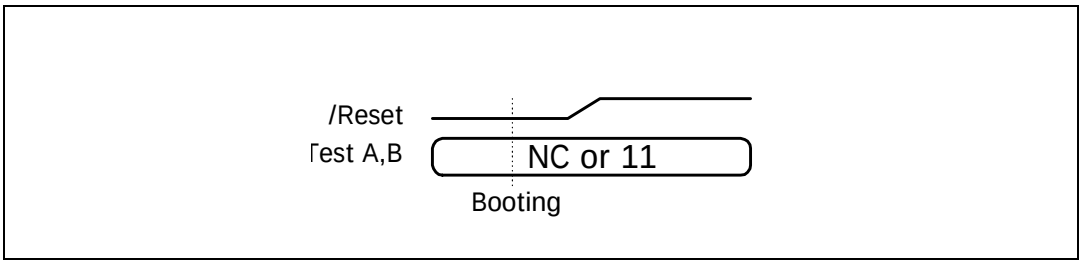
TEST Pins

PIN NAME	PIN NUMBER	I/O	FUNCTION
$\overline{\text{PLLbypass}}$	89	I	PLL bypass test mode for use in test machine only, *internal pull up* Low : Bypass PLL, High : Normal
4xF	58	O	Output, 4xClkIn, while bit En4xF in *TEST Configuration Reg.* set to high, otherwise tri-state
TestA TestB	86 85	I	*Internal pull high*, Test mode set Leave these pins NC in normal mode

CHIPSET BUS Interface:

PIN NAME	PIN NUMBER	I/O	FUNCTION
DATA[0..15]	41, 42, 43, 44, 45, 46, 47, 48, 49, 51, 52, 53, 54, 55, 56, 57	I/O	Test pins

Booting Sequence



CODEC Interface

- The interface signals for the μLaw CODEC are: SCLK, RFS, TFS, DR and DT.
- The relationship between SYSCLK and SCLK is as follows:

$$SCLK = \frac{SYSCLK}{2*(SCLKDIV+1)}$$

$$2{,}048MHz = \frac{24{,}576{,}000MHz}{2*(5+1)}$$

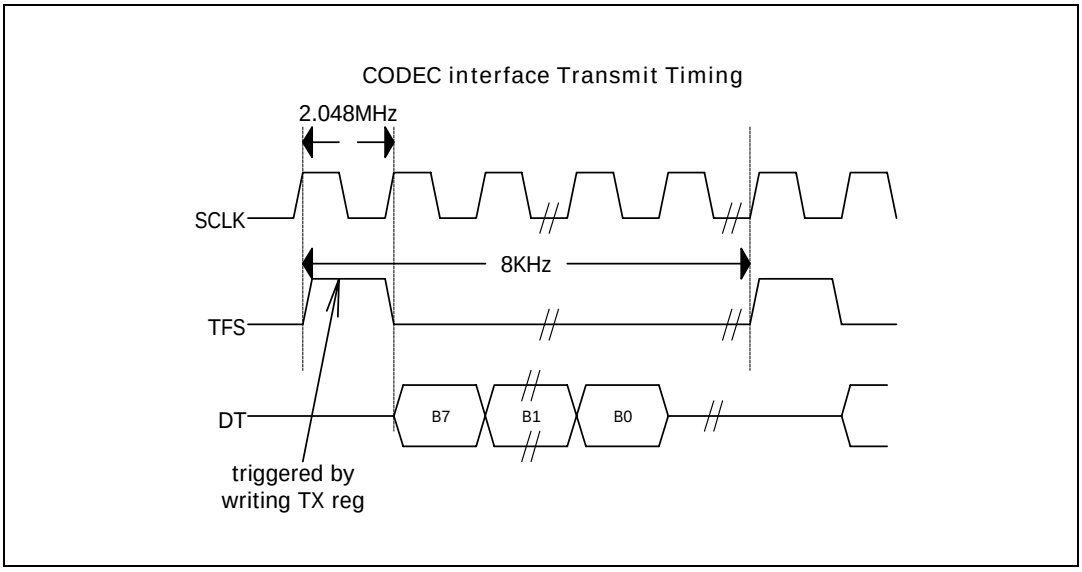
- Therefore, the value of SCLKDIV in the **Init** command should be set to five when using the CHIPSET with a SYSCLK of 24.576 MHz. This results in a sampling rate of 8 KHz.

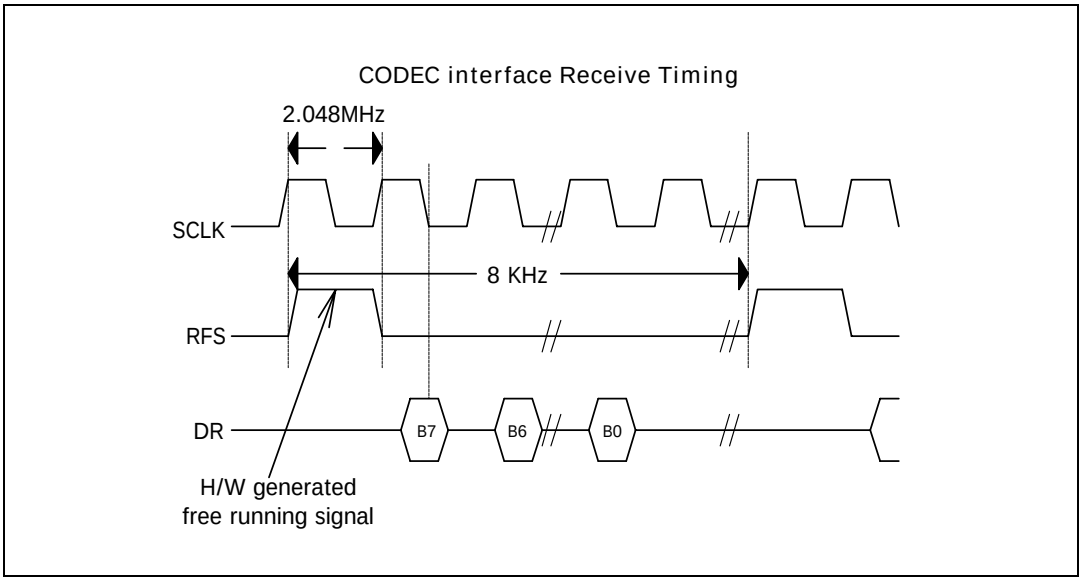
  The Receive frame sync (RFS) rate

$$\frac{2{,}048{,}000Hz}{256} = 8{,}000Hz\ .$$

TIMEING WAVEFORMS

CODEC Timing





DRAM as External Storage Memory

Selecting DRAM:

The following types of DRAM are allowed:

Type	Row	Column
1M × 4	MA 0..9	MA 0..9
4M × 4	MA 0..10	MA 0..10
4M × 4	MA 0..11	MA 0..9

DRAM Refresh:

- The DRAM controller uses **C**AS-**B**EFORE-**R**AS (CBR) in a distributed way at every 15.625 µS. There are two different refresh modes available in the DRAM controller:

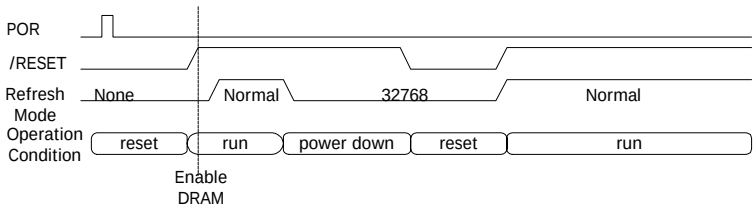
Normal Mode: While in normal operation, the DRAM controller the refresh request is determined by the value of **REFDIV** and of the SYSCLK. The exact formula can be found below:

$$\frac{1000}{24.576} * (REFDIV + 1) = refreshperiod = 15.625\mu S$$

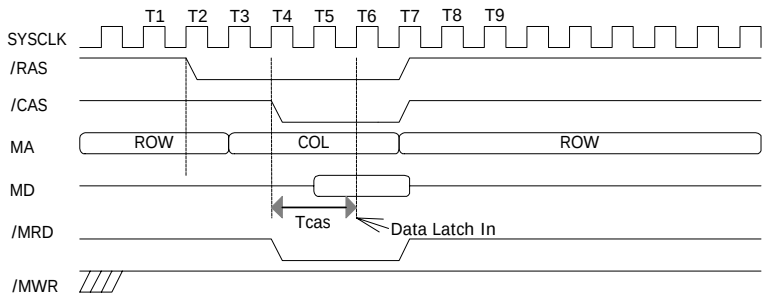
Thus, the **REFDIV** value controls the refresh period. The default value is 383.

32768 Mode: While in Power Down mode, the DRAM controller generates the refresh request at the frequency of 2 times 32,768 Hz, or about every 15.3 µS.

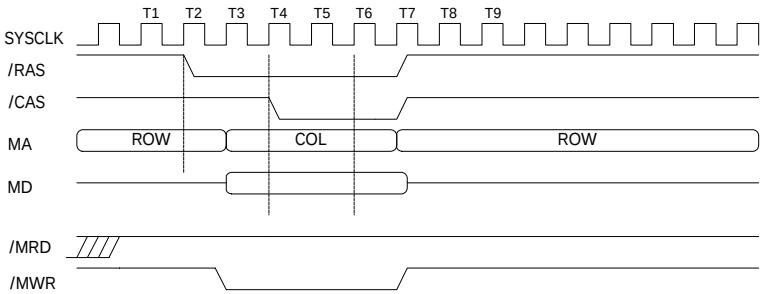
Refresh Mode in different operation conditions



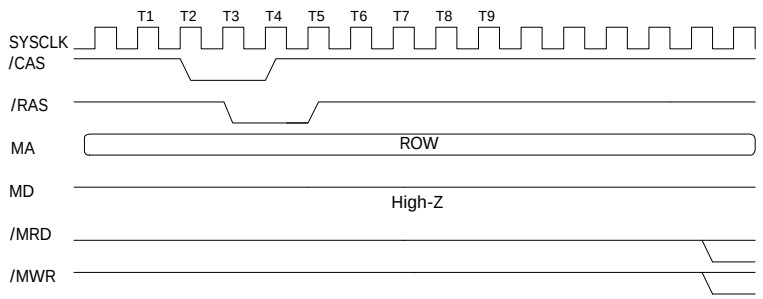
DRAM Normal Read Cycle



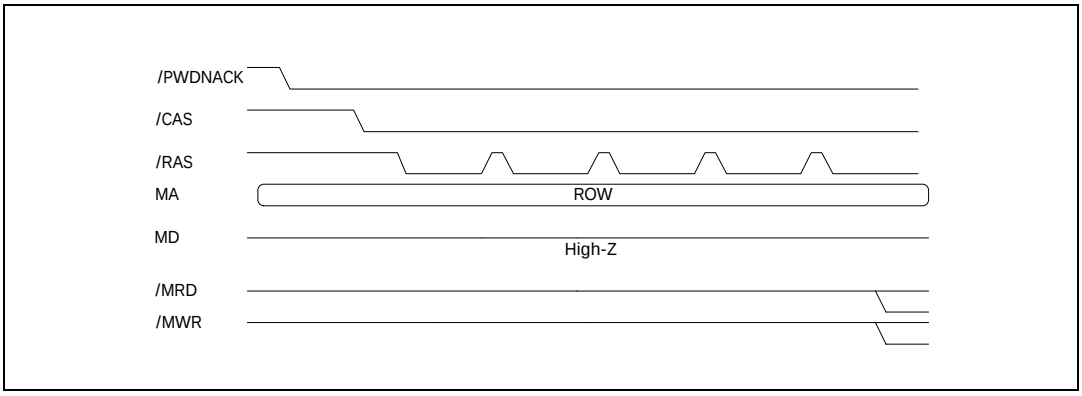
DRAM Early Write Cycle



DRAM Normal CBR Refresh Cycle

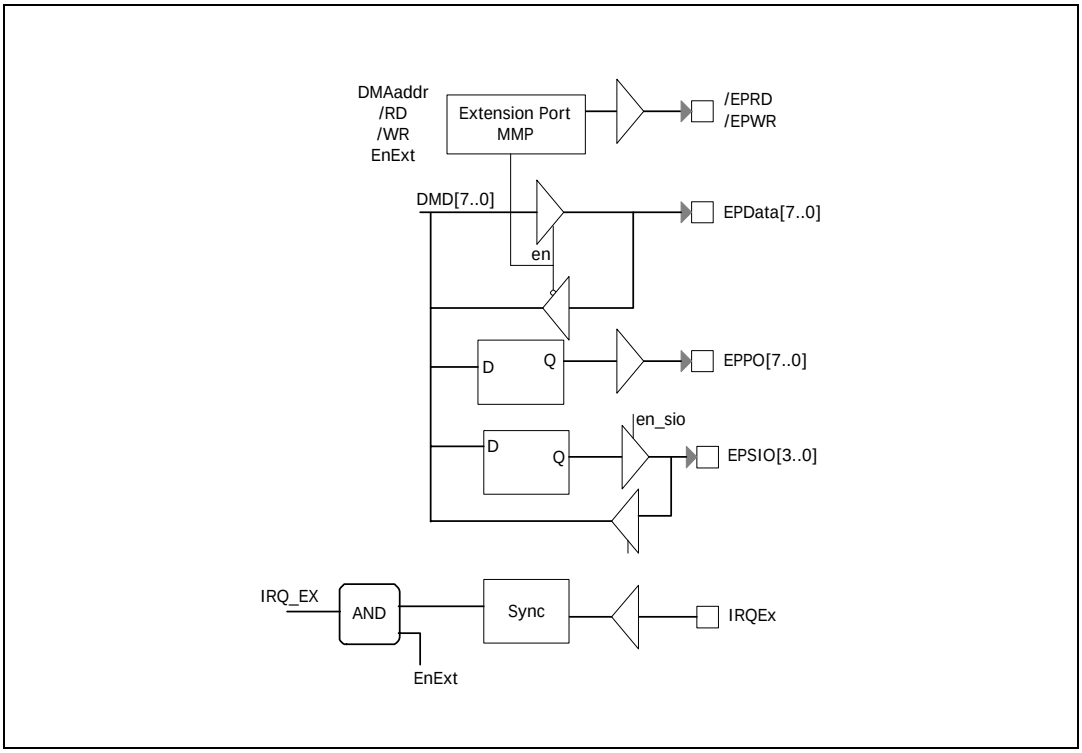


DRAM CBR Refresh Cycle

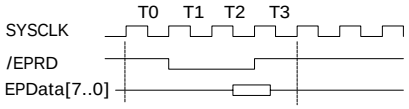


FLASH as External Storage Memory

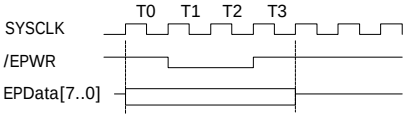
Flash interface (extension port)



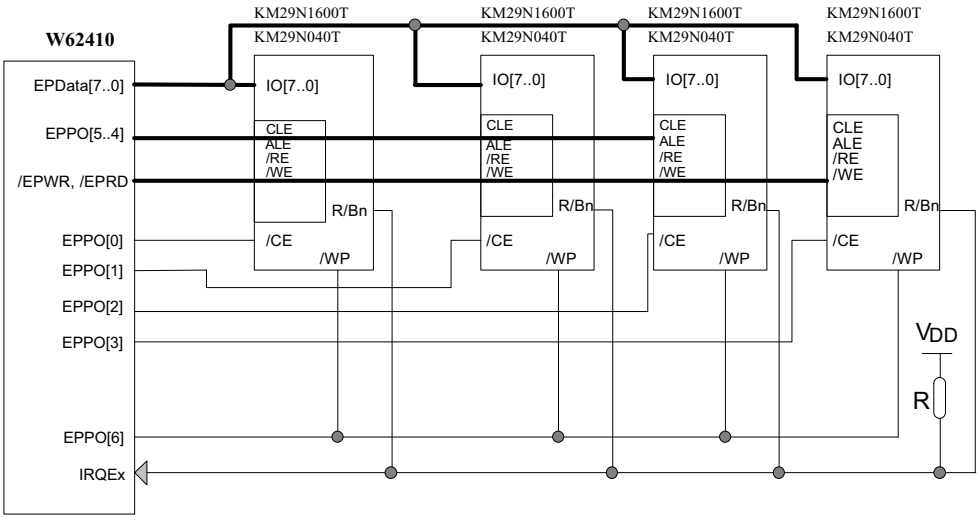
Flash Read Cycle



Flash Write Cycle

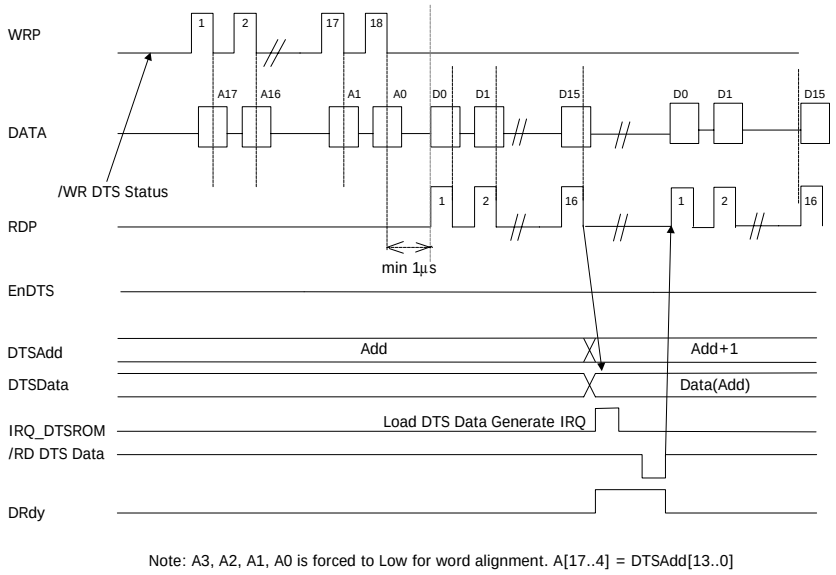


Using Flash with the W62410



External OTP Functional Waveform (for W55412 and W55412A)

The W62410 has the capability to use an external OTP instead of its own internal 256 KBits ROM for the storage of voice prompts. Below you can find the timing signals between the W62410 and either the W55412 or W55412A OTP.



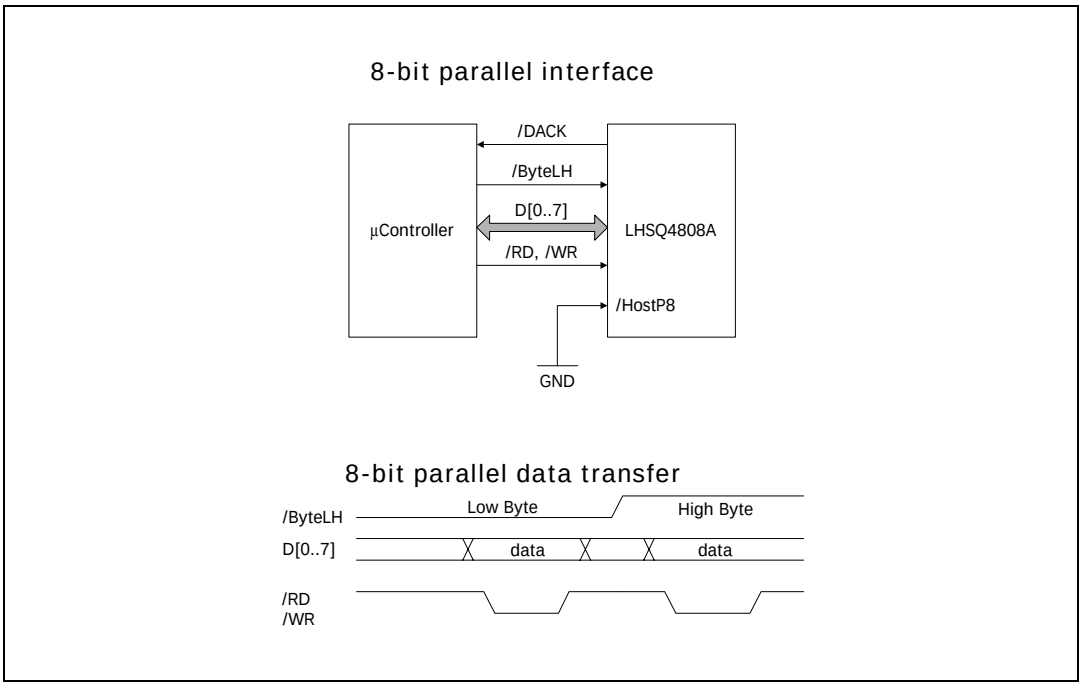
Note: A3, A2, A1, A0 is forced to Low for word alignment. A[17..4] = DTSAdd[13..0]

HOST Interface (HIF)

The W62410 allows connecting to the host controller through a serial or a 8 bits parallel (8051-like) port. The port is selected through the /HostP8pin:

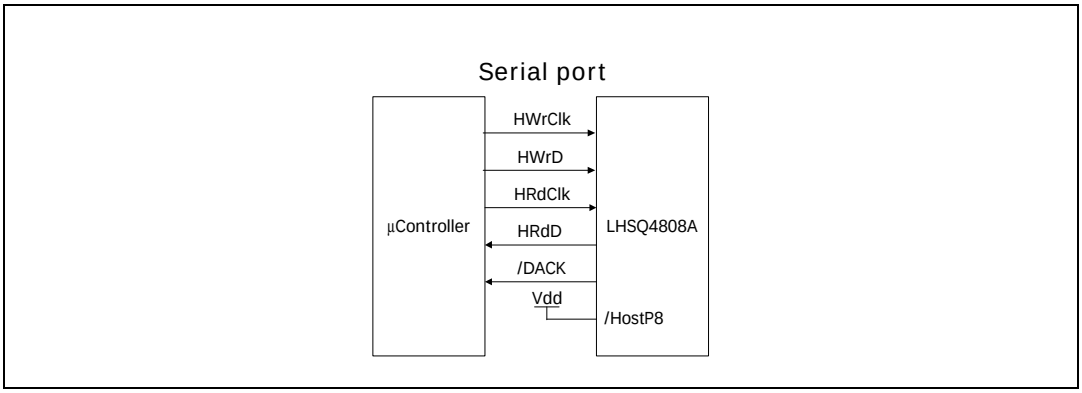
/HostP8pin	Selects
Low	8-bit parallel (8051-like) interface
High	Serial µController interface

8-bits µController interface



- The µController can send a command to the W62410 by writing the low byte first followed by the high byte of the 16-bit command word.
- The µController can read the 16-bit result from the W62410 by reading the low byte first followed by the high byte after receiving a /DACK interrupt from the W62410 to indicate that there is data to be read.

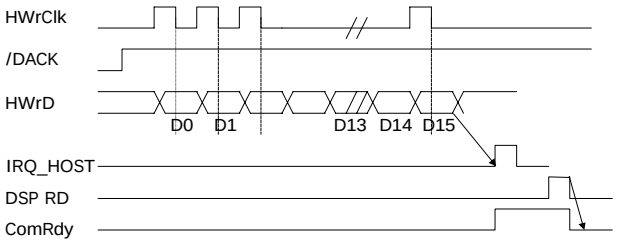
Serial µController interface



The host can write a 16-bit command in the following way:

- Check that the /DACK pin is set high to be sure you can send a new command to the W62410.
- The µController has to toggle HWrClk and HWrD to send the 16-bit command to the Command Register of the W62410. The W62410 samples in the HWrD, with LSB first, at the falling edge of HWrClk. After having received 16 falling edges, the HWrClk returns to low and the complete 16-bit command has been stored in the command register of the W62410.
- The HIF asserts ComRdy and generates an IRQ_HOST inside the W62410. After the W62410 has read the 16-bit command, the ComRdy signal will return to the low state.

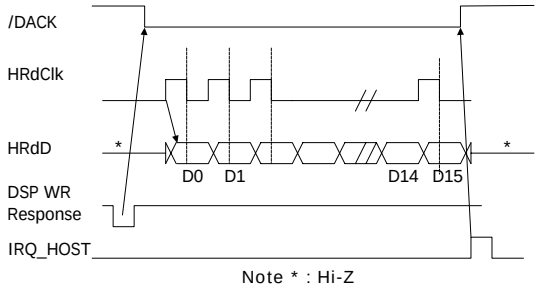
Serial Host Interface timing
Host Write, HWrClk Normal Low



The host can read the 16-bit result in the following way:

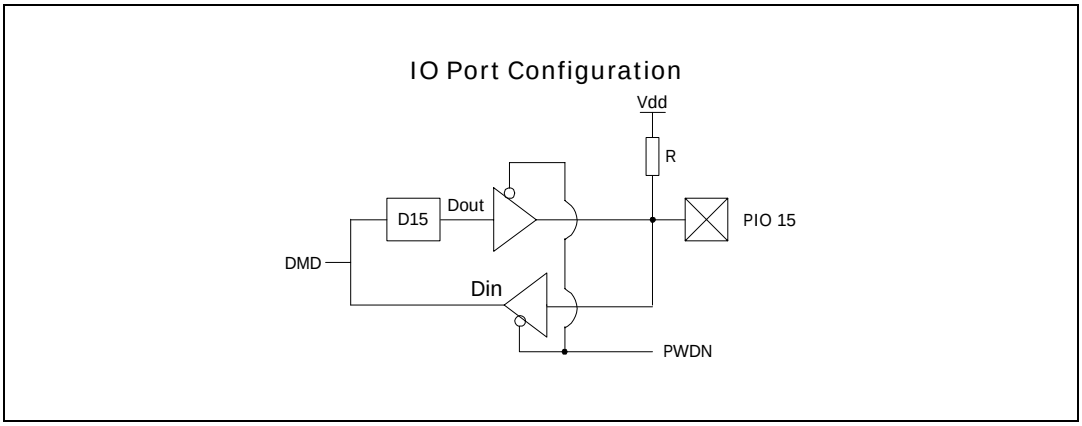
- When the W62410 writes into the result register, then the $\overline{\text{DACK}}$ pin will be set low.
- The ?Controller has to toggle the HRdClk to sample the HRdD. The ?Controller will receive the 16-bit data with LSB first on the HRdD pin, at the falling edge of HRdclk. After 16 falling edges the complete result has been received, HRdClk returns to low and the $\overline{\text{DACK}}$ pin will be set high again.

Serial Host Interface timing
Host Read, HRdClk in Normal Low



Note * : Hi-Z

PIO Controller



- The I/O ports of IO 0..15 are bi-directional.
- If user read the I/O port, the output latch will stay in tri-state mode and a weak pull high of about 40 μA will be present to have data input.
- For the transition from write to read state, a dummy read is needed.
- The I/O port will stay in output tri-state condition (including the pull high) during power down mode and the input will be gated to avoid leakage current.

Power on Reset and H/W Reset

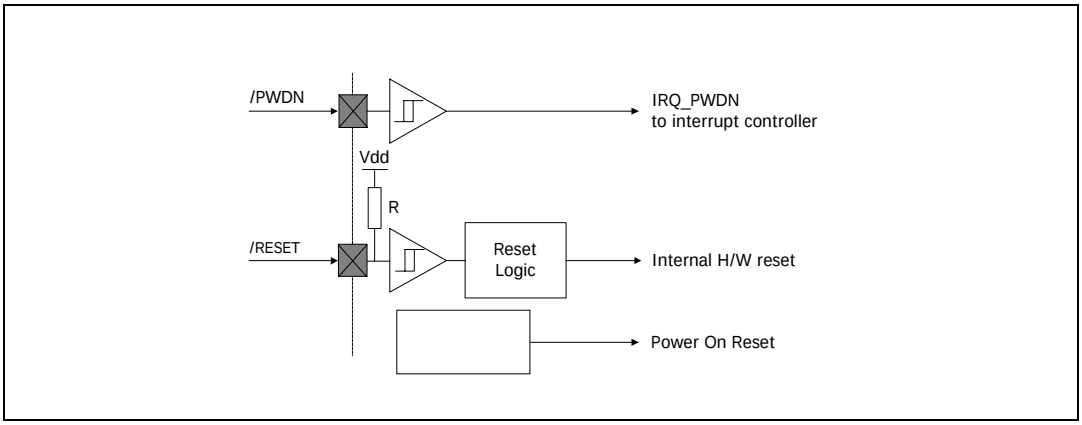
- The TAD provides an internal power on reset while power building up for the very first time (this is a different situation than resetting the W62410 after putting the W62410 in Power down mode). The power on reset signal will force the Real Time Clock to be set to zero.
- To ensure that the system crystal oscillate properly, the reset signal must be kept low for at least 200 mS. This reset signal will not affect the memory nor the Real Time Clock Value.

Power Down Mode

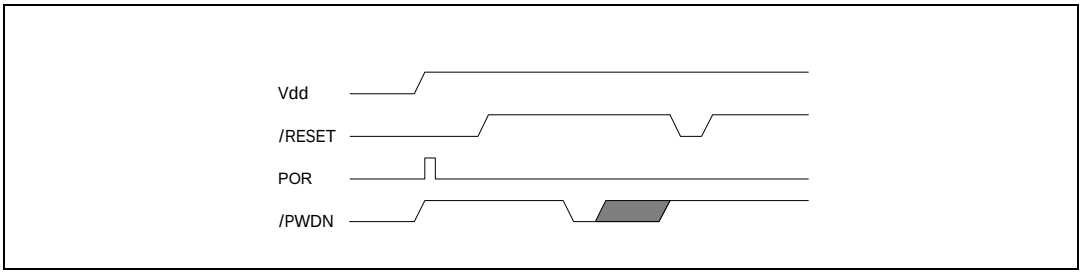
- Operation Current Idd < 80 mA at 5V
- IDLE mode Idd < 40 mA at 5V
- Power Down Mode < 100 μA at 5V
- A low signal on the $\overline{\text{PWDN}}$ pin will invoke the highest priority interrupt vector to wake up the W62410.
- During power down, the system clock oscillating at 24.576 MHz, is stopped, except the Real Time Clock and DRAM refresh. The 32768 Hz oscillator will take over to support the Real Time Clock and the DRAM refresh control signals.
- The input/output pins will be kept in tri-state mode to isolate the DC path in power down mode.
- After $\overline{\text{PWDN}}$ release, a hardware reset signal must be activated again to let the W62410 wakeup and restart.

- In case of the use of Flash as external storage memory, power can be removed totally. The 32768 oscillator may be unnecessary, if μController can maintain the Real Time Clock itself or is deemed unnecessary for the application.

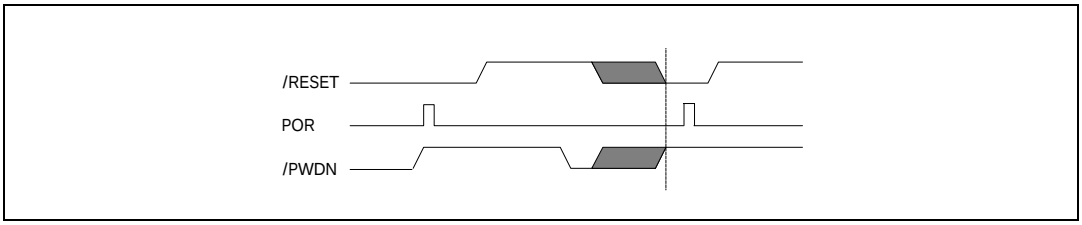
Power-up Reset, Power-down, External H/W Reset



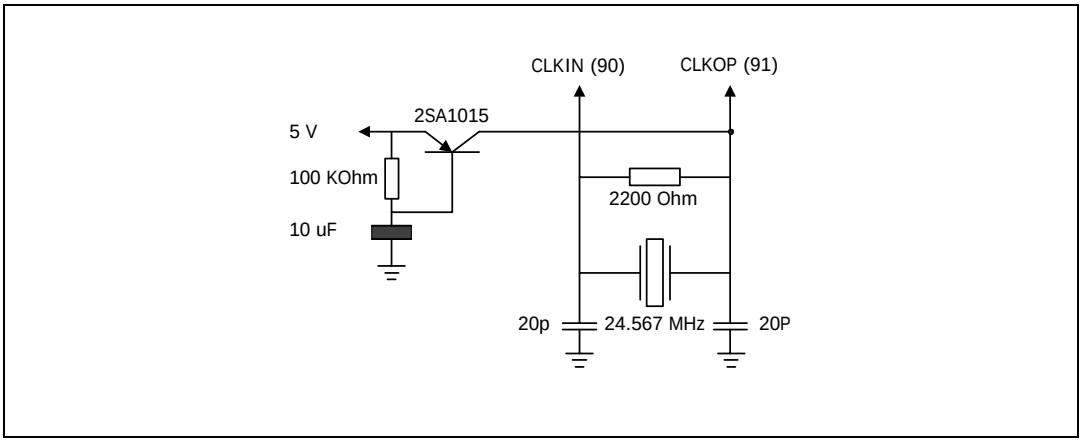
Power Down for DRAM Configuration



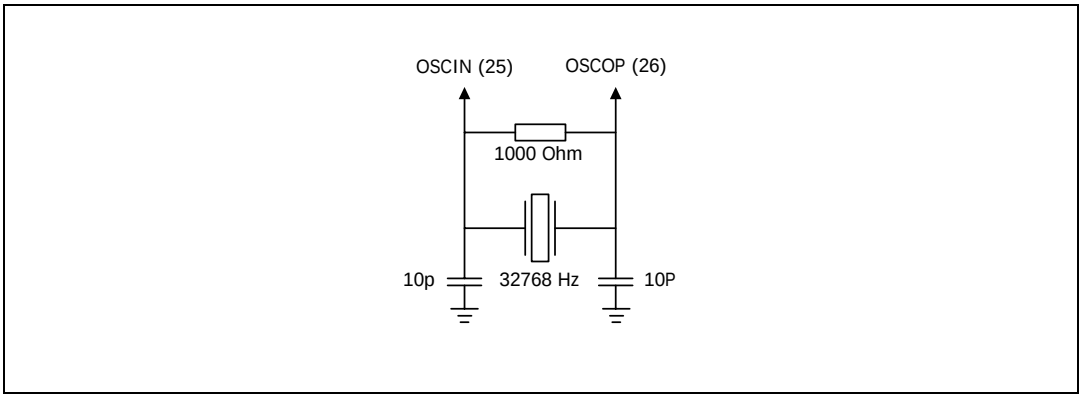
Power Down for Flash Configuration



Master Crystal Oscillator Circuit (24.576 MHz)



Real Time Clock Oscillator Circuit (32768 Hz)



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
DC Power Supply	V_{DD}–V_{SS}	-0.3	+7.0	V
Input Voltage	V_{IN}	V_{SS} -0.3	V_{DD} +0.3	V
Operating Temperature	T_A	0	70	°C
Storage Temperature	T_{ST}	-55	150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

ELECTRICAL CHARACTERISTICS

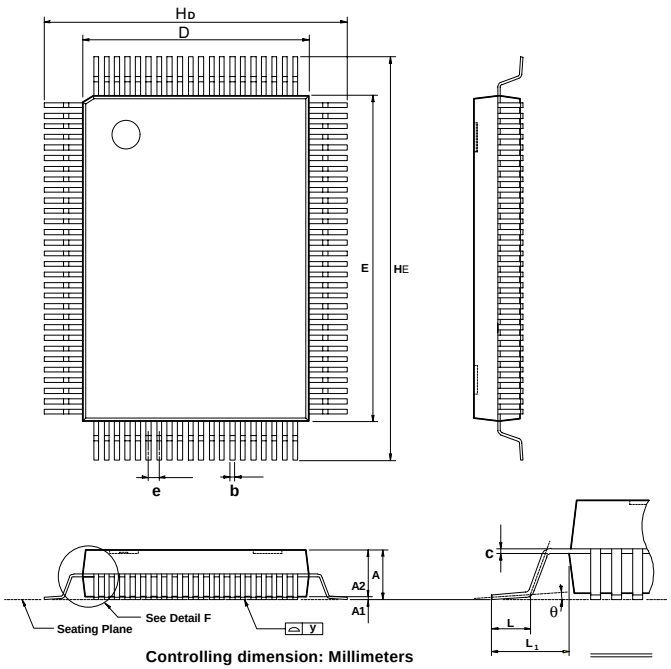
DC Characteristics

(V_{DD}–Vss = 5V ±10%, T_A = 25°, CLKIN = 24.576 MHz, OSCIN = 32768 Hz)

PARAMETER	SYM.	CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Operating Voltage	V_{DD}	-	4.5	5.0	5.5	V
Operating Current	I_{DD}	-		90		mA
Power Down Current	I_{PWD}	Power Down Mode	-		900	ì A
Input Leakage Current	I_{LK1}	All except Pull high or low, tri-state, IRQEx	-10		+10	ì A
	I_{LK2}	internal pull high pin They are $\overline{RESET}$, $\overline{PLLbypass}$, TestA, TestB,	-300		+10	
	I_{LK3}	IRQEx	-200		+100	
Output Voltage Low	V_{OL}	Iol = 8 mA	-		0.45	V
Output Voltage High	V_{OH}	Ioh = -8 mA	2.4		-	
Input Voltage Low	V_{IL}	All except $\overline{RESET}$, $\overline{PWDN}$, OSC, CLK pin	-		0.8	V
Input Voltage High	V_{IH}	All except $\overline{RESET}$, $\overline{PWDN}$, OSC, CLK pin	2.0		-	
Input Voltage Low	V_{ILS}	$\overline{RESET}$, $\overline{PWDN}$ pin, Schmitt trigger input	-		0.8	V
Input Voltage High	V_{IHS}	$\overline{RESET}$, $\overline{PWDN}$ pin, Schmitt trigger input	2.4		-	
Input Voltage Low	V_{ILX}	OSCIN, CLKIN pin, XTAL oscillator input	-		1.5	V
Input Voltage High	V_{IHX}	OSCIN, CLKIN pin, XTAL oscillator input	3.5		-	

PACKAGE DIMENSIONS

100L QFP(14 x 20 x 2.75 mm footprint 4.8 mm)



Controlling dimension: Millimeters

Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	—	—	—	—
A_1	0.010	0.014	0.018	0.25	0.35	0.45
A_2	0.101	0.107	0.113	2.57	2.72	2.87
b	0.008	0.012	0.016	0.20	0.30	0.40
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.547	0.551	0.555	13.90	14.00	14.10
E	0.783	0.787	0.791	19.90	20.00	20.10
e	0.020	0.026	0.032	0.498	0.65	0.802
H_D	0.746	0.740	0.756	18.40	18.80	19.20
H_E	0.960	0.976	0.992	24.40	24.80	25.20
L	0.039	0.047	0.055	1.00	1.20	1.40
L_1	—	0.064	—	—	2.40	—
y	—	—	0.003	—	—	0.08
θ	0°	—	7°	0°	—	7°

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