Frequency Controller with System Recovery for Intel® Integrated Core Logic

Features

- **Single chip FTG solution for Intel® Solano/810E/810**
- **Programmable clock output frequency with less than 1MHz increment**
- **Integrated fail-safe Watchdog timer for system recovery**
- **Automatically switch to HW selected or SW programmed clock frequency when watchdog timer time-out**
- **Capable of generating system RESET after a watchdog timer time-out occurs or a change in output frequency via SMBus interface**
- **Support SMBus byte read/write and block read/ write operations to simplify system BIOS development**
- **Vendor ID and Revision ID support**
- **Programmable drive strength for SDRAM and PCI output clocks**
- **Programmable output skew between CPU, AGP, PCI and SDRAM**
- **Maximized EMI suppression using Cypress's Spread Spectrum Technology**
- **Low jitter and tightly controlled clock skew**
- **Two copies of CPU clock**
- **Thirteen copies of SDRAM clock**
- **Eight copies of PCI clock**
- **One copy of synchronous APIC clock**
- **Three copies of 66 MHz outputs**
- **Two copies of 48 MHz outputs**
- **One RESET output for system recovery**
- **One copy of double strength 14.31818-MHz reference clock**
- **SMBus interface for turning off unused clocks**

Key Specifications

CPU, SDRAM Outputs Cycle-to-Cycle Jitter: ....250 ps

APIC, 48-MHz, 3V66, PCI Outputs Cycle-to-Cycle Jitter: ....500 ps

CPU, 3V66 Output Skew:..175 ps

SDRAM, APIC, 48-MHz Output Skew:........................250 ps

PCI Output Skew:...500 ps

CPU to SDRAM Skew (@ 133 MHz) ....± 0.5 ns

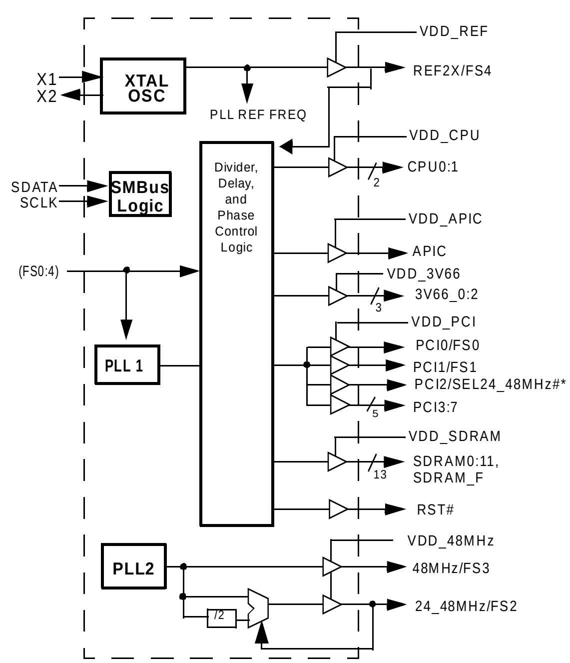
CPU to SDRAM Skew (@ 100 MHz)..................4.5 to 5.5 ns

CPU to 3V66 Skew (@ 66 MHz) ....7.0 to 8.0 ns

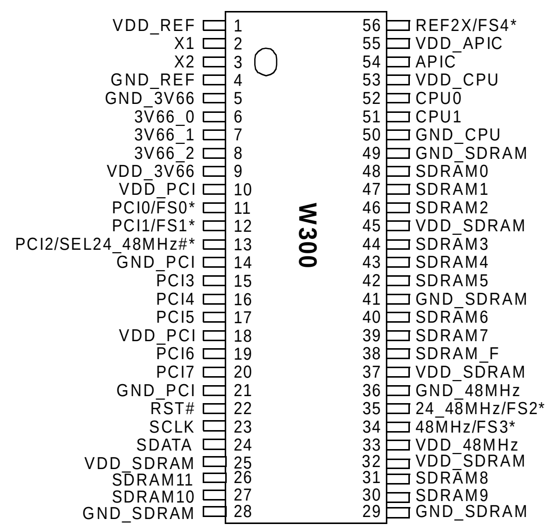
3V66 to PCI Skew (3V66 lead)..........................1.5 to 3.5 ns

PCI to APIC Skew ....± 0.5 ns

Block Diagram



Pin Configuration[1]



Note:

1. Internal 100K pull-up resistors present on inputs marked with *. Design should not rely solely on internal pull-up resistor to set I/O pins HIGH or LOW.

Pin Definitions

Pin Name	Pin No.	Pin Type	Pin Description
REF2X/FS4	56	I/O	***Reference Clock with 2x Drive/Frequency Select 4:*** 3.3V 14.318-MHz clock output. This pin also serves as the select strap to determine device operating frequency as described in *Table 5*.
X1	2	I	***Crystal Input:*** This pin has dual functions. It can be used as an external 14.318-MHz crystal connection or as an external reference frequency input.
X2	3	O	***Crystal Output:*** An input connection for an external 14.318-MHz crystal connection. If using an external reference, this pin must be left unconnected.
PCI0/FS0	11	I/O	***PCI Clock 0/Frequency Selection 0:*** 3.3V 33-MHz PCI clock outputs. This pin also serves as the select strap to determine device operating frequency as described in *Table 5*.
PCI1/FS1	12	I/O	***PCI Clock 1/Frequency Selection 1:*** 3.3V 33-MHz PCI clock outputs. This pin also serves as the select strap to determine device operating frequency as described in *Table 5*.
PCI2/SEL24_48MHz#	13	I/O	***PCI Clock 2/Select 24 or 48 MHz:*** 3.3V 33-MHz PCI clock outputs. This pin also serves as the select strap to determine the output frequency for 24_48MHz output.
PCI3:7	15, 16, 17, 19, 20	O	***PCI Clock 3 through 7:*** 3.3V 33-MHz PCI clock outputs. PCI0:7 can be individually turned off via SMBus interface.
3V66_0:2	6, 7, 8	O	***66-MHz Clock Output:*** 3.3V output clocks. The operating frequency is controlled by FS0:4 (see *Table 5*).
48MHz/FS3	34	I/O	***48-MHz Output/Frequency Selection 3:*** 3.3V 48-MHz non-spread spectrum output. This pin also serves as the select strap to determine device operating frequency as described in *Table 5*.
24_48MHz/FS2	35	I/O	***24 or 48MHz Output/Frequency Selection 2:*** 3.3V 24-or 48-MHz non-spread spectrum output. This pin also serves as the select strap to determine device operating frequency as described in *Table 5*.
RST#	22	O (open-drain)	***RESET Output:*** Open-drain system reset output.
CPU0:1	52, 51	O	***CPU Clock Outputs:*** Clock outputs for the host bus interface. Output frequencies depending on the configuration of FS0:4. Voltage swing is set by VDDQ2.
SDRAM0:11, SDRAM_F	48, 47, 46, 44, 43, 42, 40, 39, 31, 30, 27, 26, 38	O	***SDRAM Clock Outputs:*** 3.3V outputs for SDRAM and chipset. The operating frequency is controlled by FS0:4 (see *Table 5*).
APIC	54	O	***Synchronous APIC Clock Outputs:*** Clock outputs running synchronous with the PCI clock outputs. Voltage swing set by VDDQ2.
SDATA	24	I/O	Data pin for SMBus circuitry.
SCLK	23	I	Clock pin for SMBus circuitry.
VDD_REF, VDD_3V66, VDD_PCI, VDD_SDRAM, VDD_48MHz	1, 9, 10, 18, 25, 32, 37, 45, 33	P	***3.3V Power Connection:*** Power supply for SDRAM output buffers, PCI output buffers, reference output buffers and 48-MHz output buffers. Connect to 3.3V.
VDD_CPU, VDD_APIC	53, 55	P	***2.5V Power Connection:*** Power supply for APIC and CPU output buffers. Connect to 2.5V.

Pin Definitions (continued)

Pin Name	Pin No.	Pin Type	Pin Description
GND_REF, GND_3V66, GND_PCI, GND_SDRAM, GND_48MHZ, GND_CPU	4, 5, 14, 21, 28, 29, 41, 49, 50, 36	G	***Ground Connections:*** Connect all ground pins to the common system ground plane.

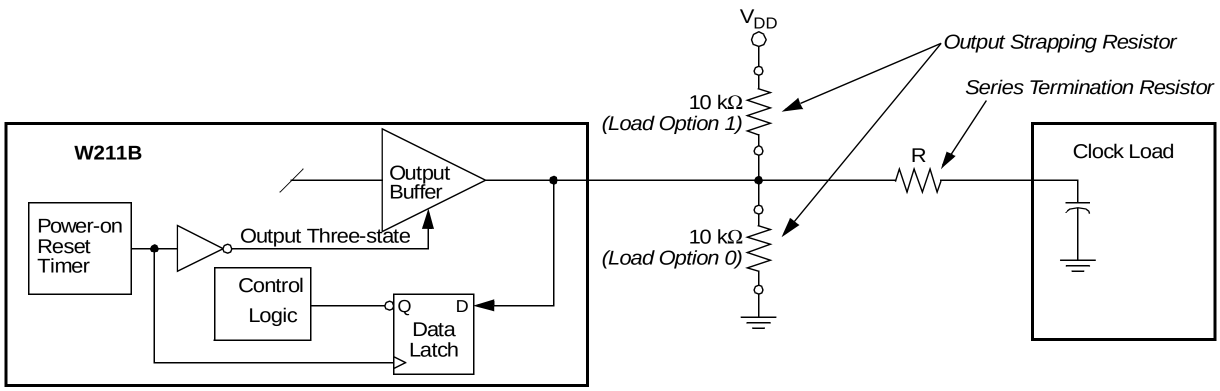


Figure 1. Input Logic Selection Through Resistor Load Option

Overview

The W300 is a highly integrated frequency timing generator, supplying all the required clock sources for an Intel® architecture platform using graphics integrated core logic.

Functional Description

I/O Pin Operation

Upon power-up the power on strap option pins act as a logic input. An external 10-kΩ strapping resistor should be used. *Figure 1* shows a suggested method for strapping resistor connections.

After 2 ms, the pin becomes an output. Assuming the power supply has stabilized by then, the specified output frequency is delivered on the pins. If the power supply has not yet reached full value, output frequency initially may be below target but will increase to target once supply voltage has stabilized. In either case, a short output clock cycle may be produced from the CPU clock outputs when the outputs are enabled.

Offsets Among Clock Signal Groups

Figure 2, *Figure 3*, and *Figure 4* represent the phase relationship among the different groups of clock outputs from W300 under different frequency modes.

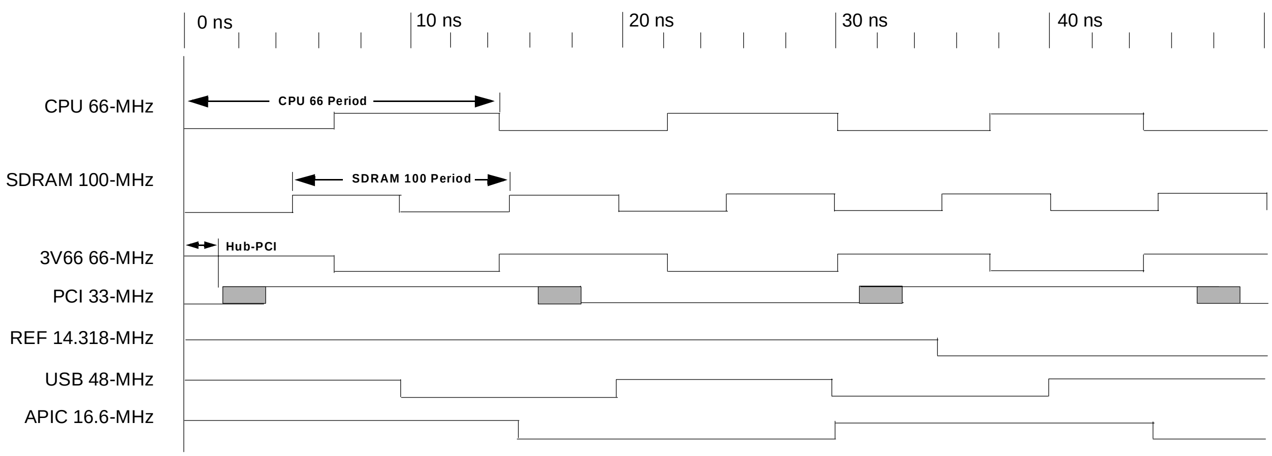


Figure 2. Group Offset Waveforms (66-MHz CPU Clock, 100-MHz SDRAM Clock)

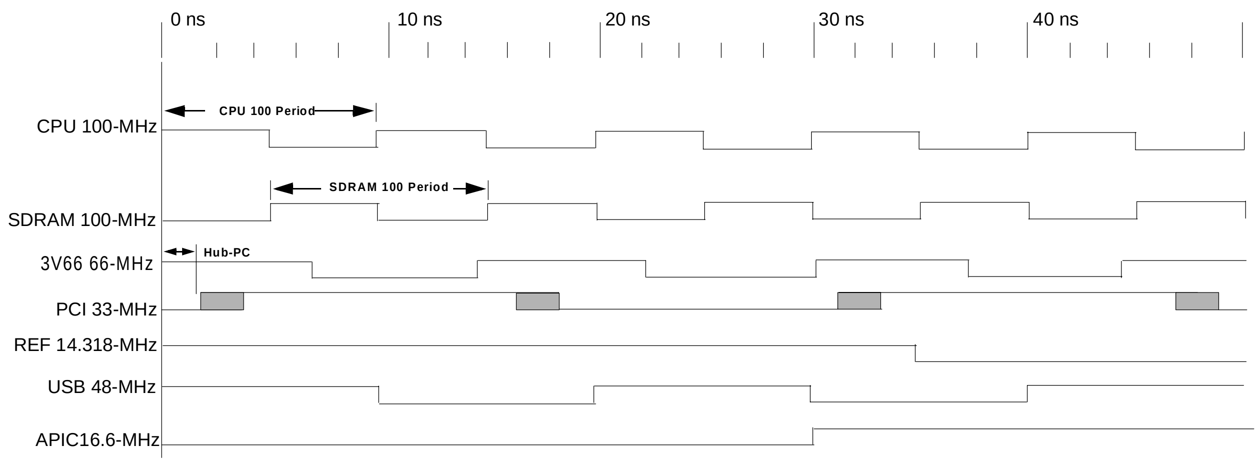


Figure 3. Group Offset Waveforms (100-MHz CPU Clock, 100-MHz SDRAM Clock)

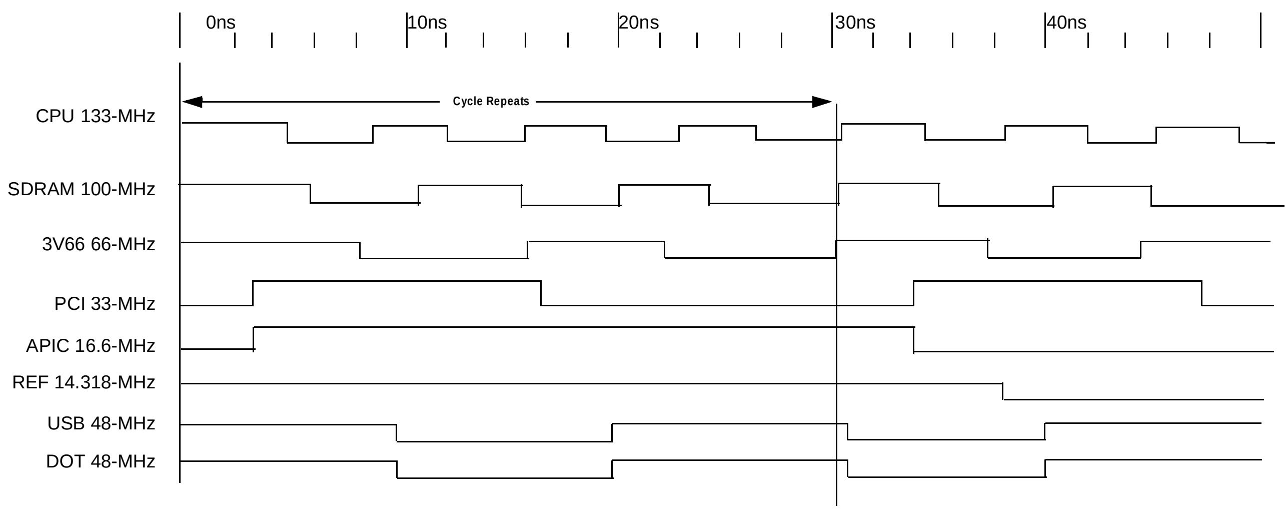


Figure 4. Group Offset Waveforms (133-MHz CPU/100 MHz-SDRAM)

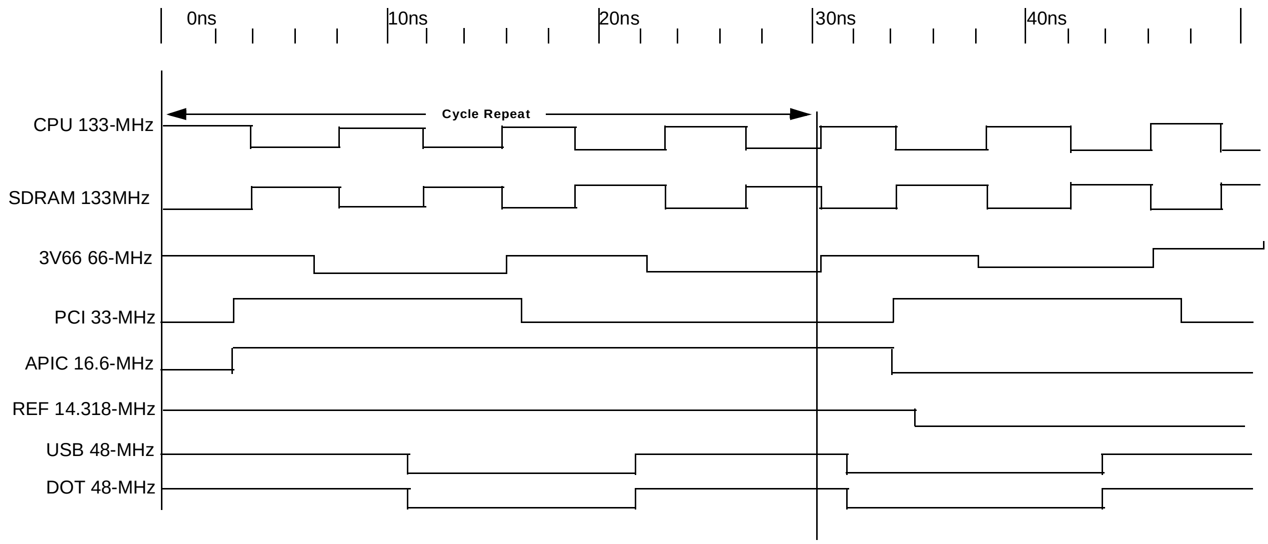


Figure 5. Group Offset Waveform (133-MHz CPU/133-MHz SDRAM)

Serial Data Interface

The W300 features a two-pin, serial data interface that can be used to configure internal register settings that control particular device functions.

Data Protocol

The clock driver serial protocol supports byte/word write, byte/word read, block write and block read operations from the controller. For block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. For byte/word write and byte read operations, system controller can access individual indexed byte. The offset of the indexed byte is encoded in the command code.

The definition for the command code is defined in *Table 1.*

Table 1. Command Code Definition

Bit	Descriptions
7	0 = Block read or block write operation 1 = Byte/Word read or byte/word write operation
6:0	Byte offset for byte/word read or write operation. For block read or write operations, these bits need to be set at ‘0000000’.

Table 2. Block Read and Block Write Protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address - 7 bit	2:8	Slave address - 7 bit
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code - 8 bit ‘00000000’ stands for block operation	11:18	Command Code - 8 bit ‘00000000’ stands for block operation
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Byte Count - 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address - 7 bits
29:36	Data byte 0 - 8 bits	28	Read
37	Acknowledge from slave	29	Acknowledge from slave
38:45	Data byte 1 - 8 bits	30:37	Byte count from slave - 8 bits
46	Acknowledge from slave	38	Acknowledge
...	Data Byte N/Slave Acknowledge...	39:46	Data byte from slave - 8 bits
...	Data Byte N - 8 bits	47	Acknowledge
...	Acknowledge from slave	48:55	Data byte from slave - 8 bits
...	Stop	56	Acknowledge
		...	Data bytes from slave/Acknowledge
		...	Data byte N from slave - 8 bits
		...	Not Acknowledge
		...	Stop

Table 3. Word read and Word write protocol

Word Write Protocol		Word Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address - 7 bit	2:8	Slave address - 7 bit
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code - 8 bit '1xxxxxxx' stands for byte or word operation bit[6:0] of the command code represents the offset of the byte to be accessed	11:18	Command Code - 8 bit '1xxxxxxx' stands for byte or word operation bit[6:0] of the command code represents the offset of the byte to be accessed
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Data byte low- 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address - 7 bits
29:36	Data byte high - 8 bits	28	Read
37	Acknowledge from slave	29	Acknowledge from slave
38	Stop	30:37	Data byte low from slave - 8 bits
		38	Acknowledge
		39:46	Data byte high from slave - 8 bits
		47	NOT acknowledge
		48	Stop

Table 4. Byte read and byte write protocol

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address - 7 bit	2:8	Slave address - 7 bit
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code - 8 bit '1xxxxxxx' stands for byte operation bit[6:0] of the command code represents the offset of the byte to be accessed	11:18	Command Code - 8 bit '1xxxxxxx' stands for byte operation bit[6:0] of the command code represents the offset of the byte to be accessed
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Data byte - 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address - 7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		30:37	Data byte from slave - 8 bits
		38	Not Acknowledge
		39	Stop

W300 Serial Configuration Map

1. The serial bits will be read by the clock driver in the following order:

   Byte 0 - Bits 7, 6, 5, 4, 3, 2, 1, 0

   Byte 1 - Bits 7, 6, 5, 4, 3, 2, 1, 0

   Byte N - Bits 7, 6, 5, 4, 3, 2, 1, 0
2. All unused register bits (reserved and N/A) should be written to a “0” level.
3. All register bits labeled “Initialize to 0" must be written to zero during initialization.

Byte 0: Control Register 0

Bit	Pin#	Name	Default	Description
Bit 7	-	SEL4	0	See *Table 4*
Bit 6	-	SEL3	0	See *Table 4*
Bit 5	-	SEL2	0	See *Table 4*
Bit 4	-	SEL1	0	See *Table 4*
Bit 3	-	SEL0	0	See *Table 4*
Bit 2	-	Spread Select2	0	‘000’ = Normal (spread off) ‘001’ = Test Mode ‘010’ = Reserved ‘011’ = Three-Stated ‘100’ = –0.5% ‘101’ = ±0.5% ‘110’ = ±0.25% ‘111’ = ±0.38%
Bit 1	-	Spread Select1	0	
Bit 0	-	Spread Select0	0	

Byte 1: Control Register 1

Bit	Pin#	Name	Default	Description
Bit 7	56	Latched FS4 input	X	Latched FS[4:0] inputs. These bits are read only.
Bit 6	34	Latched FS3 input	X	
Bit 5	35	Latched FS2 input	X	
Bit 4	12	Latched FS1 input	X	
Bit 3	11	Latched FS0 input	X	
Bit 2	-	Reserved	0	Reserved
Bit 1	56	REF2X	1	(Active/Inactive)
Bit 0	-	Reserved	0	Reserved

Byte 2: Control Register 2

Bit	Pin#	Name	Default	Description
Bit 7	20	PCI7	1	(Active/Inactive)
Bit 6	19	PCI6	1	(Active/Inactive)
Bit 5	17	PCI5	1	(Active/Inactive)
Bit 4	16	PCI4	1	(Active/Inactive)
Bit 3	15	PCI3	1	(Active/Inactive)
Bit 2	13	PCI2	1	(Active/Inactive)
Bit 1	12	PCI1	1	(Active/Inactive)
Bit 0	11	PCI0	1	(Active/Inactive)

Byte 3: Control Register 3

Bit	Pin#	Name	Default	Description
Bit 7	8	3V66_2	1	(Active/Inactive)
Bit 6	7	3V66_1	1	(Active/Inactive)
Bit 5	6	3V66_0	1	(Active/Inactive)
Bit 4	54	APIC	1	(Active/Inactive)
Bit 3	-	Reserved	0	Reserved
Bit 2	-	Reserved	0	Reserved
Bit 1	51	CPU1	1	(Active/Inactive)
Bit 0	52	CPU0	1	(Active/Inactive)

Byte 4: Control Register 4

Bit	Pin#	Name	Default	Description
Bit 7	39	SDRAM7	1	(Active/Inactive)
Bit 6	40	SDRAM6	1	(Active/Inactive)
Bit 5	42	SDRAM5	1	(Active/Inactive)
Bit 4	43	SDRAM4	1	(Active/Inactive)
Bit 3	44	SDRAM3	1	(Active/Inactive)
Bit 2	46	SDRAM2	1	(Active/Inactive)
Bit 1	47	SDRAM1	1	(Active/Inactive)
Bit 0	48	SDRAM0	1	(Active/Inactive)

Byte 5: Control Register 5

Bit	Pin#	Name	Default	Description
Bit 7	-	Reserved	0	Reserved
Bit 6	-	Reserved	0	Reserved
Bit 5	-	Reserved	0	Reserved
Bit 4	38	SDRAM_F	1	(Active/Inactive)
Bit 3	26	SDRAM11	1	(Active/Inactive)
Bit 2	27	SDRAM10	1	(Active/Inactive)
Bit 1	30	SDRAM9	1	(Active/Inactive)
Bit 0	31	SDRAM8	1	(Active/Inactive)

Byte 6: Vendor ID & Revision ID Register (Read Only)

Bit	Name	Default	Pin Description
Bit 7	Revision_ID3	0	Revision ID bit[3]
Bit 6	Revision_ID2	0	Revision ID bit[2]
Bit 5	Revision_ID1	0	Revision ID bit[1]
Bit 4	Revision_ID0	0	Revision ID bit[0]
Bit 3	Vendor_ID3	1	Bit[3] of Cypress Semiconductor's Vendor ID. This bit is read only.
Bit 2	Vendor_ID2	0	Bit[2] of Cypress Semiconductor's Vendor ID. This bit is read only.
Bit 1	Vendor _ID1	0	Bit[1] of Cypress Semiconductor's Vendor ID. This bit is read only.

Byte 6: Vendor ID & Revision ID Register (Read Only)

Bit	Name	Default	Pin Description
Bit 0	Vendor _ID0	0	Bit[0] of Cypress Semiconductor's Vendor ID. This bit is read only.

Byte 7: Control Register 7

Bit	Pin#	Name	Default	Pin Description
Bit 7	-	Reserved	0	Reserved
Bit 6	35	24_48Mhz_DRV	1	0 = Norm, 1 = High Drive
Bit 5	34	48MHz_DVR	1	0 = Norm, 1 = High Drive
Bit 4	--	Reserved	0	Reserved
Bit 3	35	24_48MHz	1	(Active/Inactive)
Bit 2	34	48 MHz	1	(Active/Inactive)
Bit 1	--	Reserved	0	Reserved
Bit 0	--	Reserved	0	Reserved

Byte 8: Watchdog TIMER Register

Bit	Name	Default	Pin Description
Bit 7	PCI_Skew1	0	PCI skew control 00 = Normal 01 = –500ps 10 = Reserved 11 = +500ps
Bit 6	PCI_Skew0	0	
Bit 5	WD_TIMER4	1	These bits store the time-out value of the Watchdog timer. The scale of the timer is determine by the pre-scaler. The timer can support a value of 150 ms to 4.8 seconds when the pre-scaler is set to 150 ms. If the pre-scaler is set to 2.5 sec, it can support a value from 2.5 sec to 80 sec. When the Watchdog timer reaches "0", it will set the WD_TO_STATUS bit and generate Reset if RST_EN_WD is enabled.
Bit 4	WD_TIMER3	1	
Bit 3	WD_TIMER2	1	
Bit 2	WD_TIMER1	1	
Bit 1	WD_TIMER0	1	
Bit 0	WD_PRE_SCALER	0	0 = 150 ms 1 = 2.5 sec

Byte 9: System RESET and Watchdog Timer Register

Bit	Name	Default	Pin Description
Bit 7	SDRAM_DRV	0	SDRAM clock output drive strength 0 = Normal 1 = High Drive
Bit 6	PCI_DRV	0	PCI clock output drive strength 0 = Normal 1 = High Drive
Bit 5	FS_Override	0	0 = Select operating frequency by FS[4:0] input pins 1 = Select operating frequency by SEL[4:0] settings
Bit 4	RST_EN_WD	0	This bit will enable the generation of a Reset pulse when a watchdog timer time-out occurs. 0 = Disabled 1 = Enabled
Bit 3	RST_EN_FC	0	This bit will enable the generation of a Reset pulse after a frequency change occurs. 0 = Disabled 1 = Enabled

Byte 9: System RESET and Watchdog Timer Register (continued)

Bit	Name	Default	Pin Description
Bit 2	WD_TO_STATUS	0	Watchdog Timer Time-out Status bit 0 = No time-out occurs (READ); Ignore (WRITE) 1 = time-out occurred (READ); Clear WD_TO_STATUS (WRITE)
Bit 1	WD_EN	0	0 = Stop and re-load Watchdog timer. Unlock W300 from recovery frequency mode. 1 = Enable Watchdog timer. It will start counting down after a frequency change occurs. **Note:** W300 will generate system reset, re-load a recovery frequency, and lock itself into a recovery frequency mode after a Watchdog timer time-out occurs. Under recovery frequency mode, W300 will not respond to any attempt to change output frequency via the SMBus control bytes. System software can unlock W300 from its recovery frequency mode by clearing the WD_EN bit.
Bit 0	Reserved	0	Reserved

Byte 10: Skew Control Register

Bit	Name	Default	Description
Bit 7	CPU_Skew2	0	CPU skew control 000 = Normal 001 = –150 ps 010 = –300 ps 011 = –450 ps 100 = +150 ps 101 = +300 ps 110 = +450 ps 111 = +600 ps
Bit 6	CPU_Skew1	0	
Bit 5	CPU_Skew0	0	
Bit 4	SDRAM_Skew2	0	SDRAM skew control 000 = Normal 001 = –150 ps 010 = –300 ps 011 = –450 ps 100 = +150 ps 101 = +300 ps 110 = +450 ps 111 = +600 ps
Bit 3	SDRAM_Skew1	0	
Bit 2	SDRAM_Skew0	0	
Bit 1	AGP_Skew1	0	AGP skew control 00 = Normal 01 = –150 ps 10 = +150 ps 11 = +300 ps
Bit 0	AGP_Skew0	0	

Byte 11: Recovery Frequency N-Value Register

Bit	Name	Default	Pin Description
Bit 7	ROCV_FREQ_N7	0	If ROCV_FREQ_SEL is set, W300 will use the values programmed in ROCV_FREQ_N[7:0] and ROCV_FREQ_M[6:0] to determine the recovery cpu output frequency when a Watchdog timer time-out occurs. The setting of FS_Override bit determines the frequency ratio for CPU, SDRAM, AGP and SDRAM. When it is cleared, W300 will use the same frequency ratio stated in the Latched FS[4:0] register. When it is set, W300 will use the frequency ratio stated in the SEL[4:0] register. W300 supports programmable CPU frequency ranging from 50 MHz to 248 MHz. W300 will change the output frequency whenever there is an update to either ROCV_FREQ_N[7:0] and ROCV_FREQ_M[6:0]. Therefore, it is recommended to use Word or Block write to update both registers within the same SMBus bus operation.
Bit 6	ROCV_FREQ_N6	0	
Bit 5	ROCV_FREQ_N5	0	
Bit 4	ROCV_FREQ_N4	0	
Bit 3	ROCV_FREQ_N3	0	
Bit 2	ROCV_FREQ_N2	0	
Bit 1	ROCV_FREQ_N1	0	
Bit 0	ROCV_FREQ_N0	0	

Byte 12: Recovery Frequency M-Value Register

Bit	Name	Default	Pin Description
Bit 7	ROCV_FREQ_SEL	0	ROCV_FREQ_SEL determines the source of the recover frequency when a Watchdog timer time-out occurs. The clock generator will automatically switch to the recovery CPU frequency based on the selection on ROCV_FREQ_SEL. 0 = From latched FS[4:0] 1 = From the settings of ROCV_FREQ_N[7:0] & ROCV_FREQ_M[6:0]
Bit 6	ROCV_FREQ_M6	0	If ROCV_FREQ_SEL is set, W300 will use the values programmed in ROCV_FREQ_N[7:0] and ROCV_FREQ_M[6:0] to determine the recovery CPU output frequency when a Watchdog timer time-out occurs The setting of FS_Override bit determines the frequency ratio for CPU, SDRAM, AGP and SDRAM. When it is cleared, W300 will use the same frequency ratio stated in the Latched FS[4:0] register. When it is set, W300 will use the frequency ratio stated in the SEL[4:0] register. W300 supports programmable CPU frequency ranging from 50 MHz to 248 MHz. W300 will change the output frequency whenever there is an update to either ROCV_FREQ_N[7:0] and ROCV_FREQ_M[6:0]. Therefore, it is recommended to use Word or Block write to update both registers within the same SMBus bus operation.
Bit 5	ROCV_FREQ_M5	0	
Bit 4	ROCV_FREQ_M4	0	
Bit 3	ROCV_FREQ_M3	0	
Bit 2	ROCV_FREQ_M2	0	
Bit 1	ROCV_FREQ_M1	0	
Bit 0	ROCV_FREQ_M0	0	

Byte 13: Programmable Frequency Select N-Value Register

Bit	Name	Default	Pin Description
Bit 7	CPU_FSEL_N7	0	If Prog_Freq_EN is set, W300 will use the values programmed in CPU_FSEL_N[7:0] and CPU_FSEL_M[6:0] to determine the CPU output frequency. The new frequency will start to load whenever CPU_FSELM[6:0] is updated. The setting of FS_Override bit determines the frequency ratio for CPU, SDRAM, AGP and SDRAM. When it is cleared, W300 will use the same frequency ratio stated in the Latched FS[4:0] register. When it is set, W300 will use the frequency ratio stated in the SEL[4:0] register. W300 supports programmable CPU frequency ranging from 50 MHz to 248 MHz.
Bit 6	CPU_FSEL_N6	0	
Bit 5	CPU_FSEL_N5	0	
Bit 4	CPU_FSEL_N4	0	
Bit 3	CPU_FSEL_N3	0	
Bit 2	CPU_FSEL_N2	0	
Bit 1	CPU_FSEL_N1	0	
Bit 0	CPU_FSEL_N0	0	

Byte 14: Programmable Frequency Select M-Value Register

Bit	Name	Default	Description
Bit 7	Pro_Freq_EN	0	Programmable output frequencies enabled 0 = disabled 1 = enabled
Bit 6	CPU_FSEL_M6	0	If Prog_Freq_EN is set, W300 will use the values programmed in CPU_FSEL_N[7:0] and CPU_FSEL_M[6:0] to determine the CPU output frequency. The new frequency will start to load whenever CPU_FSELM[6:0] is updated. The setting of FS_Override bit determines the frequency ratio for CPU, SDRAM, AGP and SDRAM. When it is cleared, W300 will use the same frequency ratio stated in the Latched FS[4:0] register. When it is set, W300 will use the frequency ratio stated in the SEL[4:0] register. W300 supports programmable CPU frequency ranging from 50 MHz to 248 MHz.
Bit 5	CPU_FSEL_M5	0	
Bit 4	CPU_FSEL_M4	0	
Bit 3	CPU_FSEL_M3	0	
Bit 2	CPU_FSEL_M2	0	
Bit 1	CPU_FSEL_M1	0	
Bit 0	CPU_FSEL_M0	0	

Byte 15: Reserved Register

Bit	Pin#	Name	Default	Description
Bit 7	-	Reserved	0	Reserved
Bit 6	-	Reserved	0	Reserved
Bit 5	-	Reserved	0	Reserved
Bit 4	-	Reserved	0	Reserved
Bit 3	-	Reserved	0	Reserved
Bit 2	-	Reserved	0	Reserved
Bit 1	-	Reserved	1	Reserved. Write with ‘1’
Bit 0	-	Reserved	1	Reserved. Write with ‘1’

Byte 16: Reserved Register

Bit	Pin#	Name	Default	Description
Bit 7	-	Reserved	0	Reserved
Bit 6	-	Reserved	0	Reserved
Bit 5	-	Reserved	0	Reserved
Bit 4	-	Reserved	0	Reserved
Bit 3	-	Reserved	0	Reserved
Bit 2	-	Reserved	0	Reserved
Bit 1	-	Reserved	0	Reserved

Byte 17: Reserved Register

Bit	Pin#	Name	Default	Description
Bit 7	-	Reserved	0	Reserved
Bit 6	-	Reserved	0	Reserved
Bit 5	-	Reserved	0	Reserved
Bit 4	-	Reserved	0	Reserved
Bit 3	-	Reserved	0	Reserved
Bit 2	-	Reserved	0	Reserved
Bit 1	-	Reserved	0	Reserved

Table 5. Pre-programmed Frequency Selection Table

Input Conditions					Output Frequency					PLL Gear Constants (G)
FS4	FS3	FS2	FS1	FS0						
SEL4	SEL3	SEL2	SEL1	SEL0	CPU	SDRAM	3V66	PCI	APIC	
0	0	0	0	0	66.6	100.0	66.6	33.3	16.6	32.00494
0	0	0	0	1	120.0	120.0	80.0	40.0	20.0	48.00741
0	0	0	1	0	66.8	100.2	66.8	33.4	16.7	32.00494
0	0	0	1	1	68.3	102.5	68.3	34.2	17.1	32.00494
0	0	1	0	0	70.0	105.0	70.0	35.0	17.5	32.00494
0	0	1	0	1	75.0	112.5	75.0	37.5	18.8	32.00494
0	0	1	1	0	80.0	120.0	80.0	40.0	20.0	32.00494
0	0	1	1	1	83.0	124.5	83.0	41.5	20.8	32.00494
0	1	0	0	0	100.0	100.0	66.6	33.3	16.6	48.00741
0	1	0	0	1	124.0	124.0	82.6	41.3	20.6	48.00741
0	1	0	1	0	100.2	100.2	66.8	33.4	16.7	48.00741
0	1	0	1	1	103.0	103.0	68.9	34.3	17.2	48.00741
0	1	1	0	0	105.0	105.0	70.0	35.0	17.5	48.00741
0	1	1	0	1	110.0	110.0	73.3	36.7	18.3	48.00741
0	1	1	1	0	115.0	115.0	76.6	38.3	19.1	48.00741
0	1	1	1	1	200.0	200.0	66.6	33.3	16.6	96.01482
1	0	0	0	0	133.3	133.3	66.6	33.3	16.6	64.00988
1	0	0	0	1	166.6	166.6	83.3	41.6	20.8	64.00988
1	0	0	1	0	133.6	133.6	66.8	33.4	16.7	64.00988
1	0	0	1	1	137.0	137.0	68.5	34.3	17.1	64.00988
1	0	1	0	0	140.0	140.0	70.0	35.0	17.5	64.00988
1	0	1	0	1	145.0	145.0	72.5	36.2	18.1	64.00988
1	0	1	1	0	150.0	150.0	75.0	37.5	18.7	64.00988
1	0	1	1	1	160.0	160.0	80.0	40.0	20.0	64.00988
1	1	0	0	0	133.3	100.0	66.6	33.3	16.6	64.00988
1	1	0	0	1	166.6	125.0	83.3	41.7	20.8	64.00988
1	1	0	1	0	133.6	100.2	66.8	33.4	16.7	64.00988
1	1	0	1	1	137.0	102.8	68.5	34.3	17.1	64.00988
1	1	1	0	0	143.0	107.3	71.5	35.8	17.9	64.00988
1	1	1	0	1	200.0	150.0	75.0	37.5	18.7	64.00988
1	1	1	1	0	150.0	112.5	75.0	37.5	18.7	64.00988
1	1	1	1	1	160.0	120.0	80.0	40.0	20.0	64.00988

Programmable Output Frequency, Watchdog Timer and Recovery Output Frequency Functional Description

The Programmable Output Frequency feature allows users to generate any CPU output frequency from the range of 50 MHz to 248 MHz. Cypress offers the most dynamic and the simplest programming interface for system developers to utilize this feature in their platforms.

The Watchdog Timer and Recovery Output Frequency features allow users to implement a recovery mechanism when the system hangs or getting unstable. System BIOS or other control software can enable the Watchdog timer before they attempt to make a frequency change. If the system hangs and a Watchdog timer time-out occurs, a system reset will be generated and a recovery frequency will be activated.

All the related registers are summarized in the following table

Table 6. Register Summary

Name	Description
Pro_Freq_EN	Programmable output frequencies enabled 0 = disabled (default) 1 = enabled When it is disabled, the operating output frequency will be determined by either the latched value of FS[4:0] inputs or the programmed value of SEL[4:0]. If FS_Override bit is clear, latched FS[4:0] inputs will be used. If FS_Override bit is set, programmed value of SEL[4:0] will be used. When it is enabled, the CPU output frequency will be determined by the programmed value of CPUFSEL_N, CPUFSEL_M and the PLL Gear Constant. The program value of FS_Override, SEL[4:0] or the latched value of FS[4:0] will determine the PLL Gear Constant and the frequency ratio between CPU and other frequency outputs.
FS_Override	When Pro_Freq_EN is cleared or disabled: 0 = Select operating frequency by FS input pins (default) 1 = Select operating frequency by SEL bits in SMBus control bytes When Pro_Freq_EN is set or enabled: 0 = Frequency output ratio between CPU and other frequency groups and the PLL Gear Constant are based on the latched value of FS input pins (default). 1 = Frequency output ratio between CPU and other frequency groups and the PLL Gear Constant are based on the programmed value of SEL bits in SMBus control bytes.
CPU_FSEL_N, CPU_FSEL_M	When Prog_Freq_EN is set or enabled, the values programmed in CPU_FSEL_N[7:0] and CPU_FSEL_M[6:0] determines the CPU output frequency. The new frequency will start to load whenever there is an update to either CPU_FSEL_N[7:0] or CPU_FSEL_M[6:0]. Therefore, it is recommended to use Word or Block write to update both registers within the same SMBus bus operation. The setting of FS_Override bit determines the frequency ratio for CPU, SDRAM, AGP and SDRAM. When FS_Override is cleared or disabled, the frequency ratio follows the latched value of the FS input pins. When FS_Override is set or enabled, the frequency ratio follows the programmed value of SEL bits in SMBus control bytes.
ROCV_FREQ_SEL	ROCV_FREQ_SEL determines the source of the recover frequency when a WATCHDOG timer time-out occurs. The clock generator will automatically switch to the recovery CPU frequency based on the selection on ROCV_FREQ_SEL. 0 = From latched FS[4:0] 1 = From the settings of ROCV_FREQ_N[7:0] & ROCV_FREQ_M[6:0]
ROCV_FREQ_N[7:0], ROCV_FREQ_M[6:0]	When ROCV_FREQ_SEL is set, the values programmed in ROCV_FREQ_N[7:0] and ROCV_FREQ_M[6:0] will be used to determine the recovery CPU output frequency when a WATCHDOG timer time-out occurs. The setting of FS_Override bit determines the frequency ratio for CPU, SDRAM, AGP and SDRAM. When it is cleared, the same frequency ratio stated in the Latched FS[4:0] register will be used. When it is set, the frequency ratio stated in the SEL[4:0] register will be used. The new frequency will start to load whenever there is an update to either ROCV_FREQ_N[7:0] and ROCV_FREQ_M[6:0]. Therefore, it is recommended to use Word or Block write to update both registers within the same SMBus bus operation.

Name	Description
WD_EN	0 = Stop and re-load Watchdog timer. Unlock W300 from recovery frequency mode. 1 = Enable Watchdog timer. It will start counting down after a frequency change occurs. **Note:** W300 will generate system reset, re-load a recovery frequency, and lock itself into a recovery frequency mode after a watchdog timer time-out occurs. Under recovery frequency mode, W300 will not respond to any attempt to change output frequency via the SMBus control bytes. System software can unlock W300 from its recovery frequency mode by clearing the WD_EN bit.
WD_TO_STATUS	WATCHDOG Timer Time-out Status bit 0 = No time-out occurs (READ); Ignore (WRITE) 1 = time-out occurred (READ); Clear WD_TO_STATUS (WRITE)
WD_TIMER[4:0]	These bits store the time-out value of the Watchdog timer. The scale of the timer is determined by the pre-scaler. The timer can support a value of 150 ms to 4.8 sec. when the pre-scaler is set to 150 ms. If the pre-scaler is set to 2.5 sec, it can support a value from 2.5 sec. to 80 sec. When the WATCHDOG timer reaches “0”, it will set the WD_TO_STATUS bit.
WD_PRE_SCALER	0 = 150 ms 1 = 2.5 sec
RST_EN_WD	This bit will enable the generation of a Reset pulse when a watchdog timer time-out occurs. 0 = Disabled 1 = Enabled
RST_EN_FC	This bit will enable the generation of a Reset pulse after a frequency change occurs. 0 = Disabled 1 = Enabled

How to program CPU output frequency?

When the programmable output frequency feature is enabled (Pro_Freq_EN bit is set), the CPU output frequency is determined by the following equation:

Fcpu = G * (N+3)/(M+3)

“N” and “M” are the values programmed in Programmable Frequency Select N-Value Register and M-Value Register, respectively.

“G” stands for the PLL Gear Constant, which is determined by the programmed value of FS[4:0] or SEL[4:0]. The value is listed in *Table 5*.

Table 7 lists the recommended frequency output ranges for each PLL Gear Constant and its associated Bus Frequency Ratio so that the maximum AGP and PCI output frequencies are less than or equal to 83.1 MHz and 41.5 MHz respectively.

Table 7. Recommended CPU Frequency Range for Different PLL Gear Ratio

Gear Constants	Bus Frequency Ratio (CPU/SDRAM/AGP/PCI)	Recommended Output Frequency Range (CPU/SDRAM/AGP/PCI)	
		Lower Limits (N=77, M=48)	**Upper Limits (N=106, M=39)**
G1 (32.00494)	66 / 100 / 66 / 33	50.2 / 75.8 / 50.2 / 25.1	83.1 / 124.7 / 83.1 / 41.5
G2 (48.00741)	100 / 100 / 66 / 33	75.3 / 75.3 / 50.2 / 25.1	124.6 / 124.6 / 83.1 / 41.5
G3 (64.00988)	133 / 133 / 66 / 33 or 133 / 100 / 66 / 33	100.4 / 100.4 / 50.2 / 25.1 or 100.4 / 75.3 / 50.2 / 25.1	166.1 / 166.1 / 83.1 / 41.5 or 166.1 / 124.5 / 83.1 / 41.5
G4 (96.01482)	200 / 200 / 66 / 33	150.6 / 150.6 / 50.2 / 25.1	249.2 / 249.2 / 83.1 / 41.5

DC Electrical Characteristics

DC parameters must be sustainable under steady state (DC) conditions.

Absolute Maximum DC Power Supply

Parameter	Description	Min.	Max.	Unit
V_{DDQ3}	3.3V Core Supply Voltage	–0.5	4.6	V
V_{DDQ2}	2.5V I/O Supply Voltage	–0.5	3.6	V
T_S	Storage Temperature	–65	150	°C

Absolute Maximum DC I/O

Parameter	Description	Min.	Max.	Unit
$V_{i/o3}$	3.3V Core Supply Voltage	–0.5	4.6	V
$V_{i/o3}$	2.5V I/O Supply Voltage	–0.5	3.6	V
ESD prot.	Input ESD Protection	2000		V

DC Operating Requirements

Parameter	Description	Condition	Min.	Max.	Unit
I_{DD}	3.3V Supply Current		400		mA
I_{DD}	2.5V Supply Current		50		mA
V_{DD3}	3.3V Core Supply Voltage	3.3V±5%	3.135	3.465	V
V_{DDQ3}	3.3V I/O Supply Voltage	3.3V±5%	3.135	3.465	V
V_{DDQ2}	2.5V I/O Supply Voltage	2.5V±5%	2.375	2.625	V
V_{DD3} = 3.3V±5%					
V_{ih3}	3.3V Input High Voltage	V_{DD3}	2.0	V_{DD} + 0.3	V
V_{il3}	3.3V Input Low Voltage		V_{SS} – 0.3	0.8	V
I_{il}	Input Leakage Current[2]	$0<V_{in}<V_{DD3}$	–5	+5	µA
V_{DDQ2} = 2.5V±5%					
V_{oh2}	2.5V Output High Voltage	I_{oh}=(–1 mA)	2.0		V
V_{ol2}	2.5V Output Low Voltage	I_{ol}=(1 mA)		0.4	V
V_{DDQ3} = 3.3V±5%					
V_{oh3}	3.3V Output High Voltage	I_{oh}=(–1 mA)	2.4		V
V_{ol3}	3.3V Output Low Voltage	I_{ol}=(1 mA)		0.4	V
V_{DDQ3} = 3.3V±5%					
V_{poh3}	PCI Bus Output High Voltage	I_{oh}=(–1 mA)	2.4		V
V_{pol3}	PCI Bus Output Low Voltage	I_{ol}=(1 mA)		0.55	V
C_{in}	Input Pin Capacitance			5	pF
C_{xtal}	Xtal Pin Capacitance		13.5	22.5	pF
C_{out}	Output Pin Capacitance			6	pF
L_{pin}	Pin Inductance		0	7	nH
T_a	Ambient Temperature	No Airflow	0	70	°C

Note:
2. Input Leakage Current does not include inputs with pull-up or pull-down resistors.

AC Electrical Characteristics

T_A = 0°C to +70°C, V_{DDQ3} = 3.3V±5%, V_{DDQ2}= 2.5V±5%
f_{XTL} = 14.31818 MHz

Parameter	Description	66.6-MHz Host		100-MHz Host		133-MHz Host		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
T_{Period}	Host/CPUCLK Period	15.0	15.5	10.0	10.5	7.5	8.0	ns	3
T_{HIGH}	Host/CPUCLK High Time	5.2	N/A	3.0	N/A	1.87	N/A	ns	4
T_{LOW}	Host/CPUCLK Low Time	5.0	N/A	2.8	N/A	1.67	N/A	ns	5
T_{RISE}	Host/CPUCLK Rise Time	0.4	1.6	0.4	1.6	0.4	1.6	ns	
T_{FALL}	Host/CPUCLK Fall Time	0.4	1.6	0.4	1.6	0.4	1.6	ns	
T_{Period}	SDRAM CLK Period	10.0	10.5	10.0	10.5	10.0	10.5	ns	3
T_{HIGH}	SDRAM CLK High Time	3.0	N/A	3.0	N/A	3.0	N/A	ns	4
T_{LOW}	SDRAM CLK Low Time	2.8	N/A	2.8	N/A	2.8	N/A	ns	5
T_{RISE}	SDRAM CLK Rise Time	0.4	1.6	0.4	1.6	0.4	1.6	ns	
T_{FALL}	SDRAM CLK Fall Time	0.4	1.6	0.4	1.6	0.4	1.6	ns	
T_{Period}	APIC CLK Period	60.0	64.0	60.0	N/A	60.0	64.0	ns	3
T_{HIGH}	APIC CLK High Time	25.5	N/A	25.5	N/A	25.5	N/A	ns	4
T_{LOW}	APIC CLK Low Time	25.3	N/A	25.30	N/A	25.30	N/A	ns	5
T_{RISE}	APIC CLK Rise Time	0.4	1.6	0.4	1.6	0.4	1.6	ns	
T_{FALL}	APIC CLK Fall Time	0.4	1.6	0.4	1.6	0.4	1.6	ns	
T_{Period}	3V66 CLK Period	15.0	16.0	15.0	16.0	15.0	16.0	ns	3, 6
T_{HIGH}	3V66 CLK High Time	5.25	N/A	5.25	N/A	5.25	N/A	ns	4
T_{LOW}	3V66 CLK Low Time	5.05	N/A	5.05	N/A	5.05	N/A	ns	5
T_{RISE}	3V66 CLK Rise Time	0.5	2.0	0.5	2.0	0.5	2.0	ns	
T_{FALL}	3V66 CLK Fall Time	0.5	2.0	0.5	2.0	0.5	2.0	ns	
T_{Period}	PCI CLK Period	30.0	N/A	30.0	N/A	30.0	N/A	ns	3, 7
T_{HIGH}	PCI CLK High Time	12.0	N/A	12.0	N/A	12.0	N/A	ns	4
T_{LOW}	PCI CLK Low Time	12.0	N/A	12.0	N/A	12.0	N/A	ns	5
T_{RISE}	PCI CLK Rise Time	0.5	2.0	0.5	2.0	0.5	2.0	ns	
T_{FALL}	PCI CLK Fall Time	0.5	2.0	0.5	2.0	0.5	2.0	ns	
tp_{ZL}, tp_{ZH}	Output Enable Delay (All outputs)	1.0	10.0	1.0	10.0	1.0	10.0	ns	
tp_{LZ}, tp_{ZH}	Output Disable Delay (All outputs)	1.0	10.0	1.0	10.0	1.0	10.0	ns	
t_{stable}	All Clock Stabilization from Power-Up		3		3		3	ms	

Notes:

3. Period, jitter, offset, and skew measured on rising edge at 1.25 for 2.5V clocks and at 1.5V for 3.3V clocks.
4. The time specified is measured from when V_{DDQ3} achieves its nominal operating level (typical condition V_{DDQ3} = 3.3V) until the frequency output is stable and operating within specification.
5. T_{RISE} and T_{FALL} are measured as a transition through the threshold region V_{ol} = 0.4V and V_{oh} = 2.0V (1 mA) JEDEC specification.
6. T_{LOW} is measured at 0.4V for all outputs
7. T_{HIGH} is measured at 2.0V for 2.5V outputs, 2.4V for 3.3V outputs.

.

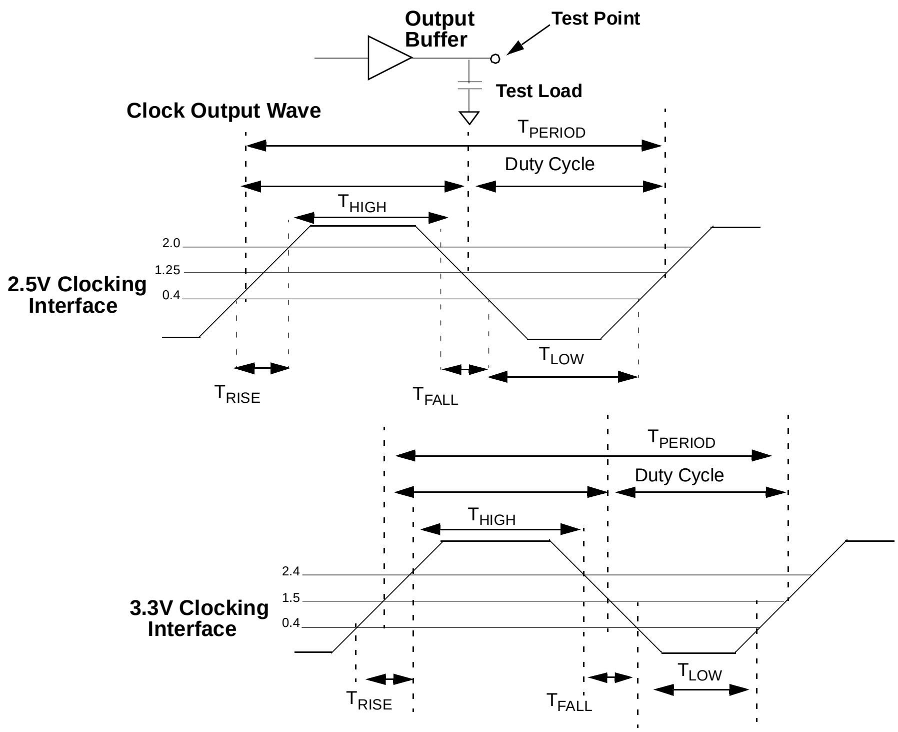


Figure 6. Output Buffer

Group Skew and Jitter Limits

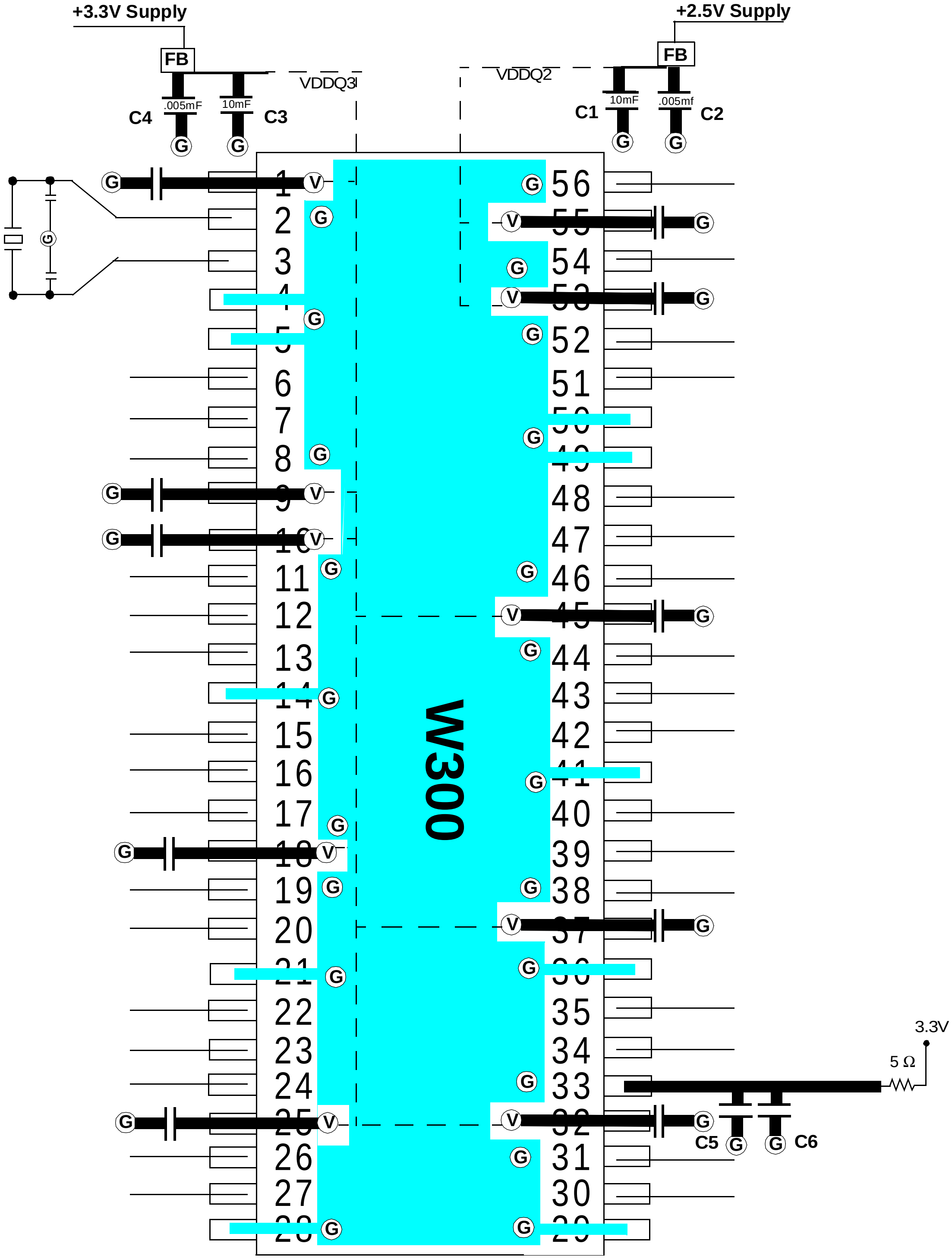
Output Group	Pin-Pin Skew Max.	Cycle-Cycle Jitter	Duty Cycle	Nom Vdd	Skew, Jitter Measure Point
CPU	175 ps	250 ps	45/55	2.5V	1.25V
SDRAM	250 ps	250 ps	45/55	3.3V	1.5V
APIC	250 ps	500 ps	45/55	2.5V	1.25V
48 MHz	250 ps	500 ps	45/55	3.3V	1.5V
3V66	175 ps	500 ps	45/55	3.3V	1.5V
PCI	500 ps	500 ps	45/55	3.3V	1.5V
REF	N/A	1000 ps	45/55	3.3V	1.5V

Ordering Information

Ordering Code	Package Name	Package Type
W300	H	56-pin SSOP (300 mils)

Document #: 38–01084–**

Layout Example



FB = Vishay ILB1206 - 300 (300Ω @ 100 MHz) or TDK ACB2012L-120

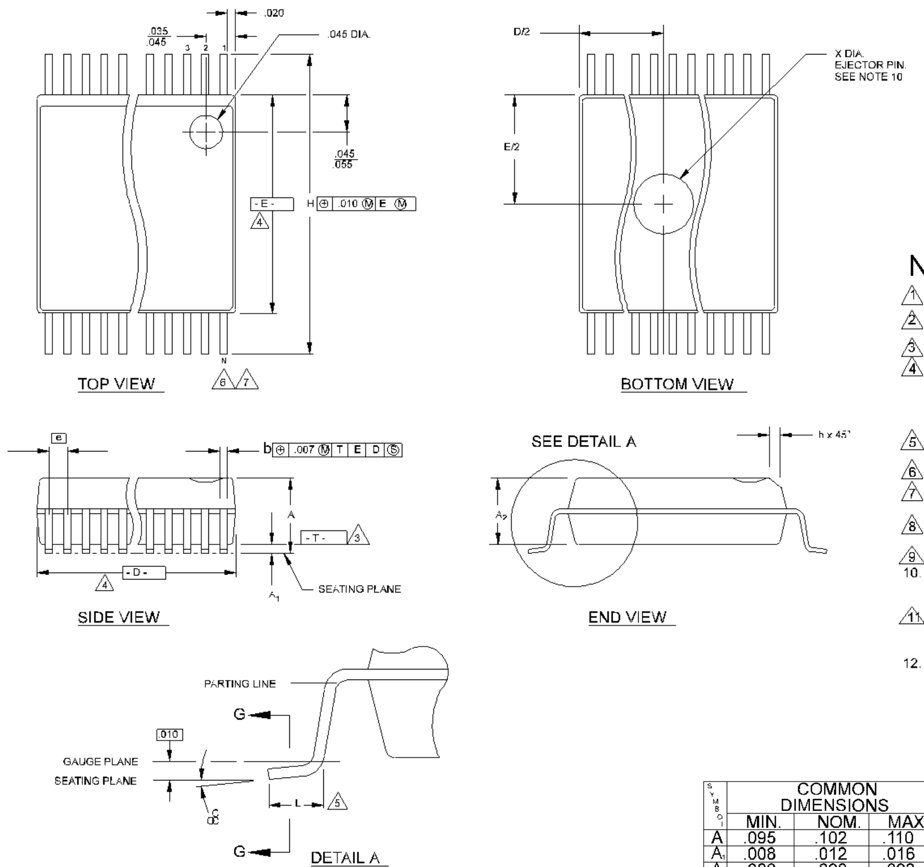
Cermaic Caps C1, C3 & C5 = 10 - 22 μF C2 & C4 = .005 μF C6 = .1 F

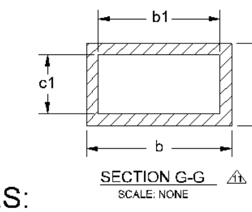
G = VIA to GND plane layer V =VIA to respective supply plane layer

Note: Each supply plane or strip should have a **ferrite bead and capacitors**

Package Diagram

56-Pin Shrink Small Outline Package (SSOP, 300 mils)





NOTES:

1. MAXIMUM DIE THICKNESS ALLOWABLE IS .025.
2. DIMENSIONING & TOLERANCING PER ANSI Y14.5M - 1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006 INCHES PER SIDE.
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
8. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
9. CONTROLLING DIMENSION: INCHES.
10. COUNTRY OF ORIGIN LOCATION AND EJECTOR PIN ON PACKAGE BOTTOM IS OPTIONAL AND DEPENDS ON ASSEMBLY LOCATION.
11. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 INCHES AND .010 INCHES FROM THE LEAD TIPS.
12. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-118, VARIATIONS AA, AB, EXCEPT CHAMFER DIMENSION h. JEDEC SPECIFICATION FOR h IS .015"/.025".

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	.095	.102	.110	
A_1	.008	.012	.016	
A_2	.088	.090	.092	
b	.008	.010	.0135	
b_1	.008	.010	.012	
c	.005	-	.010	
c_1	.005	.006	.0085	
D	SEE VARIATIONS			4
E	.292	.296	.299	
e	.025 BSC			
H	.400	.406	.410	
h	.010	.013	.016	
L	.024	.032	.040	
N	SEE VARIATIONS			6
X	.085	.093	.100	10
α	0°	5°	8°	

NOTE	4			6
VARIATIONS	D			N
	MIN.	NOM.	MAX.	
AA	.620	.625	.630	48
AB	.720	.725	.730	56

THIS TABLE IN INCHES

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	2.41	2.59	2.79	
A_1	0.20	0.31	0.41	
A_2	2.24	2.29	2.34	
b	0.203	0.254	0.343	
b_1	0.203	0.254	0.305	
c	0.127	-	0.254	
c_1	0.127	0.152	0.216	
D	SEE VARIATIONS			4
E	7.42	7.52	7.59	
e	0.635 BSC			
H	10.16	10.31	10.41	
h	0.25	0.33	0.41	
L	0.61	0.81	1.02	
N	SEE VARIATIONS			6
X	2.16	2.36	2.54	10
α	0°	5°	8°	

NOTE	4			6
VARIATIONS	D			N
	MIN.	NOM.	MAX.	
AA	15.75	15.88	16.00	48
AB	18.29	18.42	18.54	56

THIS TABLE IN MILLIMETERS